



Documentation

X2C v6.6.5031

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1 Test Settings

1.1 Test Settings for C28xx

- Environment: Texas Instruments CCS 12.8.1
- Compiler F28335: v16.9.5.LTS
- Compiler F28379D: v22.6.1 LTS
- Optimization: -O2
- Floating point support: fpu32 (when applicable)
- Conversion on target: float32
- All functions are loaded from RAM

1.2 Test Settings for dsPIC33E

- Environment: Microchip MPLABX v6.20
- Compiler: XC16 v1.70
- Optimization: -O2
- Conversion on target: float32

1.3 Test Settings for PIC32

- Environment: Microchip MPLABX v6.20
- Compiler: XC32 v5.10
- Optimization: -O2
- Conversion on target: float32

1.4 Test Settings for STM32

- Environment: STMicroelectronics STM32CubeIDE v1.19.0
- Compiler STM32F0: GNU Tools for STM32 (10.3-2021.10)
- Compiler STM32G4: GNU Tools for STM32 (13.3.rel1)
- Optimization: -O2
- Conversion on target: float32

1.5 Test Settings for TM4C

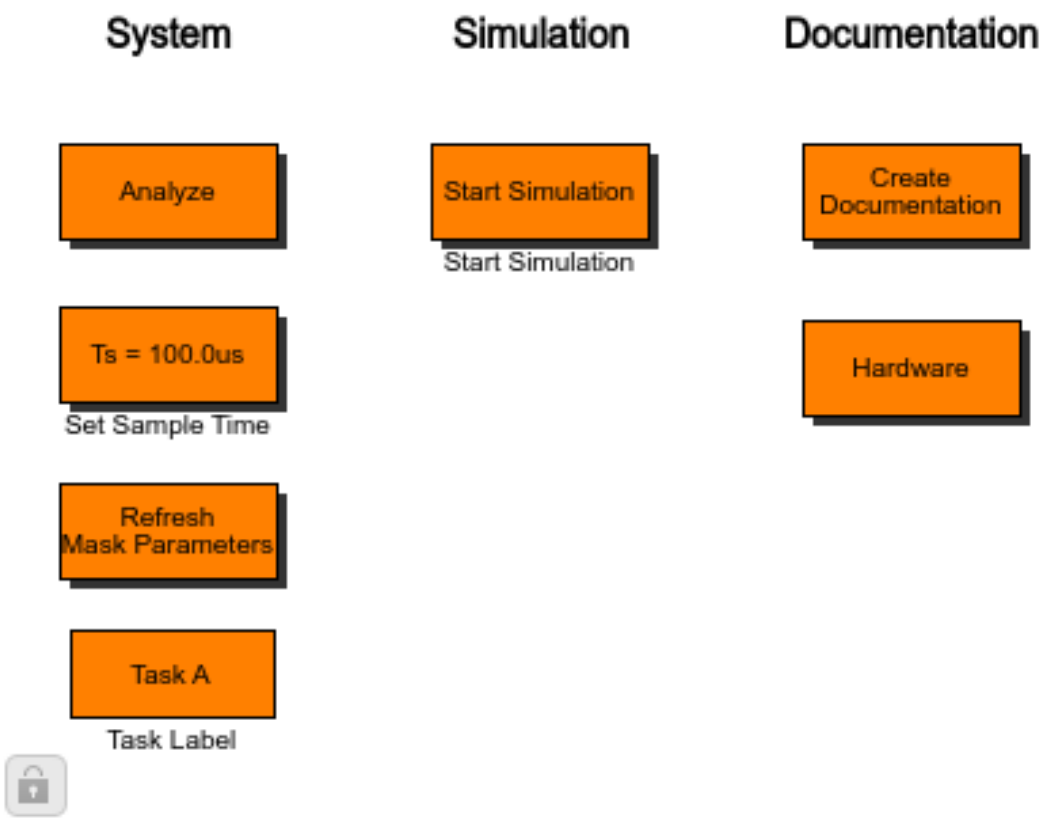
- Environment: Texas Instruments CCS 12.8.1
- Compiler: v16.9.4.LTS
- Optimization: -O2
- Floating point support: FPv4SPD166
- Conversion on target: float32

1.6 Test Settings for XMC4000

- Environment: Infineon DAVE v4.5.0
- Compiler: ARM-GCC-49
- Optimization: -O2
- Floating point support: fpv4-sp-d16
- Conversion on target: float32

2 Basic

Virtual blocks to configure basic code generation, simulation and help generation settings.



Block: CommunicatorStart (Xcos only)



Description:

ith a double-click on this block, the X2C Communicator will start. The Communicator will connect to Scilab via Java Remote Method Invocation (Java RMI) to enable data exchange between Scilab and X2C.

Block: CreateDocumentation



Description:

With a double-click on this block, a documentation with all relevant information about the current X2C project can be created. The document will be created in *<ProjectDir>\Doc* and will be called *ProjectDocumentation_<NameOfModel>.pdf*.

Parameters

User documentation: It is possible to add user specific documentation to the project documentation. When creating the project documentation, the *X2CCode* directory is scanned for the specifed tex file (*UserDoc.tex* by default). If the file is present, it will be included in the documentation.

Test reports: If the checkbox *Add test reports* is selected, test reports of the C-Unit tests of the used X2C blocks are added to the project documentation.

Requirements

In order to generate a documentation in PDF-format a TeX-compiler (e.g. *MiKTeX*) has to be installed. The software tools *Doxygen* and *Graphviz* are recommended to get documentation of the C-code.

Block: Interact (Xcos only)



Description:

When double-clicked, the block executes the Scilab script *doInteraction.sci*, if available. By customizing the script, the user can execute simple tasks, e.g. setting block parameters, read parameter values, display status information, etc., repeatedly and effortlessly.

Block: ModelTransformation (Xcos only)

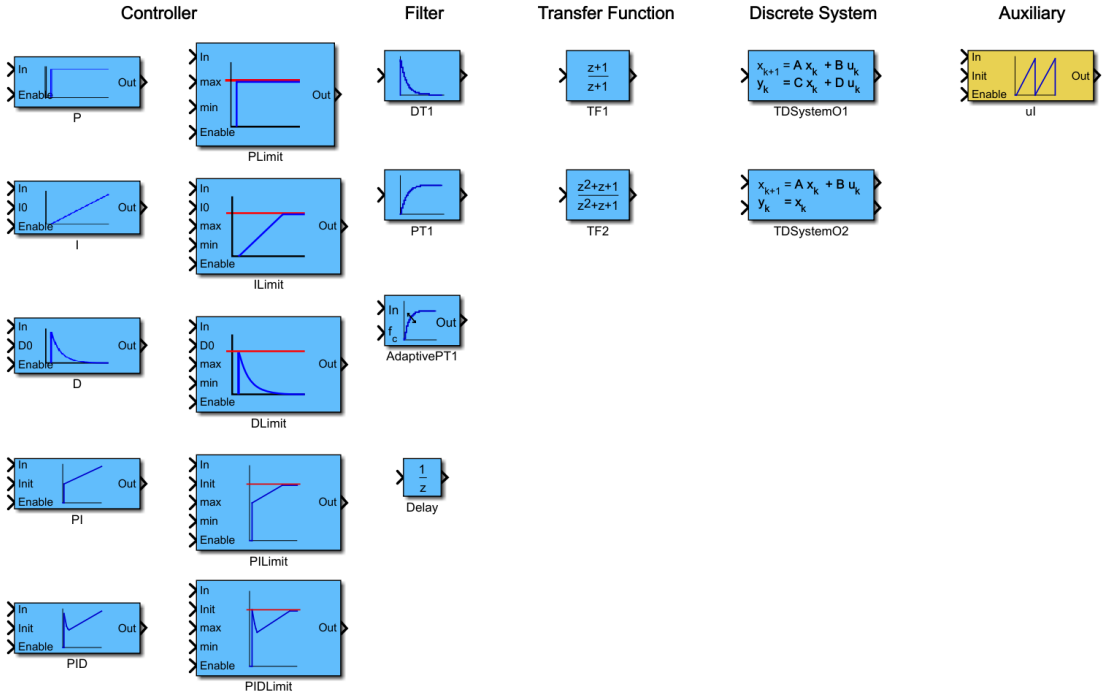


Description:

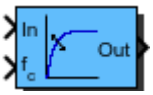
With a double-click on this block, the Xcos model will be analyzed. All relevant information for code generation are gathered, transfered to the Communicator and written to the model XML file.

3 Control

This library contains blocks for building control algorithms.



Block: AdaptivePT1



First order low pass with adaptive cut off frequency:
G(s) = V/(s/(2*pi*fc) + 1)

Inports	
In	Input In(k)
fc	Cutoff frequency

Outports	
Out	Output Out(k)

Mask Parameters		
Name	**ID**	**Description**
V	1	Gain
fmax	2	Maximum frequency [Hz] (not used in floating point implementations)
ts_fact	3	Multiplication factor of base sampling time (in integer format)
method	4	Discretization method

Description:

Transfer function (zero-order hold discretization method):

$$G(z) = V\frac{1 - e^{-2\pi f_c T_s}}{z - e^{-2\pi f_c T_s}}$$

Implementations:

FiP8	8 Bit Fixed Point Implementation
FiP16	16 Bit Fixed Point Implementation
FiP32	32 Bit Fixed Point Implementation
Float32	32 Bit Floating Point Implementation
Float64	64 Bit Floating Point Implementation

Implementation: FiP8

8 Bit Fixed Point Implementation

Inports Data Type	
In	int8
fc	int8

Outports Data Type	
Out	int8

Implementation: FiP16

16 Bit Fixed Point Implementation

Inports Data Type	
In	int16
fc	int16

Outports Data Type	
Out	int16

Implementation: FiP32

32 Bit Fixed Point Implementation

Inports Data Type	
In	int32
fc	int32

Outports Data Type	
Out	int32

Implementation: Float32

32 Bit Floating Point Implementation

Inports Data Type	
In	float32
fc	float32

Outports Data Type	
Out	float32

Implementation: Float64

64 Bit Floating Point Implementation

Inports Data Type	
In	float64
fc	float64

Outports Data Type	
Out	float64

Verification: AdaptivePT1 FiP16 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for Control block AdaptivePT1.

Test results						
Time step	1	2	3	4	...	105
CPU cycles	129	129	129	129	...	129
Inputs						
In (DSP)	0	0	0	0	...	-9830
fc (DSP)	7537	7537	7537	7537	...	7537
In	0	0	0	0	...	-0.3
fc	0.23	0.23	0.23	0.23	...	0.23
Parameters						
V	1.1					
fmax	1000					
ts_fact	1					
method	zoh					
Outputs						
Out	0	0	0	0	...	-0.329
Exp. Out	0	0	0	0	...	-0.329
Out (DSP)	0	0	0	0	...	-10778
Exp. Out (DSP)	0	0	0	0	...	-10780

Test settings	
Tolerance Out	±6,1035e-04 (±20 LSB)

Test statistics	
Min CPU cycles	129
Max CPU cycles	129
Avg CPU cycles	129

Verification: AdaptivePT1 FiP16 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for Control block AdaptivePT1.

Test results						
Time step	1	2	3	4	...	105
CPU cycles	85	85	85	85	...	85
Inputs						
In (DSP)	0	0	0	0	...	-9830
fc (DSP)	7537	7537	7537	7537	...	7537
In	0	0	0	0	...	-0.3
fc	0.23	0.23	0.23	0.23	...	0.23
Parameters						
V	1.1					
fmax	1000					
ts_fact	1					
method	zoh					
Outputs						
Out	0	0	0	0	...	-0.329
Exp. Out	0	0	0	0	...	-0.329
Out (DSP)	0	0	0	0	...	-10778
Exp. Out (DSP)	0	0	0	0	...	-10780

Test settings	
Tolerance Out	±6,1035e-04 (±20 LSB)

Test statistics	
Min CPU cycles	85
Max CPU cycles	85
Avg CPU cycles	85

Verification: AdaptivePT1 FiP16 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for Control block AdaptivePT1.

Test results						
Time step	1	2	3	4	...	105
CPU cycles	132	132	132	132	...	132
Inputs						
In (DSP)	0	0	0	0	...	-9830
fc (DSP)	7537	7537	7537	7537	...	7537
In	0	0	0	0	...	-0.3
fc	0.23	0.23	0.23	0.23	...	0.23
Parameters						
V	1.1					
fmax	1000					
ts_fact	1					
method	zoh					
Outputs						
Out	0	0	0	0	...	-0.329
Exp. Out	0	0	0	0	...	-0.329
Out (DSP)	0	0	0	0	...	-10778
Exp. Out (DSP)	0	0	0	0	...	-10780

Test settings	
Tolerance Out	±6,1035e-04 (±20 LSB)

Test statistics	
Min CPU cycles	132
Max CPU cycles	132
Avg CPU cycles	132

Verification: AdaptivePT1 FiP16 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test **OK**

Inport test for Control block AdaptivePT1.

Test results						
Time step	1	2	3	4	...	105
CPU cycles	120	120	120	120	...	120
Inputs						
In (DSP)	0	0	0	0	...	-9830
fc (DSP)	7537	7537	7537	7537	...	7537
In	0	0	0	0	...	-0.3
fc	0.23	0.23	0.23	0.23	...	0.23
Parameters						
V	1.1					
fmax	1000					
ts_fact	1					
method	zoh					
Outputs						
Out	0	0	0	0	...	-0.329
Exp. Out	0	0	0	0	...	-0.329
Out (DSP)	0	0	0	0	...	-10778
Exp. Out (DSP)	0	0	0	0	...	-10780

Test settings	
Tolerance Out	±6,1035e-04 (±20 LSB)

Test statistics	
Min CPU cycles	120
Max CPU cycles	120
Avg CPU cycles	120

Verification: AdaptivePT1 FiP16 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for Control block AdaptivePT1.

Test results						
Time step	1	2	3	4	...	105
CPU cycles	81	81	81	81	...	81
Inputs						
In (DSP)	0	0	0	0	...	-9830
fc (DSP)	7537	7537	7537	7537	...	7537
In	0	0	0	0	...	-0.3
fc	0.23	0.23	0.23	0.23	...	0.23
Parameters						
V	1.1					
fmax	1000					
ts_fact	1					
method	zoh					
Outputs						
Out	0	0	0	0	...	-0.329
Exp. Out	0	0	0	0	...	-0.329
Out (DSP)	0	0	0	0	...	-10778
Exp. Out (DSP)	0	0	0	0	...	-10780

Test settings	
Tolerance Out	±6,1035e-04 (±20 LSB)

Test statistics	
Min CPU cycles	81
Max CPU cycles	81
Avg CPU cycles	81

Verification: AdaptivePT1 FiP16 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test **OK**

Inport test for Control block AdaptivePT1.

Test results						
Time step	1	2	3	4	...	105
CPU cycles	154	127	127	127	...	127
Inputs						
In (DSP)	0	0	0	0	...	-9830
fc (DSP)	7537	7537	7537	7537	...	7537
In	0	0	0	0	...	-0.3
fc	0.23	0.23	0.23	0.23	...	0.23
Parameters						
V	1.1					
fmax	1000					
ts_fact	1					
method	zoh					
Outputs						
Out	0	0	0	0	...	-0.329
Exp. Out	0	0	0	0	...	-0.329
Out (DSP)	0	0	0	0	...	-10778
Exp. Out (DSP)	0	0	0	0	...	-10780

Test settings	
Tolerance Out	±6,1035e-04 (±20 LSB)

Test statistics	
Min CPU cycles	127
Max CPU cycles	154
Avg CPU cycles	127

Verification: AdaptivePT1 FiP16 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for Control block AdaptivePT1.

Test results						
Time step	1	2	3	4	...	105
CPU cycles	118	118	118	118	...	118
Inputs						
In (DSP)	0	0	0	0	...	-9830
fc (DSP)	7537	7537	7537	7537	...	7537
In	0	0	0	0	...	-0.3
fc	0.23	0.23	0.23	0.23	...	0.23
Parameters						
V	1.1					
fmax	1000					
ts_fact	1					
method	zoh					
Outputs						
Out	0	0	0	0	...	-0.329
Exp. Out	0	0	0	0	...	-0.329
Out (DSP)	0	0	0	0	...	-10778
Exp. Out (DSP)	0	0	0	0	...	-10780

Test settings	
Tolerance Out	±6,1035e-04 (±20 LSB)

Test statistics	
Min CPU cycles	118
Max CPU cycles	118
Avg CPU cycles	118

Verification: AdaptivePT1 FiP16 CPU dsPIC33EP256MC502

Date of Test	2026-06-23
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for Control block AdaptivePT1.

Test results						
Time step	1	2	3	4	...	105
CPU cycles	131	131	131	131	...	131
Inputs						
In (DSP)	0	0	0	0	...	-9830
fc (DSP)	7537	7537	7537	7537	...	7537
In	0	0	0	0	...	-0.3
fc	0.23	0.23	0.23	0.23	...	0.23
Parameters						
V	1.1					
fmax	1000					
ts_fact	1					
method	zoh					
Outputs						
Out	0	0	0	0	...	-0.329
Exp. Out	0	0	0	0	...	-0.329
Out (DSP)	0	0	0	0	...	-10778
Exp. Out (DSP)	0	0	0	0	...	-10780

Test settings	
Tolerance Out	±6,1035e-04 (±20 LSB)

Test statistics	
Min CPU cycles	131
Max CPU cycles	131
Avg CPU cycles	131

Verification: AdaptivePT1 FiP32 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for Control block AdaptivePT1.

Test results				
Time step	1	2	...	105
CPU cycles	276	276	...	276
Inputs				
In (DSP)	0	0	...	-644245094
fc (DSP)	493921239	493921239	...	493921239
In	0	0	...	-0.3
fc	0.23	0.23	...	0.23
Parameters				
V	1.1			
fmax	1000			
ts_fact	1			
method	zoh			
Outputs				
Out	0	0	...	-0.329
Exp. Out	0	0	...	-0.329
Out (DSP)	0	0	...	-706485147
Exp. Out (DSP)	0	0	...	-706485964

Test settings	
Tolerance Out	±2,3749e-05 (±51000 LSB)

Test statistics	
Min CPU cycles	276
Max CPU cycles	276
Avg CPU cycles	276

Verification: AdaptivePT1 FiP32 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for Control block AdaptivePT1.

Test results				
Time step	1	2	...	105
CPU cycles	171	171	...	171
Inputs				
In (DSP)	0	0	...	-644245094
fc (DSP)	493921239	493921239	...	493921239
In	0	0	...	-0.3
fc	0.23	0.23	...	0.23
Parameters				
V	1.1			
fmax	1000			
ts_fact	1			
method	zoh			
Outputs				
Out	0	0	...	-0.329
Exp. Out	0	0	...	-0.329
Out (DSP)	0	0	...	-706485147
Exp. Out (DSP)	0	0	...	-706485964

Test settings	
Tolerance Out	±2,3749e-05 (±51000 LSB)

Test statistics	
Min CPU cycles	171
Max CPU cycles	171
Avg CPU cycles	171

Verification: AdaptivePT1 FiP32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for Control block AdaptivePT1.

Test results				
Time step	1	2	...	105
CPU cycles	192	192	...	192
Inputs				
In (DSP)	0	0	...	-644245094
fc (DSP)	493921239	493921239	...	493921239
In	0	0	...	-0.3
fc	0.23	0.23	...	0.23
Parameters				
V	1.1			
fmax	1000			
ts_fact	1			
method	zoh			
Outputs				
Out	0	0	...	-0.329
Exp. Out	0	0	...	-0.329
Out (DSP)	0	0	...	-706485147
Exp. Out (DSP)	0	0	...	-706485964

Test settings	
Tolerance Out	±2,3749e-05 (±51000 LSB)

Test statistics	
Min CPU cycles	192
Max CPU cycles	192
Avg CPU cycles	192

Verification: AdaptivePT1 FiP32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for Control block AdaptivePT1.

Test results				
Time step	1	2	...	105
CPU cycles	503	503	...	500
Inputs				
In (DSP)	0	0	...	-644245094
fc (DSP)	493921239	493921239	...	493921239
In	0	0	...	-0.3
fc	0.23	0.23	...	0.23
Parameters				
V	1.1			
fmax	1000			
ts_fact	1			
method	zoh			
Outputs				
Out	0	0	...	-0.329
Exp. Out	0	0	...	-0.329
Out (DSP)	0	0	...	-706485147
Exp. Out (DSP)	0	0	...	-706485964

Test settings	
Tolerance Out	±2,3749e-05 (±51000 LSB)

Test statistics	
Min CPU cycles	500
Max CPU cycles	563
Avg CPU cycles	503

Verification: AdaptivePT1 FiP32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for Control block AdaptivePT1.

Test results				
Time step	1	2	...	105
CPU cycles	137	137	...	139
Inputs				
In (DSP)	0	0	...	-644245094
fc (DSP)	493921239	493921239	...	493921239
In	0	0	...	-0.3
fc	0.23	0.23	...	0.23
Parameters				
V	1.1			
fmax	1000			
ts_fact	1			
method	zoh			
Outputs				
Out	0	0	...	-0.329
Exp. Out	0	0	...	-0.329
Out (DSP)	0	0	...	-706485147
Exp. Out (DSP)	0	0	...	-706485964

Test settings	
Tolerance Out	±2,3749e-05 (±51000 LSB)

Test statistics	
Min CPU cycles	137
Max CPU cycles	139
Avg CPU cycles	138

Verification: AdaptivePT1 FiP32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for Control block AdaptivePT1.

Test results				
Time step	1	2	...	105
CPU cycles	208	167	...	167
Inputs				
In (DSP)	0	0	...	-644245094
fc (DSP)	493921239	493921239	...	493921239
In	0	0	...	-0.3
fc	0.23	0.23	...	0.23
Parameters				
V	1.1			
fmax	1000			
ts_fact	1			
method	zoh			
Outputs				
Out	0	0	...	-0.329
Exp. Out	0	0	...	-0.329
Out (DSP)	0	0	...	-706485147
Exp. Out (DSP)	0	0	...	-706485964

Test settings	
Tolerance Out	±2,3749e-05 (±51000 LSB)

Test statistics	
Min CPU cycles	167
Max CPU cycles	208
Avg CPU cycles	167

Verification: AdaptivePT1 FiP32 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for Control block AdaptivePT1.

Test results				
Time step	1	2	...	105
CPU cycles	239	239	...	239
Inputs				
In (DSP)	0	0	...	-644245094
fc (DSP)	493921239	493921239	...	493921239
In	0	0	...	-0.3
fc	0.23	0.23	...	0.23
Parameters				
V	1.1			
fmax	1000			
ts_fact	1			
method	zoh			
Outputs				
Out	0	0	...	-0.329
Exp. Out	0	0	...	-0.329
Out (DSP)	0	0	...	-706485147
Exp. Out (DSP)	0	0	...	-706485964

Test settings	
Tolerance Out	±2,3749e-05 (±51000 LSB)

Test statistics	
Min CPU cycles	239
Max CPU cycles	239
Avg CPU cycles	239

Verification: AdaptivePT1 FiP32 CPU dsPIC33EP256MC502

Date of Test	2026-06-23
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

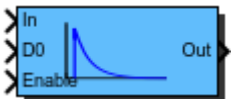
Inport test for Control block AdaptivePT1.

Test results				
Time step	1	2	...	105
CPU cycles	990	990	...	1004
Inputs				
In (DSP)	0	0	...	-644245094
fc (DSP)	493921239	493921239	...	493921239
In	0	0	...	-0.3
fc	0.23	0.23	...	0.23
Parameters				
V	1.1			
fmax	1000			
ts_fact	1			
method	zoh			
Outputs				
Out	0	0	...	-0.329
Exp. Out	0	0	...	-0.329
Out (DSP)	0	0	...	-706485147
Exp. Out (DSP)	0	0	...	-706485964

Test settings	
Tolerance Out	±2,3749e-05 (±51000 LSB)

Test statistics	
Min CPU cycles	990
Max CPU cycles	1004
Avg CPU cycles	995

Block: D



D Controller:
G(s) = Kd*s/(s/(2*pi*fc) + 1)

Inports	
In	Control error input
D0	Derivational value which is loaded during initialization. (Usually this inport is connect to the In inport.)
Enable	Enable == 0: Deactivation of block; Out set to 0 Enable 0->1: Preload of derivational part Enable == 1: Activation of block

Outports	
Out	Control value

Mask Parameters		
Name	**ID**	**Description**
Kd	1	Derivative Factor
fc	2	Cutoff frequency of realization low pass
ts_fact	3	Multiplication factor of base sampling time (in integer format)

Description:

A rising flank at the *Enable* inport will preload the derivational part with the value present on the *Init* inport.

Transfer function (zero-order hold discretization method):

$$G(z) = K_{\mathrm{d}} 2\pi f_{\mathrm{c}} \frac{z-1}{z - e^{-2\pi f_{\mathrm{c}} T_{\mathrm{s}}}}$$

Developer note: The source code of block *DLimit* is used.

Implementations:

FiP16 16 Bit Fixed Point Implementation
FiP32 32 Bit Fixed Point Implementation
Float32 32 Bit Floating Point Implementation
Float64 64 Bit Floating Point Implementation

Implementation: FiP16

16 Bit Fixed Point Implementation

Inports Data Type	
In	int16
D0	int16
Enable	bool

Outports Data Type	
Out	int16

Implementation: FiP32

32 Bit Fixed Point Implementation

Inports Data Type	
In	int32
D0	int32
Enable	bool

Outports Data Type	
Out	int32

Implementation: Float32

32 Bit Floating Point Implementation

Inports Data Type	
In	float32
D0	float32
Enable	bool

Outports Data Type	
Out	float32

Implementation: Float64

64 Bit Floating Point Implementation

Inports Data Type	
In	float64
D0	float64
Enable	bool

Outports Data Type	
Out	float64

Verification: D FiP16 CPU TMS320F28335

Date of Test 2026-06-19

Target controller TMS320F28335

Test case: Inport test OK

Inport test for Control block D.

Test results						
Time step	1	2	3	4	...	201
CPU cycles	77	77	77	125	...	120
Inputs						
In (DSP)	0	0	0	0	...	0
D0 (DSP)	655	655	655	655	...	655
Enable (DSP)	0	0	0	1	...	1
In	0	0	0	0	...	0
D0	0.02	0.02	0.02	0.02	...	0.02
Enable	0	0	0	1	...	1
Parameters						
Kd	0.003					
fc	200					
ts_fact	1					
Outputs						
Out	0	0	0	-0.075	...	0.002
Exp. Out	0	0	0	-0.075	...	0.002
Out (DSP)	0	0	0	-2470	...	61
Exp. Out (DSP)	0	0	0	-2471	...	58

Test settings	
Tolerance Out	±3,0518e-04 (±10 LSB)

Test statistics	
Min CPU cycles	77
Max CPU cycles	125
Avg CPU cycles	119

Test case: Conversion test OK

Conversion test for Control block D.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kd	-10	-9.444	-8.889	-8.333	...	10
fc	0	13.889	27.778	41.667	...	500
ts_fact	1	1	1	1	...	1
Controller parameters						
sfrd	15	5	4	3	...	0
b1d	0	-26374	-24822	-17453	...	31416
a0d	-32767	-32483	-32201	-31921	...	-23934
b0d	0	26374	24822	17453	...	-31416
Exp. sfrd	15	5	4	3	...	0
Exp. b1d	0	-26374	-24822	-17453	...	31416
Exp. a0d	-32767	-32483	-32201	-31921	...	-23934
Exp. b0d	0	26374	24822	17453	...	-31416

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±0,0000e+00
Tolerance a0d	±0,0000e+00
Tolerance b0d	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block D.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kd	-10	-9.444	-8.889	-8.333	...	10
fc	0	13.889	27.778	41.667	...	500
ts_fact	1	1	1	1	...	1
Controller parameters						
sfrd	15	5	4	3	...	0
b1d	0	-26373	-24822	-17453	...	31415
a0d	-32767	-32483	-32201	-31921	...	-23933
b0d	0	26373	24822	17453	...	-31415
Exp. sfrd	15	5	4	3	...	0
Exp. b1d	0	-26374	-24822	-17453	...	31416
Exp. a0d	-32767	-32483	-32201	-31921	...	-23934
Exp. b0d	0	26374	24822	17453	...	-31416

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±1,0000e+00
Tolerance a0d	±1,0000e+00
Tolerance b0d	±1,0000e+00

Test statistics	
Min CPU cycles	2821
Max CPU cycles	10490
Avg CPU cycles	9335

Verification: D FiP16 CPU TM4C123GH6

Date of Test 2026-06-19

Target controller TM4C123GH6

Test case: Inport test — OK

Inport test for Control block D.

Test results						
Time step	1	2	3	4	...	201
CPU cycles	51	51	51	79	...	77
Inputs						
In (DSP)	0	0	0	0	...	0
D0 (DSP)	655	655	655	655	...	655
Enable (DSP)	0	0	0	1	...	1
In	0	0	0	0	...	0
D0	0.02	0.02	0.02	0.02	...	0.02
Enable	0	0	0	1	...	1
Parameters						
Kd	0.003					
fc	200					
ts_fact	1					
Outputs						
Out	0	0	0	-0.075	...	0.002
Exp. Out	0	0	0	-0.075	...	0.002
Out (DSP)	0	0	0	-2470	...	61
Exp. Out (DSP)	0	0	0	-2471	...	58

Test settings	
Tolerance Out	±3,0518e-04 (±10 LSB)

Test statistics	
Min CPU cycles	51
Max CPU cycles	79
Avg CPU cycles	76

Test case: Conversion test — OK

Conversion test for Control block D.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kd	-10	-9.444	-8.889	-8.333	...	10
fc	0	13.889	27.778	41.667	...	500
ts_fact	1	1	1	1	...	1
Controller parameters						
sfrd	15	5	4	3	...	0
b1d	0	-26374	-24822	-17453	...	31416
a0d	-32767	-32483	-32201	-31921	...	-23934
b0d	0	26374	24822	17453	...	-31416
Exp. sfrd	15	5	4	3	...	0
Exp. b1d	0	-26374	-24822	-17453	...	31416
Exp. a0d	-32767	-32483	-32201	-31921	...	-23934
Exp. b0d	0	26374	24822	17453	...	-31416

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±0,0000e+00
Tolerance a0d	±0,0000e+00
Tolerance b0d	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block D.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kd	-10	-9.444	-8.889	-8.333	...	10
fc	0	13.889	27.778	41.667	...	500
ts_fact	1	1	1	1	...	1
Controller parameters						
sfrd	15	5	4	3	...	0
b1d	0	-26373	-24822	-17453	...	31415
a0d	-32767	-32483	-32201	-31921	...	-23933
b0d	0	26373	24822	17453	...	-31415
Exp. sfrd	15	5	4	3	...	0
Exp. b1d	0	-26374	-24822	-17453	...	31416
Exp. a0d	-32767	-32483	-32201	-31921	...	-23934
Exp. b0d	0	26374	24822	17453	...	-31416

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±1,0000e+00
Tolerance a0d	±1,0000e+00
Tolerance b0d	±1,0000e+00

Test statistics	
Min CPU cycles	1363
Max CPU cycles	6395
Avg CPU cycles	5342

Verification: D FiP16 CPU STM32G474RE

Date of Test 2026-06-19

Target controller STM32G474RE

Test case: Inport test OK

Inport test for Control block D.

Test results						
Time step	1	2	3	4	...	201
CPU cycles	73	73	73	131	...	111
Inputs						
In (DSP)	0	0	0	0	...	0
D0 (DSP)	655	655	655	655	...	655
Enable (DSP)	0	0	0	1	...	1
In	0	0	0	0	...	0
D0	0.02	0.02	0.02	0.02	...	0.02
Enable	0	0	0	1	...	1
Parameters						
Kd	0.003					
fc	200					
ts_fact	1					
Outputs						
Out	0	0	0	-0.075	...	0.002
Exp. Out	0	0	0	-0.075	...	0.002
Out (DSP)	0	0	0	-2470	...	61
Exp. Out (DSP)	0	0	0	-2471	...	58

Test settings	
Tolerance Out	±3,0518e-04 (±10 LSB)

Test statistics	
Min CPU cycles	73
Max CPU cycles	131
Avg CPU cycles	110

Test case: Conversion test OK

Conversion test for Control block D.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kd	-10	-9.444	-8.889	-8.333	...	10
fc	0	13.889	27.778	41.667	...	500
ts_fact	1	1	1	1	...	1
Controller parameters						
sfrd	15	5	4	3	...	0
b1d	0	-26374	-24822	-17453	...	31416
a0d	-32767	-32483	-32201	-31921	...	-23934
b0d	0	26374	24822	17453	...	-31416
Exp. sfrd	15	5	4	3	...	0
Exp. b1d	0	-26374	-24822	-17453	...	31416
Exp. a0d	-32767	-32483	-32201	-31921	...	-23934
Exp. b0d	0	26374	24822	17453	...	-31416

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±0,0000e+00
Tolerance a0d	±0,0000e+00
Tolerance b0d	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block D.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kd	-10	-9.444	-8.889	-8.333	...	10
fc	0	13.889	27.778	41.667	...	500
ts_fact	1	1	1	1	...	1
Controller parameters						
sfrd	15	5	4	3	...	0
b1d	0	-26373	-24822	-17453	...	31415
a0d	-32767	-32483	-32201	-31921	...	-23933
b0d	0	26373	24822	17453	...	-31415
Exp. sfrd	15	5	4	3	...	0
Exp. b1d	0	-26374	-24822	-17453	...	31416
Exp. a0d	-32767	-32483	-32201	-31921	...	-23934
Exp. b0d	0	26374	24822	17453	...	-31416

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±1,0000e+00
Tolerance a0d	±1,0000e+00
Tolerance b0d	±1,0000e+00

Test statistics	
Min CPU cycles	1668
Max CPU cycles	3699
Avg CPU cycles	3272

Verification: D FiP16 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test

OK

Inport test for Control block D.

Test results						
Time step	1	2	3	4	...	201
CPU cycles	70	70	70	126	...	114
Inputs						
In (DSP)	0	0	0	0	...	0
D0 (DSP)	655	655	655	655	...	655
Enable (DSP)	0	0	0	1	...	1
In	0	0	0	0	...	0
D0	0.02	0.02	0.02	0.02	...	0.02
Enable	0	0	0	1	...	1
Parameters						
Kd	0.003					
fc	200					
ts_fact	1					
Outputs						
Out	0	0	0	-0.075	...	0.002
Exp. Out	0	0	0	-0.075	...	0.002
Out (DSP)	0	0	0	-2470	...	61
Exp. Out (DSP)	0	0	0	-2471	...	58

Test settings	
Tolerance Out	±3,0518e-04 (±10 LSB)

Test statistics	
Min CPU cycles	70
Max CPU cycles	126
Avg CPU cycles	113

Test case: Conversion test

OK

Conversion test for Control block D.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kd	-10	-9.444	-8.889	-8.333	...	10
fc	0	13.889	27.778	41.667	...	500
ts_fact	1	1	1	1	...	1
Controller parameters						
sfrd	15	5	4	3	...	0
b1d	0	-26374	-24822	-17453	...	31416
a0d	-32767	-32483	-32201	-31921	...	-23934
b0d	0	26374	24822	17453	...	-31416
Exp. sfrd	15	5	4	3	...	0
Exp. b1d	0	-26374	-24822	-17453	...	31416
Exp. a0d	-32767	-32483	-32201	-31921	...	-23934
Exp. b0d	0	26374	24822	17453	...	-31416

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±0,0000e+00
Tolerance a0d	±0,0000e+00
Tolerance b0d	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block D.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kd	-10	-9.444	-8.889	-8.333	...	10
fc	0	13.889	27.778	41.667	...	500
ts_fact	1	1	1	1	...	1
Controller parameters						
sfrd	15	5	4	3	...	0
b1d	0	-26373	-24822	-17453	...	31415
a0d	-32767	-32483	-32201	-31921	...	-23933
b0d	0	26373	24822	17453	...	-31415
Exp. sfrd	15	5	4	3	...	0
Exp. b1d	0	-26374	-24822	-17453	...	31416
Exp. a0d	-32767	-32483	-32201	-31921	...	-23934
Exp. b0d	0	26374	24822	17453	...	-31416

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±1,0000e+00
Tolerance a0d	±1,0000e+00
Tolerance b0d	±1,0000e+00

Test statistics	
Min CPU cycles	4309
Max CPU cycles	17120
Avg CPU cycles	15168

Verification: D FiP16 CPU PIC32MX170F256

Date of Test 2026-06-19

Target controller PIC32MX170F256

Test case: Inport test OK

Inport test for Control block D.

Test results						
Time step	1	2	3	4	...	201
CPU cycles	37	37	37	78	...	73
Inputs						
In (DSP)	0	0	0	0	...	0
D0 (DSP)	655	655	655	655	...	655
Enable (DSP)	0	0	0	1	...	1
In	0	0	0	0	...	0
D0	0.02	0.02	0.02	0.02	...	0.02
Enable	0	0	0	1	...	1
Parameters						
Kd	0.003					
fc	200					
ts_fact	1					
Outputs						
Out	0	0	0	-0.075	...	0.002
Exp. Out	0	0	0	-0.075	...	0.002
Out (DSP)	0	0	0	-2470	...	61
Exp. Out (DSP)	0	0	0	-2471	...	58

Test settings	
Tolerance Out	±3,0518e-04 (±10 LSB)

Test statistics	
Min CPU cycles	37
Max CPU cycles	78
Avg CPU cycles	72

Test case: Conversion test OK

Conversion test for Control block D.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kd	-10	-9.444	-8.889	-8.333	...	10
fc	0	13.889	27.778	41.667	...	500
ts_fact	1	1	1	1	...	1
Controller parameters						
sfrd	15	5	4	3	...	0
b1d	0	-26374	-24822	-17453	...	31416
a0d	-32767	-32483	-32201	-31921	...	-23934
b0d	0	26374	24822	17453	...	-31416
Exp. sfrd	15	5	4	3	...	0
Exp. b1d	0	-26374	-24822	-17453	...	31416
Exp. a0d	-32767	-32483	-32201	-31921	...	-23934
Exp. b0d	0	26374	24822	17453	...	-31416

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±0,0000e+00
Tolerance a0d	±0,0000e+00
Tolerance b0d	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block D.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kd	-10	-9.444	-8.889	-8.333	...	10
fc	0	13.889	27.778	41.667	...	500
ts_fact	1	1	1	1	...	1
Controller parameters						
sfrd	15	5	4	3	...	0
b1d	0	-26373	-24822	-17453	...	31415
a0d	-32767	-32483	-32201	-31921	...	-23933
b0d	0	26373	24822	17453	...	-31415
Exp. sfrd	15	5	4	3	...	0
Exp. b1d	0	-26374	-24822	-17453	...	31416
Exp. a0d	-32767	-32483	-32201	-31921	...	-23934
Exp. b0d	0	26374	24822	17453	...	-31416

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±1,0000e+00
Tolerance a0d	±1,0000e+00
Tolerance b0d	±1,0000e+00

Test statistics	
Min CPU cycles	1688
Max CPU cycles	5799
Avg CPU cycles	5201

Verification: D FiP16 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for Control block D.

Test results						
Time step	1	2	3	4	...	201
CPU cycles	97	79	79	124	...	109
Inputs						
In (DSP)	0	0	0	0	...	0
D0 (DSP)	655	655	655	655	...	655
Enable (DSP)	0	0	0	1	...	1
In	0	0	0	0	...	0
D0	0.02	0.02	0.02	0.02	...	0.02
Enable	0	0	0	1	...	1
Parameters						
Kd	0.003					
fc	200					
ts_fact	1					
Outputs						
Out	0	0	0	-0.075	...	0.002
Exp. Out	0	0	0	-0.075	...	0.002
Out (DSP)	0	0	0	-2470	...	61
Exp. Out (DSP)	0	0	0	-2471	...	58

Test settings	
Tolerance Out	±3,0518e-04 (±10 LSB)

Test statistics	
Min CPU cycles	79
Max CPU cycles	124
Avg CPU cycles	108

Test case: Conversion test OK

Conversion test for Control block D.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kd	-10	-9.444	-8.889	-8.333	...	10
fc	0	13.889	27.778	41.667	...	500
ts_fact	1	1	1	1	...	1
Controller parameters						
sfrd	15	5	4	3	...	0
b1d	0	-26374	-24822	-17453	...	31416
a0d	-32767	-32483	-32201	-31921	...	-23934
b0d	0	26374	24822	17453	...	-31416
Exp. sfrd	15	5	4	3	...	0
Exp. b1d	0	-26374	-24822	-17453	...	31416
Exp. a0d	-32767	-32483	-32201	-31921	...	-23934
Exp. b0d	0	26374	24822	17453	...	-31416

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±0,0000e+00
Tolerance a0d	±0,0000e+00
Tolerance b0d	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block D.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kd	-10	-9.444	-8.889	-8.333	...	10
fc	0	13.889	27.778	41.667	...	500
ts_fact	1	1	1	1	...	1
Controller parameters						
sfrd	15	5	4	3	...	0
b1d	0	-26373	-24822	-17453	...	31415
a0d	-32767	-32483	-32201	-31921	...	-23933
b0d	0	26373	24822	17453	...	-31415
Exp. sfrd	15	5	4	3	...	0
Exp. b1d	0	-26374	-24822	-17453	...	31416
Exp. a0d	-32767	-32483	-32201	-31921	...	-23934
Exp. b0d	0	26374	24822	17453	...	-31416

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±1,0000e+00
Tolerance a0d	±1,0000e+00
Tolerance b0d	±1,0000e+00

Test statistics	
Min CPU cycles	1430
Max CPU cycles	3258
Avg CPU cycles	2900

Verification: D FiP16 CPU TMS320F28379D

Date of Test 2026-06-22

Target controller TMS320F28379D

Test case: Inport test OK

Inport test for Control block D.

Test results						
Time step	1	2	3	4	...	201
CPU cycles	70	70	70	127	...	122
Inputs						
In (DSP)	0	0	0	0	...	0
D0 (DSP)	655	655	655	655	...	655
Enable (DSP)	0	0	0	1	...	1
In	0	0	0	0	...	0
D0	0.02	0.02	0.02	0.02	...	0.02
Enable	0	0	0	1	...	1
Parameters						
Kd	0.003					
fc	200					
ts_fact	1					
Outputs						
Out	0	0	0	-0.075	...	0.002
Exp. Out	0	0	0	-0.075	...	0.002
Out (DSP)	0	0	0	-2470	...	61
Exp. Out (DSP)	0	0	0	-2471	...	58

Test settings	
Tolerance Out	±3,0518e-04 (±10 LSB)

Test statistics	
Min CPU cycles	70
Max CPU cycles	127
Avg CPU cycles	121

Test case: Conversion test OK

Conversion test for Control block D.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kd	-10	-9.444	-8.889	-8.333	...	10
fc	0	13.889	27.778	41.667	...	500
ts_fact	1	1	1	1	...	1
Controller parameters						
sfrd	15	5	4	3	...	0
b1d	0	-26374	-24822	-17453	...	31416
a0d	-32767	-32483	-32201	-31921	...	-23934
b0d	0	26374	24822	17453	...	-31416
Exp. sfrd	15	5	4	3	...	0
Exp. b1d	0	-26374	-24822	-17453	...	31416
Exp. a0d	-32767	-32483	-32201	-31921	...	-23934
Exp. b0d	0	26374	24822	17453	...	-31416

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±0,0000e+00
Tolerance a0d	±0,0000e+00
Tolerance b0d	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block D.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kd	-10	-9.444	-8.889	-8.333	...	10
fc	0	13.889	27.778	41.667	...	500
ts_fact	1	1	1	1	...	1
Controller parameters						
sfrd	15	5	4	3	...	0
b1d	0	-26373	-24822	-17453	...	31415
a0d	-32767	-32483	-32201	-31921	...	-23933
b0d	0	26373	24822	17453	...	-31415
Exp. sfrd	15	5	4	3	...	0
Exp. b1d	0	-26374	-24822	-17453	...	31416
Exp. a0d	-32767	-32483	-32201	-31921	...	-23934
Exp. b0d	0	26374	24822	17453	...	-31416

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±1,0000e+00
Tolerance a0d	±1,0000e+00
Tolerance b0d	±1,0000e+00

Test statistics	
Min CPU cycles	2028
Max CPU cycles	8070
Avg CPU cycles	7162

Verification: D FiP16 CPU dsPIC33EP256MC502

Date of Test	2026-06-23
Target controller	dsPIC33EP256MC502

Test case: Inport test

OK

Inport test for Control block D.

Test results						
Time step	1	2	3	4	...	201
CPU cycles	52	52	52	95	...	99
Inputs						
In (DSP)	0	0	0	0	...	0
D0 (DSP)	655	655	655	655	...	655
Enable (DSP)	0	0	0	1	...	1
In	0	0	0	0	...	0
D0	0.02	0.02	0.02	0.02	...	0.02
Enable	0	0	0	1	...	1
Parameters						
Kd	0.003					
fc	200					
ts_fact	1					
Outputs						
Out	0	0	0	-0.075	...	0.002
Exp. Out	0	0	0	-0.075	...	0.002
Out (DSP)	0	0	0	-2470	...	61
Exp. Out (DSP)	0	0	0	-2471	...	58

Test settings	
Tolerance Out	±3,0518e-04 (±10 LSB)

Test statistics	
Min CPU cycles	52
Max CPU cycles	99
Avg CPU cycles	98

Test case: Conversion test

OK

Conversion test for Control block D.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kd	-10	-9.444	-8.889	-8.333	...	10
fc	0	13.889	27.778	41.667	...	500
ts_fact	1	1	1	1	...	1
Controller parameters						
sfrd	15	5	4	3	...	0
b1d	0	-26374	-24822	-17453	...	31416
a0d	-32767	-32483	-32201	-31921	...	-23934
b0d	0	26374	24822	17453	...	-31416
Exp. sfrd	15	5	4	3	...	0
Exp. b1d	0	-26374	-24822	-17453	...	31416
Exp. a0d	-32767	-32483	-32201	-31921	...	-23934
Exp. b0d	0	26374	24822	17453	...	-31416

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±0,0000e+00
Tolerance a0d	±0,0000e+00
Tolerance b0d	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block D.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kd	-10	-9.444	-8.889	-8.333	...	10
fc	0	13.889	27.778	41.667	...	500
ts_fact	1	1	1	1	...	1
Controller parameters						
sfrd	15	5	4	3	...	0
b1d	0	-26373	-24822	-17453	...	31415
a0d	-32767	-32483	-32201	-31921	...	-23933
b0d	0	26373	24822	17453	...	-31415
Exp. sfrd	15	5	4	3	...	0
Exp. b1d	0	-26374	-24822	-17453	...	31416
Exp. a0d	-32767	-32483	-32201	-31921	...	-23934
Exp. b0d	0	26374	24822	17453	...	-31416

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±1,0000e+00
Tolerance a0d	±1,0000e+00
Tolerance b0d	±1,0000e+00

Test statistics	
Min CPU cycles	6401
Max CPU cycles	35059
Avg CPU cycles	31162

Verification: D FiP32 CPU TMS320F28335

Date of Test 2026-06-19

Target controller TMS320F28335

Test case: Inport test OK

Inport test for Control block D.

Test results				
Time step	1	2	...	201
CPU cycles	87	87	...	252
Inputs				
In (DSP)	0	0	...	0
D0 (DSP)	42949673	42949673	...	42949673
Enable (DSP)	0	0	...	1
In	0	0	...	0
D0	0.02	0.02	...	0.02
Enable	0	0	...	1
Parameters				
Kd	0.003			
fc	200			
ts_fact	1			
Outputs				
Out	0	0	...	0.002
Exp. Out	0	0	...	0.002
Out (DSP)	0	0	...	3772137
Exp. Out (DSP)	0	0	...	3772137

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	87
Max CPU cycles	258
Avg CPU cycles	249

Test case: Conversion test OK

Conversion test for Control block D.

Test results				
Time step	1	2	...	37
Mask parameters				
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
ts_fact	1	1	...	1
Controller parameters				
sfrd	31	21	...	16
b1d	0	-1728437568	...	2058874161
a0d	-2147483647	-2128824851	...	-1568527835
b0d	0	1728437568	...	-2058874161
Exp. sfrd	31	21	...	16
Exp. b1d	0	-1728437568	...	2058874161
Exp. a0d	-2147483647	-2128824851	...	-1568527835
Exp. b0d	0	1728437568	...	-2058874161

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±0,0000e+00
Tolerance a0d	±0,0000e+00
Tolerance b0d	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block D.

Test results				
Time step	1	2	...	37
Mask parameters				
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
ts_fact	1	1	...	1
Controller parameters				
sfrd	31	21	...	16
b1d	0	-1728437632	...	2058874240
a0d	-2147483647	-2128824832	...	-1568527872
b0d	0	1728437632	...	-2058874240
Exp. sfrd	31	21	...	16
Exp. b1d	0	-1728437568	...	2058874161
Exp. a0d	-2147483647	-2128824851	...	-1568527835
Exp. b0d	0	1728437568	...	-2058874161

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±2,0000e+02
Tolerance a0d	±2,0000e+02
Tolerance b0d	±2,0000e+02

Test statistics	
Min CPU cycles	3469
Max CPU cycles	11682
Avg CPU cycles	10135

Verification: D FiP32 CPU TM4C123GH6

Date of Test 2026-06-19

Target controller TM4C123GH6

Test case: Inport test OK

Inport test for Control block D.

Test results				
Time step	1	2	...	201
CPU cycles	53	53	...	115
Inputs				
In (DSP)	0	0	...	0
D0 (DSP)	42949673	42949673	...	42949673
Enable (DSP)	0	0	...	1
In	0	0	...	0
D0	0.02	0.02	...	0.02
Enable	0	0	...	1
Parameters				
Kd	0.003			
fc	200			
ts_fact	1			
Outputs				
Out	0	0	...	0.002
Exp. Out	0	0	...	0.002
Out (DSP)	0	0	...	3772137
Exp. Out (DSP)	0	0	...	3772137

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	53
Max CPU cycles	119
Avg CPU cycles	114

Test case: Conversion test OK

Conversion test for Control block D.

Test results				
Time step	1	2	...	37
Mask parameters				
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
ts_fact	1	1	...	1
Controller parameters				
sfrd	31	21	...	16
b1d	0	-1728437568	...	2058874161
a0d	-2147483647	-2128824851	...	-1568527835
b0d	0	1728437568	...	-2058874161
Exp. sfrd	31	21	...	16
Exp. b1d	0	-1728437568	...	2058874161
Exp. a0d	-2147483647	-2128824851	...	-1568527835
Exp. b0d	0	1728437568	...	-2058874161

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±0,0000e+00
Tolerance a0d	±0,0000e+00
Tolerance b0d	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block D.

Test results				
Time step	1	2	...	37
Mask parameters				
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
ts_fact	1	1	...	1
Controller parameters				
sfrd	31	21	...	16
b1d	0	-1728437632	...	2058874240
a0d	-2147483647	-2128824832	...	-1568527872
b0d	0	1728437632	...	-2058874240
Exp. sfrd	31	21	...	16
Exp. b1d	0	-1728437568	...	2058874161
Exp. a0d	-2147483647	-2128824851	...	-1568527835
Exp. b0d	0	1728437568	...	-2058874161

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±2,0000e+02
Tolerance a0d	±2,0000e+02
Tolerance b0d	±2,0000e+02

Test statistics	
Min CPU cycles	1431
Max CPU cycles	5085
Avg CPU cycles	4311

Verification: D FiP32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test

OK

Inport test for Control block D.

Test results				
Time step	1	2	...	201
CPU cycles	86	86	...	151
Inputs				
In (DSP)	0	0	...	0
D0 (DSP)	42949673	42949673	...	42949673
Enable (DSP)	0	0	...	1
In	0	0	...	0
D0	0.02	0.02	...	0.02
Enable	0	0	...	1
Parameters				
Kd	0.003			
fc	200			
ts_fact	1			
Outputs				
Out	0	0	...	0.002
Exp. Out	0	0	...	0.002
Out (DSP)	0	0	...	3772137
Exp. Out (DSP)	0	0	...	3772137

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	86
Max CPU cycles	176
Avg CPU cycles	150

Test case: Conversion test

OK

Conversion test for Control block D.

Test results				
Time step	1	2	...	37
Mask parameters				
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
ts_fact	1	1	...	1
Controller parameters				
sfrd	31	21	...	16
b1d	0	-1728437568	...	2058874161
a0d	-2147483647	-2128824851	...	-1568527835
b0d	0	1728437568	...	-2058874161
Exp. sfrd	31	21	...	16
Exp. b1d	0	-1728437568	...	2058874161
Exp. a0d	-2147483647	-2128824851	...	-1568527835
Exp. b0d	0	1728437568	...	-2058874161

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±0,0000e+00
Tolerance a0d	±0,0000e+00
Tolerance b0d	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block D.

Test results				
Time step	1	2	...	37
Mask parameters				
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
ts_fact	1	1	...	1
Controller parameters				
sfrd	31	21	...	16
b1d	0	-1728437632	...	2058874240
a0d	-2147483647	-2128824832	...	-1568527872
b0d	0	1728437632	...	-2058874240
Exp. sfrd	31	21	...	16
Exp. b1d	0	-1728437568	...	2058874161
Exp. a0d	-2147483647	-2128824851	...	-1568527835
Exp. b0d	0	1728437568	...	-2058874161

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±2,0000e+02
Tolerance a0d	±2,0000e+02
Tolerance b0d	±2,0000e+02

Test statistics	
Min CPU cycles	2520
Max CPU cycles	4518
Avg CPU cycles	4141

Verification: D FiP32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for Control block D.

Test results				
Time step	1	2	...	201
CPU cycles	84	84	...	371
Inputs				
In (DSP)	0	0	...	0
D0 (DSP)	42949673	42949673	...	42949673
Enable (DSP)	0	0	...	1
In	0	0	...	0
D0	0.02	0.02	...	0.02
Enable	0	0	...	1
Parameters				
Kd	0.003			
fc	200			
ts_fact	1			
Outputs				
Out	0	0	...	0.002
Exp. Out	0	0	...	0.002
Out (DSP)	0	0	...	3772137
Exp. Out (DSP)	0	0	...	3772137

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	84
Max CPU cycles	430
Avg CPU cycles	369

Test case: Conversion test OK

Conversion test for Control block D.

Test results				
Time step	1	2	...	37
Mask parameters				
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
ts_fact	1	1	...	1
Controller parameters				
sfrd	31	21	...	16
b1d	0	-1728437568	...	2058874161
a0d	-2147483647	-2128824851	...	-1568527835
b0d	0	1728437568	...	-2058874161
Exp. sfrd	31	21	...	16
Exp. b1d	0	-1728437568	...	2058874161
Exp. a0d	-2147483647	-2128824851	...	-1568527835
Exp. b0d	0	1728437568	...	-2058874161

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±0,0000e+00
Tolerance a0d	±0,0000e+00
Tolerance b0d	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block D.

Test results				
Time step	1	2	...	37
Mask parameters				
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
ts_fact	1	1	...	1
Controller parameters				
sfrd	31	21	...	16
b1d	0	-1728437632	...	2058874240
a0d	-2147483647	-2128824832	...	-1568527872
b0d	0	1728437632	...	-2058874240
Exp. sfrd	31	21	...	16
Exp. b1d	0	-1728437568	...	2058874161
Exp. a0d	-2147483647	-2128824851	...	-1568527835
Exp. b0d	0	1728437568	...	-2058874161

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±2,0000e+02
Tolerance a0d	±2,0000e+02
Tolerance b0d	±2,0000e+02

Test statistics	
Min CPU cycles	7826
Max CPU cycles	21007
Avg CPU cycles	18923

Verification: D FiP32 CPU PIC32MX170F256

Date of Test 2026-06-19

Target controller PIC32MX170F256

Test case: Inport test OK

Inport test for Control block D.

Test results				
Time step	1	2	...	201
CPU cycles	37	37	...	96
Inputs				
In (DSP)	0	0	...	0
D0 (DSP)	42949673	42949673	...	42949673
Enable (DSP)	0	0	...	1
In	0	0	...	0
D0	0.02	0.02	...	0.02
Enable	0	0	...	1
Parameters				
Kd	0.003			
fc	200			
ts_fact	1			
Outputs				
Out	0	0	...	0.002
Exp. Out	0	0	...	0.002
Out (DSP)	0	0	...	3772137
Exp. Out (DSP)	0	0	...	3772137

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	37
Max CPU cycles	101
Avg CPU cycles	95

Test case: Conversion test OK

Conversion test for Control block D.

Test results				
Time step	1	2	...	37
Mask parameters				
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
ts_fact	1	1	...	1
Controller parameters				
sfrd	31	21	...	16
b1d	0	-1728437568	...	2058874161
a0d	-2147483647	-2128824851	...	-1568527835
b0d	0	1728437568	...	-2058874161
Exp. sfrd	31	21	...	16
Exp. b1d	0	-1728437568	...	2058874161
Exp. a0d	-2147483647	-2128824851	...	-1568527835
Exp. b0d	0	1728437568	...	-2058874161

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±0,0000e+00
Tolerance a0d	±0,0000e+00
Tolerance b0d	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block D.

Test results				
Time step	1	2	...	37
Mask parameters				
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
ts_fact	1	1	...	1
Controller parameters				
sfrd	31	21	...	16
b1d	0	-1728437632	...	2058874240
a0d	-2147483647	-2128824832	...	-1568527872
b0d	0	1728437632	...	-2058874240
Exp. sfrd	31	21	...	16
Exp. b1d	0	-1728437568	...	2058874161
Exp. a0d	-2147483647	-2128824851	...	-1568527835
Exp. b0d	0	1728437568	...	-2058874161

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±2,0000e+02
Tolerance a0d	±2,0000e+02
Tolerance b0d	±2,0000e+02

Test statistics	
Min CPU cycles	2913
Max CPU cycles	7307
Avg CPU cycles	6491

Verification: D FiP32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for Control block D.

Test results				
Time step	1	2	...	201
CPU cycles	103	93	...	151
Inputs				
In (DSP)	0	0	...	0
D0 (DSP)	42949673	42949673	...	42949673
Enable (DSP)	0	0	...	1
In	0	0	...	0
D0	0.02	0.02	...	0.02
Enable	0	0	...	1
Parameters				
Kd	0.003			
fc	200			
ts_fact	1			
Outputs				
Out	0	0	...	0.002
Exp. Out	0	0	...	0.002
Out (DSP)	0	0	...	3772137
Exp. Out (DSP)	0	0	...	3772137

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	93
Max CPU cycles	191
Avg CPU cycles	150

Test case: Conversion test OK

Conversion test for Control block D.

Test results				
Time step	1	2	...	37
Mask parameters				
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
ts_fact	1	1	...	1
Controller parameters				
sfrd	31	21	...	16
b1d	0	-1728437568	...	2058874161
a0d	-2147483647	-2128824851	...	-1568527835
b0d	0	1728437568	...	-2058874161
Exp. sfrd	31	21	...	16
Exp. b1d	0	-1728437568	...	2058874161
Exp. a0d	-2147483647	-2128824851	...	-1568527835
Exp. b0d	0	1728437568	...	-2058874161

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±0,0000e+00
Tolerance a0d	±0,0000e+00
Tolerance b0d	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block D.

Test results				
Time step	1	2	...	37
Mask parameters				
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
ts_fact	1	1	...	1
Controller parameters				
sfrd	31	21	...	16
b1d	0	-1728437632	...	2058874240
a0d	-2147483647	-2128824832	...	-1568527872
b0d	0	1728437632	...	-2058874240
Exp. sfrd	31	21	...	16
Exp. b1d	0	-1728437568	...	2058874161
Exp. a0d	-2147483647	-2128824851	...	-1568527835
Exp. b0d	0	1728437568	...	-2058874161

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±2,0000e+02
Tolerance a0d	±2,0000e+02
Tolerance b0d	±2,0000e+02

Test statistics	
Min CPU cycles	2080
Max CPU cycles	3936
Avg CPU cycles	3577

Verification: D FiP32 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test

OK

Inport test for Control block D.

Test results				
Time step	1	2	...	201
CPU cycles	71	71	...	227
Inputs				
In (DSP)	0	0	...	0
D0 (DSP)	42949673	42949673	...	42949673
Enable (DSP)	0	0	...	1
In	0	0	...	0
D0	0.02	0.02	...	0.02
Enable	0	0	...	1
Parameters				
Kd	0.003			
fc	200			
ts_fact	1			
Outputs				
Out	0	0	...	0.002
Exp. Out	0	0	...	0.002
Out (DSP)	0	0	...	3772137
Exp. Out (DSP)	0	0	...	3772137

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	71
Max CPU cycles	231
Avg CPU cycles	224

Test case: Conversion test

OK

Conversion test for Control block D.

Test results				
Time step	1	2	...	37
Mask parameters				
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
ts_fact	1	1	...	1
Controller parameters				
sfrd	31	21	...	16
b1d	0	-1728437568	...	2058874161
a0d	-2147483647	-2128824851	...	-1568527835
b0d	0	1728437568	...	-2058874161
Exp. sfrd	31	21	...	16
Exp. b1d	0	-1728437568	...	2058874161
Exp. a0d	-2147483647	-2128824851	...	-1568527835
Exp. b0d	0	1728437568	...	-2058874161

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±0,0000e+00
Tolerance a0d	±0,0000e+00
Tolerance b0d	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block D.

Test results				
Time step	1	2	...	37
Mask parameters				
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
ts_fact	1	1	...	1
Controller parameters				
sfrd	31	21	...	16
b1d	0	-1728437632	...	2058874240
a0d	-2147483647	-2128824832	...	-1568527872
b0d	0	1728437632	...	-2058874240
Exp. sfrd	31	21	...	16
Exp. b1d	0	-1728437568	...	2058874161
Exp. a0d	-2147483647	-2128824851	...	-1568527835
Exp. b0d	0	1728437568	...	-2058874161

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±2,0000e+02
Tolerance a0d	±2,0000e+02
Tolerance b0d	±2,0000e+02

Test statistics	
Min CPU cycles	2457
Max CPU cycles	8937
Avg CPU cycles	7718

Verification: D FiP32 CPU dsPIC33EP256MC502

Date of Test	2026-06-23
Target controller	dsPIC33EP256MC502

Test case: Inport test

OK

Inport test for Control block D.

Test results				
Time step	1	2	...	201
CPU cycles	70	70	...	741
Inputs				
In (DSP)	0	0	...	0
D0 (DSP)	42949673	42949673	...	42949673
Enable (DSP)	0	0	...	1
In	0	0	...	0
D0	0.02	0.02	...	0.02
Enable	0	0	...	1
Parameters				
Kd	0.003			
fc	200			
ts_fact	1			
Outputs				
Out	0	0	...	0.002
Exp. Out	0	0	...	0.002
Out (DSP)	0	0	...	3772137
Exp. Out (DSP)	0	0	...	3772137

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	70
Max CPU cycles	750
Avg CPU cycles	733

Test case: Conversion test

OK

Conversion test for Control block D.

Test results				
Time step	1	2	...	37
Mask parameters				
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
ts_fact	1	1	...	1
Controller parameters				
sfrd	31	21	...	16
b1d	0	-1728437568	...	2058874161
a0d	-2147483647	-2128824851	...	-1568527835
b0d	0	1728437568	...	-2058874161
Exp. sfrd	31	21	...	16
Exp. b1d	0	-1728437568	...	2058874161
Exp. a0d	-2147483647	-2128824851	...	-1568527835
Exp. b0d	0	1728437568	...	-2058874161

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±0,0000e+00
Tolerance a0d	±0,0000e+00
Tolerance b0d	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block D.

Test results				
Time step	1	2	...	37
Mask parameters				
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
ts_fact	1	1	...	1
Controller parameters				
sfrd	31	21	...	16
b1d	0	-1728437632	...	2058874240
a0d	-2147483647	-2128824832	...	-1568527872
b0d	0	1728437632	...	-2058874240
Exp. sfrd	31	21	...	16
Exp. b1d	0	-1728437568	...	2058874161
Exp. a0d	-2147483647	-2128824851	...	-1568527835
Exp. b0d	0	1728437568	...	-2058874161

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±2,0000e+02
Tolerance a0d	±2,0000e+02
Tolerance b0d	±2,0000e+02

Test statistics	
Min CPU cycles	7460
Max CPU cycles	36680
Avg CPU cycles	31565

Verification: D Float32 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for Control block D.

Test results				
Time step	1	2	...	201
CPU cycles	81	81	...	118
Inputs				
In (DSP)	0	0	...	0
D0 (DSP)	0.02	0.02	...	0.02
Enable (DSP)	0	0	...	1
In	0	0	...	0
D0	0.02	0.02	...	0.02
Enable	0	0	...	1
Parameters				
Kd	0.003			
fc	200			
ts_fact	1			
Outputs				
Out	0	0	...	0.002
Exp. Out	0	0	...	0.002
Out (DSP)	0	0	...	0.002
Exp. Out (DSP)	0	0	...	0.002

Test settings	
Tolerance Out	±9,3132e-06 (±20000 LSB)

Test statistics	
Min CPU cycles	81
Max CPU cycles	123
Avg CPU cycles	117

Test case: Conversion test OK

Conversion test for Control block D.

Test results				
Time step	1	2	...	37
Mask parameters				
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
ts_fact	1	1	...	1
Controller parameters				
b1d	0	-824.183	...	31415.927
a0d	-1	-0.991	...	-0.73
b0d	0	824.183	...	-31415.927
Exp. b1d	0	-824.183	...	31415.927
Exp. a0d	-1	-0.991	...	-0.73
Exp. b0d	0	824.183	...	-31415.927

Test settings	
Tolerance b1d	±0,0000e+00
Tolerance a0d	±1,0000e-15
Tolerance b0d	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block D.

Test results				
Time step	1	2	...	37
Mask parameters				
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
ts_fact	1	1	...	1
Controller parameters				
b1d	0	-824.183	...	31415.928
a0d	-1	-0.991	...	-0.73
b0d	0	824.183	...	-31415.928
Exp. b1d	0	-824.183	...	31415.927
Exp. a0d	-1	-0.991	...	-0.73
Exp. b0d	0	824.183	...	-31415.927

Test settings	
Tolerance b1d	±3,0000e-03
Tolerance a0d	±1,0000e-07
Tolerance b0d	±3,0000e-03

Test statistics	
Min CPU cycles	2140
Max CPU cycles	2483
Avg CPU cycles	2463

Verification: D Float32 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for Control block D.

Test results				
Time step	1	2	...	201
CPU cycles	45	45	...	87
Inputs				
In (DSP)	0	0	...	0
D0 (DSP)	0.02	0.02	...	0.02
Enable (DSP)	0	0	...	1
In	0	0	...	0
D0	0.02	0.02	...	0.02
Enable	0	0	...	1
Parameters				
Kd	0.003			
fc	200			
ts_fact	1			
Outputs				
Out	0	0	...	0.002
Exp. Out	0	0	...	0.002
Out (DSP)	0	0	...	0.002
Exp. Out (DSP)	0	0	...	0.002

Test settings	
Tolerance Out	±9,3132e-06 (±20000 LSB)

Test statistics	
Min CPU cycles	45
Max CPU cycles	91
Avg CPU cycles	86

Test case: Conversion test OK

Conversion test for Control block D.

Test results				
Time step	1	2	...	37
Mask parameters				
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
ts_fact	1	1	...	1
Controller parameters				
b1d	0	-824.183	...	31415.927
a0d	-1	-0.991	...	-0.73
b0d	0	824.183	...	-31415.927
Exp. b1d	0	-824.183	...	31415.927
Exp. a0d	-1	-0.991	...	-0.73
Exp. b0d	0	824.183	...	-31415.927

Test settings	
Tolerance b1d	±0,0000e+00
Tolerance a0d	±1,0000e-15
Tolerance b0d	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block D.

Test results				
Time step	1	2	...	37
Mask parameters				
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
ts_fact	1	1	...	1
Controller parameters				
b1d	0	-824.183	...	31415.928
a0d	-1	-0.991	...	-0.73
b0d	0	824.183	...	-31415.928
Exp. b1d	0	-824.183	...	31415.927
Exp. a0d	-1	-0.991	...	-0.73
Exp. b0d	0	824.183	...	-31415.927

Test settings	
Tolerance b1d	±3,0000e-03
Tolerance a0d	±1,0000e-07
Tolerance b0d	±3,0000e-03

Test statistics	
Min CPU cycles	1009
Max CPU cycles	1053
Avg CPU cycles	1051

Verification: D Float32 CPU STM32G474RE

Date of Test 2026-06-19

Target controller STM32G474RE

Test case: Inport test OK

Inport test for Control block D.

Test results				
Time step	1	2	...	201
CPU cycles	73	73	...	118
Inputs				
In (DSP)	0	0	...	0
D0 (DSP)	0.02	0.02	...	0.02
Enable (DSP)	0	0	...	1
In	0	0	...	0
D0	0.02	0.02	...	0.02
Enable	0	0	...	1
Parameters				
Kd	0.003			
fc	200			
ts_fact	1			
Outputs				
Out	0	0	...	0.002
Exp. Out	0	0	...	0.002
Out (DSP)	0	0	...	0.002
Exp. Out (DSP)	0	0	...	0.002

Test settings	
Tolerance Out	±9,3132e-06 (±20000 LSB)

Test statistics	
Min CPU cycles	73
Max CPU cycles	135
Avg CPU cycles	117

Test case: Conversion test OK

Conversion test for Control block D.

Test results				
Time step	1	2	...	37
Mask parameters				
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
ts_fact	1	1	...	1
Controller parameters				
b1d	0	-824.183	...	31415.927
a0d	-1	-0.991	...	-0.73
b0d	0	824.183	...	-31415.927
Exp. b1d	0	-824.183	...	31415.927
Exp. a0d	-1	-0.991	...	-0.73
Exp. b0d	0	824.183	...	-31415.927

Test settings	
Tolerance b1d	±0,0000e+00
Tolerance a0d	±1,0000e-15
Tolerance b0d	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block D.

Test results				
Time step	1	2	...	37
Mask parameters				
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
ts_fact	1	1	...	1
Controller parameters				
b1d	0	-824.183	...	31415.928
a0d	-1	-0.991	...	-0.73
b0d	0	824.183	...	-31415.928
Exp. b1d	0	-824.183	...	31415.927
Exp. a0d	-1	-0.991	...	-0.73
Exp. b0d	0	824.183	...	-31415.927

Test settings	
Tolerance b1d	±3,0000e-03
Tolerance a0d	±1,0000e-07
Tolerance b0d	±3,0000e-03

Test statistics	
Min CPU cycles	1172
Max CPU cycles	1250
Avg CPU cycles	1243

Verification: D Float32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for Control block D.

Test results				
Time step	1	2	...	201
CPU cycles	77	77	...	870
Inputs				
In (DSP)	0	0	...	0
D0 (DSP)	0.02	0.02	...	0.02
Enable (DSP)	0	0	...	1
In	0	0	...	0
D0	0.02	0.02	...	0.02
Enable	0	0	...	1
Parameters				
Kd	0.003			
fc	200			
ts_fact	1			
Outputs				
Out	0	0	...	0.002
Exp. Out	0	0	...	0.002
Out (DSP)	0	0	...	0.002
Exp. Out (DSP)	0	0	...	0.002

Test settings	
Tolerance Out	±9,3132e-06 (±20000 LSB)

Test statistics	
Min CPU cycles	77
Max CPU cycles	1034
Avg CPU cycles	927

Test case: Conversion test OK

Conversion test for Control block D.

Test results				
Time step	1	2	...	37
Mask parameters				
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
ts_fact	1	1	...	1
Controller parameters				
b1d	0	-824.183	...	31415.927
a0d	-1	-0.991	...	-0.73
b0d	0	824.183	...	-31415.927
Exp. b1d	0	-824.183	...	31415.927
Exp. a0d	-1	-0.991	...	-0.73
Exp. b0d	0	824.183	...	-31415.927

Test settings	
Tolerance b1d	±0,0000e+00
Tolerance a0d	±1,0000e-15
Tolerance b0d	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block D.

Test results				
Time step	1	2	...	37
Mask parameters				
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
ts_fact	1	1	...	1
Controller parameters				
b1d	0	-824.183	...	31415.928
a0d	-1	-0.991	...	-0.73
b0d	0	824.183	...	-31415.928
Exp. b1d	0	-824.183	...	31415.927
Exp. a0d	-1	-0.991	...	-0.73
Exp. b0d	0	824.183	...	-31415.927

Test settings	
Tolerance b1d	±3,0000e-03
Tolerance a0d	±1,0000e-07
Tolerance b0d	±3,0000e-03

Test statistics	
Min CPU cycles	2958
Max CPU cycles	5975
Avg CPU cycles	5801

Verification: D Float32 CPU PIC32MX170F256

Date of Test 2026-06-19

Target controller PIC32MX170F256

Test case: Inport test OK

Inport test for Control block D.

Test results				
Time step	1	2	...	201
CPU cycles	63	63	...	343
Inputs				
In (DSP)	0	0	...	0
D0 (DSP)	0.02	0.02	...	0.02
Enable (DSP)	0	0	...	1
In	0	0	...	0
D0	0.02	0.02	...	0.02
Enable	0	0	...	1
Parameters				
Kd	0.003			
fc	200			
ts_fact	1			
Outputs				
Out	0	0	...	0.002
Exp. Out	0	0	...	0.002
Out (DSP)	0	0	...	0.002
Exp. Out (DSP)	0	0	...	0.002

Test settings	
Tolerance Out	±9,3132e-06 (±20000 LSB)

Test statistics	
Min CPU cycles	63
Max CPU cycles	433
Avg CPU cycles	369

Test case: Conversion test OK

Conversion test for Control block D.

Test results				
Time step	1	2	...	37
Mask parameters				
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
ts_fact	1	1	...	1
Controller parameters				
b1d	0	-824.183	...	31415.927
a0d	-1	-0.991	...	-0.73
b0d	0	824.183	...	-31415.927
Exp. b1d	0	-824.183	...	31415.927
Exp. a0d	-1	-0.991	...	-0.73
Exp. b0d	0	824.183	...	-31415.927

Test settings	
Tolerance b1d	±0,0000e+00
Tolerance a0d	±1,0000e-15
Tolerance b0d	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block D.

Test results				
Time step	1	2	...	37
Mask parameters				
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
ts_fact	1	1	...	1
Controller parameters				
b1d	0	-824.183	...	31415.928
a0d	-1	-0.991	...	-0.73
b0d	0	824.183	...	-31415.928
Exp. b1d	0	-824.183	...	31415.927
Exp. a0d	-1	-0.991	...	-0.73
Exp. b0d	0	824.183	...	-31415.927

Test settings	
Tolerance b1d	±3,0000e-03
Tolerance a0d	±1,0000e-07
Tolerance b0d	±3,0000e-03

Test statistics	
Min CPU cycles	964
Max CPU cycles	1208
Avg CPU cycles	1195

Verification: D Float32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for Control block D.

Test results				
Time step	1	2	...	201
CPU cycles	81	64	...	106
Inputs				
In (DSP)	0	0	...	0
D0 (DSP)	0.02	0.02	...	0.02
Enable (DSP)	0	0	...	1
In	0	0	...	0
D0	0.02	0.02	...	0.02
Enable	0	0	...	1
Parameters				
Kd	0.003			
fc	200			
ts_fact	1			
Outputs				
Out	0	0	...	0.002
Exp. Out	0	0	...	0.002
Out (DSP)	0	0	...	0.002
Exp. Out (DSP)	0	0	...	0.002

Test settings	
Tolerance Out	±9,3132e-06 (±20000 LSB)

Test statistics	
Min CPU cycles	64
Max CPU cycles	128
Avg CPU cycles	105

Test case: Conversion test OK

Conversion test for Control block D.

Test results				
Time step	1	2	...	37
Mask parameters				
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
ts_fact	1	1	...	1
Controller parameters				
b1d	0	-824.183	...	31415.927
a0d	-1	-0.991	...	-0.73
b0d	0	824.183	...	-31415.927
Exp. b1d	0	-824.183	...	31415.927
Exp. a0d	-1	-0.991	...	-0.73
Exp. b0d	0	824.183	...	-31415.927

Test settings	
Tolerance b1d	±0,0000e+00
Tolerance a0d	±1,0000e-15
Tolerance b0d	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block D.

Test results				
Time step	1	2	...	37
Mask parameters				
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
ts_fact	1	1	...	1
Controller parameters				
b1d	0	-824.183	...	31415.928
a0d	-1	-0.991	...	-0.73
b0d	0	824.183	...	-31415.928
Exp. b1d	0	-824.183	...	31415.927
Exp. a0d	-1	-0.991	...	-0.73
Exp. b0d	0	824.183	...	-31415.927

Test settings	
Tolerance b1d	±3,0000e-03
Tolerance a0d	±1,0000e-07
Tolerance b0d	±3,0000e-03

Test statistics	
Min CPU cycles	1051
Max CPU cycles	1151
Avg CPU cycles	1055

Verification: D Float32 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for Control block D.

Test results				
Time step	1	2	...	201
CPU cycles	74	74	...	123
Inputs				
In (DSP)	0	0	...	0
D0 (DSP)	0.02	0.02	...	0.02
Enable (DSP)	0	0	...	1
In	0	0	...	0
D0	0.02	0.02	...	0.02
Enable	0	0	...	1
Parameters				
Kd	0.003			
fc	200			
ts_fact	1			
Outputs				
Out	0	0	...	0.002
Exp. Out	0	0	...	0.002
Out (DSP)	0	0	...	0.002
Exp. Out (DSP)	0	0	...	0.002

Test settings	
Tolerance Out	±9,3132e-06 (±20000 LSB)

Test statistics	
Min CPU cycles	74
Max CPU cycles	124
Avg CPU cycles	122

Test case: Conversion test OK

Conversion test for Control block D.

Test results				
Time step	1	2	...	37
Mask parameters				
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
ts_fact	1	1	...	1
Controller parameters				
b1d	0	-824.183	...	31415.927
a0d	-1	-0.991	...	-0.73
b0d	0	824.183	...	-31415.927
Exp. b1d	0	-824.183	...	31415.927
Exp. a0d	-1	-0.991	...	-0.73
Exp. b0d	0	824.183	...	-31415.927

Test settings	
Tolerance b1d	±0,0000e+00
Tolerance a0d	±1,0000e-15
Tolerance b0d	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block D.

Test results				
Time step	1	2	...	37
Mask parameters				
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
ts_fact	1	1	...	1
Controller parameters				
b1d	0	-824.183	...	31415.928
a0d	-1	-0.991	...	-0.73
b0d	0	824.183	...	-31415.928
Exp. b1d	0	-824.183	...	31415.927
Exp. a0d	-1	-0.991	...	-0.73
Exp. b0d	0	824.183	...	-31415.927

Test settings	
Tolerance b1d	±3,0000e-03
Tolerance a0d	±1,0000e-07
Tolerance b0d	±3,0000e-03

Test statistics	
Min CPU cycles	1571
Max CPU cycles	1848
Avg CPU cycles	1830

Verification: D Float32 CPU dsPIC33EP256MC502

Date of Test 2026-06-23

Target controller dsPIC33EP256MC502

Test case: Inport test OK

Inport test for Control block D.

Test results				
Time step	1	2	...	201
CPU cycles	63	63	...	937
Inputs				
In (DSP)	0	0	...	0
D0 (DSP)	0.02	0.02	...	0.02
Enable (DSP)	0	0	...	1
In	0	0	...	0
D0	0.02	0.02	...	0.02
Enable	0	0	...	1
Parameters				
Kd	0.003			
fc	200			
ts_fact	1			
Outputs				
Out	0	0	...	0.002
Exp. Out	0	0	...	0.002
Out (DSP)	0	0	...	0.002
Exp. Out (DSP)	0	0	...	0.002

Test settings	
Tolerance Out	±9,3132e-06 (±20000 LSB)

Test statistics	
Min CPU cycles	63
Max CPU cycles	1274
Avg CPU cycles	1005

Test case: Conversion test OK

Conversion test for Control block D.

Test results				
Time step	1	2	...	37
Mask parameters				
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
ts_fact	1	1	...	1
Controller parameters				
b1d	0	-824.183	...	31415.927
a0d	-1	-0.991	...	-0.73
b0d	0	824.183	...	-31415.927
Exp. b1d	0	-824.183	...	31415.927
Exp. a0d	-1	-0.991	...	-0.73
Exp. b0d	0	824.183	...	-31415.927

Test settings	
Tolerance b1d	±0,0000e+00
Tolerance a0d	±1,0000e-15
Tolerance b0d	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block D.

Test results				
Time step	1	2	...	37
Mask parameters				
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
ts_fact	1	1	...	1
Controller parameters				
b1d	0	-824.183	...	31415.928
a0d	-1	-0.991	...	-0.73
b0d	0	824.183	...	-31415.928
Exp. b1d	0	-824.183	...	31415.927
Exp. a0d	-1	-0.991	...	-0.73
Exp. b0d	0	824.183	...	-31415.927

Test settings	
Tolerance b1d	±3,0000e-03
Tolerance a0d	±1,0000e-07
Tolerance b0d	±3,0000e-03

Test statistics	
Min CPU cycles	3639
Max CPU cycles	7392
Avg CPU cycles	7022

Block: Delay



Output delay by one sample time interval.

Inports	
In	Input In(k)

Outports	
Out	Output Out(k)=In(k-1)

Mask Parameters		
Name	**ID**	**Description**
ts_fact	1	Multiplication factor of base sampling time (in integer format)

Implementations:

Bool	Boolean Integration
FiP16	16 Bit Fixed Point Implementation
FiP32	32 Bit Fixed Point Implementation
Float32	32 Bit Floating Point Implementation
Float64	64 Bit Floating Point Implementation

Implementation: Bool

Boolean Integration

Inports Data Type	
In	bool

Outports Data Type	
Out	bool

Implementation: FiP16

16 Bit Fixed Point Implementation

Inports Data Type	
In	int16

Outports Data Type	
Out	int16

Implementation: FiP32

32 Bit Fixed Point Implementation

Inports Data Type	
In	int32

Outports Data Type	
Out	int32

Implementation: Float32

32 Bit Floating Point Implementation

Inports Data Type	
In	float32

Outports Data Type	
Out	float32

Implementation: Float64

64 Bit Floating Point Implementation

Inports Data Type	
In	float64

Outports Data Type	
Out	float64

Verification: Delay FiP16 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test **OK**

Inport test for Control block Delay.

Test results						
Time step	1	2	3	4	...	18
CPU cycles	56	56	56	56	...	56
Inputs						
In (DSP)	0	32767	32767	32767	...	0
In	0	1	1	1.1	...	0
Parameters						
ts_fact	1					
Outputs						
Out	0	0	1	1	...	0
Exp. Out	0	0	1	1	...	0
Out (DSP)	0	0	32767	32767	...	0
Exp. Out (DSP)	0	0	32767	32767	...	0

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	56
Max CPU cycles	56
Avg CPU cycles	56

Verification: Delay FiP16 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test **OK**

Inport test for Control block Delay.

Test results						
Time step	1	2	3	4	...	18
CPU cycles	25	25	25	25	...	25
Inputs						
In (DSP)	0	32767	32767	32767	...	0
In	0	1	1	1.1	...	0
Parameters						
ts_fact	1					
Outputs						
Out	0	0	1	1	...	0
Exp. Out	0	0	1	1	...	0
Out (DSP)	0	0	32767	32767	...	0
Exp. Out (DSP)	0	0	32767	32767	...	0

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	25
Max CPU cycles	25
Avg CPU cycles	25

Verification: Delay FiP16 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test **OK**

Inport test for Control block Delay.

Test results						
Time step	1	2	3	4	...	18
CPU cycles	61	61	61	61	...	61
Inputs						
In (DSP)	0	32767	32767	32767	...	0
In	0	1	1	1.1	...	0
Parameters						
ts_fact	1					
Outputs						
Out	0	0	1	1	...	0
Exp. Out	0	0	1	1	...	0
Out (DSP)	0	0	32767	32767	...	0
Exp. Out (DSP)	0	0	32767	32767	...	0

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	61
Max CPU cycles	61
Avg CPU cycles	61

Verification: Delay FiP16 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test **OK**

Inport test for Control block Delay.

Test results						
Time step	1	2	3	4	...	18
CPU cycles	51	51	51	51	...	51
Inputs						
In (DSP)	0	32767	32767	32767	...	0
In	0	1	1	1.1	...	0
Parameters						
ts_fact	1					
Outputs						
Out	0	0	1	1	...	0
Exp. Out	0	0	1	1	...	0
Out (DSP)	0	0	32767	32767	...	0
Exp. Out (DSP)	0	0	32767	32767	...	0

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	51
Max CPU cycles	51
Avg CPU cycles	51

Verification: Delay FiP16 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test **OK**

Inport test for Control block Delay.

Test results						
Time step	1	2	3	4	...	18
CPU cycles	30	30	30	30	...	30
Inputs						
In (DSP)	0	32767	32767	32767	...	0
In	0	1	1	1.1	...	0
Parameters						
ts_fact	1					
Outputs						
Out	0	0	1	1	...	0
Exp. Out	0	0	1	1	...	0
Out (DSP)	0	0	32767	32767	...	0
Exp. Out (DSP)	0	0	32767	32767	...	0

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	30
Max CPU cycles	30
Avg CPU cycles	30

Verification: Delay FiP16 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test **OK**

Inport test for Control block Delay.

Test results						
Time step	1	2	3	4	...	18
CPU cycles	65	54	54	54	...	54
Inputs						
In (DSP)	0	32767	32767	32767	...	0
In	0	1	1	1.1	...	0
Parameters						
ts_fact	1					
Outputs						
Out	0	0	1	1	...	0
Exp. Out	0	0	1	1	...	0
Out (DSP)	0	0	32767	32767	...	0
Exp. Out (DSP)	0	0	32767	32767	...	0

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	54
Max CPU cycles	65
Avg CPU cycles	54

Verification: Delay FiP16 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for Control block Delay.

Test results						
Time step	1	2	3	4	...	18
CPU cycles	43	43	43	43	...	43
Inputs						
In (DSP)	0	32767	32767	32767	...	0
In	0	1	1	1.1	...	0
Parameters						
ts_fact	1					
Outputs						
Out	0	0	1	1	...	0
Exp. Out	0	0	1	1	...	0
Out (DSP)	0	0	32767	32767	...	0
Exp. Out (DSP)	0	0	32767	32767	...	0

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	43
Max CPU cycles	43
Avg CPU cycles	43

Verification: Delay FiP16 CPU dsPIC33EP256MC502

Date of Test	2026-06-23
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for Control block Delay.

Test results						
Time step	1	2	3	4	...	18
CPU cycles	39	39	39	39	...	39
Inputs						
In (DSP)	0	32767	32767	32767	...	0
In	0	1	1	1.1	...	0
Parameters						
ts_fact	1					
Outputs						
Out	0	0	1	1	...	0
Exp. Out	0	0	1	1	...	0
Out (DSP)	0	0	32767	32767	...	0
Exp. Out (DSP)	0	0	32767	32767	...	0

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	39
Max CPU cycles	39
Avg CPU cycles	39

Verification: Delay FiP32 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for Control block Delay.

Test results				
Time step	1	2	...	18
CPU cycles	56	56	...	56
Inputs				
In (DSP)	0	2147483647	...	0
In	0	1	...	0
Parameters				
ts_fact	1			
Outputs				
Out	0	0	...	0
Exp. Out	0	0	...	0
Out (DSP)	0	0	...	0
Exp. Out (DSP)	0	0	...	0

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	56
Max CPU cycles	56
Avg CPU cycles	56

Verification: Delay FiP32 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test **OK**

Inport test for Control block Delay.

Test results				
Time step	1	2	...	18
CPU cycles	25	25	...	25
Inputs				
In (DSP)	0	2147483647	...	0
In	0	1	...	0
Parameters				
ts_fact	1			
Outputs				
Out	0	0	...	0
Exp. Out	0	0	...	0
Out (DSP)	0	0	...	0
Exp. Out (DSP)	0	0	...	0

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	25
Max CPU cycles	25
Avg CPU cycles	25

Verification: Delay FiP32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test **OK**

Inport test for Control block Delay.

Test results				
Time step	1	2	...	18
CPU cycles	58	58	...	58
Inputs				
In (DSP)	0	2147483647	...	0
In	0	1	...	0
Parameters				
ts_fact	1			
Outputs				
Out	0	0	...	0
Exp. Out	0	0	...	0
Out (DSP)	0	0	...	0
Exp. Out (DSP)	0	0	...	0

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	58
Max CPU cycles	58
Avg CPU cycles	58

Verification: Delay FiP32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for Control block Delay.

Test results				
Time step	1	2	...	18
CPU cycles	50	50	...	50
Inputs				
In (DSP)	0	2147483647	...	0
In	0	1	...	0
Parameters				
ts_fact	1			
Outputs				
Out	0	0	...	0
Exp. Out	0	0	...	0
Out (DSP)	0	0	...	0
Exp. Out (DSP)	0	0	...	0

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	50
Max CPU cycles	50
Avg CPU cycles	50

Verification: Delay FiP32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for Control block Delay.

Test results				
Time step	1	2	...	18
CPU cycles	30	30	...	30
Inputs				
In (DSP)	0	2147483647	...	0
In	0	1	...	0
Parameters				
ts_fact	1			
Outputs				
Out	0	0	...	0
Exp. Out	0	0	...	0
Out (DSP)	0	0	...	0
Exp. Out (DSP)	0	0	...	0

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	30
Max CPU cycles	30
Avg CPU cycles	30

Verification: Delay FiP32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for Control block Delay.

Test results				
Time step	1	2	...	18
CPU cycles	54	54	...	54
Inputs				
In (DSP)	0	2147483647	...	0
In	0	1	...	0
Parameters				
ts_fact	1			
Outputs				
Out	0	0	...	0
Exp. Out	0	0	...	0
Out (DSP)	0	0	...	0
Exp. Out (DSP)	0	0	...	0

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	54
Max CPU cycles	54
Avg CPU cycles	54

Verification: Delay FiP32 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for Control block Delay.

Test results				
Time step	1	2	...	18
CPU cycles	45	45	...	45
Inputs				
In (DSP)	0	2147483647	...	0
In	0	1	...	0
Parameters				
ts_fact	1			
Outputs				
Out	0	0	...	0
Exp. Out	0	0	...	0
Out (DSP)	0	0	...	0
Exp. Out (DSP)	0	0	...	0

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	45
Max CPU cycles	45
Avg CPU cycles	45

Verification: Delay FiP32 CPU dsPIC33EP256MC502

Date of Test	2026-06-23
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for Control block Delay.

Test results				
Time step	1	2	...	18
CPU cycles	43	43	...	43
Inputs				
In (DSP)	0	2147483647	...	0
In	0	1	...	0
Parameters				
ts_fact	1			
Outputs				
Out	0	0	...	0
Exp. Out	0	0	...	0
Out (DSP)	0	0	...	0
Exp. Out (DSP)	0	0	...	0

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	43
Max CPU cycles	43
Avg CPU cycles	43

Verification: Delay Float32 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for Control block Delay.

Test results				
Time step	1	2	...	18
CPU cycles	56	56	...	56
Inputs				
In (DSP)	0	1	...	0
In	0	1	...	0
Parameters				
ts_fact	1			
Outputs				
Out	0	0	...	0
Exp. Out	0	0	...	0
Out (DSP)	0	0	...	0
Exp. Out (DSP)	0	0	...	0

Test settings	
Tolerance Out	±3,2596e-08 (±70 LSB)

Test statistics	
Min CPU cycles	56
Max CPU cycles	56
Avg CPU cycles	56

Verification: Delay Float32 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for Control block Delay.

Test results				
Time step	1	2	...	18
CPU cycles	25	25	...	25
Inputs				
In (DSP)	0	1	...	0
In	0	1	...	0
Parameters				
ts_fact	1			
Outputs				
Out	0	0	...	0
Exp. Out	0	0	...	0
Out (DSP)	0	0	...	0
Exp. Out (DSP)	0	0	...	0

Test settings	
Tolerance Out	±3,2596e-08 (±70 LSB)

Test statistics	
Min CPU cycles	25
Max CPU cycles	25
Avg CPU cycles	25

Verification: Delay Float32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for Control block Delay.

Test results				
Time step	1	2	...	18
CPU cycles	58	58	...	58
Inputs				
In (DSP)	0	1	...	0
In	0	1	...	0
Parameters				
ts_fact	1			
Outputs				
Out	0	0	...	0
Exp. Out	0	0	...	0
Out (DSP)	0	0	...	0
Exp. Out (DSP)	0	0	...	0

Test settings	
Tolerance Out	±3,2596e-08 (±70 LSB)

Test statistics	
Min CPU cycles	58
Max CPU cycles	58
Avg CPU cycles	58

Verification: Delay Float32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for Control block Delay.

Test results				
Time step	1	2	...	18
CPU cycles	50	50	...	50
Inputs				
In (DSP)	0	1	...	0
In	0	1	...	0
Parameters				
ts_fact	1			
Outputs				
Out	0	0	...	0
Exp. Out	0	0	...	0
Out (DSP)	0	0	...	0
Exp. Out (DSP)	0	0	...	0

Test settings	
Tolerance Out	±3,2596e-08 (±70 LSB)

Test statistics	
Min CPU cycles	50
Max CPU cycles	50
Avg CPU cycles	50

Verification: Delay Float32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for Control block Delay.

Test results				
Time step	1	2	...	18
CPU cycles	30	30	...	30
Inputs				
In (DSP)	0	1	...	0
In	0	1	...	0
Parameters				
ts_fact	1			
Outputs				
Out	0	0	...	0
Exp. Out	0	0	...	0
Out (DSP)	0	0	...	0
Exp. Out (DSP)	0	0	...	0

Test settings	
Tolerance Out	±3,2596e-08 (±70 LSB)

Test statistics	
Min CPU cycles	30
Max CPU cycles	30
Avg CPU cycles	30

Verification: Delay Float32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for Control block Delay.

Test results				
Time step	1	2	...	18
CPU cycles	65	54	...	54
Inputs				
In (DSP)	0	1	...	0
In	0	1	...	0
Parameters				
ts_fact	1			
Outputs				
Out	0	0	...	0
Exp. Out	0	0	...	0
Out (DSP)	0	0	...	0
Exp. Out (DSP)	0	0	...	0

Test settings	
Tolerance Out	±3,2596e-08 (±70 LSB)

Test statistics	
Min CPU cycles	54
Max CPU cycles	65
Avg CPU cycles	54

Verification: Delay Float32 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for Control block Delay.

Test results				
Time step	1	2	...	18
CPU cycles	45	45	...	45
Inputs				
In (DSP)	0	1	...	0
In	0	1	...	0
Parameters				
ts_fact	1			
Outputs				
Out	0	0	...	0
Exp. Out	0	0	...	0
Out (DSP)	0	0	...	0
Exp. Out (DSP)	0	0	...	0

Test settings	
Tolerance Out	±3,2596e-08 (±70 LSB)

Test statistics	
Min CPU cycles	45
Max CPU cycles	45
Avg CPU cycles	45

Verification: Delay Float32 CPU dsPIC33EP256MC502

Date of Test	2026-06-23
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

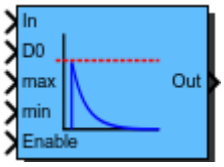
Inport test for Control block Delay.

Test results				
Time step	1	2	...	18
CPU cycles	43	43	...	43
Inputs				
In (DSP)	0	1	...	0
In	0	1	...	0
Parameters				
ts_fact	1			
Outputs				
Out	0	0	...	0
Exp. Out	0	0	...	0
Out (DSP)	0	0	...	0
Exp. Out (DSP)	0	0	...	0

Test settings	
Tolerance Out	±3,2596e-08 (±70 LSB)

Test statistics	
Min CPU cycles	43
Max CPU cycles	43
Avg CPU cycles	43

Block: DLimit



D Controller with Output Limitation:
G(s) = Kd*s/(s/(2*pi*fc) + 1)

Inports	
In	Control error input
D0	Derivational value which is loaded during initialization. (Usually this inport is connect to the In inport.)
max	Maximum output value
min	Minimum output value
Enable	Enable == 0: Deactivation of block; Out set to 0 Enable == 1: Activation of block

Outports	
Out	Control value

Mask Parameters		
Name	**ID**	**Description**
Kd	1	Derivative Factor
fc	2	Cutoff frequency of realization low pass
ts_fact	3	Multiplication factor of base sampling time (in integer format)

Description:

A rising flank at the *Enable* inport will preload the derivational part with the value present on the *Init* inport.

Transfer function (zero-order hold discretization method):

$$G(z) = K_{\mathrm{d}} 2\pi f_{\mathrm{c}} \frac{z-1}{z - e^{-2\pi f_{\mathrm{c}} T_{\mathrm{s}}}}$$

Developer note: The source code of this block is used for block *D*.

Implementations:

FiP16 16 Bit Fixed Point Implementation
FiP32 32 Bit Fixed Point Implementation
Float32 32 Bit Floating Point Implementation
Float64 64 Bit Floating Point Implementation

Implementation: FiP16

16 Bit Fixed Point Implementation

Inports Data Type	
In	int16
D0	int16
max	int16
min	int16
Enable	bool

Outports Data Type	
Out	int16

Implementation: FiP32

32 Bit Fixed Point Implementation

Inports Data Type	
In	int32
D0	int32
max	int32
min	int32
Enable	bool

Outports Data Type	
Out	int32

Implementation: Float32

32 Bit Floating Point Implementation

Inports Data Type	
In	float32
D0	float32
max	float32
min	float32
Enable	bool

Outports Data Type	
Out	float32

Implementation: Float64

64 Bit Floating Point Implementation

Inports Data Type	
In	float64
D0	float64
max	float64
min	float64
Enable	bool

Outports Data Type	
Out	float64

Verification: DLimit FiP16 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for Control block DLimit.

Test results						
Time step	1	2	3	4	...	201
CPU cycles	79	79	79	151	...	146
Inputs						
In (DSP)	0	0	0	0	...	0
D0 (DSP)	655	655	655	655	...	655
max (DSP)	26214	26214	26214	26214	...	26214
min (DSP)	4915	4915	4915	4915	...	4915
Enable (DSP)	0	0	0	1	...	1
In	0	0	0	0	...	0
D0	0.02	0.02	0.02	0.02	...	0.02
max	0.8	0.8	0.8	0.8	...	0.8
min	0.15	0.15	0.15	0.15	...	0.15
Enable	0	0	0	1	...	1
Parameters						
Kd	0.003					
fc	200					
ts_fact	1					
Outputs						
Out	0	0	0	0.15	...	0.15
Exp. Out	0	0	0	0.15	...	0.15
Out (DSP)	0	0	0	4915	...	4915
Exp. Out (DSP)	0	0	0	4915	...	4915

Test settings	
Tolerance Out	±3,0518e-04 (±10 LSB)

Test statistics	
Min CPU cycles	79
Max CPU cycles	151
Avg CPU cycles	144

Test case: Conversion test OK

Conversion test for Control block DLimit.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kd	-10	-9.444	-8.889	-8.333	...	10
fc	0	13.889	27.778	41.667	...	500
ts_fact	1	1	1	1	...	1
Controller parameters						
sfrd	15	5	4	3	...	0
b1d	0	-26374	-24822	-17453	...	31416
a0d	-32767	-32483	-32201	-31921	...	-23934
b0d	0	26374	24822	17453	...	-31416
Exp. sfrd	15	5	4	3	...	0
Exp. b1d	0	-26374	-24822	-17453	...	31416
Exp. a0d	-32767	-32483	-32201	-31921	...	-23934
Exp. b0d	0	26374	24822	17453	...	-31416

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±0,0000e+00
Tolerance a0d	±0,0000e+00
Tolerance b0d	±0,0000e+00

Test case: Conversion-on-Target test OK

Conversion-on-Target test for Control block DLimit.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kd	-10	-9.444	-8.889	-8.333	...	10
fc	0	13.889	27.778	41.667	...	500
ts_fact	1	1	1	1	...	1
Controller parameters						
sfrd	15	5	4	3	...	0
b1d	0	-26373	-24822	-17453	...	31415
a0d	-32767	-32483	-32201	-31921	...	-23933
b0d	0	26373	24822	17453	...	-31415
Exp. sfrd	15	5	4	3	...	0
Exp. b1d	0	-26374	-24822	-17453	...	31416
Exp. a0d	-32767	-32483	-32201	-31921	...	-23934
Exp. b0d	0	26374	24822	17453	...	-31416

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±1,0000e+00
Tolerance a0d	±1,0000e+00
Tolerance b0d	±1,0000e+00

Test statistics	
Min CPU cycles	2816
Max CPU cycles	10485
Avg CPU cycles	9330

Verification: DLimit FiP16 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for Control block DLimit.

Test results						
Time step	1	2	3	4	...	201
CPU cycles	51	51	51	101	...	99
Inputs						
In (DSP)	0	0	0	0	...	0
D0 (DSP)	655	655	655	655	...	655
max (DSP)	26214	26214	26214	26214	...	26214
min (DSP)	4915	4915	4915	4915	...	4915
Enable (DSP)	0	0	0	1	...	1
In	0	0	0	0	...	0
D0	0.02	0.02	0.02	0.02	...	0.02
max	0.8	0.8	0.8	0.8	...	0.8
min	0.15	0.15	0.15	0.15	...	0.15
Enable	0	0	0	1	...	1
Parameters						
Kd	0.003					
fc	200					
ts_fact	1					
Outputs						
Out	0	0	0	0.15	...	0.15
Exp. Out	0	0	0	0.15	...	0.15
Out (DSP)	0	0	0	4915	...	4915
Exp. Out (DSP)	0	0	0	4915	...	4915

Test settings	
Tolerance Out	±3,0518e-04 (±10 LSB)

Test statistics	
Min CPU cycles	51
Max CPU cycles	101
Avg CPU cycles	98

Test case: Conversion test OK

Conversion test for Control block DLimit.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kd	-10	-9.444	-8.889	-8.333	...	10
fc	0	13.889	27.778	41.667	...	500
ts_fact	1	1	1	1	...	1
Controller parameters						
sfrd	15	5	4	3	...	0
b1d	0	-26374	-24822	-17453	...	31416
a0d	-32767	-32483	-32201	-31921	...	-23934
b0d	0	26374	24822	17453	...	-31416
Exp. sfrd	15	5	4	3	...	0
Exp. b1d	0	-26374	-24822	-17453	...	31416
Exp. a0d	-32767	-32483	-32201	-31921	...	-23934
Exp. b0d	0	26374	24822	17453	...	-31416

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±0,0000e+00
Tolerance a0d	±0,0000e+00
Tolerance b0d	±0,0000e+00

Test case: Conversion-on-Target test OK

Conversion-on-Target test for Control block DLimit.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kd	-10	-9.444	-8.889	-8.333	...	10
fc	0	13.889	27.778	41.667	...	500
ts_fact	1	1	1	1	...	1
Controller parameters						
sfrd	15	5	4	3	...	0
b1d	0	-26373	-24822	-17453	...	31415
a0d	-32767	-32483	-32201	-31921	...	-23933
b0d	0	26373	24822	17453	...	-31415
Exp. sfrd	15	5	4	3	...	0
Exp. b1d	0	-26374	-24822	-17453	...	31416
Exp. a0d	-32767	-32483	-32201	-31921	...	-23934
Exp. b0d	0	26374	24822	17453	...	-31416

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±1,0000e+00
Tolerance a0d	±1,0000e+00
Tolerance b0d	±1,0000e+00

Test statistics	
Min CPU cycles	1363
Max CPU cycles	6395
Avg CPU cycles	5342

Verification: DLimit FiP16 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test **OK**

Inport test for Control block DLimit.

Test results						
Time step	1	2	3	4	...	201
CPU cycles	78	78	78	148	...	133
Inputs						
In (DSP)	0	0	0	0	...	0
D0 (DSP)	655	655	655	655	...	655
max (DSP)	26214	26214	26214	26214	...	26214
min (DSP)	4915	4915	4915	4915	...	4915
Enable (DSP)	0	0	0	1	...	1
In	0	0	0	0	...	0
D0	0.02	0.02	0.02	0.02	...	0.02
max	0.8	0.8	0.8	0.8	...	0.8
min	0.15	0.15	0.15	0.15	...	0.15
Enable	0	0	0	1	...	1
Parameters						
Kd	0.003					
fc	200					
ts_fact	1					
Outputs						
Out	0	0	0	0.15	...	0.15
Exp. Out	0	0	0	0.15	...	0.15
Out (DSP)	0	0	0	4915	...	4915
Exp. Out (DSP)	0	0	0	4915	...	4915

Test settings	
Tolerance Out	±3,0518e-04 (±10 LSB)

Test statistics	
Min CPU cycles	78
Max CPU cycles	191
Avg CPU cycles	132

Test case: Conversion test OK

Conversion test for Control block DLimit.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kd	-10	-9.444	-8.889	-8.333	...	10
fc	0	13.889	27.778	41.667	...	500
ts_fact	1	1	1	1	...	1
Controller parameters						
sfrd	15	5	4	3	...	0
b1d	0	-26374	-24822	-17453	...	31416
a0d	-32767	-32483	-32201	-31921	...	-23934
b0d	0	26374	24822	17453	...	-31416
Exp. sfrd	15	5	4	3	...	0
Exp. b1d	0	-26374	-24822	-17453	...	31416
Exp. a0d	-32767	-32483	-32201	-31921	...	-23934
Exp. b0d	0	26374	24822	17453	...	-31416

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±0,0000e+00
Tolerance a0d	±0,0000e+00
Tolerance b0d	±0,0000e+00

Test case: Conversion-on-Target test OK

Conversion-on-Target test for Control block DLimit.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kd	-10	-9.444	-8.889	-8.333	...	10
fc	0	13.889	27.778	41.667	...	500
ts_fact	1	1	1	1	...	1
Controller parameters						
sfrd	15	5	4	3	...	0
b1d	0	-26373	-24822	-17453	...	31415
a0d	-32767	-32483	-32201	-31921	...	-23933
b0d	0	26373	24822	17453	...	-31415
Exp. sfrd	15	5	4	3	...	0
Exp. b1d	0	-26374	-24822	-17453	...	31416
Exp. a0d	-32767	-32483	-32201	-31921	...	-23934
Exp. b0d	0	26374	24822	17453	...	-31416

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±1,0000e+00
Tolerance a0d	±1,0000e+00
Tolerance b0d	±1,0000e+00

Test statistics	
Min CPU cycles	1668
Max CPU cycles	3646
Avg CPU cycles	3276

Verification: DLimit FiP16 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for Control block DLimit.

Test results						
Time step	1	2	3	4	...	201
CPU cycles	72	72	72	145	...	132
Inputs						
In (DSP)	0	0	0	0	...	0
D0 (DSP)	655	655	655	655	...	655
max (DSP)	26214	26214	26214	26214	...	26214
min (DSP)	4915	4915	4915	4915	...	4915
Enable (DSP)	0	0	0	1	...	1
In	0	0	0	0	...	0
D0	0.02	0.02	0.02	0.02	...	0.02
max	0.8	0.8	0.8	0.8	...	0.8
min	0.15	0.15	0.15	0.15	...	0.15
Enable	0	0	0	1	...	1
Parameters						
Kd	0.003					
fc	200					
ts_fact	1					
Outputs						
Out	0	0	0	0.15	...	0.15
Exp. Out	0	0	0	0.15	...	0.15
Out (DSP)	0	0	0	4915	...	4915
Exp. Out (DSP)	0	0	0	4915	...	4915

Test settings	
Tolerance Out	±3,0518e-04 (±10 LSB)

Test statistics	
Min CPU cycles	72
Max CPU cycles	194
Avg CPU cycles	132

Test case: Conversion test OK

Conversion test for Control block DLimit.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kd	-10	-9.444	-8.889	-8.333	...	10
fc	0	13.889	27.778	41.667	...	500
ts_fact	1	1	1	1	...	1
Controller parameters						
sfrd	15	5	4	3	...	0
b1d	0	-26374	-24822	-17453	...	31416
a0d	-32767	-32483	-32201	-31921	...	-23934
b0d	0	26374	24822	17453	...	-31416
Exp. sfrd	15	5	4	3	...	0
Exp. b1d	0	-26374	-24822	-17453	...	31416
Exp. a0d	-32767	-32483	-32201	-31921	...	-23934
Exp. b0d	0	26374	24822	17453	...	-31416

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±0,0000e+00
Tolerance a0d	±0,0000e+00
Tolerance b0d	±0,0000e+00

Test case: Conversion-on-Target test OK

Conversion-on-Target test for Control block DLimit.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kd	-10	-9.444	-8.889	-8.333	...	10
fc	0	13.889	27.778	41.667	...	500
ts_fact	1	1	1	1	...	1
Controller parameters						
sfrd	15	5	4	3	...	0
b1d	0	-26373	-24822	-17453	...	31415
a0d	-32767	-32483	-32201	-31921	...	-23933
b0d	0	26373	24822	17453	...	-31415
Exp. sfrd	15	5	4	3	...	0
Exp. b1d	0	-26374	-24822	-17453	...	31416
Exp. a0d	-32767	-32483	-32201	-31921	...	-23934
Exp. b0d	0	26374	24822	17453	...	-31416

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±1,0000e+00
Tolerance a0d	±1,0000e+00
Tolerance b0d	±1,0000e+00

Test statistics	
Min CPU cycles	4310
Max CPU cycles	17162
Avg CPU cycles	15165

Verification: DLimit FiP16 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for Control block DLimit.

Test results						
Time step	1	2	3	4	...	201
CPU cycles	37	37	37	93	...	88
Inputs						
In (DSP)	0	0	0	0	...	0
D0 (DSP)	655	655	655	655	...	655
max (DSP)	26214	26214	26214	26214	...	26214
min (DSP)	4915	4915	4915	4915	...	4915
Enable (DSP)	0	0	0	1	...	1
In	0	0	0	0	...	0
D0	0.02	0.02	0.02	0.02	...	0.02
max	0.8	0.8	0.8	0.8	...	0.8
min	0.15	0.15	0.15	0.15	...	0.15
Enable	0	0	0	1	...	1
Parameters						
Kd	0.003					
fc	200					
ts_fact	1					
Outputs						
Out	0	0	0	0.15	...	0.15
Exp. Out	0	0	0	0.15	...	0.15
Out (DSP)	0	0	0	4915	...	4915
Exp. Out (DSP)	0	0	0	4915	...	4915

Test settings	
Tolerance Out	±3,0518e-04 (±10 LSB)

Test statistics	
Min CPU cycles	37
Max CPU cycles	93
Avg CPU cycles	87

Test case: Conversion test OK

Conversion test for Control block DLimit.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kd	-10	-9.444	-8.889	-8.333	...	10
fc	0	13.889	27.778	41.667	...	500
ts_fact	1	1	1	1	...	1
Controller parameters						
sfrd	15	5	4	3	...	0
b1d	0	-26374	-24822	-17453	...	31416
a0d	-32767	-32483	-32201	-31921	...	-23934
b0d	0	26374	24822	17453	...	-31416
Exp. sfrd	15	5	4	3	...	0
Exp. b1d	0	-26374	-24822	-17453	...	31416
Exp. a0d	-32767	-32483	-32201	-31921	...	-23934
Exp. b0d	0	26374	24822	17453	...	-31416

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±0,0000e+00
Tolerance a0d	±0,0000e+00
Tolerance b0d	±0,0000e+00

Test case: Conversion-on-Target test OK

Conversion-on-Target test for Control block DLimit.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kd	-10	-9.444	-8.889	-8.333	...	10
fc	0	13.889	27.778	41.667	...	500
ts_fact	1	1	1	1	...	1
Controller parameters						
sfrd	15	5	4	3	...	0
b1d	0	-26373	-24822	-17453	...	31415
a0d	-32767	-32483	-32201	-31921	...	-23933
b0d	0	26373	24822	17453	...	-31415
Exp. sfrd	15	5	4	3	...	0
Exp. b1d	0	-26374	-24822	-17453	...	31416
Exp. a0d	-32767	-32483	-32201	-31921	...	-23934
Exp. b0d	0	26374	24822	17453	...	-31416

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±1,0000e+00
Tolerance a0d	±1,0000e+00
Tolerance b0d	±1,0000e+00

Test statistics	
Min CPU cycles	1688
Max CPU cycles	5799
Avg CPU cycles	5201

Verification: DLimit FiP16 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for Control block DLimit.

Test results						
Time step	1	2	3	4	...	201
CPU cycles	95	77	77	147	...	126
Inputs						
In (DSP)	0	0	0	0	...	0
D0 (DSP)	655	655	655	655	...	655
max (DSP)	26214	26214	26214	26214	...	26214
min (DSP)	4915	4915	4915	4915	...	4915
Enable (DSP)	0	0	0	1	...	1
In	0	0	0	0	...	0
D0	0.02	0.02	0.02	0.02	...	0.02
max	0.8	0.8	0.8	0.8	...	0.8
min	0.15	0.15	0.15	0.15	...	0.15
Enable	0	0	0	1	...	1
Parameters						
Kd	0.003					
fc	200					
ts_fact	1					
Outputs						
Out	0	0	0	0.15	...	0.15
Exp. Out	0	0	0	0.15	...	0.15
Out (DSP)	0	0	0	4915	...	4915
Exp. Out (DSP)	0	0	0	4915	...	4915

Test settings	
Tolerance Out	±3,0518e-04 (±10 LSB)

Test statistics	
Min CPU cycles	77
Max CPU cycles	147
Avg CPU cycles	125

Test case: Conversion test OK

Conversion test for Control block DLimit.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kd	-10	-9.444	-8.889	-8.333	...	10
fc	0	13.889	27.778	41.667	...	500
ts_fact	1	1	1	1	...	1
Controller parameters						
sfrd	15	5	4	3	...	0
b1d	0	-26374	-24822	-17453	...	31416
a0d	-32767	-32483	-32201	-31921	...	-23934
b0d	0	26374	24822	17453	...	-31416
Exp. sfrd	15	5	4	3	...	0
Exp. b1d	0	-26374	-24822	-17453	...	31416
Exp. a0d	-32767	-32483	-32201	-31921	...	-23934
Exp. b0d	0	26374	24822	17453	...	-31416

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±0,0000e+00
Tolerance a0d	±0,0000e+00
Tolerance b0d	±0,0000e+00

Test case: Conversion-on-Target test OK

Conversion-on-Target test for Control block DLimit.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kd	-10	-9.444	-8.889	-8.333	...	10
fc	0	13.889	27.778	41.667	...	500
ts_fact	1	1	1	1	...	1
Controller parameters						
sfrd	15	5	4	3	...	0
b1d	0	-26373	-24822	-17453	...	31415
a0d	-32767	-32483	-32201	-31921	...	-23933
b0d	0	26373	24822	17453	...	-31415
Exp. sfrd	15	5	4	3	...	0
Exp. b1d	0	-26374	-24822	-17453	...	31416
Exp. a0d	-32767	-32483	-32201	-31921	...	-23934
Exp. b0d	0	26374	24822	17453	...	-31416

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±1,0000e+00
Tolerance a0d	±1,0000e+00
Tolerance b0d	±1,0000e+00

Test statistics	
Min CPU cycles	1257
Max CPU cycles	3084
Avg CPU cycles	2729

Verification: DLimit FiP16 CPU TMS320F28379D

Date of Test 2026-06-22

Target controller TMS320F28379D

Test case: Inport test OK

Inport test for Control block DLimit.

Test results						
Time step	1	2	3	4	...	201
CPU cycles	70	70	70	153	...	148
Inputs						
In (DSP)	0	0	0	0	...	0
D0 (DSP)	655	655	655	655	...	655
max (DSP)	26214	26214	26214	26214	...	26214
min (DSP)	4915	4915	4915	4915	...	4915
Enable (DSP)	0	0	0	1	...	1
In	0	0	0	0	...	0
D0	0.02	0.02	0.02	0.02	...	0.02
max	0.8	0.8	0.8	0.8	...	0.8
min	0.15	0.15	0.15	0.15	...	0.15
Enable	0	0	0	1	...	1
Parameters						
Kd	0.003					
fc	200					
ts_fact	1					
Outputs						
Out	0	0	0	0.15	...	0.15
Exp. Out	0	0	0	0.15	...	0.15
Out (DSP)	0	0	0	4915	...	4915
Exp. Out (DSP)	0	0	0	4915	...	4915

Test settings	
Tolerance Out	±3,0518e-04 (±10 LSB)

Test statistics	
Min CPU cycles	70
Max CPU cycles	153
Avg CPU cycles	146

Test case: Conversion test OK

Conversion test for Control block DLimit.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kd	-10	-9.444	-8.889	-8.333	...	10
fc	0	13.889	27.778	41.667	...	500
ts_fact	1	1	1	1	...	1
Controller parameters						
sfrd	15	5	4	3	...	0
b1d	0	-26374	-24822	-17453	...	31416
a0d	-32767	-32483	-32201	-31921	...	-23934
b0d	0	26374	24822	17453	...	-31416
Exp. sfrd	15	5	4	3	...	0
Exp. b1d	0	-26374	-24822	-17453	...	31416
Exp. a0d	-32767	-32483	-32201	-31921	...	-23934
Exp. b0d	0	26374	24822	17453	...	-31416

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±0,0000e+00
Tolerance a0d	±0,0000e+00
Tolerance b0d	±0,0000e+00

Test case: Conversion-on-Target test OK

Conversion-on-Target test for Control block DLimit.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kd	-10	-9.444	-8.889	-8.333	...	10
fc	0	13.889	27.778	41.667	...	500
ts_fact	1	1	1	1	...	1
Controller parameters						
sfrd	15	5	4	3	...	0
b1d	0	-26373	-24822	-17453	...	31415
a0d	-32767	-32483	-32201	-31921	...	-23933
b0d	0	26373	24822	17453	...	-31415
Exp. sfrd	15	5	4	3	...	0
Exp. b1d	0	-26374	-24822	-17453	...	31416
Exp. a0d	-32767	-32483	-32201	-31921	...	-23934
Exp. b0d	0	26374	24822	17453	...	-31416

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±1,0000e+00
Tolerance a0d	±1,0000e+00
Tolerance b0d	±1,0000e+00

Test statistics	
Min CPU cycles	2019
Max CPU cycles	8061
Avg CPU cycles	7153

Verification: DLimit FiP16 CPU dsPIC33EP256MC502

Date of Test	2026-06-23
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for Control block DLimit.

Test results						
Time step	1	2	3	4	...	201
CPU cycles	52	52	52	120	...	124
Inputs						
In (DSP)	0	0	0	0	...	0
D0 (DSP)	655	655	655	655	...	655
max (DSP)	26214	26214	26214	26214	...	26214
min (DSP)	4915	4915	4915	4915	...	4915
Enable (DSP)	0	0	0	1	...	1
In	0	0	0	0	...	0
D0	0.02	0.02	0.02	0.02	...	0.02
max	0.8	0.8	0.8	0.8	...	0.8
min	0.15	0.15	0.15	0.15	...	0.15
Enable	0	0	0	1	...	1
Parameters						
Kd	0.003					
fc	200					
ts_fact	1					
Outputs						
Out	0	0	0	0.15	...	0.15
Exp. Out	0	0	0	0.15	...	0.15
Out (DSP)	0	0	0	4915	...	4915
Exp. Out (DSP)	0	0	0	4915	...	4915

Test settings	
Tolerance Out	±3,0518e-04 (±10 LSB)

Test statistics	
Min CPU cycles	52
Max CPU cycles	124
Avg CPU cycles	121

Test case: Conversion test OK

Conversion test for Control block DLimit.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kd	-10	-9.444	-8.889	-8.333	...	10
fc	0	13.889	27.778	41.667	...	500
ts_fact	1	1	1	1	...	1
Controller parameters						
sfrd	15	5	4	3	...	0
b1d	0	-26374	-24822	-17453	...	31416
a0d	-32767	-32483	-32201	-31921	...	-23934
b0d	0	26374	24822	17453	...	-31416
Exp. sfrd	15	5	4	3	...	0
Exp. b1d	0	-26374	-24822	-17453	...	31416
Exp. a0d	-32767	-32483	-32201	-31921	...	-23934
Exp. b0d	0	26374	24822	17453	...	-31416

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±0,0000e+00
Tolerance a0d	±0,0000e+00
Tolerance b0d	±0,0000e+00

Test case: Conversion-on-Target test OK

Conversion-on-Target test for Control block DLimit.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kd	-10	-9.444	-8.889	-8.333	...	10
fc	0	13.889	27.778	41.667	...	500
ts_fact	1	1	1	1	...	1
Controller parameters						
sfrd	15	5	4	3	...	0
b1d	0	-26373	-24822	-17453	...	31415
a0d	-32767	-32483	-32201	-31921	...	-23933
b0d	0	26373	24822	17453	...	-31415
Exp. sfrd	15	5	4	3	...	0
Exp. b1d	0	-26374	-24822	-17453	...	31416
Exp. a0d	-32767	-32483	-32201	-31921	...	-23934
Exp. b0d	0	26374	24822	17453	...	-31416

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±1,0000e+00
Tolerance a0d	±1,0000e+00
Tolerance b0d	±1,0000e+00

Test statistics	
Min CPU cycles	6401
Max CPU cycles	35059
Avg CPU cycles	31162

Verification: DLimit FiP32 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for Control block DLimit.

Test results				
Time step	1	2	...	201
CPU cycles	88	88	...	360
Inputs				
In (DSP)	0	0	...	0
D0 (DSP)	42949673	42949673	...	42949673
max (DSP)	1717986918	1717986918	...	1717986918
min (DSP)	322122547	322122547	...	322122547
Enable (DSP)	0	0	...	1
In	0	0	...	0
D0	0.02	0.02	...	0.02
max	0.8	0.8	...	0.8
min	0.15	0.15	...	0.15
Enable	0	0	...	1
Parameters				
Kd	0.003			
fc	200			
ts_fact	1			
Outputs				
Out	0	0	...	0.15
Exp. Out	0	0	...	0.15
Out (DSP)	0	0	...	322122547
Exp. Out (DSP)	0	0	...	322122547

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	88
Max CPU cycles	401
Avg CPU cycles	355

Test case: Conversion test OK

Conversion test for Control block DLimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
ts_fact	1	1	...	1
Controller parameters				
sfrd	31	21	...	16
b1d	0	-1728437568	...	2058874161
a0d	-2147483647	-2128824851	...	-1568527835
b0d	0	1728437568	...	-2058874161
Exp. sfrd	31	21	...	16
Exp. b1d	0	-1728437568	...	2058874161
Exp. a0d	-2147483647	-2128824851	...	-1568527835
Exp. b0d	0	1728437568	...	-2058874161

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±0,0000e+00
Tolerance a0d	±0,0000e+00
Tolerance b0d	±0,0000e+00

Test case: Conversion-on-Target test OK

Conversion-on-Target test for Control block DLimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
ts_fact	1	1	...	1
Controller parameters				
sfrd	31	21	...	16
b1d	0	-1728437632	...	2058874240
a0d	-2147483647	-2128824832	...	-1568527872
b0d	0	1728437632	...	-2058874240
Exp. sfrd	31	21	...	16
Exp. b1d	0	-1728437568	...	2058874161
Exp. a0d	-2147483647	-2128824851	...	-1568527835
Exp. b0d	0	1728437568	...	-2058874161

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±2,0000e+02
Tolerance a0d	±2,0000e+02
Tolerance b0d	±2,0000e+02

Test statistics	
Min CPU cycles	3452
Max CPU cycles	11665
Avg CPU cycles	10118

Verification: DLimit FiP32 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for Control block DLimit.

Test results				
Time step	1	2	...	201
CPU cycles	53	53	...	135
Inputs				
In (DSP)	0	0	...	0
D0 (DSP)	42949673	42949673	...	42949673
max (DSP)	1717986918	1717986918	...	1717986918
min (DSP)	322122547	322122547	...	322122547
Enable (DSP)	0	0	...	1
In	0	0	...	0
D0	0.02	0.02	...	0.02
max	0.8	0.8	...	0.8
min	0.15	0.15	...	0.15
Enable	0	0	...	1
Parameters				
Kd	0.003			
fc	200			
ts_fact	1			
Outputs				
Out	0	0	...	0.15
Exp. Out	0	0	...	0.15
Out (DSP)	0	0	...	322122547
Exp. Out (DSP)	0	0	...	322122547

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	53
Max CPU cycles	137
Avg CPU cycles	133

Test case: Conversion test OK

Conversion test for Control block DLimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
ts_fact	1	1	...	1
Controller parameters				
sfrd	31	21	...	16
b1d	0	-1728437568	...	2058874161
a0d	-2147483647	-2128824851	...	-1568527835
b0d	0	1728437568	...	-2058874161
Exp. sfrd	31	21	...	16
Exp. b1d	0	-1728437568	...	2058874161
Exp. a0d	-2147483647	-2128824851	...	-1568527835
Exp. b0d	0	1728437568	...	-2058874161

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±0,0000e+00
Tolerance a0d	±0,0000e+00
Tolerance b0d	±0,0000e+00

Test case: Conversion-on-Target test OK

Conversion-on-Target test for Control block DLimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
ts_fact	1	1	...	1
Controller parameters				
sfrd	31	21	...	16
b1d	0	-1728437632	...	2058874240
a0d	-2147483647	-2128824832	...	-1568527872
b0d	0	1728437632	...	-2058874240
Exp. sfrd	31	21	...	16
Exp. b1d	0	-1728437568	...	2058874161
Exp. a0d	-2147483647	-2128824851	...	-1568527835
Exp. b0d	0	1728437568	...	-2058874161

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±2,0000e+02
Tolerance a0d	±2,0000e+02
Tolerance b0d	±2,0000e+02

Test statistics	
Min CPU cycles	1431
Max CPU cycles	5085
Avg CPU cycles	4311

Verification: DLimit FiP32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for Control block DLimit.

Test results				
Time step	1	2	...	201
CPU cycles	86	86	...	172
Inputs				
In (DSP)	0	0	...	0
D0 (DSP)	42949673	42949673	...	42949673
max (DSP)	1717986918	1717986918	...	1717986918
min (DSP)	322122547	322122547	...	322122547
Enable (DSP)	0	0	...	1
In	0	0	...	0
D0	0.02	0.02	...	0.02
max	0.8	0.8	...	0.8
min	0.15	0.15	...	0.15
Enable	0	0	...	1
Parameters				
Kd	0.003			
fc	200			
ts_fact	1			
Outputs				
Out	0	0	...	0.15
Exp. Out	0	0	...	0.15
Out (DSP)	0	0	...	322122547
Exp. Out (DSP)	0	0	...	322122547

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	86
Max CPU cycles	194
Avg CPU cycles	170

Test case: Conversion test OK

Conversion test for Control block DLimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
ts_fact	1	1	...	1
Controller parameters				
sfrd	31	21	...	16
b1d	0	-1728437568	...	2058874161
a0d	-2147483647	-2128824851	...	-1568527835
b0d	0	1728437568	...	-2058874161
Exp. sfrd	31	21	...	16
Exp. b1d	0	-1728437568	...	2058874161
Exp. a0d	-2147483647	-2128824851	...	-1568527835
Exp. b0d	0	1728437568	...	-2058874161

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±0,0000e+00
Tolerance a0d	±0,0000e+00
Tolerance b0d	±0,0000e+00

Test case: Conversion-on-Target test OK

Conversion-on-Target test for Control block DLimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
ts_fact	1	1	...	1
Controller parameters				
sfrd	31	21	...	16
b1d	0	-1728437632	...	2058874240
a0d	-2147483647	-2128824832	...	-1568527872
b0d	0	1728437632	...	-2058874240
Exp. sfrd	31	21	...	16
Exp. b1d	0	-1728437568	...	2058874161
Exp. a0d	-2147483647	-2128824851	...	-1568527835
Exp. b0d	0	1728437568	...	-2058874161

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±2,0000e+02
Tolerance a0d	±2,0000e+02
Tolerance b0d	±2,0000e+02

Test statistics	
Min CPU cycles	2520
Max CPU cycles	4575
Avg CPU cycles	4143

Verification: DLimit FiP32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for Control block DLimit.

Test results				
Time step	1	2	...	201
CPU cycles	87	87	...	404
Inputs				
In (DSP)	0	0	...	0
D0 (DSP)	42949673	42949673	...	42949673
max (DSP)	1717986918	1717986918	...	1717986918
min (DSP)	322122547	322122547	...	322122547
Enable (DSP)	0	0	...	1
In	0	0	...	0
D0	0.02	0.02	...	0.02
max	0.8	0.8	...	0.8
min	0.15	0.15	...	0.15
Enable	0	0	...	1
Parameters				
Kd	0.003			
fc	200			
ts_fact	1			
Outputs				
Out	0	0	...	0.15
Exp. Out	0	0	...	0.15
Out (DSP)	0	0	...	322122547
Exp. Out (DSP)	0	0	...	322122547

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	87
Max CPU cycles	410
Avg CPU cycles	399

Test case: Conversion test OK

Conversion test for Control block DLimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
ts_fact	1	1	...	1
Controller parameters				
sfrd	31	21	...	16
b1d	0	-1728437568	...	2058874161
a0d	-2147483647	-2128824851	...	-1568527835
b0d	0	1728437568	...	-2058874161
Exp. sfrd	31	21	...	16
Exp. b1d	0	-1728437568	...	2058874161
Exp. a0d	-2147483647	-2128824851	...	-1568527835
Exp. b0d	0	1728437568	...	-2058874161

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±0,0000e+00
Tolerance a0d	±0,0000e+00
Tolerance b0d	±0,0000e+00

Test case: Conversion-on-Target test OK

Conversion-on-Target test for Control block DLimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
ts_fact	1	1	...	1
Controller parameters				
sfrd	31	21	...	16
b1d	0	-1728437632	...	2058874240
a0d	-2147483647	-2128824832	...	-1568527872
b0d	0	1728437632	...	-2058874240
Exp. sfrd	31	21	...	16
Exp. b1d	0	-1728437568	...	2058874161
Exp. a0d	-2147483647	-2128824851	...	-1568527835
Exp. b0d	0	1728437568	...	-2058874161

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±2,0000e+02
Tolerance a0d	±2,0000e+02
Tolerance b0d	±2,0000e+02

Test statistics	
Min CPU cycles	7766
Max CPU cycles	20968
Avg CPU cycles	18920

Verification: DLimit FiP32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for Control block DLimit.

Test results				
Time step	1	2	...	201
CPU cycles	37	37	...	119
Inputs				
In (DSP)	0	0	...	0
D0 (DSP)	42949673	42949673	...	42949673
max (DSP)	1717986918	1717986918	...	1717986918
min (DSP)	322122547	322122547	...	322122547
Enable (DSP)	0	0	...	1
In	0	0	...	0
D0	0.02	0.02	...	0.02
max	0.8	0.8	...	0.8
min	0.15	0.15	...	0.15
Enable	0	0	...	1
Parameters				
Kd	0.003			
fc	200			
ts_fact	1			
Outputs				
Out	0	0	...	0.15
Exp. Out	0	0	...	0.15
Out (DSP)	0	0	...	322122547
Exp. Out (DSP)	0	0	...	322122547

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	37
Max CPU cycles	123
Avg CPU cycles	118

Test case: Conversion test OK

Conversion test for Control block DLimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
ts_fact	1	1	...	1
Controller parameters				
sfrd	31	21	...	16
b1d	0	-1728437568	...	2058874161
a0d	-2147483647	-2128824851	...	-1568527835
b0d	0	1728437568	...	-2058874161
Exp. sfrd	31	21	...	16
Exp. b1d	0	-1728437568	...	2058874161
Exp. a0d	-2147483647	-2128824851	...	-1568527835
Exp. b0d	0	1728437568	...	-2058874161

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±0,0000e+00
Tolerance a0d	±0,0000e+00
Tolerance b0d	±0,0000e+00

Test case: Conversion-on-Target test OK

Conversion-on-Target test for Control block DLimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
ts_fact	1	1	...	1
Controller parameters				
sfrd	31	21	...	16
b1d	0	-1728437632	...	2058874240
a0d	-2147483647	-2128824832	...	-1568527872
b0d	0	1728437632	...	-2058874240
Exp. sfrd	31	21	...	16
Exp. b1d	0	-1728437568	...	2058874161
Exp. a0d	-2147483647	-2128824851	...	-1568527835
Exp. b0d	0	1728437568	...	-2058874161

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±2,0000e+02
Tolerance a0d	±2,0000e+02
Tolerance b0d	±2,0000e+02

Test statistics	
Min CPU cycles	2913
Max CPU cycles	7307
Avg CPU cycles	6491

Verification: DLimit FiP32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for Control block DLimit.

Test results				
Time step	1	2	...	201
CPU cycles	103	83	...	157
Inputs				
In (DSP)	0	0	...	0
D0 (DSP)	42949673	42949673	...	42949673
max (DSP)	1717986918	1717986918	...	1717986918
min (DSP)	322122547	322122547	...	322122547
Enable (DSP)	0	0	...	1
In	0	0	...	0
D0	0.02	0.02	...	0.02
max	0.8	0.8	...	0.8
min	0.15	0.15	...	0.15
Enable	0	0	...	1
Parameters				
Kd	0.003			
fc	200			
ts_fact	1			
Outputs				
Out	0	0	...	0.15
Exp. Out	0	0	...	0.15
Out (DSP)	0	0	...	322122547
Exp. Out (DSP)	0	0	...	322122547

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	83
Max CPU cycles	189
Avg CPU cycles	156

Test case: Conversion test OK

Conversion test for Control block DLimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
ts_fact	1	1	...	1
Controller parameters				
sfrd	31	21	...	16
b1d	0	-1728437568	...	2058874161
a0d	-2147483647	-2128824851	...	-1568527835
b0d	0	1728437568	...	-2058874161
Exp. sfrd	31	21	...	16
Exp. b1d	0	-1728437568	...	2058874161
Exp. a0d	-2147483647	-2128824851	...	-1568527835
Exp. b0d	0	1728437568	...	-2058874161

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±0,0000e+00
Tolerance a0d	±0,0000e+00
Tolerance b0d	±0,0000e+00

Test case: Conversion-on-Target test OK

Conversion-on-Target test for Control block DLimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
ts_fact	1	1	...	1
Controller parameters				
sfrd	31	21	...	16
b1d	0	-1728437632	...	2058874240
a0d	-2147483647	-2128824832	...	-1568527872
b0d	0	1728437632	...	-2058874240
Exp. sfrd	31	21	...	16
Exp. b1d	0	-1728437568	...	2058874161
Exp. a0d	-2147483647	-2128824851	...	-1568527835
Exp. b0d	0	1728437568	...	-2058874161

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±2,0000e+02
Tolerance a0d	±2,0000e+02
Tolerance b0d	±2,0000e+02

Test statistics	
Min CPU cycles	2097
Max CPU cycles	3961
Avg CPU cycles	3599

Verification: DLimit FiP32 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for Control block DLimit.

Test results				
Time step	1	2	...	201
CPU cycles	73	73	...	317
Inputs				
In (DSP)	0	0	...	0
D0 (DSP)	42949673	42949673	...	42949673
max (DSP)	1717986918	1717986918	...	1717986918
min (DSP)	322122547	322122547	...	322122547
Enable (DSP)	0	0	...	1
In	0	0	...	0
D0	0.02	0.02	...	0.02
max	0.8	0.8	...	0.8
min	0.15	0.15	...	0.15
Enable	0	0	...	1
Parameters				
Kd	0.003			
fc	200			
ts_fact	1			
Outputs				
Out	0	0	...	0.15
Exp. Out	0	0	...	0.15
Out (DSP)	0	0	...	322122547
Exp. Out (DSP)	0	0	...	322122547

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	73
Max CPU cycles	343
Avg CPU cycles	313

Test case: Conversion test OK

Conversion test for Control block DLimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
ts_fact	1	1	...	1
Controller parameters				
sfrd	31	21	...	16
b1d	0	-1728437568	...	2058874161
a0d	-2147483647	-2128824851	...	-1568527835
b0d	0	1728437568	...	-2058874161
Exp. sfrd	31	21	...	16
Exp. b1d	0	-1728437568	...	2058874161
Exp. a0d	-2147483647	-2128824851	...	-1568527835
Exp. b0d	0	1728437568	...	-2058874161

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±0,0000e+00
Tolerance a0d	±0,0000e+00
Tolerance b0d	±0,0000e+00

Test case: Conversion-on-Target test OK

Conversion-on-Target test for Control block DLimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
ts_fact	1	1	...	1
Controller parameters				
sfrd	31	21	...	16
b1d	0	-1728437632	...	2058874240
a0d	-2147483647	-2128824832	...	-1568527872
b0d	0	1728437632	...	-2058874240
Exp. sfrd	31	21	...	16
Exp. b1d	0	-1728437568	...	2058874161
Exp. a0d	-2147483647	-2128824851	...	-1568527835
Exp. b0d	0	1728437568	...	-2058874161

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±2,0000e+02
Tolerance a0d	±2,0000e+02
Tolerance b0d	±2,0000e+02

Test statistics	
Min CPU cycles	2458
Max CPU cycles	8938
Avg CPU cycles	7719

Verification: DLimit FiP32 CPU dsPIC33EP256MC502

Date of Test	2026-06-23
Target controller	dsPIC33EP256MC502

Test case: Inport test

OK

Inport test for Control block DLimit.

Test results				
Time step	1	2	...	201
CPU cycles	70	70	...	778
Inputs				
In (DSP)	0	0	...	0
D0 (DSP)	42949673	42949673	...	42949673
max (DSP)	1717986918	1717986918	...	1717986918
min (DSP)	322122547	322122547	...	322122547
Enable (DSP)	0	0	...	1
In	0	0	...	0
D0	0.02	0.02	...	0.02
max	0.8	0.8	...	0.8
min	0.15	0.15	...	0.15
Enable	0	0	...	1
Parameters				
Kd	0.003			
fc	200			
ts_fact	1			
Outputs				
Out	0	0	...	0.15
Exp. Out	0	0	...	0.15
Out (DSP)	0	0	...	322122547
Exp. Out (DSP)	0	0	...	322122547

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	70
Max CPU cycles	786
Avg CPU cycles	768

Test case: Conversion test OK

Conversion test for Control block DLimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
ts_fact	1	1	...	1
Controller parameters				
sfrd	31	21	...	16
b1d	0	-1728437568	...	2058874161
a0d	-2147483647	-2128824851	...	-1568527835
b0d	0	1728437568	...	-2058874161
Exp. sfrd	31	21	...	16
Exp. b1d	0	-1728437568	...	2058874161
Exp. a0d	-2147483647	-2128824851	...	-1568527835
Exp. b0d	0	1728437568	...	-2058874161

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±0,0000e+00
Tolerance a0d	±0,0000e+00
Tolerance b0d	±0,0000e+00

Test case: Conversion-on-Target test OK

Conversion-on-Target test for Control block DLimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
ts_fact	1	1	...	1
Controller parameters				
sfrd	31	21	...	16
b1d	0	-1728437632	...	2058874240
a0d	-2147483647	-2128824832	...	-1568527872
b0d	0	1728437632	...	-2058874240
Exp. sfrd	31	21	...	16
Exp. b1d	0	-1728437568	...	2058874161
Exp. a0d	-2147483647	-2128824851	...	-1568527835
Exp. b0d	0	1728437568	...	-2058874161

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±2,0000e+02
Tolerance a0d	±2,0000e+02
Tolerance b0d	±2,0000e+02

Test statistics	
Min CPU cycles	7460
Max CPU cycles	36680
Avg CPU cycles	31565

Verification: DLimit Float32 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for Control block DLimit.

Test results				
Time step	1	2	...	201
CPU cycles	82	82	...	125
Inputs				
In (DSP)	0	0	...	0
D0 (DSP)	0.02	0.02	...	0.02
max (DSP)	0.8	0.8	...	0.8
min (DSP)	0.15	0.15	...	0.15
Enable (DSP)	0	0	...	1
In	0	0	...	0
D0	0.02	0.02	...	0.02
max	0.8	0.8	...	0.8
min	0.15	0.15	...	0.15
Enable	0	0	...	1
Parameters				
Kd	0.003			
fc	200			
ts_fact	1			
Outputs				
Out	0	0	...	0.15
Exp. Out	0	0	...	0.15
Out (DSP)	0	0	...	0.15
Exp. Out (DSP)	0	0	...	0.15

Test settings	
Tolerance Out	±9,3132e-06 (±20000 LSB)

Test statistics	
Min CPU cycles	82
Max CPU cycles	130
Avg CPU cycles	124

Test case: Conversion test OK

Conversion test for Control block DLimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
ts_fact	1	1	...	1
Controller parameters				
b1d	0	-824.183	...	31415.927
a0d	-1	-0.991	...	-0.73
b0d	0	824.183	...	-31415.927
Exp. b1d	0	-824.183	...	31415.927
Exp. a0d	-1	-0.991	...	-0.73
Exp. b0d	0	824.183	...	-31415.927

Test settings	
Tolerance b1d	±0,0000e+00
Tolerance a0d	±1,0000e-15
Tolerance b0d	±0,0000e+00

Test case: Conversion-on-Target test OK

Conversion-on-Target test for Control block DLimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
ts_fact	1	1	...	1
Controller parameters				
b1d	0	-824.183	...	31415.928
a0d	-1	-0.991	...	-0.73
b0d	0	824.183	...	-31415.928
Exp. b1d	0	-824.183	...	31415.927
Exp. a0d	-1	-0.991	...	-0.73
Exp. b0d	0	824.183	...	-31415.927

Test settings	
Tolerance b1d	±3,0000e-03
Tolerance a0d	±1,0000e-07
Tolerance b0d	±3,0000e-03

Test statistics	
Min CPU cycles	2153
Max CPU cycles	2496
Avg CPU cycles	2476

Verification: DLimit Float32 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for Control block DLimit.

Test results				
Time step	1	2	...	201
CPU cycles	45	45	...	87
Inputs				
In (DSP)	0	0	...	0
D0 (DSP)	0.02	0.02	...	0.02
max (DSP)	0.8	0.8	...	0.8
min (DSP)	0.15	0.15	...	0.15
Enable (DSP)	0	0	...	1
In	0	0	...	0
D0	0.02	0.02	...	0.02
max	0.8	0.8	...	0.8
min	0.15	0.15	...	0.15
Enable	0	0	...	1
Parameters				
Kd	0.003			
fc	200			
ts_fact	1			
Outputs				
Out	0	0	...	0.15
Exp. Out	0	0	...	0.15
Out (DSP)	0	0	...	0.15
Exp. Out (DSP)	0	0	...	0.15

Test settings	
Tolerance Out	±9,3132e-06 (±20000 LSB)

Test statistics	
Min CPU cycles	45
Max CPU cycles	91
Avg CPU cycles	86

Test case: Conversion test OK

Conversion test for Control block DLimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
ts_fact	1	1	...	1
Controller parameters				
b1d	0	-824.183	...	31415.927
a0d	-1	-0.991	...	-0.73
b0d	0	824.183	...	-31415.927
Exp. b1d	0	-824.183	...	31415.927
Exp. a0d	-1	-0.991	...	-0.73
Exp. b0d	0	824.183	...	-31415.927

Test settings	
Tolerance b1d	±0,0000e+00
Tolerance a0d	±1,0000e-15
Tolerance b0d	±0,0000e+00

Test case: Conversion-on-Target test OK

Conversion-on-Target test for Control block DLimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
ts_fact	1	1	...	1
Controller parameters				
b1d	0	-824.183	...	31415.928
a0d	-1	-0.991	...	-0.73
b0d	0	824.183	...	-31415.928
Exp. b1d	0	-824.183	...	31415.927
Exp. a0d	-1	-0.991	...	-0.73
Exp. b0d	0	824.183	...	-31415.927

Test settings	
Tolerance b1d	±3,0000e-03
Tolerance a0d	±1,0000e-07
Tolerance b0d	±3,0000e-03

Test statistics	
Min CPU cycles	1009
Max CPU cycles	1053
Avg CPU cycles	1051

Verification: DLimit Float32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for Control block DLimit.

Test results				
Time step	1	2	...	201
CPU cycles	78	78	...	113
Inputs				
In (DSP)	0	0	...	0
D0 (DSP)	0.02	0.02	...	0.02
max (DSP)	0.8	0.8	...	0.8
min (DSP)	0.15	0.15	...	0.15
Enable (DSP)	0	0	...	1
In	0	0	...	0
D0	0.02	0.02	...	0.02
max	0.8	0.8	...	0.8
min	0.15	0.15	...	0.15
Enable	0	0	...	1
Parameters				
Kd	0.003			
fc	200			
ts_fact	1			
Outputs				
Out	0	0	...	0.15
Exp. Out	0	0	...	0.15
Out (DSP)	0	0	...	0.15
Exp. Out (DSP)	0	0	...	0.15

Test settings	
Tolerance Out	±9,3132e-06 (±20000 LSB)

Test statistics	
Min CPU cycles	78
Max CPU cycles	130
Avg CPU cycles	112

Test case: Conversion test OK

Conversion test for Control block DLimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
ts_fact	1	1	...	1
Controller parameters				
b1d	0	-824.183	...	31415.927
a0d	-1	-0.991	...	-0.73
b0d	0	824.183	...	-31415.927
Exp. b1d	0	-824.183	...	31415.927
Exp. a0d	-1	-0.991	...	-0.73
Exp. b0d	0	824.183	...	-31415.927

Test settings	
Tolerance b1d	±0,0000e+00
Tolerance a0d	±1,0000e-15
Tolerance b0d	±0,0000e+00

Test case: Conversion-on-Target test OK

Conversion-on-Target test for Control block DLimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
ts_fact	1	1	...	1
Controller parameters				
b1d	0	-824.183	...	31415.928
a0d	-1	-0.991	...	-0.73
b0d	0	824.183	...	-31415.928
Exp. b1d	0	-824.183	...	31415.927
Exp. a0d	-1	-0.991	...	-0.73
Exp. b0d	0	824.183	...	-31415.927

Test settings	
Tolerance b1d	±3,0000e-03
Tolerance a0d	±1,0000e-07
Tolerance b0d	±3,0000e-03

Test statistics	
Min CPU cycles	1170
Max CPU cycles	1245
Avg CPU cycles	1238

Verification: DLimit Float32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for Control block DLimit.

Test results				
Time step	1	2	...	201
CPU cycles	80	80	...	891
Inputs				
In (DSP)	0	0	...	0
D0 (DSP)	0.02	0.02	...	0.02
max (DSP)	0.8	0.8	...	0.8
min (DSP)	0.15	0.15	...	0.15
Enable (DSP)	0	0	...	1
In	0	0	...	0
D0	0.02	0.02	...	0.02
max	0.8	0.8	...	0.8
min	0.15	0.15	...	0.15
Enable	0	0	...	1
Parameters				
Kd	0.003			
fc	200			
ts_fact	1			
Outputs				
Out	0	0	...	0.15
Exp. Out	0	0	...	0.15
Out (DSP)	0	0	...	0.15
Exp. Out (DSP)	0	0	...	0.15

Test settings	
Tolerance Out	±9,3132e-06 (±20000 LSB)

Test statistics	
Min CPU cycles	80
Max CPU cycles	1070
Avg CPU cycles	954

Test case: Conversion test OK

Conversion test for Control block DLimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
ts_fact	1	1	...	1
Controller parameters				
b1d	0	-824.183	...	31415.927
a0d	-1	-0.991	...	-0.73
b0d	0	824.183	...	-31415.927
Exp. b1d	0	-824.183	...	31415.927
Exp. a0d	-1	-0.991	...	-0.73
Exp. b0d	0	824.183	...	-31415.927

Test settings	
Tolerance b1d	±0,0000e+00
Tolerance a0d	±1,0000e-15
Tolerance b0d	±0,0000e+00

Test case: Conversion-on-Target test OK

Conversion-on-Target test for Control block DLimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
ts_fact	1	1	...	1
Controller parameters				
b1d	0	-824.183	...	31415.928
a0d	-1	-0.991	...	-0.73
b0d	0	824.183	...	-31415.928
Exp. b1d	0	-824.183	...	31415.927
Exp. a0d	-1	-0.991	...	-0.73
Exp. b0d	0	824.183	...	-31415.927

Test settings	
Tolerance b1d	±3,0000e-03
Tolerance a0d	±1,0000e-07
Tolerance b0d	±3,0000e-03

Test statistics	
Min CPU cycles	2958
Max CPU cycles	5933
Avg CPU cycles	5798

Verification: DLimit Float32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for Control block DLimit.

Test results				
Time step	1	2	...	201
CPU cycles	63	63	...	347
Inputs				
In (DSP)	0	0	...	0
D0 (DSP)	0.02	0.02	...	0.02
max (DSP)	0.8	0.8	...	0.8
min (DSP)	0.15	0.15	...	0.15
Enable (DSP)	0	0	...	1
In	0	0	...	0
D0	0.02	0.02	...	0.02
max	0.8	0.8	...	0.8
min	0.15	0.15	...	0.15
Enable	0	0	...	1
Parameters				
Kd	0.003			
fc	200			
ts_fact	1			
Outputs				
Out	0	0	...	0.15
Exp. Out	0	0	...	0.15
Out (DSP)	0	0	...	0.15
Exp. Out (DSP)	0	0	...	0.15

Test settings	
Tolerance Out	±9,3132e-06 (±20000 LSB)

Test statistics	
Min CPU cycles	63
Max CPU cycles	436
Avg CPU cycles	373

Test case: Conversion test OK

Conversion test for Control block DLimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
ts_fact	1	1	...	1
Controller parameters				
b1d	0	-824.183	...	31415.927
a0d	-1	-0.991	...	-0.73
b0d	0	824.183	...	-31415.927
Exp. b1d	0	-824.183	...	31415.927
Exp. a0d	-1	-0.991	...	-0.73
Exp. b0d	0	824.183	...	-31415.927

Test settings	
Tolerance b1d	±0,0000e+00
Tolerance a0d	±1,0000e-15
Tolerance b0d	±0,0000e+00

Test case: Conversion-on-Target test OK

Conversion-on-Target test for Control block DLimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
ts_fact	1	1	...	1
Controller parameters				
b1d	0	-824.183	...	31415.928
a0d	-1	-0.991	...	-0.73
b0d	0	824.183	...	-31415.928
Exp. b1d	0	-824.183	...	31415.927
Exp. a0d	-1	-0.991	...	-0.73
Exp. b0d	0	824.183	...	-31415.927

Test settings	
Tolerance b1d	±3,0000e-03
Tolerance a0d	±1,0000e-07
Tolerance b0d	±3,0000e-03

Test statistics	
Min CPU cycles	964
Max CPU cycles	1208
Avg CPU cycles	1195

Verification: DLimit Float32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for Control block DLimit.

Test results				
Time step	1	2	...	201
CPU cycles	76	64	...	108
Inputs				
In (DSP)	0	0	...	0
D0 (DSP)	0.02	0.02	...	0.02
max (DSP)	0.8	0.8	...	0.8
min (DSP)	0.15	0.15	...	0.15
Enable (DSP)	0	0	...	1
In	0	0	...	0
D0	0.02	0.02	...	0.02
max	0.8	0.8	...	0.8
min	0.15	0.15	...	0.15
Enable	0	0	...	1
Parameters				
Kd	0.003			
fc	200			
ts_fact	1			
Outputs				
Out	0	0	...	0.15
Exp. Out	0	0	...	0.15
Out (DSP)	0	0	...	0.15
Exp. Out (DSP)	0	0	...	0.15

Test settings	
Tolerance Out	±9,3132e-06 (±20000 LSB)

Test statistics	
Min CPU cycles	64
Max CPU cycles	121
Avg CPU cycles	107

Test case: Conversion test OK

Conversion test for Control block DLimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
ts_fact	1	1	...	1
Controller parameters				
b1d	0	-824.183	...	31415.927
a0d	-1	-0.991	...	-0.73
b0d	0	824.183	...	-31415.927
Exp. b1d	0	-824.183	...	31415.927
Exp. a0d	-1	-0.991	...	-0.73
Exp. b0d	0	824.183	...	-31415.927

Test settings	
Tolerance b1d	±0,0000e+00
Tolerance a0d	±1,0000e-15
Tolerance b0d	±0,0000e+00

Test case: Conversion-on-Target test OK

Conversion-on-Target test for Control block DLimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
ts_fact	1	1	...	1
Controller parameters				
b1d	0	-824.183	...	31415.928
a0d	-1	-0.991	...	-0.73
b0d	0	824.183	...	-31415.928
Exp. b1d	0	-824.183	...	31415.927
Exp. a0d	-1	-0.991	...	-0.73
Exp. b0d	0	824.183	...	-31415.927

Test settings	
Tolerance b1d	±3,0000e-03
Tolerance a0d	±1,0000e-07
Tolerance b0d	±3,0000e-03

Test statistics	
Min CPU cycles	1122
Max CPU cycles	1129
Avg CPU cycles	1128

Verification: DLimit Float32 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for Control block DLimit.

Test results				
Time step	1	2	...	201
CPU cycles	74	74	...	129
Inputs				
In (DSP)	0	0	...	0
D0 (DSP)	0.02	0.02	...	0.02
max (DSP)	0.8	0.8	...	0.8
min (DSP)	0.15	0.15	...	0.15
Enable (DSP)	0	0	...	1
In	0	0	...	0
D0	0.02	0.02	...	0.02
max	0.8	0.8	...	0.8
min	0.15	0.15	...	0.15
Enable	0	0	...	1
Parameters				
Kd	0.003			
fc	200			
ts_fact	1			
Outputs				
Out	0	0	...	0.15
Exp. Out	0	0	...	0.15
Out (DSP)	0	0	...	0.15
Exp. Out (DSP)	0	0	...	0.15

Test settings	
Tolerance Out	±9,3132e-06 (±20000 LSB)

Test statistics	
Min CPU cycles	74
Max CPU cycles	134
Avg CPU cycles	128

Test case: Conversion test **OK**

Conversion test for Control block DLimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
ts_fact	1	1	...	1
Controller parameters				
b1d	0	-824.183	...	31415.927
a0d	-1	-0.991	...	-0.73
b0d	0	824.183	...	-31415.927
Exp. b1d	0	-824.183	...	31415.927
Exp. a0d	-1	-0.991	...	-0.73
Exp. b0d	0	824.183	...	-31415.927

Test settings	
Tolerance b1d	±0,0000e+00
Tolerance a0d	±1,0000e-15
Tolerance b0d	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block DLimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
ts_fact	1	1	...	1
Controller parameters				
b1d	0	-824.183	...	31415.928
a0d	-1	-0.991	...	-0.73
b0d	0	824.183	...	-31415.928
Exp. b1d	0	-824.183	...	31415.927
Exp. a0d	-1	-0.991	...	-0.73
Exp. b0d	0	824.183	...	-31415.927

Test settings	
Tolerance b1d	±3,0000e-03
Tolerance a0d	±1,0000e-07
Tolerance b0d	±3,0000e-03

Test statistics	
Min CPU cycles	1568
Max CPU cycles	1845
Avg CPU cycles	1827

Verification: DLimit Float32 CPU dsPIC33EP256MC502

Date of Test	2026-06-23
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for Control block DLimit.

Test results				
Time step	1	2	...	201
CPU cycles	67	67	...	952
Inputs				
In (DSP)	0	0	...	0
D0 (DSP)	0.02	0.02	...	0.02
max (DSP)	0.8	0.8	...	0.8
min (DSP)	0.15	0.15	...	0.15
Enable (DSP)	0	0	...	1
In	0	0	...	0
D0	0.02	0.02	...	0.02
max	0.8	0.8	...	0.8
min	0.15	0.15	...	0.15
Enable	0	0	...	1
Parameters				
Kd	0.003			
fc	200			
ts_fact	1			
Outputs				
Out	0	0	...	0.15
Exp. Out	0	0	...	0.15
Out (DSP)	0	0	...	0.15
Exp. Out (DSP)	0	0	...	0.15

Test settings	
Tolerance Out	±9,3132e-06 (±20000 LSB)

Test statistics	
Min CPU cycles	67
Max CPU cycles	1118
Avg CPU cycles	1017

Test case: Conversion test OK

Conversion test for Control block DLimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
ts_fact	1	1	...	1
Controller parameters				
b1d	0	-824.183	...	31415.927
a0d	-1	-0.991	...	-0.73
b0d	0	824.183	...	-31415.927
Exp. b1d	0	-824.183	...	31415.927
Exp. a0d	-1	-0.991	...	-0.73
Exp. b0d	0	824.183	...	-31415.927

Test settings	
Tolerance b1d	±0,0000e+00
Tolerance a0d	±1,0000e-15
Tolerance b0d	±0,0000e+00

Test case: Conversion-on-Target test OK

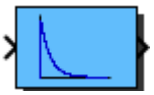
Conversion-on-Target test for Control block DLimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
ts_fact	1	1	...	1
Controller parameters				
b1d	0	-824.183	...	31415.928
a0d	-1	-0.991	...	-0.73
b0d	0	824.183	...	-31415.928
Exp. b1d	0	-824.183	...	31415.927
Exp. a0d	-1	-0.991	...	-0.73
Exp. b0d	0	824.183	...	-31415.927

Test settings	
Tolerance b1d	±3,0000e-03
Tolerance a0d	±1,0000e-07
Tolerance b0d	±3,0000e-03

Test statistics	
Min CPU cycles	3639
Max CPU cycles	7392
Avg CPU cycles	7022

Block: DT1



First order high pass:
G(s) = V*s/(s/w + 1)

Inports	
In	Input In(k)

Outports	
Out	Output Out(k)

Mask Parameters		
Name	**ID**	**Description**
V	1	Gain
fc	2	Cut off frequency of low pass filter
ts_fact	3	Multiplication factor of base sampling time (in integer format)
method	4	Discretization method

Description:

Due to limited value range in the 8 bit fixed point implementation rather high deviations from expected output values may occur.

Developer note: The source code of block *TF1* is used.

Implementations:

FiP8	8 Bit Fixed Point Implementation
FiP16	16 Bit Fixed Point Implementation
FiP32	32 Bit Fixed Point Implementation
Float32	32 Bit Floating Point Implementation
Float64	64 Bit Floating Point Implementation

Implementation: FiP8

8 Bit Fixed Point Implementation

Inports Data Type	
In	int8

Outports Data Type	
Out	int8

Implementation: FiP16

16 Bit Fixed Point Implementation

Inports Data Type	
In	int16

Outports Data Type	
Out	int16

Implementation: FiP32

32 Bit Fixed Point Implementation

Inports Data Type	
In	int32

Outports Data Type	
Out	int32

Implementation: Float32

32 Bit Floating Point Implementation

Inports Data Type	
In	float32

Outports Data Type	
Out	float32

Implementation: Float64

64 Bit Floating Point Implementation

Inports Data Type	
In	float64

Outports Data Type	
Out	float64

Verification: DT1 FiP16 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test — OK

Inport test for Control block DT1.

Test results						
Time step	1	2	3	4	...	105
CPU cycles	88	88	88	88	...	88
Inputs						
In (DSP)	0	0	0	0	...	-4915
In	0	0	0	0	...	-0.15
Parameters						
V	0.01					
fc	47					
ts_fact	1					
method	zoh					
Outputs						
Out	0	0	0	0	...	-0.157
Exp. Out	0	0	0	0	...	-0.158
Out (DSP)	0	0	0	0	...	-5153
Exp. Out (DSP)	0	0	0	0	...	-5172

Test settings	
Tolerance Out	±6,1035e-04 (±20 LSB)

Test statistics	
Min CPU cycles	88
Max CPU cycles	88
Avg CPU cycles	88

Verification: DT1 FiP16 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for Control block DT1.

Test results						
Time step	1	2	3	4	...	105
CPU cycles	69	69	69	69	...	69
Inputs						
In (DSP)	0	0	0	0	...	-4915
In	0	0	0	0	...	-0.15
Parameters						
V	0.01					
fc	47					
ts_fact	1					
method	zoh					
Outputs						
Out	0	0	0	0	...	-0.157
Exp. Out	0	0	0	0	...	-0.158
Out (DSP)	0	0	0	0	...	-5153
Exp. Out (DSP)	0	0	0	0	...	-5172

Test settings	
Tolerance Out	±6,1035e-04 (±20 LSB)

Test statistics	
Min CPU cycles	69
Max CPU cycles	69
Avg CPU cycles	69

Verification: DT1 FiP16 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for Control block DT1.

Test results						
Time step	1	2	3	4	...	105
CPU cycles	104	104	104	104	...	104
Inputs						
In (DSP)	0	0	0	0	...	-4915
In	0	0	0	0	...	-0.15
Parameters						
V	0.01					
fc	47					
ts_fact	1					
method	zoh					
Outputs						
Out	0	0	0	0	...	-0.157
Exp. Out	0	0	0	0	...	-0.158
Out (DSP)	0	0	0	0	...	-5153
Exp. Out (DSP)	0	0	0	0	...	-5172

Test settings	
Tolerance Out	±6,1035e-04 (±20 LSB)

Test statistics	
Min CPU cycles	104
Max CPU cycles	104
Avg CPU cycles	104

Verification: DT1 FiP16 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for Control block DT1.

Test results						
Time step	1	2	3	4	...	105
CPU cycles	96	96	96	96	...	96
Inputs						
In (DSP)	0	0	0	0	...	-4915
In	0	0	0	0	...	-0.15
Parameters						
V	0.01					
fc	47					
ts_fact	1					
method	zoh					
Outputs						
Out	0	0	0	0	...	-0.157
Exp. Out	0	0	0	0	...	-0.158
Out (DSP)	0	0	0	0	...	-5153
Exp. Out (DSP)	0	0	0	0	...	-5172

Test settings	
Tolerance Out	±6,1035e-04 (±20 LSB)

Test statistics	
Min CPU cycles	96
Max CPU cycles	155
Avg CPU cycles	96

Verification: DT1 FiP16 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for Control block DT1.

Test results						
Time step	1	2	3	4	...	105
CPU cycles	59	59	59	59	...	59
Inputs						
In (DSP)	0	0	0	0	...	-4915
In	0	0	0	0	...	-0.15
Parameters						
V	0.01					
fc	47					
ts_fact	1					
method	zoh					
Outputs						
Out	0	0	0	0	...	-0.157
Exp. Out	0	0	0	0	...	-0.158
Out (DSP)	0	0	0	0	...	-5153
Exp. Out (DSP)	0	0	0	0	...	-5172

Test settings	
Tolerance Out	±6,1035e-04 (±20 LSB)

Test statistics	
Min CPU cycles	59
Max CPU cycles	59
Avg CPU cycles	59

Verification: DT1 FiP16 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for Control block DT1.

Test results						
Time step	1	2	3	4	...	105
CPU cycles	122	96	96	96	...	96
Inputs						
In (DSP)	0	0	0	0	...	-4915
In	0	0	0	0	...	-0.15
Parameters						
V	0.01					
fc	47					
ts_fact	1					
method	zoh					
Outputs						
Out	0	0	0	0	...	-0.157
Exp. Out	0	0	0	0	...	-0.158
Out (DSP)	0	0	0	0	...	-5153
Exp. Out (DSP)	0	0	0	0	...	-5172

Test settings	
Tolerance Out	±6,1035e-04 (±20 LSB)

Test statistics	
Min CPU cycles	96
Max CPU cycles	122
Avg CPU cycles	96

Verification: DT1 FiP16 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for Control block DT1.

Test results						
Time step	1	2	3	4	...	105
CPU cycles	86	86	86	86	...	86
Inputs						
In (DSP)	0	0	0	0	...	-4915
In	0	0	0	0	...	-0.15
Parameters						
V	0.01					
fc	47					
ts_fact	1					
method	zoh					
Outputs						
Out	0	0	0	0	...	-0.157
Exp. Out	0	0	0	0	...	-0.158
Out (DSP)	0	0	0	0	...	-5153
Exp. Out (DSP)	0	0	0	0	...	-5172

Test settings	
Tolerance Out	±6,1035e-04 (±20 LSB)

Test statistics	
Min CPU cycles	86
Max CPU cycles	86
Avg CPU cycles	86

Verification: DT1 FiP16 CPU dsPIC33EP256MC502

Date of Test	2026-06-23
Target controller	dsPIC33EP256MC502

Test case: Inport test

OK

Inport test for Control block DT1.

Test results						
Time step	1	2	3	4	...	105
CPU cycles	91	91	91	91	...	91
Inputs						
In (DSP)	0	0	0	0	...	-4915
In	0	0	0	0	...	-0.15
Parameters						
V	0.01					
fc	47					
ts_fact	1					
method	zoh					
Outputs						
Out	0	0	0	0	...	-0.157
Exp. Out	0	0	0	0	...	-0.158
Out (DSP)	0	0	0	0	...	-5153
Exp. Out (DSP)	0	0	0	0	...	-5172

Test settings	
Tolerance Out	±6,1035e-04 (±20 LSB)

Test statistics	
Min CPU cycles	91
Max CPU cycles	91
Avg CPU cycles	91

Verification: DT1 FiP32 CPU TMS320F28335

Date of Test 2026-06-19

Target controller TMS320F28335

Test case: Inport test OK

Inport test for Control block DT1.

Test results				
Time step	1	2	...	105
CPU cycles	221	221	...	221
Inputs				
In (DSP)	0	0	...	-322122547
In	0	0	...	-0.15
Parameters				
V	0.01			
fc	47			
ts_fact	1			
method	zoh			
Outputs				
Out	0	0	...	-0.158
Exp. Out	0	0	...	-0.158
Out (DSP)	0	0	...	-338924496
Exp. Out (DSP)	0	0	...	-338924509

Test settings	
Tolerance Out	±9,3132e-09 (±20 LSB)

Test statistics	
Min CPU cycles	221
Max CPU cycles	221
Avg CPU cycles	221

Verification: DT1 FiP32 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test — OK

Inport test for Control block DT1.

Test results				
Time step	1	2	...	105
CPU cycles	121	121	...	121
Inputs				
In (DSP)	0	0	...	-322122547
In	0	0	...	-0.15
Parameters				
V	0.01			
fc	47			
ts_fact	1			
method	zoh			
Outputs				
Out	0	0	...	-0.158
Exp. Out	0	0	...	-0.158
Out (DSP)	0	0	...	-338924496
Exp. Out (DSP)	0	0	...	-338924509

Test settings	
Tolerance Out	±9,3132e-09 (±20 LSB)

Test statistics	
Min CPU cycles	121
Max CPU cycles	121
Avg CPU cycles	121

Verification: DT1 FiP32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for Control block DT1.

Test results				
Time step	1	2	...	105
CPU cycles	142	142	...	142
Inputs				
In (DSP)	0	0	...	-322122547
In	0	0	...	-0.15
Parameters				
V	0.01			
fc	47			
ts_fact	1			
method	zoh			
Outputs				
Out	0	0	...	-0.158
Exp. Out	0	0	...	-0.158
Out (DSP)	0	0	...	-338924496
Exp. Out (DSP)	0	0	...	-338924509

Test settings	
Tolerance Out	±9,3132e-09 (±20 LSB)

Test statistics	
Min CPU cycles	142
Max CPU cycles	142
Avg CPU cycles	142

Verification: DT1 FiP32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for Control block DT1.

Test results				
Time step	1	2	...	105
CPU cycles	373	373	...	381
Inputs				
In (DSP)	0	0	...	-322122547
In	0	0	...	-0.15
Parameters				
V	0.01			
fc	47			
ts_fact	1			
method	zoh			
Outputs				
Out	0	0	...	-0.158
Exp. Out	0	0	...	-0.158
Out (DSP)	0	0	...	-338924496
Exp. Out (DSP)	0	0	...	-338924509

Test settings	
Tolerance Out	±9,3132e-09 (±20 LSB)

Test statistics	
Min CPU cycles	373
Max CPU cycles	442
Avg CPU cycles	377

Verification: DT1 FiP32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for Control block DT1.

Test results				
Time step	1	2	...	105
CPU cycles	87	87	...	89
Inputs				
In (DSP)	0	0	...	-322122547
In	0	0	...	-0.15
Parameters				
V	0.01			
fc	47			
ts_fact	1			
method	zoh			
Outputs				
Out	0	0	...	-0.158
Exp. Out	0	0	...	-0.158
Out (DSP)	0	0	...	-338924496
Exp. Out (DSP)	0	0	...	-338924509

Test settings	
Tolerance Out	±9,3132e-09 (±20 LSB)

Test statistics	
Min CPU cycles	87
Max CPU cycles	89
Avg CPU cycles	88

Verification: DT1 FiP32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for Control block DT1.

Test results				
Time step	1	2	...	105
CPU cycles	150	133	...	133
Inputs				
In (DSP)	0	0	...	-322122547
In	0	0	...	-0.15
Parameters				
V	0.01			
fc	47			
ts_fact	1			
method	zoh			
Outputs				
Out	0	0	...	-0.158
Exp. Out	0	0	...	-0.158
Out (DSP)	0	0	...	-338924496
Exp. Out (DSP)	0	0	...	-338924509

Test settings	
Tolerance Out	±9,3132e-09 (±20 LSB)

Test statistics	
Min CPU cycles	133
Max CPU cycles	150
Avg CPU cycles	133

Verification: DT1 FiP32 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for Control block DT1.

Test results				
Time step	1	2	...	105
CPU cycles	191	191	...	191
Inputs				
In (DSP)	0	0	...	-322122547
In	0	0	...	-0.15
Parameters				
V	0.01			
fc	47			
ts_fact	1			
method	zoh			
Outputs				
Out	0	0	...	-0.158
Exp. Out	0	0	...	-0.158
Out (DSP)	0	0	...	-338924496
Exp. Out (DSP)	0	0	...	-338924509

Test settings	
Tolerance Out	±9,3132e-09 (±20 LSB)

Test statistics	
Min CPU cycles	191
Max CPU cycles	191
Avg CPU cycles	191

Verification: DT1 FiP32 CPU dsPIC33EP256MC502

Date of Test	2026-06-23
Target controller	dsPIC33EP256MC502

Test case: Inport test — OK

Inport test for Control block DT1.

Test results				
Time step	1	2	...	105
CPU cycles	1025	1025	...	1034
Inputs				
In (DSP)	0	0	...	-322122547
In	0	0	...	-0.15
Parameters				
V	0.01			
fc	47			
ts_fact	1			
method	zoh			
Outputs				
Out	0	0	...	-0.158
Exp. Out	0	0	...	-0.158
Out (DSP)	0	0	...	-338924496
Exp. Out (DSP)	0	0	...	-338924509

Test settings	
Tolerance Out	±9,3132e-09 (±20 LSB)

Test statistics	
Min CPU cycles	1025
Max CPU cycles	1034
Avg CPU cycles	1029

Block: I



I controller:
G(s) = Ki/s = 1/(Ti*s)

Inports	
In	Control error input
I0	Integral value which is loaded at initialization function call
Enable	Enable == 0: Deactivation of block; Out set to 0 Enable 0->1: Preload of integral part Enable == 1: Activation of block

Outports	
Out	Control value

Mask Parameters		
Name	**ID**	**Description**
Ki	1	Integral Factor
ts_fact	2	Multiplication factor of base sampling time (in integer format)

Description:

Each fixed point implementation uses the next higher integer datatype for the integrational value storage variable.
A rising flank at the *Enable* inport will preload the integrational part with the value present on the *Init* inport.

Transfer function (zero-order hold discretization method):

$$G(z) = K_{\mathrm{i}} T_{\mathrm{s}} \frac{1}{z-1}$$

Developer note: The source code of block *ILimit* is used.

Implementations:

FiP16 16 Bit Fixed Point Implementation
FiP32 32 Bit Fixed Point Implementation
Float32 32 Bit Floating Point Implementation
Float64 64 Bit Floating Point Implementation

Implementation: FiP16

16 Bit Fixed Point Implementation

Inports Data Type	
In	int16
I0	int16
Enable	bool

Outports Data Type	
Out	int16

Implementation: FiP32

32 Bit Fixed Point Implementation

Inports Data Type	
In	int32
I0	int32
Enable	bool

Outports Data Type	
Out	int32

Implementation: Float32

32 Bit Floating Point Implementation

Inports Data Type	
In	float32
I0	float32
Enable	bool

Outports Data Type	
Out	float32

Implementation: Float64

64 Bit Floating Point Implementation

Inports Data Type	
In	float64
I0	float64
Enable	bool

Outports Data Type	
Out	float64

Verification: I FiP16 CPU TMS320F28335

Date of Test 2026-06-19

Target controller TMS320F28335

Test case: Inport test OK

Inport test for Control block I.

Test results						
Time step	1	2	3	4	...	201
CPU cycles	68	68	68	120	...	115
Inputs						
In (DSP)	0	0	0	0	...	0
I0 (DSP)	3604	3604	3604	3604	...	3604
Enable (DSP)	0	0	0	1	...	1
In	0	0	0	0	...	0
I0	0.11	0.11	0.11	0.11	...	0.11
Enable	0	0	0	1	...	1
Parameters						
Ki	2500					
ts_fact	1					
Outputs						
Out	0	0	0	0.11	...	-1
Exp. Out	0	0	0	0.11	...	-1
Out (DSP)	0	0	0	3604	...	-32767
Exp. Out (DSP)	0	0	0	3604	...	-32768

Test settings	
Tolerance Out	±3,0518e-04 (±10 LSB)

Test statistics	
Min CPU cycles	68
Max CPU cycles	124
Avg CPU cycles	114

Test case: Conversion test OK

Conversion test for Control block I.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Ki	-11	-10.389	-9.778	-9.167	...	11
ts_fact	1	2	3	4	...	37
Controller parameters						
b0	-36	-68	-96	-120	...	1334
sfr	15	15	15	15	...	15
Exp. b0	-36	-68	-96	-120	...	1334
Exp. sfr	15	15	15	15	...	15

Test settings	
Tolerance b0	±0,0000e+00
Tolerance sfr	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block I.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Ki	-11	-10.389	-9.778	-9.167	...	11
ts_fact	1	2	3	4	...	37
Controller parameters						
b0	-36	-68	-96	-120	...	1333
sfr	15	15	15	15	...	15
Exp. b0	-36	-68	-96	-120	...	1334
Exp. sfr	15	15	15	15	...	15

Test settings	
Tolerance b0	±1,0000e+00
Tolerance sfr	±0,0000e+00

Test statistics	
Min CPU cycles	2082
Max CPU cycles	2176
Avg CPU cycles	2166

Verification: I FiP16 CPU TM4C123GH6

Date of Test 2026-06-19

Target controller TM4C123GH6

Test case: Inport test OK

Inport test for Control block I.

Test results						
Time step	1	2	3	4	...	201
CPU cycles	45	45	45	73	...	69
Inputs						
In (DSP)	0	0	0	0	...	0
I0 (DSP)	3604	3604	3604	3604	...	3604
Enable (DSP)	0	0	0	1	...	1
In	0	0	0	0	...	0
I0	0.11	0.11	0.11	0.11	...	0.11
Enable	0	0	0	1	...	1
Parameters						
Ki	2500					
ts_fact	1					
Outputs						
Out	0	0	0	0.11	...	-1
Exp. Out	0	0	0	0.11	...	-1
Out (DSP)	0	0	0	3604	...	-32767
Exp. Out (DSP)	0	0	0	3604	...	-32768

Test settings	
Tolerance Out	±3,0518e-04 (±10 LSB)

Test statistics	
Min CPU cycles	45
Max CPU cycles	81
Avg CPU cycles	69

Test case: Conversion test OK

Conversion test for Control block I.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Ki	-11	-10.389	-9.778	-9.167	...	11
ts_fact	1	2	3	4	...	37
Controller parameters						
b0	-36	-68	-96	-120	...	1334
sfr	15	15	15	15	...	15
Exp. b0	-36	-68	-96	-120	...	1334
Exp. sfr	15	15	15	15	...	15

Test settings	
Tolerance b0	±0,0000e+00
Tolerance sfr	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block I.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Ki	-11	-10.389	-9.778	-9.167	...	11
ts_fact	1	2	3	4	...	37
Controller parameters						
b0	-36	-68	-96	-120	...	1333
sfr	15	15	15	15	...	15
Exp. b0	-36	-68	-96	-120	...	1334
Exp. sfr	15	15	15	15	...	15

Test settings	
Tolerance b0	±1,0000e+00
Tolerance sfr	±0,0000e+00

Test statistics	
Min CPU cycles	1071
Max CPU cycles	1141
Avg CPU cycles	1139

Verification: I FiP16 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for Control block I.

Test results						
Time step	1	2	3	4	...	201
CPU cycles	68	68	68	112	...	137
Inputs						
In (DSP)	0	0	0	0	...	0
I0 (DSP)	3604	3604	3604	3604	...	3604
Enable (DSP)	0	0	0	1	...	1
In	0	0	0	0	...	0
I0	0.11	0.11	0.11	0.11	...	0.11
Enable	0	0	0	1	...	1
Parameters						
Ki	2500					
ts_fact	1					
Outputs						
Out	0	0	0	0.11	...	-1
Exp. Out	0	0	0	0.11	...	-1
Out (DSP)	0	0	0	3604	...	-32767
Exp. Out (DSP)	0	0	0	3604	...	-32768

Test settings	
Tolerance Out	±3,0518e-04 (±10 LSB)

Test statistics	
Min CPU cycles	68
Max CPU cycles	141
Avg CPU cycles	134

Test case: Conversion test OK

Conversion test for Control block I.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Ki	-11	-10.389	-9.778	-9.167	...	11
ts_fact	1	2	3	4	...	37
Controller parameters						
b0	-36	-68	-96	-120	...	1334
sfr	15	15	15	15	...	15
Exp. b0	-36	-68	-96	-120	...	1334
Exp. sfr	15	15	15	15	...	15

Test settings	
Tolerance b0	±0,0000e+00
Tolerance sfr	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block I.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Ki	-11	-10.389	-9.778	-9.167	...	11
ts_fact	1	2	3	4	...	37
Controller parameters						
b0	-36	-68	-96	-120	...	1333
sfr	15	15	15	15	...	15
Exp. b0	-36	-68	-96	-120	...	1334
Exp. sfr	15	15	15	15	...	15

Test settings	
Tolerance b0	±1,0000e+00
Tolerance sfr	±0,0000e+00

Test statistics	
Min CPU cycles	1186
Max CPU cycles	1299
Avg CPU cycles	1225

Verification: I FiP16 CPU STM32F072RB

Date of Test 2026-06-19

Target controller STM32F072RB

Test case: Inport test OK

Inport test for Control block I.

Test results						
Time step	1	2	3	4	...	201
CPU cycles	65	65	65	102	...	111
Inputs						
In (DSP)	0	0	0	0	...	0
I0 (DSP)	3604	3604	3604	3604	...	3604
Enable (DSP)	0	0	0	1	...	1
In	0	0	0	0	...	0
I0	0.11	0.11	0.11	0.11	...	0.11
Enable	0	0	0	1	...	1
Parameters						
Ki	2500					
ts_fact	1					
Outputs						
Out	0	0	0	0.11	...	-1
Exp. Out	0	0	0	0.11	...	-1
Out (DSP)	0	0	0	3604	...	-32767
Exp. Out (DSP)	0	0	0	3604	...	-32768

Test settings	
Tolerance Out	±3,0518e-04 (±10 LSB)

Test statistics	
Min CPU cycles	65
Max CPU cycles	111
Avg CPU cycles	109

Test case: Conversion test OK

Conversion test for Control block I.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Ki	-11	-10.389	-9.778	-9.167	...	11
ts_fact	1	2	3	4	...	37
Controller parameters						
b0	-36	-68	-96	-120	...	1334
sfr	15	15	15	15	...	15
Exp. b0	-36	-68	-96	-120	...	1334
Exp. sfr	15	15	15	15	...	15

Test settings	
Tolerance b0	±0,0000e+00
Tolerance sfr	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block I.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Ki	-11	-10.389	-9.778	-9.167	...	11
ts_fact	1	2	3	4	...	37
Controller parameters						
b0	-36	-68	-96	-120	...	1333
sfr	15	15	15	15	...	15
Exp. b0	-36	-68	-96	-120	...	1334
Exp. sfr	15	15	15	15	...	15

Test settings	
Tolerance b0	±1,0000e+00
Tolerance sfr	±0,0000e+00

Test statistics	
Min CPU cycles	2537
Max CPU cycles	3021
Avg CPU cycles	2947

Verification: I FiP16 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test

OK

Inport test for Control block I.

Test results						
Time step	1	2	3	4	...	201
CPU cycles	31	31	31	60	...	61
Inputs						
In (DSP)	0	0	0	0	...	0
I0 (DSP)	3604	3604	3604	3604	...	3604
Enable (DSP)	0	0	0	1	...	1
In	0	0	0	0	...	0
I0	0.11	0.11	0.11	0.11	...	0.11
Enable	0	0	0	1	...	1
Parameters						
Ki	2500					
ts_fact	1					
Outputs						
Out	0	0	0	0.11	...	-1
Exp. Out	0	0	0	0.11	...	-1
Out (DSP)	0	0	0	3604	...	-32767
Exp. Out (DSP)	0	0	0	3604	...	-32768

Test settings	
Tolerance Out	±3,0518e-04 (±10 LSB)

Test statistics	
Min CPU cycles	31
Max CPU cycles	69
Avg CPU cycles	61

Test case: Conversion test

OK

Conversion test for Control block I.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Ki	-11	-10.389	-9.778	-9.167	...	11
ts_fact	1	2	3	4	...	37
Controller parameters						
b0	-36	-68	-96	-120	...	1334
sfr	15	15	15	15	...	15
Exp. b0	-36	-68	-96	-120	...	1334
Exp. sfr	15	15	15	15	...	15

Test settings	
Tolerance b0	±0,0000e+00
Tolerance sfr	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block I.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Ki	-11	-10.389	-9.778	-9.167	...	11
ts_fact	1	2	3	4	...	37
Controller parameters						
b0	-36	-68	-96	-120	...	1333
sfr	15	15	15	15	...	15
Exp. b0	-36	-68	-96	-120	...	1334
Exp. sfr	15	15	15	15	...	15

Test settings	
Tolerance b0	±1,0000e+00
Tolerance sfr	±0,0000e+00

Test statistics	
Min CPU cycles	1072
Max CPU cycles	1188
Avg CPU cycles	1179

Verification: I FiP16 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for Control block I.

Test results						
Time step	1	2	3	4	...	201
CPU cycles	73	59	59	115	...	90
Inputs						
In (DSP)	0	0	0	0	...	0
I0 (DSP)	3604	3604	3604	3604	...	3604
Enable (DSP)	0	0	0	1	...	1
In	0	0	0	0	...	0
I0	0.11	0.11	0.11	0.11	...	0.11
Enable	0	0	0	1	...	1
Parameters						
Ki	2500					
ts_fact	1					
Outputs						
Out	0	0	0	0.11	...	-1
Exp. Out	0	0	0	0.11	...	-1
Out (DSP)	0	0	0	3604	...	-32767
Exp. Out (DSP)	0	0	0	3604	...	-32768

Test settings	
Tolerance Out	±3,0518e-04 (±10 LSB)

Test statistics	
Min CPU cycles	59
Max CPU cycles	115
Avg CPU cycles	90

Test case: Conversion test OK

Conversion test for Control block I.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Ki	-11	-10.389	-9.778	-9.167	...	11
ts_fact	1	2	3	4	...	37
Controller parameters						
b0	-36	-68	-96	-120	...	1334
sfr	15	15	15	15	...	15
Exp. b0	-36	-68	-96	-120	...	1334
Exp. sfr	15	15	15	15	...	15

Test settings	
Tolerance b0	±0,0000e+00
Tolerance sfr	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block I.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Ki	-11	-10.389	-9.778	-9.167	...	11
ts_fact	1	2	3	4	...	37
Controller parameters						
b0	-36	-68	-96	-120	...	1333
sfr	15	15	15	15	...	15
Exp. b0	-36	-68	-96	-120	...	1334
Exp. sfr	15	15	15	15	...	15

Test settings	
Tolerance b0	±1,0000e+00
Tolerance sfr	±0,0000e+00

Test statistics	
Min CPU cycles	843
Max CPU cycles	966
Avg CPU cycles	864

Verification: I FiP16 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for Control block I.

Test results						
Time step	1	2	3	4	...	201
CPU cycles	61	61	61	128	...	120
Inputs						
In (DSP)	0	0	0	0	...	0
I0 (DSP)	3604	3604	3604	3604	...	3604
Enable (DSP)	0	0	0	1	...	1
In	0	0	0	0	...	0
I0	0.11	0.11	0.11	0.11	...	0.11
Enable	0	0	0	1	...	1
Parameters						
Ki	2500					
ts_fact	1					
Outputs						
Out	0	0	0	0.11	...	-1
Exp. Out	0	0	0	0.11	...	-1
Out (DSP)	0	0	0	3604	...	-32767
Exp. Out (DSP)	0	0	0	3604	...	-32768

Test settings	
Tolerance Out	±3,0518e-04 (±10 LSB)

Test statistics	
Min CPU cycles	61
Max CPU cycles	128
Avg CPU cycles	119

Test case: Conversion test OK

Conversion test for Control block I.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Ki	-11	-10.389	-9.778	-9.167	...	11
ts_fact	1	2	3	4	...	37
Controller parameters						
b0	-36	-68	-96	-120	...	1334
sfr	15	15	15	15	...	15
Exp. b0	-36	-68	-96	-120	...	1334
Exp. sfr	15	15	15	15	...	15

Test settings	
Tolerance b0	±0,0000e+00
Tolerance sfr	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block I.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Ki	-11	-10.389	-9.778	-9.167	...	11
ts_fact	1	2	3	4	...	37
Controller parameters						
b0	-36	-68	-96	-120	...	1333
sfr	15	15	15	15	...	15
Exp. b0	-36	-68	-96	-120	...	1334
Exp. sfr	15	15	15	15	...	15

Test settings	
Tolerance b0	±1,0000e+00
Tolerance sfr	±0,0000e+00

Test statistics	
Min CPU cycles	1582
Max CPU cycles	1652
Avg CPU cycles	1647

Verification: I FiP16 CPU dsPIC33EP256MC502

Date of Test	2026-06-23
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for Control block I.

Test results						
Time step	1	2	3	4	...	201
CPU cycles	52	52	52	100	...	92
Inputs						
In (DSP)	0	0	0	0	...	0
I0 (DSP)	3604	3604	3604	3604	...	3604
Enable (DSP)	0	0	0	1	...	1
In	0	0	0	0	...	0
I0	0.11	0.11	0.11	0.11	...	0.11
Enable	0	0	0	1	...	1
Parameters						
Ki	2500					
ts_fact	1					
Outputs						
Out	0	0	0	0.11	...	-1
Exp. Out	0	0	0	0.11	...	-1
Out (DSP)	0	0	0	3604	...	-32767
Exp. Out (DSP)	0	0	0	3604	...	-32768

Test settings	
Tolerance Out	±3,0518e-04 (±10 LSB)

Test statistics	
Min CPU cycles	52
Max CPU cycles	101
Avg CPU cycles	92

Test case: Conversion test OK

Conversion test for Control block I.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Ki	-11	-10.389	-9.778	-9.167	...	11
ts_fact	1	2	3	4	...	37
Controller parameters						
b0	-36	-68	-96	-120	...	1334
sfr	15	15	15	15	...	15
Exp. b0	-36	-68	-96	-120	...	1334
Exp. sfr	15	15	15	15	...	15

Test settings	
Tolerance b0	±0,0000e+00
Tolerance sfr	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block I.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Ki	-11	-10.389	-9.778	-9.167	...	11
ts_fact	1	2	3	4	...	37
Controller parameters						
b0	-36	-68	-96	-120	...	1333
sfr	15	15	15	15	...	15
Exp. b0	-36	-68	-96	-120	...	1334
Exp. sfr	15	15	15	15	...	15

Test settings	
Tolerance b0	±1,0000e+00
Tolerance sfr	±0,0000e+00

Test statistics	
Min CPU cycles	4133
Max CPU cycles	5289
Avg CPU cycles	5242

Verification: I FiP32 CPU TMS320F28335

Date of Test 2026-06-19

Target controller TMS320F28335

Test case: Inport test OK

Inport test for Control block I.

Test results				
Time step	1	2	...	201
CPU cycles	84	84	...	250
Inputs				
In (DSP)	0	0	...	0
I0 (DSP)	236223201	236223201	...	236223201
Enable (DSP)	0	0	...	1
In	0	0	...	0
I0	0.11	0.11	...	0.11
Enable	0	0	...	1
Parameters				
Ki	2500			
ts_fact	1			
Outputs				
Out	0	0	...	-1
Exp. Out	0	0	...	-1
Out (DSP)	0	0	...	-2147483647
Exp. Out (DSP)	0	0	...	-2147483647

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	84
Max CPU cycles	328
Avg CPU cycles	251

Test case: Conversion test OK

Conversion test for Control block I.

Test results				
Time step	1	2	...	37
Mask parameters				
Ki	-11	-10.389	...	11
ts_fact	1	2	...	37
Controller parameters				
b0	-2362232	-4461994	...	87402584
sfr	31	31	...	31
Exp. b0	-2362232	-4461994	...	87402584
Exp. sfr	31	31	...	31

Test settings	
Tolerance b0	±0,0000e+00
Tolerance sfr	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block I.

Test results				
Time step	1	2	...	37
Mask parameters				
Ki	-11	-10.389	...	11
ts_fact	1	2	...	37
Controller parameters				
b0	-2362232	-4461994	...	87402584
sfr	31	31	...	31
Exp. b0	-2362232	-4461994	...	87402584
Exp. sfr	31	31	...	31

Test settings	
Tolerance b0	±1,0000e+01
Tolerance sfr	±0,0000e+00

Test statistics	
Min CPU cycles	2275
Max CPU cycles	2417
Avg CPU cycles	2402

Verification: I FiP32 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for Control block I.

Test results				
Time step	1	2	...	201
CPU cycles	55	55	...	127
Inputs				
In (DSP)	0	0	...	0
I0 (DSP)	236223201	236223201	...	236223201
Enable (DSP)	0	0	...	1
In	0	0	...	0
I0	0.11	0.11	...	0.11
Enable	0	0	...	1
Parameters				
Ki	2500			
ts_fact	1			
Outputs				
Out	0	0	...	-1
Exp. Out	0	0	...	-1
Out (DSP)	0	0	...	-2147483647
Exp. Out (DSP)	0	0	...	-2147483647

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	55
Max CPU cycles	139
Avg CPU cycles	126

Test case: Conversion test OK

Conversion test for Control block I.

Test results				
Time step	1	2	...	37
Mask parameters				
Ki	-11	-10.389	...	11
ts_fact	1	2	...	37
Controller parameters				
b0	-2362232	-4461994	...	87402584
sfr	31	31	...	31
Exp. b0	-2362232	-4461994	...	87402584
Exp. sfr	31	31	...	31

Test settings	
Tolerance b0	±0,0000e+00
Tolerance sfr	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block I.

Test results				
Time step	1	2	...	37
Mask parameters				
Ki	-11	-10.389	...	11
ts_fact	1	2	...	37
Controller parameters				
b0	-2362232	-4461994	...	87402584
sfr	31	31	...	31
Exp. b0	-2362232	-4461994	...	87402584
Exp. sfr	31	31	...	31

Test settings	
Tolerance b0	±1,0000e+01
Tolerance sfr	±0,0000e+00

Test statistics	
Min CPU cycles	1027
Max CPU cycles	1125
Avg CPU cycles	1121

Verification: I FiP32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for Control block I.

Test results				
Time step	1	2	...	201
CPU cycles	81	81	...	169
Inputs				
In (DSP)	0	0	...	0
I0 (DSP)	236223201	236223201	...	236223201
Enable (DSP)	0	0	...	1
In	0	0	...	0
I0	0.11	0.11	...	0.11
Enable	0	0	...	1
Parameters				
Ki	2500			
ts_fact	1			
Outputs				
Out	0	0	...	-1
Exp. Out	0	0	...	-1
Out (DSP)	0	0	...	-2147483647
Exp. Out (DSP)	0	0	...	-2147483647

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	81
Max CPU cycles	176
Avg CPU cycles	167

Test case: Conversion test OK

Conversion test for Control block I.

Test results				
Time step	1	2	...	37
Mask parameters				
Ki	-11	-10.389	...	11
ts_fact	1	2	...	37
Controller parameters				
b0	-2362232	-4461994	...	87402584
sfr	31	31	...	31
Exp. b0	-2362232	-4461994	...	87402584
Exp. sfr	31	31	...	31

Test settings	
Tolerance b0	±0,0000e+00
Tolerance sfr	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block I.

Test results				
Time step	1	2	...	37
Mask parameters				
Ki	-11	-10.389	...	11
ts_fact	1	2	...	37
Controller parameters				
b0	-2362232	-4461994	...	87402584
sfr	31	31	...	31
Exp. b0	-2362232	-4461994	...	87402584
Exp. sfr	31	31	...	31

Test settings	
Tolerance b0	±1,0000e+01
Tolerance sfr	±0,0000e+00

Test statistics	
Min CPU cycles	1563
Max CPU cycles	1667
Avg CPU cycles	1596

Verification: I FiP32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for Control block I.

Test results				
Time step	1	2	...	201
CPU cycles	91	91	...	248
Inputs				
In (DSP)	0	0	...	0
I0 (DSP)	236223201	236223201	...	236223201
Enable (DSP)	0	0	...	1
In	0	0	...	0
I0	0.11	0.11	...	0.11
Enable	0	0	...	1
Parameters				
Ki	2500			
ts_fact	1			
Outputs				
Out	0	0	...	-1
Exp. Out	0	0	...	-1
Out (DSP)	0	0	...	-2147483647
Exp. Out (DSP)	0	0	...	-2147483647

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	91
Max CPU cycles	296
Avg CPU cycles	241

Test case: Conversion test OK

Conversion test for Control block I.

Test results				
Time step	1	2	...	37
Mask parameters				
Ki	-11	-10.389	...	11
ts_fact	1	2	...	37
Controller parameters				
b0	-2362232	-4461994	...	87402584
sfr	31	31	...	31
Exp. b0	-2362232	-4461994	...	87402584
Exp. sfr	31	31	...	31

Test settings	
Tolerance b0	±0,0000e+00
Tolerance sfr	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block I.

Test results				
Time step	1	2	...	37
Mask parameters				
Ki	-11	-10.389	...	11
ts_fact	1	2	...	37
Controller parameters				
b0	-2362232	-4461994	...	87402584
sfr	31	31	...	31
Exp. b0	-2362232	-4461994	...	87402584
Exp. sfr	31	31	...	31

Test settings	
Tolerance b0	±1,0000e+01
Tolerance sfr	±0,0000e+00

Test statistics	
Min CPU cycles	3570
Max CPU cycles	4293
Avg CPU cycles	4224

Verification: I FiP32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for Control block I.

Test results				
Time step	1	2	...	201
CPU cycles	31	31	...	84
Inputs				
In (DSP)	0	0	...	0
I0 (DSP)	236223201	236223201	...	236223201
Enable (DSP)	0	0	...	1
In	0	0	...	0
I0	0.11	0.11	...	0.11
Enable	0	0	...	1
Parameters				
Ki	2500			
ts_fact	1			
Outputs				
Out	0	0	...	-1
Exp. Out	0	0	...	-1
Out (DSP)	0	0	...	-2147483647
Exp. Out (DSP)	0	0	...	-2147483647

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	31
Max CPU cycles	97
Avg CPU cycles	84

Test case: Conversion test OK

Conversion test for Control block I.

Test results				
Time step	1	2	...	37
Mask parameters				
Ki	-11	-10.389	...	11
ts_fact	1	2	...	37
Controller parameters				
b0	-2362232	-4461994	...	87402584
sfr	31	31	...	31
Exp. b0	-2362232	-4461994	...	87402584
Exp. sfr	31	31	...	31

Test settings	
Tolerance b0	±0,0000e+00
Tolerance sfr	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block I.

Test results				
Time step	1	2	...	37
Mask parameters				
Ki	-11	-10.389	...	11
ts_fact	1	2	...	37
Controller parameters				
b0	-2362232	-4461994	...	87402584
sfr	31	31	...	31
Exp. b0	-2362232	-4461994	...	87402584
Exp. sfr	31	31	...	31

Test settings	
Tolerance b0	±1,0000e+01
Tolerance sfr	±0,0000e+00

Test statistics	
Min CPU cycles	1528
Max CPU cycles	1722
Avg CPU cycles	1707

Verification: I FiP32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for Control block I.

Test results				
Time step	1	2	...	201
CPU cycles	77	59	...	130
Inputs				
In (DSP)	0	0	...	0
I0 (DSP)	236223201	236223201	...	236223201
Enable (DSP)	0	0	...	1
In	0	0	...	0
I0	0.11	0.11	...	0.11
Enable	0	0	...	1
Parameters				
Ki	2500			
ts_fact	1			
Outputs				
Out	0	0	...	-1
Exp. Out	0	0	...	-1
Out (DSP)	0	0	...	-2147483647
Exp. Out (DSP)	0	0	...	-2147483647

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	59
Max CPU cycles	161
Avg CPU cycles	129

Test case: Conversion test OK

Conversion test for Control block I.

Test results				
Time step	1	2	...	37
Mask parameters				
Ki	-11	-10.389	...	11
ts_fact	1	2	...	37
Controller parameters				
b0	-2362232	-4461994	...	87402584
sfr	31	31	...	31
Exp. b0	-2362232	-4461994	...	87402584
Exp. sfr	31	31	...	31

Test settings	
Tolerance b0	±0,0000e+00
Tolerance sfr	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block I.

Test results				
Time step	1	2	...	37
Mask parameters				
Ki	-11	-10.389	...	11
ts_fact	1	2	...	37
Controller parameters				
b0	-2362232	-4461994	...	87402584
sfr	31	31	...	31
Exp. b0	-2362232	-4461994	...	87402584
Exp. sfr	31	31	...	31

Test settings	
Tolerance b0	±1,0000e+01
Tolerance sfr	±0,0000e+00

Test statistics	
Min CPU cycles	1165
Max CPU cycles	1308
Avg CPU cycles	1193

Verification: I FiP32 CPU TMS320F28379D

Date of Test 2026-06-22

Target controller TMS320F28379D

Test case: Inport test OK

Inport test for Control block I.

Test results				
Time step	1	2	...	201
CPU cycles	73	73	...	227
Inputs				
In (DSP)	0	0	...	0
I0 (DSP)	236223201	236223201	...	236223201
Enable (DSP)	0	0	...	1
In	0	0	...	0
I0	0.11	0.11	...	0.11
Enable	0	0	...	1
Parameters				
Ki	2500			
ts_fact	1			
Outputs				
Out	0	0	...	-1
Exp. Out	0	0	...	-1
Out (DSP)	0	0	...	-2147483647
Exp. Out (DSP)	0	0	...	-2147483647

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	73
Max CPU cycles	289
Avg CPU cycles	228

Test case: Conversion test OK

Conversion test for Control block I.

Test results				
Time step	1	2	...	37
Mask parameters				
Ki	-11	-10.389	...	11
ts_fact	1	2	...	37
Controller parameters				
b0	-2362232	-4461994	...	87402584
sfr	31	31	...	31
Exp. b0	-2362232	-4461994	...	87402584
Exp. sfr	31	31	...	31

Test settings	
Tolerance b0	±0,0000e+00
Tolerance sfr	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block I.

Test results				
Time step	1	2	...	37
Mask parameters				
Ki	-11	-10.389	...	11
ts_fact	1	2	...	37
Controller parameters				
b0	-2362232	-4461994	...	87402584
sfr	31	31	...	31
Exp. b0	-2362232	-4461994	...	87402584
Exp. sfr	31	31	...	31

Test settings	
Tolerance b0	±1,0000e+01
Tolerance sfr	±0,0000e+00

Test statistics	
Min CPU cycles	1692
Max CPU cycles	1805
Avg CPU cycles	1795

Verification: I FiP32 CPU dsPIC33EP256MC502

Date of Test	2026-06-23
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for Control block I.

Test results				
Time step	1	2	...	201
CPU cycles	53	53	...	238
Inputs				
In (DSP)	0	0	...	0
I0 (DSP)	236223201	236223201	...	236223201
Enable (DSP)	0	0	...	1
In	0	0	...	0
I0	0.11	0.11	...	0.11
Enable	0	0	...	1
Parameters				
Ki	2500			
ts_fact	1			
Outputs				
Out	0	0	...	-1
Exp. Out	0	0	...	-1
Out (DSP)	0	0	...	-2147483647
Exp. Out (DSP)	0	0	...	-2147483647

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	53
Max CPU cycles	261
Avg CPU cycles	237

Test case: Conversion test OK

Conversion test for Control block I.

Test results				
Time step	1	2	...	37
Mask parameters				
Ki	-11	-10.389	...	11
ts_fact	1	2	...	37
Controller parameters				
b0	-2362232	-4461994	...	87402584
sfr	31	31	...	31
Exp. b0	-2362232	-4461994	...	87402584
Exp. sfr	31	31	...	31

Test settings	
Tolerance b0	±0,0000e+00
Tolerance sfr	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block I.

Test results				
Time step	1	2	...	37
Mask parameters				
Ki	-11	-10.389	...	11
ts_fact	1	2	...	37
Controller parameters				
b0	-2362232	-4461994	...	87402584
sfr	31	31	...	31
Exp. b0	-2362232	-4461994	...	87402584
Exp. sfr	31	31	...	31

Test settings	
Tolerance b0	±1,0000e+01
Tolerance sfr	±0,0000e+00

Test statistics	
Min CPU cycles	4539
Max CPU cycles	5609
Avg CPU cycles	5551

Verification: I Float32 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for Control block I.

Test results				
Time step	1	2	...	201
CPU cycles	69	69	...	104
Inputs				
In (DSP)	0	0	...	0
I0 (DSP)	0.11	0.11	...	0.11
Enable (DSP)	0	0	...	1
In	0	0	...	0
I0	0.11	0.11	...	0.11
Enable	0	0	...	1
Parameters				
Ki	2500			
ts_fact	1			
Outputs				
Out	0	0	...	-1.84
Exp. Out	0	0	...	-1.84
Out (DSP)	0	0	...	-1.84
Exp. Out (DSP)	0	0	...	-1.84

Test settings	
Tolerance Out	±9,3132e-07 (±2000 LSB)

Test statistics	
Min CPU cycles	69
Max CPU cycles	109
Avg CPU cycles	103

Test case: Conversion test OK

Conversion test for Control block I.

Test results				
Time step	1	2	...	37
Mask parameters				
Ki	-11	-10.389	...	11
ts_fact	1	2	...	37
Controller parameters				
b0	-0.001	-0.002	...	0.041
Exp. b0	-0.001	-0.002	...	0.041

Test settings	
Tolerance b0	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block I.

Test results				
Time step	1	2	...	37
Mask parameters				
Ki	-11	-10.389	...	11
ts_fact	1	2	...	37
Controller parameters				
b0	-0.001	-0.002	...	0.041
Exp. b0	-0.001	-0.002	...	0.041

Test settings	
Tolerance b0	±1,0000e-08

Test statistics	
Min CPU cycles	1495
Max CPU cycles	1518
Avg CPU cycles	1500

Verification: I Float32 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for Control block I.

Test results				
Time step	1	2	...	201
CPU cycles	41	41	...	77
Inputs				
In (DSP)	0	0	...	0
I0 (DSP)	0.11	0.11	...	0.11
Enable (DSP)	0	0	...	1
In	0	0	...	0
I0	0.11	0.11	...	0.11
Enable	0	0	...	1
Parameters				
Ki	2500			
ts_fact	1			
Outputs				
Out	0	0	...	-1.84
Exp. Out	0	0	...	-1.84
Out (DSP)	0	0	...	-1.84
Exp. Out (DSP)	0	0	...	-1.84

Test settings	
Tolerance Out	±9,3132e-07 (±2000 LSB)

Test statistics	
Min CPU cycles	41
Max CPU cycles	77
Avg CPU cycles	76

Test case: Conversion test OK

Conversion test for Control block I.

Test results				
Time step	1	2	...	37
Mask parameters				
Ki	-11	-10.389	...	11
ts_fact	1	2	...	37
Controller parameters				
b0	-0.001	-0.002	...	0.041
Exp. b0	-0.001	-0.002	...	0.041

Test settings	
Tolerance b0	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block I.

Test results				
Time step	1	2	...	37
Mask parameters				
Ki	-11	-10.389	...	11
ts_fact	1	2	...	37
Controller parameters				
b0	-0.001	-0.002	...	0.041
Exp. b0	-0.001	-0.002	...	0.041

Test settings	
Tolerance b0	±1,0000e-08

Test statistics	
Min CPU cycles	741
Max CPU cycles	741
Avg CPU cycles	741

Verification: I Float32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for Control block I.

Test results				
Time step	1	2	...	201
CPU cycles	78	78	...	123
Inputs				
In (DSP)	0	0	...	0
I0 (DSP)	0.11	0.11	...	0.11
Enable (DSP)	0	0	...	1
In	0	0	...	0
I0	0.11	0.11	...	0.11
Enable	0	0	...	1
Parameters				
Ki	2500			
ts_fact	1			
Outputs				
Out	0	0	...	-1.84
Exp. Out	0	0	...	-1.84
Out (DSP)	0	0	...	-1.84
Exp. Out (DSP)	0	0	...	-1.84

Test settings	
Tolerance Out	±9,3132e-07 (±2000 LSB)

Test statistics	
Min CPU cycles	78
Max CPU cycles	130
Avg CPU cycles	122

Test case: Conversion test OK

Conversion test for Control block I.

Test results				
Time step	1	2	...	37
Mask parameters				
Ki	-11	-10.389	...	11
ts_fact	1	2	...	37
Controller parameters				
b0	-0.001	-0.002	...	0.041
Exp. b0	-0.001	-0.002	...	0.041

Test settings	
Tolerance b0	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block I.

Test results				
Time step	1	2	...	37
Mask parameters				
Ki	-11	-10.389	...	11
ts_fact	1	2	...	37
Controller parameters				
b0	-0.001	-0.002	...	0.041
Exp. b0	-0.001	-0.002	...	0.041

Test settings	
Tolerance b0	±1,0000e-08

Test statistics	
Min CPU cycles	771
Max CPU cycles	868
Avg CPU cycles	806

Verification: I Float32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for Control block I.

Test results				
Time step	1	2	...	201
CPU cycles	73	73	...	467
Inputs				
In (DSP)	0	0	...	0
I0 (DSP)	0.11	0.11	...	0.11
Enable (DSP)	0	0	...	1
In	0	0	...	0
I0	0.11	0.11	...	0.11
Enable	0	0	...	1
Parameters				
Ki	2500			
ts_fact	1			
Outputs				
Out	0	0	...	-1.84
Exp. Out	0	0	...	-1.84
Out (DSP)	0	0	...	-1.84
Exp. Out (DSP)	0	0	...	-1.84

Test settings	
Tolerance Out	±9,3132e-07 (±2000 LSB)

Test statistics	
Min CPU cycles	73
Max CPU cycles	643
Avg CPU cycles	542

Test case: Conversion test OK

Conversion test for Control block I.

Test results				
Time step	1	2	...	37
Mask parameters				
Ki	-11	-10.389	...	11
ts_fact	1	2	...	37
Controller parameters				
b0	-0.001	-0.002	...	0.041
Exp. b0	-0.001	-0.002	...	0.041

Test settings	
Tolerance b0	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block I.

Test results				
Time step	1	2	...	37
Mask parameters				
Ki	-11	-10.389	...	11
ts_fact	1	2	...	37
Controller parameters				
b0	-0.001	-0.002	...	0.041
Exp. b0	-0.001	-0.002	...	0.041

Test settings	
Tolerance b0	±1,0000e-08

Test statistics	
Min CPU cycles	1589
Max CPU cycles	1735
Avg CPU cycles	1670

Verification: I Float32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for Control block I.

Test results				
Time step	1	2	...	201
CPU cycles	57	57	...	214
Inputs				
In (DSP)	0	0	...	0
I0 (DSP)	0.11	0.11	...	0.11
Enable (DSP)	0	0	...	1
In	0	0	...	0
I0	0.11	0.11	...	0.11
Enable	0	0	...	1
Parameters				
Ki	2500			
ts_fact	1			
Outputs				
Out	0	0	...	-1.84
Exp. Out	0	0	...	-1.84
Out (DSP)	0	0	...	-1.84
Exp. Out (DSP)	0	0	...	-1.84

Test settings	
Tolerance Out	±9,3132e-07 (±2000 LSB)

Test statistics	
Min CPU cycles	57
Max CPU cycles	264
Avg CPU cycles	241

Test case: Conversion test OK

Conversion test for Control block I.

Test results				
Time step	1	2	...	37
Mask parameters				
Ki	-11	-10.389	...	11
ts_fact	1	2	...	37
Controller parameters				
b0	-0.001	-0.002	...	0.041
Exp. b0	-0.001	-0.002	...	0.041

Test settings	
Tolerance b0	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block I.

Test results				
Time step	1	2	...	37
Mask parameters				
Ki	-11	-10.389	...	11
ts_fact	1	2	...	37
Controller parameters				
b0	-0.001	-0.002	...	0.041
Exp. b0	-0.001	-0.002	...	0.041

Test settings	
Tolerance b0	±1,0000e-08

Test statistics	
Min CPU cycles	583
Max CPU cycles	602
Avg CPU cycles	597

Verification: I Float32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for Control block I.

Test results				
Time step	1	2	...	201
CPU cycles	79	60	...	93
Inputs				
In (DSP)	0	0	...	0
I0 (DSP)	0.11	0.11	...	0.11
Enable (DSP)	0	0	...	1
In	0	0	...	0
I0	0.11	0.11	...	0.11
Enable	0	0	...	1
Parameters				
Ki	2500			
ts_fact	1			
Outputs				
Out	0	0	...	-1.84
Exp. Out	0	0	...	-1.84
Out (DSP)	0	0	...	-1.84
Exp. Out (DSP)	0	0	...	-1.84

Test settings	
Tolerance Out	±9,3132e-07 (±2000 LSB)

Test statistics	
Min CPU cycles	60
Max CPU cycles	110
Avg CPU cycles	92

Test case: Conversion test OK

Conversion test for Control block I.

Test results				
Time step	1	2	...	37
Mask parameters				
Ki	-11	-10.389	...	11
ts_fact	1	2	...	37
Controller parameters				
b0	-0.001	-0.002	...	0.041
Exp. b0	-0.001	-0.002	...	0.041

Test settings	
Tolerance b0	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block I.

Test results				
Time step	1	2	...	37
Mask parameters				
Ki	-11	-10.389	...	11
ts_fact	1	2	...	37
Controller parameters				
b0	-0.001	-0.002	...	0.041
Exp. b0	-0.001	-0.002	...	0.041

Test settings	
Tolerance b0	±1,0000e-08

Test statistics	
Min CPU cycles	595
Max CPU cycles	683
Avg CPU cycles	614

Verification: I Float32 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test

OK

Inport test for Control block I.

Test results				
Time step	1	2	...	201
CPU cycles	65	65	...	105
Inputs				
In (DSP)	0	0	...	0
I0 (DSP)	0.11	0.11	...	0.11
Enable (DSP)	0	0	...	1
In	0	0	...	0
I0	0.11	0.11	...	0.11
Enable	0	0	...	1
Parameters				
Ki	2500			
ts_fact	1			
Outputs				
Out	0	0	...	-1.84
Exp. Out	0	0	...	-1.84
Out (DSP)	0	0	...	-1.84
Exp. Out (DSP)	0	0	...	-1.84

Test settings	
Tolerance Out	±9,3132e-07 (±2000 LSB)

Test statistics	
Min CPU cycles	65
Max CPU cycles	108
Avg CPU cycles	104

Test case: Conversion test

OK

Conversion test for Control block I.

Test results				
Time step	1	2	...	37
Mask parameters				
Ki	-11	-10.389	...	11
ts_fact	1	2	...	37
Controller parameters				
b0	-0.001	-0.002	...	0.041
Exp. b0	-0.001	-0.002	...	0.041

Test settings	
Tolerance b0	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block I.

Test results				
Time step	1	2	...	37
Mask parameters				
Ki	-11	-10.389	...	11
ts_fact	1	2	...	37
Controller parameters				
b0	-0.001	-0.002	...	0.041
Exp. b0	-0.001	-0.002	...	0.041

Test settings	
Tolerance b0	±1,0000e-08

Test statistics	
Min CPU cycles	1163
Max CPU cycles	1179
Avg CPU cycles	1165

Verification: I Float32 CPU dsPIC33EP256MC502

Date of Test	2026-06-23
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for Control block I.

Test results				
Time step	1	2	...	201
CPU cycles	59	59	...	500
Inputs				
In (DSP)	0	0	...	0
I0 (DSP)	0.11	0.11	...	0.11
Enable (DSP)	0	0	...	1
In	0	0	...	0
I0	0.11	0.11	...	0.11
Enable	0	0	...	1
Parameters				
Ki	2500			
ts_fact	1			
Outputs				
Out	0	0	...	-1.84
Exp. Out	0	0	...	-1.84
Out (DSP)	0	0	...	-1.84
Exp. Out (DSP)	0	0	...	-1.84

Test settings	
Tolerance Out	±9,3132e-07 (±2000 LSB)

Test statistics	
Min CPU cycles	59
Max CPU cycles	659
Avg CPU cycles	589

Test case: Conversion test OK

Conversion test for Control block I.

Test results				
Time step	1	2	...	37
Mask parameters				
Ki	-11	-10.389	...	11
ts_fact	1	2	...	37
Controller parameters				
b0	-0.001	-0.002	...	0.041
Exp. b0	-0.001	-0.002	...	0.041

Test settings	
Tolerance b0	±0,0000e+00

Test case: Conversion-on-Target test **OK**

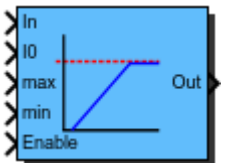
Conversion-on-Target test for Control block I.

Test results				
Time step	1	2	...	37
Mask parameters				
Ki	-11	-10.389	...	11
ts_fact	1	2	...	37
Controller parameters				
b0	-0.001	-0.002	...	0.041
Exp. b0	-0.001	-0.002	...	0.041

Test settings	
Tolerance b0	±1,0000e-08

Test statistics	
Min CPU cycles	2155
Max CPU cycles	2551
Avg CPU cycles	2531

Block: ILimit



I controller with output limitation:
G(s) = Ki/s = 1/(Ti*s)

Inports	
In	Control error input
I0	Integral value which is loaded at initialization function call
max	Maximum output value
min	Minimum output value
Enable	Enable == 0: Deactivation of block; Out set to 0 Enable 0->1: Preload of integral part Enable == 1: Activation of block

Outports	
Out	Control value

Mask Parameters		
Name	**ID**	**Description**
Ki	1	Integral Factor
ts_fact	2	Multiplication factor of base sampling time (in integer format)

Description:

Each fixed point implementation uses the next higher integer datatype for the integrational value storage variable.
A rising flank at the *Enable* inport will preload the integrational part with the value present on the *Init* inport.

Transfer function (zero-order hold discretization method):

$$G(z) = K_{\mathrm{i}} T_{\mathrm{s}} \frac{1}{z-1}$$

Developer note: The source code of this block is used for block *I*.

Implementations:

FiP16	16 Bit Fixed Point Implementation
FiP32	32 Bit Fixed Point Implementation
Float32	32 Bit Floating Point Implementation
Float64	64 Bit Floating Point Implementation

Implementation: FiP16

16 Bit Fixed Point Implementation

Inports Data Type	
In	int16
I0	int16
max	int16
min	int16
Enable	bool

Outports Data Type	
Out	int16

Implementation: FiP32

32 Bit Fixed Point Implementation

Inports Data Type	
In	int32
I0	int32
max	int32
min	int32
Enable	bool

Outports Data Type	
Out	int32

Implementation: Float32

32 Bit Floating Point Implementation

Inports Data Type	
In	float32
I0	float32
max	float32
min	float32
Enable	bool

Outports Data Type	
Out	float32

Implementation: Float64

64 Bit Floating Point Implementation

Inports Data Type	
In	float64
I0	float64
max	float64
min	float64
Enable	bool

Outports Data Type	
Out	float64

Verification: ILimit FiP16 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for Control block ILimit.

Test results						
Time step	1	2	3	4	...	201
CPU cycles	69	69	69	134	...	120
Inputs						
In (DSP)	0	0	0	0	...	0
I0 (DSP)	3604	3604	3604	3604	...	3604
max (DSP)	26214	26214	26214	26214	...	26214
min (DSP)	4915	4915	4915	4915	...	4915
Enable (DSP)	0	0	0	1	...	1
In	0	0	0	0	...	0
I0	0.11	0.11	0.11	0.11	...	0.11
max	0.8	0.8	0.8	0.8	...	0.8
min	0.15	0.15	0.15	0.15	...	0.15
Enable	0	0	0	1	...	1
Parameters						
Ki	2500					
ts_fact	1					
Outputs						
Out	0	0	0	0.15	...	0.15
Exp. Out	0	0	0	0.15	...	0.15
Out (DSP)	0	0	0	4915	...	4915
Exp. Out (DSP)	0	0	0	4915	...	4915

Test settings	
Tolerance Out	±3,0518e-04 (±10 LSB)

Test statistics	
Min CPU cycles	69
Max CPU cycles	134
Avg CPU cycles	119

Test case: Conversion test OK

Conversion test for Control block ILimit.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Ki	-11	-10.389	-9.778	-9.167	...	11
ts_fact	1	2	3	4	...	37
Controller parameters						
b0	-36	-68	-96	-120	...	1334
sfr	15	15	15	15	...	15
Exp. b0	-36	-68	-96	-120	...	1334
Exp. sfr	15	15	15	15	...	15

Test settings	
Tolerance b0	±0,0000e+00
Tolerance sfr	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block ILimit.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Ki	-11	-10.389	-9.778	-9.167	...	11
ts_fact	1	2	3	4	...	37
Controller parameters						
b0	-36	-68	-96	-120	...	1333
sfr	15	15	15	15	...	15
Exp. b0	-36	-68	-96	-120	...	1334
Exp. sfr	15	15	15	15	...	15

Test settings	
Tolerance b0	±1,0000e+00
Tolerance sfr	±0,0000e+00

Test statistics	
Min CPU cycles	2076
Max CPU cycles	2170
Avg CPU cycles	2160

Verification: ILimit FiP16 CPU TM4C123GH6

Date of Test 2026-06-19

Target controller TM4C123GH6

Test case: Inport test OK

Inport test for Control block ILimit.

Test results						
Time step	1	2	3	4	...	201
CPU cycles	47	47	47	93	...	77
Inputs						
In (DSP)	0	0	0	0	...	0
I0 (DSP)	3604	3604	3604	3604	...	3604
max (DSP)	26214	26214	26214	26214	...	26214
min (DSP)	4915	4915	4915	4915	...	4915
Enable (DSP)	0	0	0	1	...	1
In	0	0	0	0	...	0
I0	0.11	0.11	0.11	0.11	...	0.11
max	0.8	0.8	0.8	0.8	...	0.8
min	0.15	0.15	0.15	0.15	...	0.15
Enable	0	0	0	1	...	1
Parameters						
Ki	2500					
ts_fact	1					
Outputs						
Out	0	0	0	0.15	...	0.15
Exp. Out	0	0	0	0.15	...	0.15
Out (DSP)	0	0	0	4915	...	4915
Exp. Out (DSP)	0	0	0	4915	...	4915

Test settings	
Tolerance Out	±3,0518e-04 (±10 LSB)

Test statistics	
Min CPU cycles	47
Max CPU cycles	93
Avg CPU cycles	77

Test case: Conversion test OK

Conversion test for Control block ILimit.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Ki	-11	-10.389	-9.778	-9.167	...	11
ts_fact	1	2	3	4	...	37
Controller parameters						
b0	-36	-68	-96	-120	...	1334
sfr	15	15	15	15	...	15
Exp. b0	-36	-68	-96	-120	...	1334
Exp. sfr	15	15	15	15	...	15

Test settings	
Tolerance b0	±0,0000e+00
Tolerance sfr	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block ILimit.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Ki	-11	-10.389	-9.778	-9.167	...	11
ts_fact	1	2	3	4	...	37
Controller parameters						
b0	-36	-68	-96	-120	...	1333
sfr	15	15	15	15	...	15
Exp. b0	-36	-68	-96	-120	...	1334
Exp. sfr	15	15	15	15	...	15

Test settings	
Tolerance b0	±1,0000e+00
Tolerance sfr	±0,0000e+00

Test statistics	
Min CPU cycles	1071
Max CPU cycles	1141
Avg CPU cycles	1139

Verification: ILimit FiP16 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test

OK

Inport test for Control block ILimit.

Test results						
Time step	1	2	3	4	...	201
CPU cycles	71	71	71	137	...	121
Inputs						
In (DSP)	0	0	0	0	...	0
I0 (DSP)	3604	3604	3604	3604	...	3604
max (DSP)	26214	26214	26214	26214	...	26214
min (DSP)	4915	4915	4915	4915	...	4915
Enable (DSP)	0	0	0	1	...	1
In	0	0	0	0	...	0
I0	0.11	0.11	0.11	0.11	...	0.11
max	0.8	0.8	0.8	0.8	...	0.8
min	0.15	0.15	0.15	0.15	...	0.15
Enable	0	0	0	1	...	1
Parameters						
Ki	2500					
ts_fact	1					
Outputs						
Out	0	0	0	0.15	...	0.15
Exp. Out	0	0	0	0.15	...	0.15
Out (DSP)	0	0	0	4915	...	4915
Exp. Out (DSP)	0	0	0	4915	...	4915

Test settings	
Tolerance Out	±3,0518e-04 (±10 LSB)

Test statistics	
Min CPU cycles	71
Max CPU cycles	137
Avg CPU cycles	119

Test case: Conversion test

OK

Conversion test for Control block ILimit.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Ki	-11	-10.389	-9.778	-9.167	...	11
ts_fact	1	2	3	4	...	37
Controller parameters						
b0	-36	-68	-96	-120	...	1334
sfr	15	15	15	15	...	15
Exp. b0	-36	-68	-96	-120	...	1334
Exp. sfr	15	15	15	15	...	15

Test settings	
Tolerance b0	±0,0000e+00
Tolerance sfr	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block ILimit.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Ki	-11	-10.389	-9.778	-9.167	...	11
ts_fact	1	2	3	4	...	37
Controller parameters						
b0	-36	-68	-96	-120	...	1333
sfr	15	15	15	15	...	15
Exp. b0	-36	-68	-96	-120	...	1334
Exp. sfr	15	15	15	15	...	15

Test settings	
Tolerance b0	±1,0000e+00
Tolerance sfr	±0,0000e+00

Test statistics	
Min CPU cycles	1180
Max CPU cycles	1235
Avg CPU cycles	1217

Verification: ILimit FiP16 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test

OK

Inport test for Control block ILimit.

Test results						
Time step	1	2	3	4	...	201
CPU cycles	66	66	66	125	...	113
Inputs						
In (DSP)	0	0	0	0	...	0
I0 (DSP)	3604	3604	3604	3604	...	3604
max (DSP)	26214	26214	26214	26214	...	26214
min (DSP)	4915	4915	4915	4915	...	4915
Enable (DSP)	0	0	0	1	...	1
In	0	0	0	0	...	0
I0	0.11	0.11	0.11	0.11	...	0.11
max	0.8	0.8	0.8	0.8	...	0.8
min	0.15	0.15	0.15	0.15	...	0.15
Enable	0	0	0	1	...	1
Parameters						
Ki	2500					
ts_fact	1					
Outputs						
Out	0	0	0	0.15	...	0.15
Exp. Out	0	0	0	0.15	...	0.15
Out (DSP)	0	0	0	4915	...	4915
Exp. Out (DSP)	0	0	0	4915	...	4915

Test settings	
Tolerance Out	±3,0518e-04 (±10 LSB)

Test statistics	
Min CPU cycles	66
Max CPU cycles	125
Avg CPU cycles	110

Test case: Conversion test

OK

Conversion test for Control block ILimit.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Ki	-11	-10.389	-9.778	-9.167	...	11
ts_fact	1	2	3	4	...	37
Controller parameters						
b0	-36	-68	-96	-120	...	1334
sfr	15	15	15	15	...	15
Exp. b0	-36	-68	-96	-120	...	1334
Exp. sfr	15	15	15	15	...	15

Test settings	
Tolerance b0	±0,0000e+00
Tolerance sfr	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block ILimit.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Ki	-11	-10.389	-9.778	-9.167	...	11
ts_fact	1	2	3	4	...	37
Controller parameters						
b0	-36	-68	-96	-120	...	1333
sfr	15	15	15	15	...	15
Exp. b0	-36	-68	-96	-120	...	1334
Exp. sfr	15	15	15	15	...	15

Test settings	
Tolerance b0	±1,0000e+00
Tolerance sfr	±0,0000e+00

Test statistics	
Min CPU cycles	2537
Max CPU cycles	3016
Avg CPU cycles	2946

Verification: ILimit FiP16 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test

OK

Inport test for Control block ILimit.

Test results						
Time step	1	2	3	4	...	201
CPU cycles	31	31	31	81	...	70
Inputs						
In (DSP)	0	0	0	0	...	0
I0 (DSP)	3604	3604	3604	3604	...	3604
max (DSP)	26214	26214	26214	26214	...	26214
min (DSP)	4915	4915	4915	4915	...	4915
Enable (DSP)	0	0	0	1	...	1
In	0	0	0	0	...	0
I0	0.11	0.11	0.11	0.11	...	0.11
max	0.8	0.8	0.8	0.8	...	0.8
min	0.15	0.15	0.15	0.15	...	0.15
Enable	0	0	0	1	...	1
Parameters						
Ki	2500					
ts_fact	1					
Outputs						
Out	0	0	0	0.15	...	0.15
Exp. Out	0	0	0	0.15	...	0.15
Out (DSP)	0	0	0	4915	...	4915
Exp. Out (DSP)	0	0	0	4915	...	4915

Test settings	
Tolerance Out	±3,0518e-04 (±10 LSB)

Test statistics	
Min CPU cycles	31
Max CPU cycles	81
Avg CPU cycles	69

Test case: Conversion test

OK

Conversion test for Control block ILimit.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Ki	-11	-10.389	-9.778	-9.167	...	11
ts_fact	1	2	3	4	...	37
Controller parameters						
b0	-36	-68	-96	-120	...	1334
sfr	15	15	15	15	...	15
Exp. b0	-36	-68	-96	-120	...	1334
Exp. sfr	15	15	15	15	...	15

Test settings	
Tolerance b0	±0,0000e+00
Tolerance sfr	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block ILimit.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Ki	-11	-10.389	-9.778	-9.167	...	11
ts_fact	1	2	3	4	...	37
Controller parameters						
b0	-36	-68	-96	-120	...	1333
sfr	15	15	15	15	...	15
Exp. b0	-36	-68	-96	-120	...	1334
Exp. sfr	15	15	15	15	...	15

Test settings	
Tolerance b0	±1,0000e+00
Tolerance sfr	±0,0000e+00

Test statistics	
Min CPU cycles	1072
Max CPU cycles	1188
Avg CPU cycles	1179

Verification: ILimit FiP16 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test

OK

Inport test for Control block ILimit.

Test results						
Time step	1	2	3	4	...	201
CPU cycles	74	59	59	119	...	102
Inputs						
In (DSP)	0	0	0	0	...	0
I0 (DSP)	3604	3604	3604	3604	...	3604
max (DSP)	26214	26214	26214	26214	...	26214
min (DSP)	4915	4915	4915	4915	...	4915
Enable (DSP)	0	0	0	1	...	1
In	0	0	0	0	...	0
I0	0.11	0.11	0.11	0.11	...	0.11
max	0.8	0.8	0.8	0.8	...	0.8
min	0.15	0.15	0.15	0.15	...	0.15
Enable	0	0	0	1	...	1
Parameters						
Ki	2500					
ts_fact	1					
Outputs						
Out	0	0	0	0.15	...	0.15
Exp. Out	0	0	0	0.15	...	0.15
Out (DSP)	0	0	0	4915	...	4915
Exp. Out (DSP)	0	0	0	4915	...	4915

Test settings	
Tolerance Out	±3,0518e-04 (±10 LSB)

Test statistics	
Min CPU cycles	59
Max CPU cycles	119
Avg CPU cycles	100

Test case: Conversion test

OK

Conversion test for Control block ILimit.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Ki	-11	-10.389	-9.778	-9.167	...	11
ts_fact	1	2	3	4	...	37
Controller parameters						
b0	-36	-68	-96	-120	...	1334
sfr	15	15	15	15	...	15
Exp. b0	-36	-68	-96	-120	...	1334
Exp. sfr	15	15	15	15	...	15

Test settings	
Tolerance b0	±0,0000e+00
Tolerance sfr	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block ILimit.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Ki	-11	-10.389	-9.778	-9.167	...	11
ts_fact	1	2	3	4	...	37
Controller parameters						
b0	-36	-68	-96	-120	...	1333
sfr	15	15	15	15	...	15
Exp. b0	-36	-68	-96	-120	...	1334
Exp. sfr	15	15	15	15	...	15

Test settings	
Tolerance b0	±1,0000e+00
Tolerance sfr	±0,0000e+00

Test statistics	
Min CPU cycles	833
Max CPU cycles	941
Avg CPU cycles	854

Verification: ILimit FiP16 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for Control block ILimit.

Test results						
Time step	1	2	3	4	...	201
CPU cycles	65	65	65	137	...	125
Inputs						
In (DSP)	0	0	0	0	...	0
I0 (DSP)	3604	3604	3604	3604	...	3604
max (DSP)	26214	26214	26214	26214	...	26214
min (DSP)	4915	4915	4915	4915	...	4915
Enable (DSP)	0	0	0	1	...	1
In	0	0	0	0	...	0
I0	0.11	0.11	0.11	0.11	...	0.11
max	0.8	0.8	0.8	0.8	...	0.8
min	0.15	0.15	0.15	0.15	...	0.15
Enable	0	0	0	1	...	1
Parameters						
Ki	2500					
ts_fact	1					
Outputs						
Out	0	0	0	0.15	...	0.15
Exp. Out	0	0	0	0.15	...	0.15
Out (DSP)	0	0	0	4915	...	4915
Exp. Out (DSP)	0	0	0	4915	...	4915

Test settings	
Tolerance Out	±3,0518e-04 (±10 LSB)

Test statistics	
Min CPU cycles	65
Max CPU cycles	137
Avg CPU cycles	124

Test case: Conversion test OK

Conversion test for Control block ILimit.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Ki	-11	-10.389	-9.778	-9.167	...	11
ts_fact	1	2	3	4	...	37
Controller parameters						
b0	-36	-68	-96	-120	...	1334
sfr	15	15	15	15	...	15
Exp. b0	-36	-68	-96	-120	...	1334
Exp. sfr	15	15	15	15	...	15

Test settings	
Tolerance b0	±0,0000e+00
Tolerance sfr	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block ILimit.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Ki	-11	-10.389	-9.778	-9.167	...	11
ts_fact	1	2	3	4	...	37
Controller parameters						
b0	-36	-68	-96	-120	...	1333
sfr	15	15	15	15	...	15
Exp. b0	-36	-68	-96	-120	...	1334
Exp. sfr	15	15	15	15	...	15

Test settings	
Tolerance b0	±1,0000e+00
Tolerance sfr	±0,0000e+00

Test statistics	
Min CPU cycles	1579
Max CPU cycles	1649
Avg CPU cycles	1644

Verification: ILimit FiP16 CPU dsPIC33EP256MC502

Date of Test	2026-06-23
Target controller	dsPIC33EP256MC502

Test case: Inport test

OK

Inport test for Control block ILimit.

Test results						
Time step	1	2	3	4	...	201
CPU cycles	52	52	52	115	...	103
Inputs						
In (DSP)	0	0	0	0	...	0
I0 (DSP)	3604	3604	3604	3604	...	3604
max (DSP)	26214	26214	26214	26214	...	26214
min (DSP)	4915	4915	4915	4915	...	4915
Enable (DSP)	0	0	0	1	...	1
In	0	0	0	0	...	0
I0	0.11	0.11	0.11	0.11	...	0.11
max	0.8	0.8	0.8	0.8	...	0.8
min	0.15	0.15	0.15	0.15	...	0.15
Enable	0	0	0	1	...	1
Parameters						
Ki	2500					
ts_fact	1					
Outputs						
Out	0	0	0	0.15	...	0.15
Exp. Out	0	0	0	0.15	...	0.15
Out (DSP)	0	0	0	4915	...	4915
Exp. Out (DSP)	0	0	0	4915	...	4915

Test settings	
Tolerance Out	±3,0518e-04 (±10 LSB)

Test statistics	
Min CPU cycles	52
Max CPU cycles	115
Avg CPU cycles	102

Test case: Conversion test

OK

Conversion test for Control block ILimit.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Ki	-11	-10.389	-9.778	-9.167	...	11
ts_fact	1	2	3	4	...	37
Controller parameters						
b0	-36	-68	-96	-120	...	1334
sfr	15	15	15	15	...	15
Exp. b0	-36	-68	-96	-120	...	1334
Exp. sfr	15	15	15	15	...	15

Test settings	
Tolerance b0	±0,0000e+00
Tolerance sfr	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block ILimit.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Ki	-11	-10.389	-9.778	-9.167	...	11
ts_fact	1	2	3	4	...	37
Controller parameters						
b0	-36	-68	-96	-120	...	1333
sfr	15	15	15	15	...	15
Exp. b0	-36	-68	-96	-120	...	1334
Exp. sfr	15	15	15	15	...	15

Test settings	
Tolerance b0	±1,0000e+00
Tolerance sfr	±0,0000e+00

Test statistics	
Min CPU cycles	4133
Max CPU cycles	5289
Avg CPU cycles	5242

Verification: ILimit FiP32 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for Control block ILimit.

Test results				
Time step	1	2	...	201
CPU cycles	85	85	...	245
Inputs				
In (DSP)	0	0	...	0
I0 (DSP)	236223201	236223201	...	236223201
max (DSP)	1717986918	1717986918	...	1717986918
min (DSP)	322122547	322122547	...	322122547
Enable (DSP)	0	0	...	1
In	0	0	...	0
I0	0.11	0.11	...	0.11
max	0.8	0.8	...	0.8
min	0.15	0.15	...	0.15
Enable	0	0	...	1
Parameters				
Ki	2500			
ts_fact	1			
Outputs				
Out	0	0	...	0.15
Exp. Out	0	0	...	0.15
Out (DSP)	0	0	...	322122547
Exp. Out (DSP)	0	0	...	322122547

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	85
Max CPU cycles	333
Avg CPU cycles	254

Test case: Conversion test OK

Conversion test for Control block ILimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Ki	-11	-10.389	...	11
ts_fact	1	2	...	37
Controller parameters				
b0	-2362232	-4461994	...	87402584
sfr	31	31	...	31
Exp. b0	-2362232	-4461994	...	87402584
Exp. sfr	31	31	...	31

Test settings	
Tolerance b0	±0,0000e+00
Tolerance sfr	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block ILimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Ki	-11	-10.389	...	11
ts_fact	1	2	...	37
Controller parameters				
b0	-2362232	-4461994	...	87402584
sfr	31	31	...	31
Exp. b0	-2362232	-4461994	...	87402584
Exp. sfr	31	31	...	31

Test settings	
Tolerance b0	±1,0000e+01
Tolerance sfr	±0,0000e+00

Test statistics	
Min CPU cycles	2274
Max CPU cycles	2416
Avg CPU cycles	2401

Verification: ILimit FiP32 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for Control block ILimit.

Test results				
Time step	1	2	...	201
CPU cycles	55	55	...	129
Inputs				
In (DSP)	0	0	...	0
I0 (DSP)	236223201	236223201	...	236223201
max (DSP)	1717986918	1717986918	...	1717986918
min (DSP)	322122547	322122547	...	322122547
Enable (DSP)	0	0	...	1
In	0	0	...	0
I0	0.11	0.11	...	0.11
max	0.8	0.8	...	0.8
min	0.15	0.15	...	0.15
Enable	0	0	...	1
Parameters				
Ki	2500			
ts_fact	1			
Outputs				
Out	0	0	...	0.15
Exp. Out	0	0	...	0.15
Out (DSP)	0	0	...	322122547
Exp. Out (DSP)	0	0	...	322122547

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	55
Max CPU cycles	153
Avg CPU cycles	130

Test case: Conversion test OK

Conversion test for Control block ILimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Ki	-11	-10.389	...	11
ts_fact	1	2	...	37
Controller parameters				
b0	-2362232	-4461994	...	87402584
sfr	31	31	...	31
Exp. b0	-2362232	-4461994	...	87402584
Exp. sfr	31	31	...	31

Test settings	
Tolerance b0	±0,0000e+00
Tolerance sfr	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block ILimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Ki	-11	-10.389	...	11
ts_fact	1	2	...	37
Controller parameters				
b0	-2362232	-4461994	...	87402584
sfr	31	31	...	31
Exp. b0	-2362232	-4461994	...	87402584
Exp. sfr	31	31	...	31

Test settings	
Tolerance b0	±1,0000e+01
Tolerance sfr	±0,0000e+00

Test statistics	
Min CPU cycles	1027
Max CPU cycles	1125
Avg CPU cycles	1121

Verification: ILimit FiP32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for Control block ILimit.

Test results				
Time step	1	2	...	201
CPU cycles	82	82	...	154
Inputs				
In (DSP)	0	0	...	0
I0 (DSP)	236223201	236223201	...	236223201
max (DSP)	1717986918	1717986918	...	1717986918
min (DSP)	322122547	322122547	...	322122547
Enable (DSP)	0	0	...	1
In	0	0	...	0
I0	0.11	0.11	...	0.11
max	0.8	0.8	...	0.8
min	0.15	0.15	...	0.15
Enable	0	0	...	1
Parameters				
Ki	2500			
ts_fact	1			
Outputs				
Out	0	0	...	0.15
Exp. Out	0	0	...	0.15
Out (DSP)	0	0	...	322122547
Exp. Out (DSP)	0	0	...	322122547

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	82
Max CPU cycles	182
Avg CPU cycles	152

Test case: Conversion test OK

Conversion test for Control block ILimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Ki	-11	-10.389	...	11
ts_fact	1	2	...	37
Controller parameters				
b0	-2362232	-4461994	...	87402584
sfr	31	31	...	31
Exp. b0	-2362232	-4461994	...	87402584
Exp. sfr	31	31	...	31

Test settings	
Tolerance b0	±0,0000e+00
Tolerance sfr	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block ILimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Ki	-11	-10.389	...	11
ts_fact	1	2	...	37
Controller parameters				
b0	-2362232	-4461994	...	87402584
sfr	31	31	...	31
Exp. b0	-2362232	-4461994	...	87402584
Exp. sfr	31	31	...	31

Test settings	
Tolerance b0	±1,0000e+01
Tolerance sfr	±0,0000e+00

Test statistics	
Min CPU cycles	1555
Max CPU cycles	1614
Avg CPU cycles	1599

Verification: ILimit FiP32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for Control block ILimit.

Test results				
Time step	1	2	...	201
CPU cycles	88	88	...	253
Inputs				
In (DSP)	0	0	...	0
I0 (DSP)	236223201	236223201	...	236223201
max (DSP)	1717986918	1717986918	...	1717986918
min (DSP)	322122547	322122547	...	322122547
Enable (DSP)	0	0	...	1
In	0	0	...	0
I0	0.11	0.11	...	0.11
max	0.8	0.8	...	0.8
min	0.15	0.15	...	0.15
Enable	0	0	...	1
Parameters				
Ki	2500			
ts_fact	1			
Outputs				
Out	0	0	...	0.15
Exp. Out	0	0	...	0.15
Out (DSP)	0	0	...	322122547
Exp. Out (DSP)	0	0	...	322122547

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	88
Max CPU cycles	313
Avg CPU cycles	251

Test case: Conversion test OK

Conversion test for Control block ILimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Ki	-11	-10.389	...	11
ts_fact	1	2	...	37
Controller parameters				
b0	-2362232	-4461994	...	87402584
sfr	31	31	...	31
Exp. b0	-2362232	-4461994	...	87402584
Exp. sfr	31	31	...	31

Test settings	
Tolerance b0	±0,0000e+00
Tolerance sfr	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block ILimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Ki	-11	-10.389	...	11
ts_fact	1	2	...	37
Controller parameters				
b0	-2362232	-4461994	...	87402584
sfr	31	31	...	31
Exp. b0	-2362232	-4461994	...	87402584
Exp. sfr	31	31	...	31

Test settings	
Tolerance b0	±1,0000e+01
Tolerance sfr	±0,0000e+00

Test statistics	
Min CPU cycles	3571
Max CPU cycles	4311
Avg CPU cycles	4227

Verification: ILimit FiP32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for Control block ILimit.

Test results				
Time step	1	2	...	201
CPU cycles	31	31	...	104
Inputs				
In (DSP)	0	0	...	0
I0 (DSP)	236223201	236223201	...	236223201
max (DSP)	1717986918	1717986918	...	1717986918
min (DSP)	322122547	322122547	...	322122547
Enable (DSP)	0	0	...	1
In	0	0	...	0
I0	0.11	0.11	...	0.11
max	0.8	0.8	...	0.8
min	0.15	0.15	...	0.15
Enable	0	0	...	1
Parameters				
Ki	2500			
ts_fact	1			
Outputs				
Out	0	0	...	0.15
Exp. Out	0	0	...	0.15
Out (DSP)	0	0	...	322122547
Exp. Out (DSP)	0	0	...	322122547

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	31
Max CPU cycles	114
Avg CPU cycles	102

Test case: Conversion test OK

Conversion test for Control block ILimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Ki	-11	-10.389	...	11
ts_fact	1	2	...	37
Controller parameters				
b0	-2362232	-4461994	...	87402584
sfr	31	31	...	31
Exp. b0	-2362232	-4461994	...	87402584
Exp. sfr	31	31	...	31

Test settings	
Tolerance b0	±0,0000e+00
Tolerance sfr	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block ILimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Ki	-11	-10.389	...	11
ts_fact	1	2	...	37
Controller parameters				
b0	-2362232	-4461994	...	87402584
sfr	31	31	...	31
Exp. b0	-2362232	-4461994	...	87402584
Exp. sfr	31	31	...	31

Test settings	
Tolerance b0	±1,0000e+01
Tolerance sfr	±0,0000e+00

Test statistics	
Min CPU cycles	1528
Max CPU cycles	1722
Avg CPU cycles	1707

Verification: ILimit FiP32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for Control block ILimit.

Test results				
Time step	1	2	...	201
CPU cycles	99	79	...	137
Inputs				
In (DSP)	0	0	...	0
I0 (DSP)	236223201	236223201	...	236223201
max (DSP)	1717986918	1717986918	...	1717986918
min (DSP)	322122547	322122547	...	322122547
Enable (DSP)	0	0	...	1
In	0	0	...	0
I0	0.11	0.11	...	0.11
max	0.8	0.8	...	0.8
min	0.15	0.15	...	0.15
Enable	0	0	...	1
Parameters				
Ki	2500			
ts_fact	1			
Outputs				
Out	0	0	...	0.15
Exp. Out	0	0	...	0.15
Out (DSP)	0	0	...	322122547
Exp. Out (DSP)	0	0	...	322122547

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	79
Max CPU cycles	172
Avg CPU cycles	136

Test case: Conversion test OK

Conversion test for Control block ILimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Ki	-11	-10.389	...	11
ts_fact	1	2	...	37
Controller parameters				
b0	-2362232	-4461994	...	87402584
sfr	31	31	...	31
Exp. b0	-2362232	-4461994	...	87402584
Exp. sfr	31	31	...	31

Test settings	
Tolerance b0	±0,0000e+00
Tolerance sfr	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block ILimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Ki	-11	-10.389	...	11
ts_fact	1	2	...	37
Controller parameters				
b0	-2362232	-4461994	...	87402584
sfr	31	31	...	31
Exp. b0	-2362232	-4461994	...	87402584
Exp. sfr	31	31	...	31

Test settings	
Tolerance b0	±1,0000e+01
Tolerance sfr	±0,0000e+00

Test statistics	
Min CPU cycles	1092
Max CPU cycles	1271
Avg CPU cycles	1121

Verification: ILimit FiP32 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for Control block ILimit.

Test results				
Time step	1	2	...	201
CPU cycles	70	70	...	226
Inputs				
In (DSP)	0	0	...	0
I0 (DSP)	236223201	236223201	...	236223201
max (DSP)	1717986918	1717986918	...	1717986918
min (DSP)	322122547	322122547	...	322122547
Enable (DSP)	0	0	...	1
In	0	0	...	0
I0	0.11	0.11	...	0.11
max	0.8	0.8	...	0.8
min	0.15	0.15	...	0.15
Enable	0	0	...	1
Parameters				
Ki	2500			
ts_fact	1			
Outputs				
Out	0	0	...	0.15
Exp. Out	0	0	...	0.15
Out (DSP)	0	0	...	322122547
Exp. Out (DSP)	0	0	...	322122547

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	70
Max CPU cycles	295
Avg CPU cycles	232

Test case: Conversion test OK

Conversion test for Control block ILimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Ki	-11	-10.389	...	11
ts_fact	1	2	...	37
Controller parameters				
b0	-2362232	-4461994	...	87402584
sfr	31	31	...	31
Exp. b0	-2362232	-4461994	...	87402584
Exp. sfr	31	31	...	31

Test settings	
Tolerance b0	±0,0000e+00
Tolerance sfr	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block ILimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Ki	-11	-10.389	...	11
ts_fact	1	2	...	37
Controller parameters				
b0	-2362232	-4461994	...	87402584
sfr	31	31	...	31
Exp. b0	-2362232	-4461994	...	87402584
Exp. sfr	31	31	...	31

Test settings	
Tolerance b0	±1,0000e+01
Tolerance sfr	±0,0000e+00

Test statistics	
Min CPU cycles	1688
Max CPU cycles	1801
Avg CPU cycles	1791

Verification: ILimit FiP32 CPU dsPIC33EP256MC502

Date of Test	2026-06-23
Target controller	dsPIC33EP256MC502

Test case: Inport test

OK

Inport test for Control block ILimit.

Test results				
Time step	1	2	...	201
CPU cycles	55	55	...	267
Inputs				
In (DSP)	0	0	...	0
I0 (DSP)	236223201	236223201	...	236223201
max (DSP)	1717986918	1717986918	...	1717986918
min (DSP)	322122547	322122547	...	322122547
Enable (DSP)	0	0	...	1
In	0	0	...	0
I0	0.11	0.11	...	0.11
max	0.8	0.8	...	0.8
min	0.15	0.15	...	0.15
Enable	0	0	...	1
Parameters				
Ki	2500			
ts_fact	1			
Outputs				
Out	0	0	...	0.15
Exp. Out	0	0	...	0.15
Out (DSP)	0	0	...	322122547
Exp. Out (DSP)	0	0	...	322122547

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	55
Max CPU cycles	293
Avg CPU cycles	266

Test case: Conversion test

OK

Conversion test for Control block ILimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Ki	-11	-10.389	...	11
ts_fact	1	2	...	37
Controller parameters				
b0	-2362232	-4461994	...	87402584
sfr	31	31	...	31
Exp. b0	-2362232	-4461994	...	87402584
Exp. sfr	31	31	...	31

Test settings	
Tolerance b0	±0,0000e+00
Tolerance sfr	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block ILimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Ki	-11	-10.389	...	11
ts_fact	1	2	...	37
Controller parameters				
b0	-2362232	-4461994	...	87402584
sfr	31	31	...	31
Exp. b0	-2362232	-4461994	...	87402584
Exp. sfr	31	31	...	31

Test settings	
Tolerance b0	±1,0000e+01
Tolerance sfr	±0,0000e+00

Test statistics	
Min CPU cycles	4539
Max CPU cycles	5609
Avg CPU cycles	5551

Verification: ILimit Float32 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for Control block ILimit.

Test results				
Time step	1	2	...	201
CPU cycles	73	73	...	113
Inputs				
In (DSP)	0	0	...	0
I0 (DSP)	0.11	0.11	...	0.11
max (DSP)	0.8	0.8	...	0.8
min (DSP)	0.15	0.15	...	0.15
Enable (DSP)	0	0	...	1
In	0	0	...	0
I0	0.11	0.11	...	0.11
max	0.8	0.8	...	0.8
min	0.15	0.15	...	0.15
Enable	0	0	...	1
Parameters				
Ki	2500			
ts_fact	1			
Outputs				
Out	0	0	...	0.15
Exp. Out	0	0	...	0.15
Out (DSP)	0	0	...	0.15
Exp. Out (DSP)	0	0	...	0.15

Test settings	
Tolerance Out	±9,3132e-07 (±2000 LSB)

Test statistics	
Min CPU cycles	73
Max CPU cycles	127
Avg CPU cycles	113

Test case: Conversion test OK

Conversion test for Control block ILimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Ki	-11	-10.389	...	11
ts_fact	1	2	...	37
Controller parameters				
b0	-0.001	-0.002	...	0.041
Exp. b0	-0.001	-0.002	...	0.041

Test settings	
Tolerance b0	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block ILimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Ki	-11	-10.389	...	11
ts_fact	1	2	...	37
Controller parameters				
b0	-0.001	-0.002	...	0.041
Exp. b0	-0.001	-0.002	...	0.041

Test settings	
Tolerance b0	±1,0000e-08

Test statistics	
Min CPU cycles	1495
Max CPU cycles	1518
Avg CPU cycles	1500

Verification: ILimit Float32 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test — OK

Inport test for Control block ILimit.

Test results				
Time step	1	2	...	201
CPU cycles	41	41	...	79
Inputs				
In (DSP)	0	0	...	0
I0 (DSP)	0.11	0.11	...	0.11
max (DSP)	0.8	0.8	...	0.8
min (DSP)	0.15	0.15	...	0.15
Enable (DSP)	0	0	...	1
In	0	0	...	0
I0	0.11	0.11	...	0.11
max	0.8	0.8	...	0.8
min	0.15	0.15	...	0.15
Enable	0	0	...	1
Parameters				
Ki	2500			
ts_fact	1			
Outputs				
Out	0	0	...	0.15
Exp. Out	0	0	...	0.15
Out (DSP)	0	0	...	0.15
Exp. Out (DSP)	0	0	...	0.15

Test settings	
Tolerance Out	±9,3132e-07 (±2000 LSB)

Test statistics	
Min CPU cycles	41
Max CPU cycles	95
Avg CPU cycles	79

Test case: Conversion test — OK

Conversion test for Control block ILimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Ki	-11	-10.389	...	11
ts_fact	1	2	...	37
Controller parameters				
b0	-0.001	-0.002	...	0.041
Exp. b0	-0.001	-0.002	...	0.041

Test settings	
Tolerance b0	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block ILimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Ki	-11	-10.389	...	11
ts_fact	1	2	...	37
Controller parameters				
b0	-0.001	-0.002	...	0.041
Exp. b0	-0.001	-0.002	...	0.041

Test settings	
Tolerance b0	±1,0000e-08

Test statistics	
Min CPU cycles	741
Max CPU cycles	741
Avg CPU cycles	741

Verification: ILimit Float32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for Control block ILimit.

Test results				
Time step	1	2	...	201
CPU cycles	78	78	...	123
Inputs				
In (DSP)	0	0	...	0
I0 (DSP)	0.11	0.11	...	0.11
max (DSP)	0.8	0.8	...	0.8
min (DSP)	0.15	0.15	...	0.15
Enable (DSP)	0	0	...	1
In	0	0	...	0
I0	0.11	0.11	...	0.11
max	0.8	0.8	...	0.8
min	0.15	0.15	...	0.15
Enable	0	0	...	1
Parameters				
Ki	2500			
ts_fact	1			
Outputs				
Out	0	0	...	0.15
Exp. Out	0	0	...	0.15
Out (DSP)	0	0	...	0.15
Exp. Out (DSP)	0	0	...	0.15

Test settings	
Tolerance Out	±9,3132e-07 (±2000 LSB)

Test statistics	
Min CPU cycles	78
Max CPU cycles	139
Avg CPU cycles	120

Test case: Conversion test OK

Conversion test for Control block ILimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Ki	-11	-10.389	...	11
ts_fact	1	2	...	37
Controller parameters				
b0	-0.001	-0.002	...	0.041
Exp. b0	-0.001	-0.002	...	0.041

Test settings	
Tolerance b0	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block ILimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Ki	-11	-10.389	...	11
ts_fact	1	2	...	37
Controller parameters				
b0	-0.001	-0.002	...	0.041
Exp. b0	-0.001	-0.002	...	0.041

Test settings	
Tolerance b0	±1,0000e-08

Test statistics	
Min CPU cycles	789
Max CPU cycles	890
Avg CPU cycles	824

Verification: ILimit Float32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for Control block ILimit.

Test results				
Time step	1	2	...	201
CPU cycles	74	74	...	486
Inputs				
In (DSP)	0	0	...	0
I0 (DSP)	0.11	0.11	...	0.11
max (DSP)	0.8	0.8	...	0.8
min (DSP)	0.15	0.15	...	0.15
Enable (DSP)	0	0	...	1
In	0	0	...	0
I0	0.11	0.11	...	0.11
max	0.8	0.8	...	0.8
min	0.15	0.15	...	0.15
Enable	0	0	...	1
Parameters				
Ki	2500			
ts_fact	1			
Outputs				
Out	0	0	...	0.15
Exp. Out	0	0	...	0.15
Out (DSP)	0	0	...	0.15
Exp. Out (DSP)	0	0	...	0.15

Test settings	
Tolerance Out	±9,3132e-07 (±2000 LSB)

Test statistics	
Min CPU cycles	74
Max CPU cycles	703
Avg CPU cycles	575

Test case: Conversion test OK

Conversion test for Control block ILimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Ki	-11	-10.389	...	11
ts_fact	1	2	...	37
Controller parameters				
b0	-0.001	-0.002	...	0.041
Exp. b0	-0.001	-0.002	...	0.041

Test settings	
Tolerance b0	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block ILimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Ki	-11	-10.389	...	11
ts_fact	1	2	...	37
Controller parameters				
b0	-0.001	-0.002	...	0.041
Exp. b0	-0.001	-0.002	...	0.041

Test settings	
Tolerance b0	±1,0000e-08

Test statistics	
Min CPU cycles	1589
Max CPU cycles	1733
Avg CPU cycles	1670

Verification: ILimit Float32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test

OK

Inport test for Control block ILimit.

Test results				
Time step	1	2	...	201
CPU cycles	57	57	...	217
Inputs				
In (DSP)	0	0	...	0
I0 (DSP)	0.11	0.11	...	0.11
max (DSP)	0.8	0.8	...	0.8
min (DSP)	0.15	0.15	...	0.15
Enable (DSP)	0	0	...	1
In	0	0	...	0
I0	0.11	0.11	...	0.11
max	0.8	0.8	...	0.8
min	0.15	0.15	...	0.15
Enable	0	0	...	1
Parameters				
Ki	2500			
ts_fact	1			
Outputs				
Out	0	0	...	0.15
Exp. Out	0	0	...	0.15
Out (DSP)	0	0	...	0.15
Exp. Out (DSP)	0	0	...	0.15

Test settings	
Tolerance Out	±9,3132e-07 (±2000 LSB)

Test statistics	
Min CPU cycles	57
Max CPU cycles	305
Avg CPU cycles	249

Test case: Conversion test

OK

Conversion test for Control block ILimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Ki	-11	-10.389	...	11
ts_fact	1	2	...	37
Controller parameters				
b0	-0.001	-0.002	...	0.041
Exp. b0	-0.001	-0.002	...	0.041

Test settings	
Tolerance b0	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block ILimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Ki	-11	-10.389	...	11
ts_fact	1	2	...	37
Controller parameters				
b0	-0.001	-0.002	...	0.041
Exp. b0	-0.001	-0.002	...	0.041

Test settings	
Tolerance b0	±1,0000e-08

Test statistics	
Min CPU cycles	583
Max CPU cycles	602
Avg CPU cycles	597

Verification: ILimit Float32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test

OK

Inport test for Control block ILimit.

Test results				
Time step	1	2	...	201
CPU cycles	82	60	...	98
Inputs				
In (DSP)	0	0	...	0
I0 (DSP)	0.11	0.11	...	0.11
max (DSP)	0.8	0.8	...	0.8
min (DSP)	0.15	0.15	...	0.15
Enable (DSP)	0	0	...	1
In	0	0	...	0
I0	0.11	0.11	...	0.11
max	0.8	0.8	...	0.8
min	0.15	0.15	...	0.15
Enable	0	0	...	1
Parameters				
Ki	2500			
ts_fact	1			
Outputs				
Out	0	0	...	0.15
Exp. Out	0	0	...	0.15
Out (DSP)	0	0	...	0.15
Exp. Out (DSP)	0	0	...	0.15

Test settings	
Tolerance Out	±9,3132e-07 (±2000 LSB)

Test statistics	
Min CPU cycles	60
Max CPU cycles	118
Avg CPU cycles	97

Test case: Conversion test

OK

Conversion test for Control block ILimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Ki	-11	-10.389	...	11
ts_fact	1	2	...	37
Controller parameters				
b0	-0.001	-0.002	...	0.041
Exp. b0	-0.001	-0.002	...	0.041

Test settings	
Tolerance b0	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block ILimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Ki	-11	-10.389	...	11
ts_fact	1	2	...	37
Controller parameters				
b0	-0.001	-0.002	...	0.041
Exp. b0	-0.001	-0.002	...	0.041

Test settings	
Tolerance b0	±1,0000e-08

Test statistics	
Min CPU cycles	634
Max CPU cycles	694
Avg CPU cycles	652

Verification: ILimit Float32 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for Control block ILimit.

Test results				
Time step	1	2	...	201
CPU cycles	68	68	...	117
Inputs				
In (DSP)	0	0	...	0
I0 (DSP)	0.11	0.11	...	0.11
max (DSP)	0.8	0.8	...	0.8
min (DSP)	0.15	0.15	...	0.15
Enable (DSP)	0	0	...	1
In	0	0	...	0
I0	0.11	0.11	...	0.11
max	0.8	0.8	...	0.8
min	0.15	0.15	...	0.15
Enable	0	0	...	1
Parameters				
Ki	2500			
ts_fact	1			
Outputs				
Out	0	0	...	0.15
Exp. Out	0	0	...	0.15
Out (DSP)	0	0	...	0.15
Exp. Out (DSP)	0	0	...	0.15

Test settings	
Tolerance Out	±9,3132e-07 (±2000 LSB)

Test statistics	
Min CPU cycles	68
Max CPU cycles	132
Avg CPU cycles	118

Test case: Conversion test OK

Conversion test for Control block ILimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Ki	-11	-10.389	...	11
ts_fact	1	2	...	37
Controller parameters				
b0	-0.001	-0.002	...	0.041
Exp. b0	-0.001	-0.002	...	0.041

Test settings	
Tolerance b0	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block ILimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Ki	-11	-10.389	...	11
ts_fact	1	2	...	37
Controller parameters				
b0	-0.001	-0.002	...	0.041
Exp. b0	-0.001	-0.002	...	0.041

Test settings	
Tolerance b0	±1,0000e-08

Test statistics	
Min CPU cycles	1150
Max CPU cycles	1166
Avg CPU cycles	1152

Verification: ILimit Float32 CPU dsPIC33EP256MC502

Date of Test	2026-06-23
Target controller	dsPIC33EP256MC502

Test case: Inport test

OK

Inport test for Control block ILimit.

Test results				
Time step	1	2	...	201
CPU cycles	64	64	...	522
Inputs				
In (DSP)	0	0	...	0
I0 (DSP)	0.11	0.11	...	0.11
max (DSP)	0.8	0.8	...	0.8
min (DSP)	0.15	0.15	...	0.15
Enable (DSP)	0	0	...	1
In	0	0	...	0
I0	0.11	0.11	...	0.11
max	0.8	0.8	...	0.8
min	0.15	0.15	...	0.15
Enable	0	0	...	1
Parameters				
Ki	2500			
ts_fact	1			
Outputs				
Out	0	0	...	0.15
Exp. Out	0	0	...	0.15
Out (DSP)	0	0	...	0.15
Exp. Out (DSP)	0	0	...	0.15

Test settings	
Tolerance Out	±9,3132e-07 (±2000 LSB)

Test statistics	
Min CPU cycles	64
Max CPU cycles	733
Avg CPU cycles	621

Test case: Conversion test

OK

Conversion test for Control block ILimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Ki	-11	-10.389	...	11
ts_fact	1	2	...	37
Controller parameters				
b0	-0.001	-0.002	...	0.041
Exp. b0	-0.001	-0.002	...	0.041

Test settings	
Tolerance b0	±0,0000e+00

Test case: Conversion-on-Target test **OK**

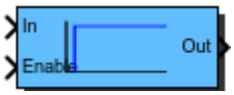
Conversion-on-Target test for Control block ILimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Ki	-11	-10.389	...	11
ts_fact	1	2	...	37
Controller parameters				
b0	-0.001	-0.002	...	0.041
Exp. b0	-0.001	-0.002	...	0.041

Test settings	
Tolerance b0	±1,0000e-08

Test statistics	
Min CPU cycles	2155
Max CPU cycles	2551
Avg CPU cycles	2531

Block: P



P controller:
G(s) = Kp

Inports	
In	Control error input
Enable	Enable == 0: Deactivation of block; Out set to 0 Enable == 1: Activation of block

Outports	
Out	Control value

Mask Parameters		
Name	**ID**	**Description**
Kp	1	Proportional Factor

Description:

Transfer function (zero-order hold discretization method):

$$G(z) = K_{\mathrm{p}}$$

Developer note: The source code of block *PLimit* is used.

Implementations:

FiP16 16 Bit Fixed Point Implementation
FiP32 32 Bit Fixed Point Implementation
Float32 32 Bit Floating Point Implementation
Float64 64 Bit Floating Point Implementation

Implementation: FiP16

16 Bit Fixed Point Implementation

Inports Data Type	
In	int16
Enable	bool

Outports Data Type	
Out	int16

Implementation: FiP32

32 Bit Fixed Point Implementation

Inports Data Type	
In	int32
Enable	bool

Outports Data Type	
Out	int32

Implementation: Float32

32 Bit Floating Point Implementation

Inports Data Type	
In	float32
Enable	bool

Outports Data Type	
Out	float32

Implementation: Float64

64 Bit Floating Point Implementation

Inports Data Type	
In	float64
Enable	bool

Outports Data Type	
Out	float64

Verification: P FiP16 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test

OK

Inport test for Control block P.

Test results						
Time step	1	2	3	4	...	201
CPU cycles	63	63	63	84	...	84
Inputs						
In (DSP)	0	0	0	0	...	0
Enable (DSP)	0	0	0	1	...	1
In	0	0	0	0	...	0
Enable	0	0	0	1	...	1
Parameters						
Kp	2					
Outputs						
Out	0	0	0	0	...	0
Exp. Out	0	0	0	0	...	0
Out (DSP)	0	0	0	0	...	0
Exp. Out (DSP)	0	0	0	0	...	0

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	63
Max CPU cycles	84
Avg CPU cycles	83

Test case: Conversion test

OK

Conversion test for Control block P.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kp	-10	-9.444	-8.889	-8.333	...	10
Controller parameters						
sfrb1	11	11	11	11	...	11
b1	-20480	-19342	-18204	-17067	...	20480
Exp. sfrb1	11	11	11	11	...	11
Exp. b1	-20480	-19342	-18204	-17067	...	20480

Test settings	
Tolerance sfrb1	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block P.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kp	-10	-9.444	-8.889	-8.333	...	10
Controller parameters						
sfrb1	11	11	11	11	...	11
b1	-20480	-19342	-18204	-17066	...	20480
Exp. sfrb1	11	11	11	11	...	11
Exp. b1	-20480	-19342	-18204	-17067	...	20480

Test settings	
Tolerance sfrb1	±0,0000e+00
Tolerance b1	±1,0000e+00

Test statistics	
Min CPU cycles	1389
Max CPU cycles	3539
Avg CPU cycles	2786

Verification: P FiP16 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test — OK

Inport test for Control block P.

Test results						
Time step	1	2	3	4	...	201
CPU cycles	31	31	31	45	...	45
Inputs						
In (DSP)	0	0	0	0	...	0
Enable (DSP)	0	0	0	1	...	1
In	0	0	0	0	...	0
Enable	0	0	0	1	...	1
Parameters						
Kp	2					
Outputs						
Out	0	0	0	0	...	0
Exp. Out	0	0	0	0	...	0
Out (DSP)	0	0	0	0	...	0
Exp. Out (DSP)	0	0	0	0	...	0

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	31
Max CPU cycles	45
Avg CPU cycles	44

Test case: Conversion test — OK

Conversion test for Control block P.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kp	-10	-9.444	-8.889	-8.333	...	10
Controller parameters						
sfrb1	11	11	11	11	...	11
b1	-20480	-19342	-18204	-17067	...	20480
Exp. sfrb1	11	11	11	11	...	11
Exp. b1	-20480	-19342	-18204	-17067	...	20480

Test settings	
Tolerance sfrb1	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block P.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kp	-10	-9.444	-8.889	-8.333	...	10
Controller parameters						
sfrb1	11	11	11	11	...	11
b1	-20480	-19342	-18204	-17066	...	20480
Exp. sfrb1	11	11	11	11	...	11
Exp. b1	-20480	-19342	-18204	-17067	...	20480

Test settings	
Tolerance sfrb1	±0,0000e+00
Tolerance b1	±1,0000e+00

Test statistics	
Min CPU cycles	727
Max CPU cycles	1979
Avg CPU cycles	1536

Verification: P FiP16 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test

OK

Inport test for Control block P.

Test results						
Time step	1	2	3	4	...	201
CPU cycles	71	71	71	86	...	86
Inputs						
In (DSP)	0	0	0	0	...	0
Enable (DSP)	0	0	0	1	...	1
In	0	0	0	0	...	0
Enable	0	0	0	1	...	1
Parameters						
Kp	2					
Outputs						
Out	0	0	0	0	...	0
Exp. Out	0	0	0	0	...	0
Out (DSP)	0	0	0	0	...	0
Exp. Out (DSP)	0	0	0	0	...	0

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	71
Max CPU cycles	86
Avg CPU cycles	85

Test case: Conversion test

OK

Conversion test for Control block P.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kp	-10	-9.444	-8.889	-8.333	...	10
Controller parameters						
sfrb1	11	11	11	11	...	11
b1	-20480	-19342	-18204	-17067	...	20480
Exp. sfrb1	11	11	11	11	...	11
Exp. b1	-20480	-19342	-18204	-17067	...	20480

Test settings	
Tolerance sfrb1	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block P.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kp	-10	-9.444	-8.889	-8.333	...	10
Controller parameters						
sfrb1	11	11	11	11	...	11
b1	-20480	-19342	-18204	-17066	...	20480
Exp. sfrb1	11	11	11	11	...	11
Exp. b1	-20480	-19342	-18204	-17067	...	20480

Test settings	
Tolerance sfrb1	±0,0000e+00
Tolerance b1	±1,0000e+00

Test statistics	
Min CPU cycles	924
Max CPU cycles	1516
Avg CPU cycles	1264

Verification: P FiP16 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test

OK

Inport test for Control block P.

Test results						
Time step	1	2	3	4	...	201
CPU cycles	53	53	53	71	...	71
Inputs						
In (DSP)	0	0	0	0	...	0
Enable (DSP)	0	0	0	1	...	1
In	0	0	0	0	...	0
Enable	0	0	0	1	...	1
Parameters						
Kp	2					
Outputs						
Out	0	0	0	0	...	0
Exp. Out	0	0	0	0	...	0
Out (DSP)	0	0	0	0	...	0
Exp. Out (DSP)	0	0	0	0	...	0

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	53
Max CPU cycles	131
Avg CPU cycles	71

Test case: Conversion test

OK

Conversion test for Control block P.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kp	-10	-9.444	-8.889	-8.333	...	10
Controller parameters						
sfrb1	11	11	11	11	...	11
b1	-20480	-19342	-18204	-17067	...	20480
Exp. sfrb1	11	11	11	11	...	11
Exp. b1	-20480	-19342	-18204	-17067	...	20480

Test settings	
Tolerance sfrb1	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block P.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kp	-10	-9.444	-8.889	-8.333	...	10
Controller parameters						
sfrb1	11	11	11	11	...	11
b1	-20480	-19342	-18204	-17066	...	20480
Exp. sfrb1	11	11	11	11	...	11
Exp. b1	-20480	-19342	-18204	-17067	...	20480

Test settings	
Tolerance sfrb1	±0,0000e+00
Tolerance b1	±1,0000e+00

Test statistics	
Min CPU cycles	1698
Max CPU cycles	4552
Avg CPU cycles	3615

Verification: P FiP16 CPU PIC32MX170F256

Date of Test 2026-06-19

Target controller PIC32MX170F256

Test case: Inport test OK

Inport test for Control block P.

Test results						
Time step	1	2	3	4	...	201
CPU cycles	30	30	30	50	...	50
Inputs						
In (DSP)	0	0	0	0	...	0
Enable (DSP)	0	0	0	1	...	1
In	0	0	0	0	...	0
Enable	0	0	0	1	...	1
Parameters						
Kp	2					
Outputs						
Out	0	0	0	0	...	0
Exp. Out	0	0	0	0	...	0
Out (DSP)	0	0	0	0	...	0
Exp. Out (DSP)	0	0	0	0	...	0

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	30
Max CPU cycles	50
Avg CPU cycles	49

Test case: Conversion test OK

Conversion test for Control block P.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kp	-10	-9.444	-8.889	-8.333	...	10
Controller parameters						
sfrb1	11	11	11	11	...	11
b1	-20480	-19342	-18204	-17067	...	20480
Exp. sfrb1	11	11	11	11	...	11
Exp. b1	-20480	-19342	-18204	-17067	...	20480

Test settings	
Tolerance sfrb1	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block P.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kp	-10	-9.444	-8.889	-8.333	...	10
Controller parameters						
sfrb1	11	11	11	11	...	11
b1	-20480	-19342	-18204	-17066	...	20480
Exp. sfrb1	11	11	11	11	...	11
Exp. b1	-20480	-19342	-18204	-17067	...	20480

Test settings	
Tolerance sfrb1	±0,0000e+00
Tolerance b1	±1,0000e+00

Test statistics	
Min CPU cycles	774
Max CPU cycles	1943
Avg CPU cycles	1547

Verification: P FiP16 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test

OK

Inport test for Control block P.

Test results						
Time step	1	2	3	4	...	201
CPU cycles	71	58	58	84	...	84
Inputs						
In (DSP)	0	0	0	0	...	0
Enable (DSP)	0	0	0	1	...	1
In	0	0	0	0	...	0
Enable	0	0	0	1	...	1
Parameters						
Kp	2					
Outputs						
Out	0	0	0	0	...	0
Exp. Out	0	0	0	0	...	0
Out (DSP)	0	0	0	0	...	0
Exp. Out (DSP)	0	0	0	0	...	0

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	58
Max CPU cycles	84
Avg CPU cycles	83

Test case: Conversion test

OK

Conversion test for Control block P.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kp	-10	-9.444	-8.889	-8.333	...	10
Controller parameters						
sfrb1	11	11	11	11	...	11
b1	-20480	-19342	-18204	-17067	...	20480
Exp. sfrb1	11	11	11	11	...	11
Exp. b1	-20480	-19342	-18204	-17067	...	20480

Test settings	
Tolerance sfrb1	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block P.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kp	-10	-9.444	-8.889	-8.333	...	10
Controller parameters						
sfrb1	11	11	11	11	...	11
b1	-20480	-19342	-18204	-17066	...	20480
Exp. sfrb1	11	11	11	11	...	11
Exp. b1	-20480	-19342	-18204	-17067	...	20480

Test settings	
Tolerance sfrb1	±0,0000e+00
Tolerance b1	±1,0000e+00

Test statistics	
Min CPU cycles	640
Max CPU cycles	1191
Avg CPU cycles	952

Verification: P FiP16 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test

OK

Inport test for Control block P.

Test results						
Time step	1	2	3	4	...	201
CPU cycles	53	53	53	74	...	74
Inputs						
In (DSP)	0	0	0	0	...	0
Enable (DSP)	0	0	0	1	...	1
In	0	0	0	0	...	0
Enable	0	0	0	1	...	1
Parameters						
Kp	2					
Outputs						
Out	0	0	0	0	...	0
Exp. Out	0	0	0	0	...	0
Out (DSP)	0	0	0	0	...	0
Exp. Out (DSP)	0	0	0	0	...	0

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	53
Max CPU cycles	74
Avg CPU cycles	73

Test case: Conversion test

OK

Conversion test for Control block P.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kp	-10	-9.444	-8.889	-8.333	...	10
Controller parameters						
sfrb1	11	11	11	11	...	11
b1	-20480	-19342	-18204	-17067	...	20480
Exp. sfrb1	11	11	11	11	...	11
Exp. b1	-20480	-19342	-18204	-17067	...	20480

Test settings	
Tolerance sfrb1	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block P.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kp	-10	-9.444	-8.889	-8.333	...	10
Controller parameters						
sfrb1	11	11	11	11	...	11
b1	-20480	-19342	-18204	-17066	...	20480
Exp. sfrb1	11	11	11	11	...	11
Exp. b1	-20480	-19342	-18204	-17067	...	20480

Test settings	
Tolerance sfrb1	±0,0000e+00
Tolerance b1	±1,0000e+00

Test statistics	
Min CPU cycles	1074
Max CPU cycles	2764
Avg CPU cycles	2171

Verification: P FiP16 CPU dsPIC33EP256MC502

Date of Test	2026-06-23
Target controller	dsPIC33EP256MC502

Test case: Inport test

OK

Inport test for Control block P.

Test results						
Time step	1	2	3	4	...	201
CPU cycles	39	39	39	65	...	65
Inputs						
In (DSP)	0	0	0	0	...	0
Enable (DSP)	0	0	0	1	...	1
In	0	0	0	0	...	0
Enable	0	0	0	1	...	1
Parameters						
Kp	2					
Outputs						
Out	0	0	0	0	...	0
Exp. Out	0	0	0	0	...	0
Out (DSP)	0	0	0	0	...	0
Exp. Out (DSP)	0	0	0	0	...	0

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	39
Max CPU cycles	65
Avg CPU cycles	64

Test case: Conversion test

OK

Conversion test for Control block P.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kp	-10	-9.444	-8.889	-8.333	...	10
Controller parameters						
sfrb1	11	11	11	11	...	11
b1	-20480	-19342	-18204	-17067	...	20480
Exp. sfrb1	11	11	11	11	...	11
Exp. b1	-20480	-19342	-18204	-17067	...	20480

Test settings	
Tolerance sfrb1	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block P.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kp	-10	-9.444	-8.889	-8.333	...	10
Controller parameters						
sfrb1	11	11	11	11	...	11
b1	-20480	-19342	-18204	-17066	...	20480
Exp. sfrb1	11	11	11	11	...	11
Exp. b1	-20480	-19342	-18204	-17067	...	20480

Test settings	
Tolerance sfrb1	±0,0000e+00
Tolerance b1	±1,0000e+00

Test statistics	
Min CPU cycles	2497
Max CPU cycles	10438
Avg CPU cycles	7887

Verification: P FiP32 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test

OK

Inport test for Control block P.

Test results				
Time step	1	2	...	201
CPU cycles	65	65	...	190
Inputs				
In (DSP)	0	0	...	0
Enable (DSP)	0	0	...	1
In	0	0	...	0
Enable	0	0	...	1
Parameters				
Kp	2			
Outputs				
Out	0	0	...	0
Exp. Out	0	0	...	0
Out (DSP)	0	0	...	0
Exp. Out (DSP)	0	0	...	0

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	65
Max CPU cycles	190
Avg CPU cycles	188

Test case: Conversion test

OK

Conversion test for Control block P.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Controller parameters				
sfrb1	27	27	...	27
b1	-1342177280	-1267611876	...	1342177280
Exp. sfrb1	27	27	...	27
Exp. b1	-1342177280	-1267611876	...	1342177280

Test settings	
Tolerance sfrb1	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block P.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Controller parameters				
sfrb1	27	27	...	27
b1	-1342177280	-1267611904	...	1342177280
Exp. sfrb1	27	27	...	27
Exp. b1	-1342177280	-1267611876	...	1342177280

Test settings	
Tolerance sfrb1	±0,0000e+00
Tolerance b1	±1,0000e+02

Test statistics	
Min CPU cycles	1597
Max CPU cycles	3795
Avg CPU cycles	3037

Verification: P FiP32 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test — OK

Inport test for Control block P.

Test results				
Time step	1	2	...	201
CPU cycles	43	43	...	85
Inputs				
In (DSP)	0	0	...	0
Enable (DSP)	0	0	...	1
In	0	0	...	0
Enable	0	0	...	1
Parameters				
Kp	2			
Outputs				
Out	0	0	...	0
Exp. Out	0	0	...	0
Out (DSP)	0	0	...	0
Exp. Out (DSP)	0	0	...	0

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	43
Max CPU cycles	85
Avg CPU cycles	84

Test case: Conversion test — OK

Conversion test for Control block P.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Controller parameters				
sfrb1	27	27	...	27
b1	-1342177280	-1267611876	...	1342177280
Exp. sfrb1	27	27	...	27
Exp. b1	-1342177280	-1267611876	...	1342177280

Test settings	
Tolerance sfrb1	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block P.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Controller parameters				
sfrb1	27	27	...	27
b1	-1342177280	-1267611904	...	1342177280
Exp. sfrb1	27	27	...	27
Exp. b1	-1342177280	-1267611876	...	1342177280

Test settings	
Tolerance sfrb1	±0,0000e+00
Tolerance b1	±1,0000e+02

Test statistics	
Min CPU cycles	689
Max CPU cycles	1585
Avg CPU cycles	1281

Verification: P FiP32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test

OK

Inport test for Control block P.

Test results				
Time step	1	2	...	201
CPU cycles	68	68	...	114
Inputs				
In (DSP)	0	0	...	0
Enable (DSP)	0	0	...	1
In	0	0	...	0
Enable	0	0	...	1
Parameters				
Kp	2			
Outputs				
Out	0	0	...	0
Exp. Out	0	0	...	0
Out (DSP)	0	0	...	0
Exp. Out (DSP)	0	0	...	0

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	68
Max CPU cycles	114
Avg CPU cycles	113

Test case: Conversion test

OK

Conversion test for Control block P.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Controller parameters				
sfrb1	27	27	...	27
b1	-1342177280	-1267611876	...	1342177280
Exp. sfrb1	27	27	...	27
Exp. b1	-1342177280	-1267611876	...	1342177280

Test settings	
Tolerance sfrb1	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block P.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Controller parameters				
sfrb1	27	27	...	27
b1	-1342177280	-1267611904	...	1342177280
Exp. sfrb1	27	27	...	27
Exp. b1	-1342177280	-1267611876	...	1342177280

Test settings	
Tolerance sfrb1	±0,0000e+00
Tolerance b1	±1,0000e+02

Test statistics	
Min CPU cycles	1262
Max CPU cycles	1828
Avg CPU cycles	1637

Verification: P FiP32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test

OK

Inport test for Control block P.

Test results				
Time step	1	2	...	201
CPU cycles	63	63	...	173
Inputs				
In (DSP)	0	0	...	0
Enable (DSP)	0	0	...	1
In	0	0	...	0
Enable	0	0	...	1
Parameters				
Kp	2			
Outputs				
Out	0	0	...	0
Exp. Out	0	0	...	0
Out (DSP)	0	0	...	0
Exp. Out (DSP)	0	0	...	0

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	63
Max CPU cycles	233
Avg CPU cycles	170

Test case: Conversion test

OK

Conversion test for Control block P.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Controller parameters				
sfrb1	27	27	...	27
b1	-1342177280	-1267611876	...	1342177280
Exp. sfrb1	27	27	...	27
Exp. b1	-1342177280	-1267611876	...	1342177280

Test settings	
Tolerance sfrb1	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block P.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Controller parameters				
sfrb1	27	27	...	27
b1	-1342177280	-1267611904	...	1342177280
Exp. sfrb1	27	27	...	27
Exp. b1	-1342177280	-1267611876	...	1342177280

Test settings	
Tolerance sfrb1	±0,0000e+00
Tolerance b1	±1,0000e+02

Test statistics	
Min CPU cycles	2673
Max CPU cycles	5824
Avg CPU cycles	4879

Verification: P FiP32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test

OK

Inport test for Control block P.

Test results				
Time step	1	2	...	201
CPU cycles	30	30	...	65
Inputs				
In (DSP)	0	0	...	0
Enable (DSP)	0	0	...	1
In	0	0	...	0
Enable	0	0	...	1
Parameters				
Kp	2			
Outputs				
Out	0	0	...	0
Exp. Out	0	0	...	0
Out (DSP)	0	0	...	0
Exp. Out (DSP)	0	0	...	0

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	30
Max CPU cycles	66
Avg CPU cycles	64

Test case: Conversion test

OK

Conversion test for Control block P.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Controller parameters				
sfrb1	27	27	...	27
b1	-1342177280	-1267611876	...	1342177280
Exp. sfrb1	27	27	...	27
Exp. b1	-1342177280	-1267611876	...	1342177280

Test settings	
Tolerance sfrb1	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block P.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Controller parameters				
sfrb1	27	27	...	27
b1	-1342177280	-1267611904	...	1342177280
Exp. sfrb1	27	27	...	27
Exp. b1	-1342177280	-1267611876	...	1342177280

Test settings	
Tolerance sfrb1	±0,0000e+00
Tolerance b1	±1,0000e+02

Test statistics	
Min CPU cycles	1230
Max CPU cycles	2413
Avg CPU cycles	2016

Verification: P FiP32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test

OK

Inport test for Control block P.

Test results				
Time step	1	2	...	201
CPU cycles	80	58	...	106
Inputs				
In (DSP)	0	0	...	0
Enable (DSP)	0	0	...	1
In	0	0	...	0
Enable	0	0	...	1
Parameters				
Kp	2			
Outputs				
Out	0	0	...	0
Exp. Out	0	0	...	0
Out (DSP)	0	0	...	0
Exp. Out (DSP)	0	0	...	0

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	58
Max CPU cycles	108
Avg CPU cycles	105

Test case: Conversion test

OK

Conversion test for Control block P.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Controller parameters				
sfrb1	27	27	...	27
b1	-1342177280	-1267611876	...	1342177280
Exp. sfrb1	27	27	...	27
Exp. b1	-1342177280	-1267611876	...	1342177280

Test settings	
Tolerance sfrb1	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block P.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Controller parameters				
sfrb1	27	27	...	27
b1	-1342177280	-1267611904	...	1342177280
Exp. sfrb1	27	27	...	27
Exp. b1	-1342177280	-1267611876	...	1342177280

Test settings	
Tolerance sfrb1	±0,0000e+00
Tolerance b1	±1,0000e+02

Test statistics	
Min CPU cycles	958
Max CPU cycles	1527
Avg CPU cycles	1278

Verification: P FiP32 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test — OK

Inport test for Control block P.

Test results				
Time step	1	2	...	201
CPU cycles	57	57	...	161
Inputs				
In (DSP)	0	0	...	0
Enable (DSP)	0	0	...	1
In	0	0	...	0
Enable	0	0	...	1
Parameters				
Kp	2			
Outputs				
Out	0	0	...	0
Exp. Out	0	0	...	0
Out (DSP)	0	0	...	0
Exp. Out (DSP)	0	0	...	0

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	57
Max CPU cycles	161
Avg CPU cycles	159

Test case: Conversion test — OK

Conversion test for Control block P.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Controller parameters				
sfrb1	27	27	...	27
b1	-1342177280	-1267611876	...	1342177280
Exp. sfrb1	27	27	...	27
Exp. b1	-1342177280	-1267611876	...	1342177280

Test settings	
Tolerance sfrb1	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block P.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Controller parameters				
sfrb1	27	27	...	27
b1	-1342177280	-1267611904	...	1342177280
Exp. sfrb1	27	27	...	27
Exp. b1	-1342177280	-1267611876	...	1342177280

Test settings	
Tolerance sfrb1	±0,0000e+00
Tolerance b1	±1,0000e+02

Test statistics	
Min CPU cycles	1198
Max CPU cycles	2931
Avg CPU cycles	2333

Verification: P FiP32 CPU dsPIC33EP256MC502

Date of Test	2026-06-23
Target controller	dsPIC33EP256MC502

Test case: Inport test — OK

Inport test for Control block P.

Test results				
Time step	1	2	...	201
CPU cycles	47	47	...	460
Inputs				
In (DSP)	0	0	...	0
Enable (DSP)	0	0	...	1
In	0	0	...	0
Enable	0	0	...	1
Parameters				
Kp	2			
Outputs				
Out	0	0	...	0
Exp. Out	0	0	...	0
Out (DSP)	0	0	...	0
Exp. Out (DSP)	0	0	...	0

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	47
Max CPU cycles	467
Avg CPU cycles	455

Test case: Conversion test — OK

Conversion test for Control block P.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Controller parameters				
sfrb1	27	27	...	27
b1	-1342177280	-1267611876	...	1342177280
Exp. sfrb1	27	27	...	27
Exp. b1	-1342177280	-1267611876	...	1342177280

Test settings	
Tolerance sfrb1	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block P.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Controller parameters				
sfrb1	27	27	...	27
b1	-1342177280	-1267611904	...	1342177280
Exp. sfrb1	27	27	...	27
Exp. b1	-1342177280	-1267611876	...	1342177280

Test settings	
Tolerance sfrb1	±0,0000e+00
Tolerance b1	±1,0000e+02

Test statistics	
Min CPU cycles	2903
Max CPU cycles	10578
Avg CPU cycles	8126

Verification: P Float32 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test

OK

Inport test for Control block P.

Test results				
Time step	1	2	...	201
CPU cycles	66	66	...	83
Inputs				
In (DSP)	0	0	...	0
Enable (DSP)	0	0	...	1
In	0	0	...	0
Enable	0	0	...	1
Parameters				
Kp	2			
Outputs				
Out	0	0	...	0
Exp. Out	0	0	...	0
Out (DSP)	0	0	...	0
Exp. Out (DSP)	0	0	...	0

Test settings	
Tolerance Out	±2,3283e-09 (±5 LSB)

Test statistics	
Min CPU cycles	66
Max CPU cycles	83
Avg CPU cycles	82

Test case: Conversion test

OK

Conversion test for Control block P.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Controller parameters				
b1	-10	-9.444	...	10
Exp. b1	-10	-9.444	...	10

Test settings	
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block P.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Controller parameters				
b1	-10	-9.444	...	10
Exp. b1	-10	-9.444	...	10

Test settings	
Tolerance b1	±1,0000e-06

Test statistics	
Min CPU cycles	818
Max CPU cycles	829
Avg CPU cycles	818

Verification: P Float32 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test

OK

Inport test for Control block P.

Test results				
Time step	1	2	...	201
CPU cycles	29	29	...	53
Inputs				
In (DSP)	0	0	...	0
Enable (DSP)	0	0	...	1
In	0	0	...	0
Enable	0	0	...	1
Parameters				
Kp	2			
Outputs				
Out	0	0	...	0
Exp. Out	0	0	...	0
Out (DSP)	0	0	...	0
Exp. Out (DSP)	0	0	...	0

Test settings	
Tolerance Out	±2,3283e-09 (±5 LSB)

Test statistics	
Min CPU cycles	29
Max CPU cycles	53
Avg CPU cycles	52

Test case: Conversion test

OK

Conversion test for Control block P.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Controller parameters				
b1	-10	-9.444	...	10
Exp. b1	-10	-9.444	...	10

Test settings	
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block P.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Controller parameters				
b1	-10	-9.444	...	10
Exp. b1	-10	-9.444	...	10

Test settings	
Tolerance b1	±1,0000e-06

Test statistics	
Min CPU cycles	397
Max CPU cycles	397
Avg CPU cycles	397

Verification: P Float32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test

OK

Inport test for Control block P.

Test results				
Time step	1	2	...	201
CPU cycles	76	76	...	106
Inputs				
In (DSP)	0	0	...	0
Enable (DSP)	0	0	...	1
In	0	0	...	0
Enable	0	0	...	1
Parameters				
Kp	2			
Outputs				
Out	0	0	...	0
Exp. Out	0	0	...	0
Out (DSP)	0	0	...	0
Exp. Out (DSP)	0	0	...	0

Test settings	
Tolerance Out	±2,3283e-09 (±5 LSB)

Test statistics	
Min CPU cycles	76
Max CPU cycles	106
Avg CPU cycles	105

Test case: Conversion test

OK

Conversion test for Control block P.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Controller parameters				
b1	-10	-9.444	...	10
Exp. b1	-10	-9.444	...	10

Test settings	
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block P.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Controller parameters				
b1	-10	-9.444	...	10
Exp. b1	-10	-9.444	...	10

Test settings	
Tolerance b1	±1,0000e-06

Test statistics	
Min CPU cycles	475
Max CPU cycles	541
Avg CPU cycles	476

Verification: P Float32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test

OK

Inport test for Control block P.

Test results				
Time step	1	2	...	201
CPU cycles	64	64	...	340
Inputs				
In (DSP)	0	0	...	0
Enable (DSP)	0	0	...	1
In	0	0	...	0
Enable	0	0	...	1
Parameters				
Kp	2			
Outputs				
Out	0	0	...	0
Exp. Out	0	0	...	0
Out (DSP)	0	0	...	0
Exp. Out (DSP)	0	0	...	0

Test settings	
Tolerance Out	±2,3283e-09 (±5 LSB)

Test statistics	
Min CPU cycles	64
Max CPU cycles	416
Avg CPU cycles	388

Test case: Conversion test

OK

Conversion test for Control block P.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Controller parameters				
b1	-10	-9.444	...	10
Exp. b1	-10	-9.444	...	10

Test settings	
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block P.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Controller parameters				
b1	-10	-9.444	...	10
Exp. b1	-10	-9.444	...	10

Test settings	
Tolerance b1	±1,0000e-06

Test statistics	
Min CPU cycles	667
Max CPU cycles	696
Avg CPU cycles	694

Verification: P Float32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test

OK

Inport test for Control block P.

Test results				
Time step	1	2	...	201
CPU cycles	30	30	...	163
Inputs				
In (DSP)	0	0	...	0
Enable (DSP)	0	0	...	1
In	0	0	...	0
Enable	0	0	...	1
Parameters				
Kp	2			
Outputs				
Out	0	0	...	0
Exp. Out	0	0	...	0
Out (DSP)	0	0	...	0
Exp. Out (DSP)	0	0	...	0

Test settings	
Tolerance Out	±2,3283e-09 (±5 LSB)

Test statistics	
Min CPU cycles	30
Max CPU cycles	183
Avg CPU cycles	174

Test case: Conversion test

OK

Conversion test for Control block P.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Controller parameters				
b1	-10	-9.444	...	10
Exp. b1	-10	-9.444	...	10

Test settings	
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block P.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Controller parameters				
b1	-10	-9.444	...	10
Exp. b1	-10	-9.444	...	10

Test settings	
Tolerance b1	±1,0000e-06

Test statistics	
Min CPU cycles	277
Max CPU cycles	278
Avg CPU cycles	277

Verification: P Float32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test

OK

Inport test for Control block P.

Test results				
Time step	1	2	...	201
CPU cycles	77	59	...	80
Inputs				
In (DSP)	0	0	...	0
Enable (DSP)	0	0	...	1
In	0	0	...	0
Enable	0	0	...	1
Parameters				
Kp	2			
Outputs				
Out	0	0	...	0
Exp. Out	0	0	...	0
Out (DSP)	0	0	...	0
Exp. Out (DSP)	0	0	...	0

Test settings	
Tolerance Out	±2,3283e-09 (±5 LSB)

Test statistics	
Min CPU cycles	59
Max CPU cycles	80
Avg CPU cycles	79

Test case: Conversion test

OK

Conversion test for Control block P.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Controller parameters				
b1	-10	-9.444	...	10
Exp. b1	-10	-9.444	...	10

Test settings	
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block P.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Controller parameters				
b1	-10	-9.444	...	10
Exp. b1	-10	-9.444	...	10

Test settings	
Tolerance b1	±1,0000e-06

Test statistics	
Min CPU cycles	389
Max CPU cycles	433
Avg CPU cycles	391

Verification: P Float32 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test

OK

Inport test for Control block P.

Test results				
Time step	1	2	...	201
CPU cycles	59	59	...	83
Inputs				
In (DSP)	0	0	...	0
Enable (DSP)	0	0	...	1
In	0	0	...	0
Enable	0	0	...	1
Parameters				
Kp	2			
Outputs				
Out	0	0	...	0
Exp. Out	0	0	...	0
Out (DSP)	0	0	...	0
Exp. Out (DSP)	0	0	...	0

Test settings	
Tolerance Out	±2,3283e-09 (±5 LSB)

Test statistics	
Min CPU cycles	59
Max CPU cycles	83
Avg CPU cycles	82

Test case: Conversion test

OK

Conversion test for Control block P.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Controller parameters				
b1	-10	-9.444	...	10
Exp. b1	-10	-9.444	...	10

Test settings	
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block P.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Controller parameters				
b1	-10	-9.444	...	10
Exp. b1	-10	-9.444	...	10

Test settings	
Tolerance b1	±1,0000e-06

Test statistics	
Min CPU cycles	649
Max CPU cycles	660
Avg CPU cycles	649

Verification: P Float32 CPU dsPIC33EP256MC502

Date of Test	2026-06-23
Target controller	dsPIC33EP256MC502

Test case: Inport test

OK

Inport test for Control block P.

Test results				
Time step	1	2	...	201
CPU cycles	51	51	...	365
Inputs				
In (DSP)	0	0	...	0
Enable (DSP)	0	0	...	1
In	0	0	...	0
Enable	0	0	...	1
Parameters				
Kp	2			
Outputs				
Out	0	0	...	0
Exp. Out	0	0	...	0
Out (DSP)	0	0	...	0
Exp. Out (DSP)	0	0	...	0

Test settings	
Tolerance Out	±2,3283e-09 (±5 LSB)

Test statistics	
Min CPU cycles	51
Max CPU cycles	407
Avg CPU cycles	390

Test case: Conversion test

OK

Conversion test for Control block P.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Controller parameters				
b1	-10	-9.444	...	10
Exp. b1	-10	-9.444	...	10

Test settings	
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

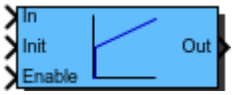
Conversion-on-Target test for Control block P.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Controller parameters				
b1	-10	-9.444	...	10
Exp. b1	-10	-9.444	...	10

Test settings	
Tolerance b1	±1,0000e-06

Test statistics	
Min CPU cycles	515
Max CPU cycles	860
Avg CPU cycles	848

Block: PI



PI controller:
G(s) = Kp + Ki/s

Inports	
In	Control error input
Init	Initial value of output Out when enabled
Enable	Enable == 0: Deactivation of block; Out set to 0 Enable 0->1: Preload of integral part Enable == 1: Activation of block

Outports	
Out	Control value

Mask Parameters		
Name	**ID**	**Description**
Kp	1	Proportional Factor
Ki	2	Integral Factor
initHandling	3	Determines what the signal provided on Init input is used for
ts_fact	4	Multiplication factor of base sampling time (in integer format)

Description:

Preloading Integral
A rising edge at the *Enable* inport enables the controller and preloads the integral.
One may choose from two options how to preload the integral value:

- Preload the integral from the *Init* inport.
- Preload the integral such that the first output of the controller matches the current value at the *Init* inport.
  This option allows controller switching without disturbing the control.

Note: Each fixed point implementation uses the next higher integer data type for the integral value storage variable.
Transfer function (zero-order hold discretization method):
When the block is enabled, the PI controller realizes the following transfer function:

$$G(z) = K_\mathrm{p} + K_\mathrm{i} T_\mathrm{s} \frac{1}{z-1}$$

Developer note: The source code of block *PILimit* is used.

Implementations:

FiP8	8 Bit Fixed Point Implementation
FiP16	16 Bit Fixed Point Implementation
FiP32	32 Bit Fixed Point Implementation
Float32	32 Bit Floating Point Implementation
Float64	64 Bit Floating Point Implementation

Implementation: FiP8

8 Bit Fixed Point Implementation

Inports Data Type	
In	int8
Init	int8
Enable	bool

Outports Data Type	
Out	int8

Implementation: FiP16

16 Bit Fixed Point Implementation

Inports Data Type	
In	int16
Init	int16
Enable	bool

Outports Data Type	
Out	int16

Implementation: FiP32

32 Bit Fixed Point Implementation

Inports Data Type	
In	int32
Init	int32
Enable	bool

Outports Data Type	
Out	int32

Implementation: Float32

32 Bit Floating Point Implementation

Inports Data Type	
In	float32
Init	float32
Enable	bool

Outports Data Type	
Out	float32

Implementation: Float64

64 Bit Floating Point Implementation

Inports Data Type	
In	float64
Init	float64
Enable	bool

Outports Data Type	
Out	float64

Verification: PI FiP16 CPU TMS320F28335

Date of Test 2026-06-19

Target controller TMS320F28335

Test case: Inport test OK

Inport test for Control block PI.

Test results						
Time step	1	2	3	4	...	201
CPU cycles	67	67	67	131	...	122
Inputs						
In (DSP)	0	0	0	0	...	0
Init (DSP)	3604	3604	3604	3604	...	3604
Enable (DSP)	0	0	0	1	...	1
In	0	0	0	0	...	0
Init	0.11	0.11	0.11	0.11	...	0.11
Enable	0	0	0	1	...	1
Parameters						
Kp	2					
Ki	2500					
initHandling	initialize integral					
ts_fact	1					
Outputs						
Out	0	0	0	0.11	...	-0.528
Exp. Out	0	0	0	0.11	...	-0.528
Out (DSP)	0	0	0	3604	...	-17292
Exp. Out (DSP)	0	0	0	3604	...	-17285

Test settings	
Tolerance Out	±3,0518e-04 (±10 LSB)

Test statistics	
Min CPU cycles	67
Max CPU cycles	131
Avg CPU cycles	119

Test case: Conversion test OK

Conversion test for Control block PI.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kp	-10	-9.444	-8.889	-8.333	...	10
Ki	-11	-10.389	-9.778	-9.167	...	11
initHandling	initialize integral	initialize integral	initialize integral	initialize integral	...	initialize
ts_fact	1	1	1	1	...	1
Controller parameters						
initHandling	0	0	0	0	...	1
sfrb0	15	15	15	15	...	15
sfrb1	11	11	11	11	...	11
b0	-36	-34	-32	-30	...	36
b1	-20480	-19342	-18204	-17067	...	204
Exp. initHandling	0	0	0	0	...	1
Exp. sfrb0	15	15	15	15	...	15
Exp. sfrb1	11	11	11	11	...	11
Exp. b0	-36	-34	-32	-30	...	36
Exp. b1	-20480	-19342	-18204	-17067	...	204

Test settings	
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block PI.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kp	-10	-9.444	-8.889	-8.333	...	10
Ki	-11	-10.389	-9.778	-9.167	...	11
initHandling	initialize integral	initialize integral	initialize integral	initialize integral	...	initialize
ts_fact	1	1	1	1	...	1
Controller parameters						
initHandling	0	0	0	0	...	1
sfrb0	15	15	15	15	...	15
sfrb1	11	11	11	11	...	11
b0	-36	-34	-32	-30	...	36
b1	-20480	-19342	-18204	-17066	...	204
Exp. initHandling	0	0	0	0	...	1
Exp. sfrb0	15	15	15	15	...	15
Exp. sfrb1	11	11	11	11	...	11
Exp. b0	-36	-34	-32	-30	...	36
Exp. b1	-20480	-19342	-18204	-17067	...	204

Test settings	
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±1,0000e+00
Tolerance b1	±1,0000e+00

Test statistics	
Min CPU cycles	3083
Max CPU cycles	5333
Avg CPU cycles	4571

Verification: PI FiP16 CPU TM4C123GH6

Date of Test 2026-06-19

Target controller TM4C123GH6

Test case: Inport test OK

Inport test for Control block PI.

Test results						
Time step	1	2	3	4	...	201
CPU cycles	43	43	43	91	...	85
Inputs						
In (DSP)	0	0	0	0	...	0
Init (DSP)	3604	3604	3604	3604	...	3604
Enable (DSP)	0	0	0	1	...	1
In	0	0	0	0	...	0
Init	0.11	0.11	0.11	0.11	...	0.11
Enable	0	0	0	1	...	1
Parameters						
Kp	2					
Ki	2500					
initHandling	initialize integral					
ts_fact	1					
Outputs						
Out	0	0	0	0.11	...	-0.528
Exp. Out	0	0	0	0.11	...	-0.528
Out (DSP)	0	0	0	3604	...	-17292
Exp. Out (DSP)	0	0	0	3604	...	-17285

Test settings	
Tolerance Out	±3,0518e-04 (±10 LSB)

Test statistics	
Min CPU cycles	43
Max CPU cycles	91
Avg CPU cycles	83

Test case: Conversion test OK

Conversion test for Control block PI.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kp	-10	-9.444	-8.889	-8.333	...	10
Ki	-11	-10.389	-9.778	-9.167	...	11
initHandling	initialize integral	initialize integral	initialize integral	initialize integral	...	initialize
ts_fact	1	1	1	1	...	1
Controller parameters						
initHandling	0	0	0	0	...	1
sfrb0	15	15	15	15	...	15
sfrb1	11	11	11	11	...	11
b0	-36	-34	-32	-30	...	36
b1	-20480	-19342	-18204	-17067	...	204
Exp. initHandling	0	0	0	0	...	1
Exp. sfrb0	15	15	15	15	...	15
Exp. sfrb1	11	11	11	11	...	11
Exp. b0	-36	-34	-32	-30	...	36
Exp. b1	-20480	-19342	-18204	-17067	...	204

Test settings	
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block PI.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kp	-10	-9.444	-8.889	-8.333	...	10
Ki	-11	-10.389	-9.778	-9.167	...	11
initHandling	initialize integral	initialize integral	initialize integral	initialize integral	...	initialize
ts_fact	1	1	1	1	...	1
Controller parameters						
initHandling	0	0	0	0	...	1
sfrb0	15	15	15	15	...	15
sfrb1	11	11	11	11	...	11
b0	-36	-34	-32	-30	...	36
b1	-20480	-19342	-18204	-17066	...	204
Exp. initHandling	0	0	0	0	...	1
Exp. sfrb0	15	15	15	15	...	15
Exp. sfrb1	11	11	11	11	...	11
Exp. b0	-36	-34	-32	-30	...	36
Exp. b1	-20480	-19342	-18204	-17067	...	204

Test settings	
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±1,0000e+00
Tolerance b1	±1,0000e+00

Test statistics	
Min CPU cycles	1561
Max CPU cycles	2887
Avg CPU cycles	2439

Verification: PI FiP16 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for Control block PI.

Test results						
Time step	1	2	3	4	...	201
CPU cycles	68	68	68	154	...	142
Inputs						
In (DSP)	0	0	0	0	...	0
Init (DSP)	3604	3604	3604	3604	...	3604
Enable (DSP)	0	0	0	1	...	1
In	0	0	0	0	...	0
Init	0.11	0.11	0.11	0.11	...	0.11
Enable	0	0	0	1	...	1
Parameters						
Kp	2					
Ki	2500					
initHandling	initialize integral					
ts_fact	1					
Outputs						
Out	0	0	0	0.11	...	-0.528
Exp. Out	0	0	0	0.11	...	-0.528
Out (DSP)	0	0	0	3604	...	-17292
Exp. Out (DSP)	0	0	0	3604	...	-17285

Test settings	
Tolerance Out	±3,0518e-04 (±10 LSB)

Test statistics	
Min CPU cycles	68
Max CPU cycles	154
Avg CPU cycles	129

Test case: Conversion test OK

Conversion test for Control block PI.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kp	-10	-9.444	-8.889	-8.333	...	10
Ki	-11	-10.389	-9.778	-9.167	...	11
initHandling	initialize integral	initialize integral	initialize integral	initialize integral	...	initialize
ts_fact	1	1	1	1	...	1
Controller parameters						
initHandling	0	0	0	0	...	1
sfrb0	15	15	15	15	...	15
sfrb1	11	11	11	11	...	11
b0	-36	-34	-32	-30	...	36
b1	-20480	-19342	-18204	-17067	...	204
Exp. initHandling	0	0	0	0	...	1
Exp. sfrb0	15	15	15	15	...	15
Exp. sfrb1	11	11	11	11	...	11
Exp. b0	-36	-34	-32	-30	...	36
Exp. b1	-20480	-19342	-18204	-17067	...	204

Test settings	
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block PI.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kp	-10	-9.444	-8.889	-8.333	...	10
Ki	-11	-10.389	-9.778	-9.167	...	11
initHandling	initialize integral	initialize integral	initialize integral	initialize integral	...	initialize
ts_fact	1	1	1	1	...	1
Controller parameters						
initHandling	0	0	0	0	...	1
sfrb0	15	15	15	15	...	15
sfrb1	11	11	11	11	...	11
b0	-36	-34	-32	-30	...	36
b1	-20480	-19342	-18204	-17066	...	204
Exp. initHandling	0	0	0	0	...	1
Exp. sfrb0	15	15	15	15	...	15
Exp. sfrb1	11	11	11	11	...	11
Exp. b0	-36	-34	-32	-30	...	36
Exp. b1	-20480	-19342	-18204	-17067	...	204

Test settings	
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±1,0000e+00
Tolerance b1	±1,0000e+00

Test statistics	
Min CPU cycles	1580
Max CPU cycles	2085
Avg CPU cycles	1901

Verification: PI FiP16 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for Control block PI.

Test results						
Time step	1	2	3	4	...	201
CPU cycles	67	67	67	135	...	123
Inputs						
In (DSP)	0	0	0	0	...	0
Init (DSP)	3604	3604	3604	3604	...	3604
Enable (DSP)	0	0	0	1	...	1
In	0	0	0	0	...	0
Init	0.11	0.11	0.11	0.11	...	0.11
Enable	0	0	0	1	...	1
Parameters						
Kp	2					
Ki	2500					
initHandling	initialize integral					
ts_fact	1					
Outputs						
Out	0	0	0	0.11	...	-0.528
Exp. Out	0	0	0	0.11	...	-0.528
Out (DSP)	0	0	0	3604	...	-17292
Exp. Out (DSP)	0	0	0	3604	...	-17285

Test settings	
Tolerance Out	±3,0518e-04 (±10 LSB)

Test statistics	
Min CPU cycles	67
Max CPU cycles	183
Avg CPU cycles	115

Test case: Conversion test OK

Conversion test for Control block PI.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kp	-10	-9.444	-8.889	-8.333	...	10
Ki	-11	-10.389	-9.778	-9.167	...	11
initHandling	initialize integral	initialize integral	initialize integral	initialize integral	...	initialize
ts_fact	1	1	1	1	...	1
Controller parameters						
initHandling	0	0	0	0	...	1
sfrb0	15	15	15	15	...	15
sfrb1	11	11	11	11	...	11
b0	-36	-34	-32	-30	...	36
b1	-20480	-19342	-18204	-17067	...	204
Exp. initHandling	0	0	0	0	...	1
Exp. sfrb0	15	15	15	15	...	15
Exp. sfrb1	11	11	11	11	...	11
Exp. b0	-36	-34	-32	-30	...	36
Exp. b1	-20480	-19342	-18204	-17067	...	204

Test settings	
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block PI.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kp	-10	-9.444	-8.889	-8.333	...	10
Ki	-11	-10.389	-9.778	-9.167	...	11
initHandling	initialize integral	initialize integral	initialize integral	initialize integral	...	initialize
ts_fact	1	1	1	1	...	1
Controller parameters						
initHandling	0	0	0	0	...	1
sfrb0	15	15	15	15	...	15
sfrb1	11	11	11	11	...	11
b0	-36	-34	-32	-30	...	36
b1	-20480	-19342	-18204	-17066	...	204
Exp. initHandling	0	0	0	0	...	1
Exp. sfrb0	15	15	15	15	...	15
Exp. sfrb1	11	11	11	11	...	11
Exp. b0	-36	-34	-32	-30	...	36
Exp. b1	-20480	-19342	-18204	-17067	...	204

Test settings	
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±1,0000e+00
Tolerance b1	±1,0000e+00

Test statistics	
Min CPU cycles	4005
Max CPU cycles	7385
Avg CPU cycles	6391

Verification: PI FiP16 CPU PIC32MX170F256

Date of Test 2026-06-19

Target controller PIC32MX170F256

Test case: Inport test OK

Inport test for Control block PI.

Test results						
Time step	1	2	3	4	...	201
CPU cycles	31	31	31	83	...	74
Inputs						
In (DSP)	0	0	0	0	...	0
Init (DSP)	3604	3604	3604	3604	...	3604
Enable (DSP)	0	0	0	1	...	1
In	0	0	0	0	...	0
Init	0.11	0.11	0.11	0.11	...	0.11
Enable	0	0	0	1	...	1
Parameters						
Kp	2					
Ki	2500					
initHandling	initialize integral					
ts_fact	1					
Outputs						
Out	0	0	0	0.11	...	-0.528
Exp. Out	0	0	0	0.11	...	-0.528
Out (DSP)	0	0	0	3604	...	-17292
Exp. Out (DSP)	0	0	0	3604	...	-17285

Test settings	
Tolerance Out	±3,0518e-04 (±10 LSB)

Test statistics	
Min CPU cycles	31
Max CPU cycles	83
Avg CPU cycles	69

Test case: Conversion test OK

Conversion test for Control block PI.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kp	-10	-9.444	-8.889	-8.333	...	10
Ki	-11	-10.389	-9.778	-9.167	...	11
initHandling	initialize integral	initialize integral	initialize integral	initialize integral	...	initialize
ts_fact	1	1	1	1	...	1
Controller parameters						
initHandling	0	0	0	0	...	1
sfrb0	15	15	15	15	...	15
sfrb1	11	11	11	11	...	11
b0	-36	-34	-32	-30	...	36
b1	-20480	-19342	-18204	-17067	...	204
Exp. initHandling	0	0	0	0	...	1
Exp. sfrb0	15	15	15	15	...	15
Exp. sfrb1	11	11	11	11	...	11
Exp. b0	-36	-34	-32	-30	...	36
Exp. b1	-20480	-19342	-18204	-17067	...	204

Test settings	
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block PI.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kp	-10	-9.444	-8.889	-8.333	...	10
Ki	-11	-10.389	-9.778	-9.167	...	11
initHandling	initialize integral	initialize integral	initialize integral	initialize integral	...	initialize
ts_fact	1	1	1	1	...	1
Controller parameters						
initHandling	0	0	0	0	...	1
sfrb0	15	15	15	15	...	15
sfrb1	11	11	11	11	...	11
b0	-36	-34	-32	-30	...	36
b1	-20480	-19342	-18204	-17066	...	204
Exp. initHandling	0	0	0	0	...	1
Exp. sfrb0	15	15	15	15	...	15
Exp. sfrb1	11	11	11	11	...	11
Exp. b0	-36	-34	-32	-30	...	36
Exp. b1	-20480	-19342	-18204	-17067	...	204

Test settings	
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±1,0000e+00
Tolerance b1	±1,0000e+00

Test statistics	
Min CPU cycles	1749
Max CPU cycles	3034
Avg CPU cycles	2632

Verification: PI FiP16 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for Control block PI.

Test results						
Time step	1	2	3	4	...	201
CPU cycles	78	59	59	122	...	98
Inputs						
In (DSP)	0	0	0	0	...	0
Init (DSP)	3604	3604	3604	3604	...	3604
Enable (DSP)	0	0	0	1	...	1
In	0	0	0	0	...	0
Init	0.11	0.11	0.11	0.11	...	0.11
Enable	0	0	0	1	...	1
Parameters						
Kp	2					
Ki	2500					
initHandling	initialize integral					
ts_fact	1					
Outputs						
Out	0	0	0	0.11	...	-0.528
Exp. Out	0	0	0	0.11	...	-0.528
Out (DSP)	0	0	0	3604	...	-17292
Exp. Out (DSP)	0	0	0	3604	...	-17285

Test settings	
Tolerance Out	±3,0518e-04 (±10 LSB)

Test statistics	
Min CPU cycles	59
Max CPU cycles	122
Avg CPU cycles	95

Test case: Conversion test OK

Conversion test for Control block PI.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kp	-10	-9.444	-8.889	-8.333	...	10
Ki	-11	-10.389	-9.778	-9.167	...	11
initHandling	initialize integral	initialize integral	initialize integral	initialize integral	...	initialize
ts_fact	1	1	1	1	...	1
Controller parameters						
initHandling	0	0	0	0	...	1
sfrb0	15	15	15	15	...	15
sfrb1	11	11	11	11	...	11
b0	-36	-34	-32	-30	...	36
b1	-20480	-19342	-18204	-17067	...	204
Exp. initHandling	0	0	0	0	...	1
Exp. sfrb0	15	15	15	15	...	15
Exp. sfrb1	11	11	11	11	...	11
Exp. b0	-36	-34	-32	-30	...	36
Exp. b1	-20480	-19342	-18204	-17067	...	204

Test settings	
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block PI.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kp	-10	-9.444	-8.889	-8.333	...	10
Ki	-11	-10.389	-9.778	-9.167	...	11
initHandling	initialize integral	initialize integral	initialize integral	initialize integral	...	initialize
ts_fact	1	1	1	1	...	1
Controller parameters						
initHandling	0	0	0	0	...	1
sfrb0	15	15	15	15	...	15
sfrb1	11	11	11	11	...	11
b0	-36	-34	-32	-30	...	36
b1	-20480	-19342	-18204	-17066	...	204
Exp. initHandling	0	0	0	0	...	1
Exp. sfrb0	15	15	15	15	...	15
Exp. sfrb1	11	11	11	11	...	11
Exp. b0	-36	-34	-32	-30	...	36
Exp. b1	-20480	-19342	-18204	-17067	...	204

Test settings	
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±1,0000e+00
Tolerance b1	±1,0000e+00

Test statistics	
Min CPU cycles	1375
Max CPU cycles	2015
Avg CPU cycles	1690

Verification: PI FiP16 CPU TMS320F28379D

Date of Test 2026-06-22

Target controller TMS320F28379D

Test case: Inport test OK

Inport test for Control block PI.

Test results						
Time step	1	2	3	4	...	201
CPU cycles	61	61	61	134	...	122
Inputs						
In (DSP)	0	0	0	0	...	0
Init (DSP)	3604	3604	3604	3604	...	3604
Enable (DSP)	0	0	0	1	...	1
In	0	0	0	0	...	0
Init	0.11	0.11	0.11	0.11	...	0.11
Enable	0	0	0	1	...	1
Parameters						
Kp	2					
Ki	2500					
initHandling	initialize integral					
ts_fact	1					
Outputs						
Out	0	0	0	0.11	...	-0.528
Exp. Out	0	0	0	0.11	...	-0.528
Out (DSP)	0	0	0	3604	...	-17292
Exp. Out (DSP)	0	0	0	3604	...	-17285

Test settings	
Tolerance Out	±3,0518e-04 (±10 LSB)

Test statistics	
Min CPU cycles	61
Max CPU cycles	134
Avg CPU cycles	119

Test case: Conversion test OK

Conversion test for Control block PI.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kp	-10	-9.444	-8.889	-8.333	...	10
Ki	-11	-10.389	-9.778	-9.167	...	11
initHandling	initialize integral	initialize integral	initialize integral	initialize integral	...	initialize
ts_fact	1	1	1	1	...	1
Controller parameters						
initHandling	0	0	0	0	...	1
sfrb0	15	15	15	15	...	15
sfrb1	11	11	11	11	...	11
b0	-36	-34	-32	-30	...	36
b1	-20480	-19342	-18204	-17067	...	204
Exp. initHandling	0	0	0	0	...	1
Exp. sfrb0	15	15	15	15	...	15
Exp. sfrb1	11	11	11	11	...	11
Exp. b0	-36	-34	-32	-30	...	36
Exp. b1	-20480	-19342	-18204	-17067	...	204

Test settings	
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block PI.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kp	-10	-9.444	-8.889	-8.333	...	10
Ki	-11	-10.389	-9.778	-9.167	...	11
initHandling	initialize integral	initialize integral	initialize integral	initialize integral	...	initialize
ts_fact	1	1	1	1	...	1
Controller parameters						
initHandling	0	0	0	0	...	1
sfrb0	15	15	15	15	...	15
sfrb1	11	11	11	11	...	11
b0	-36	-34	-32	-30	...	36
b1	-20480	-19342	-18204	-17066	...	204
Exp. initHandling	0	0	0	0	...	1
Exp. sfrb0	15	15	15	15	...	15
Exp. sfrb1	11	11	11	11	...	11
Exp. b0	-36	-34	-32	-30	...	36
Exp. b1	-20480	-19342	-18204	-17067	...	204

Test settings	
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±1,0000e+00
Tolerance b1	±1,0000e+00

Test statistics	
Min CPU cycles	2308
Max CPU cycles	4073
Avg CPU cycles	3473

Verification: PI FiP16 CPU dsPIC33EP256MC502

Date of Test 2026-06-23

Target controller dsPIC33EP256MC502

Test case: Inport test OK

Inport test for Control block PI.

Test results						
Time step	1	2	3	4	...	201
CPU cycles	47	47	47	126	...	126
Inputs						
In (DSP)	0	0	0	0	...	0
Init (DSP)	3604	3604	3604	3604	...	3604
Enable (DSP)	0	0	0	1	...	1
In	0	0	0	0	...	0
Init	0.11	0.11	0.11	0.11	...	0.11
Enable	0	0	0	1	...	1
Parameters						
Kp	2					
Ki	2500					
initHandling	initialize integral					
ts_fact	1					
Outputs						
Out	0	0	0	0.11	...	-0.528
Exp. Out	0	0	0	0.11	...	-0.528
Out (DSP)	0	0	0	3604	...	-17292
Exp. Out (DSP)	0	0	0	3604	...	-17285

Test settings	
Tolerance Out	±3,0518e-04 (±10 LSB)

Test statistics	
Min CPU cycles	47
Max CPU cycles	126
Avg CPU cycles	116

Test case: Conversion test OK

Conversion test for Control block PI.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kp	-10	-9.444	-8.889	-8.333	...	10
Ki	-11	-10.389	-9.778	-9.167	...	11
initHandling	initialize integral	initialize integral	initialize integral	initialize integral	...	initialize
ts_fact	1	1	1	1	...	1
Controller parameters						
initHandling	0	0	0	0	...	1
sfrb0	15	15	15	15	...	15
sfrb1	11	11	11	11	...	11
b0	-36	-34	-32	-30	...	36
b1	-20480	-19342	-18204	-17067	...	204
Exp. initHandling	0	0	0	0	...	1
Exp. sfrb0	15	15	15	15	...	15
Exp. sfrb1	11	11	11	11	...	11
Exp. b0	-36	-34	-32	-30	...	36
Exp. b1	-20480	-19342	-18204	-17067	...	204

Test settings	
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block PI.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kp	-10	-9.444	-8.889	-8.333	...	10
Ki	-11	-10.389	-9.778	-9.167	...	11
initHandling	initialize integral	initialize integral	initialize integral	initialize integral	...	initialize
ts_fact	1	1	1	1	...	1
Controller parameters						
initHandling	0	0	0	0	...	1
sfrb0	15	15	15	15	...	15
sfrb1	11	11	11	11	...	11
b0	-36	-34	-32	-30	...	36
b1	-20480	-19342	-18204	-17066	...	204
Exp. initHandling	0	0	0	0	...	1
Exp. sfrb0	15	15	15	15	...	15
Exp. sfrb1	11	11	11	11	...	11
Exp. b0	-36	-34	-32	-30	...	36
Exp. b1	-20480	-19342	-18204	-17067	...	204

Test settings	
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±1,0000e+00
Tolerance b1	±1,0000e+00

Test statistics	
Min CPU cycles	6441
Max CPU cycles	15553
Avg CPU cycles	12970

Verification: PI FiP32 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for Control block PI.

Test results				
Time step	1	2	...	201
CPU cycles	86	86	...	254
Inputs				
In (DSP)	0	0	...	0
Init (DSP)	236223201	236223201	...	236223201
Enable (DSP)	0	0	...	1
In	0	0	...	0
Init	0.11	0.11	...	0.11
Enable	0	0	...	1
Parameters				
Kp	2			
Ki	2500			
initHandling	initialize integral			
ts_fact	1			
Outputs				
Out	0	0	...	-0.528
Exp. Out	0	0	...	-0.528
Out (DSP)	0	0	...	-1132797631
Exp. Out (DSP)	0	0	...	-1132797631

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	86
Max CPU cycles	269
Avg CPU cycles	238

Test case: Conversion test OK

Conversion test for Control block PI.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
initHandling	0	0	...	1
sfrb0	31	31	...	31
sfrb1	27	27	...	27
b0	-2362232	-2230997	...	2362232
b1	-1342177280	-1267611876	...	1342177280
Exp. initHandling	0	0	...	1
Exp. sfrb0	31	31	...	31
Exp. sfrb1	27	27	...	27
Exp. b0	-2362232	-2230997	...	2362232
Exp. b1	-1342177280	-1267611876	...	1342177280

Test settings	
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block PI.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
initHandling	0	0	...	1
sfrb0	31	31	...	31
sfrb1	27	27	...	27
b0	-2362232	-2230997	...	2362232
b1	-1342177280	-1267611904	...	1342177280
Exp. initHandling	0	0	...	1
Exp. sfrb0	31	31	...	31
Exp. sfrb1	27	27	...	27
Exp. b0	-2362232	-2230997	...	2362232
Exp. b1	-1342177280	-1267611876	...	1342177280

Test settings	
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±1,0000e+02
Tolerance b1	±1,0000e+02

Test statistics	
Min CPU cycles	3436
Max CPU cycles	5782
Avg CPU cycles	5011

Verification: PI FiP32 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for Control block PI.

Test results				
Time step	1	2	...	201
CPU cycles	59	59	...	167
Inputs				
In (DSP)	0	0	...	0
Init (DSP)	236223201	236223201	...	236223201
Enable (DSP)	0	0	...	1
In	0	0	...	0
Init	0.11	0.11	...	0.11
Enable	0	0	...	1
Parameters				
Kp	2			
Ki	2500			
initHandling	initialize integral			
ts_fact	1			
Outputs				
Out	0	0	...	-0.528
Exp. Out	0	0	...	-0.528
Out (DSP)	0	0	...	-1132797631
Exp. Out (DSP)	0	0	...	-1132797631

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	59
Max CPU cycles	179
Avg CPU cycles	155

Test case: Conversion test OK

Conversion test for Control block PI.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
initHandling	0	0	...	1
sfrb0	31	31	...	31
sfrb1	27	27	...	27
b0	-2362232	-2230997	...	2362232
b1	-1342177280	-1267611876	...	1342177280
Exp. initHandling	0	0	...	1
Exp. sfrb0	31	31	...	31
Exp. sfrb1	27	27	...	27
Exp. b0	-2362232	-2230997	...	2362232
Exp. b1	-1342177280	-1267611876	...	1342177280

Test settings	
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block PI.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
initHandling	0	0	...	1
sfrb0	31	31	...	31
sfrb1	27	27	...	27
b0	-2362232	-2230997	...	2362232
b1	-1342177280	-1267611904	...	1342177280
Exp. initHandling	0	0	...	1
Exp. sfrb0	31	31	...	31
Exp. sfrb1	27	27	...	27
Exp. b0	-2362232	-2230997	...	2362232
Exp. b1	-1342177280	-1267611876	...	1342177280

Test settings	
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±1,0000e+02
Tolerance b1	±1,0000e+02

Test statistics	
Min CPU cycles	1461
Max CPU cycles	2455
Avg CPU cycles	2147

Verification: PI FiP32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for Control block PI.

Test results				
Time step	1	2	...	201
CPU cycles	83	83	...	199
Inputs				
In (DSP)	0	0	...	0
Init (DSP)	236223201	236223201	...	236223201
Enable (DSP)	0	0	...	1
In	0	0	...	0
Init	0.11	0.11	...	0.11
Enable	0	0	...	1
Parameters				
Kp	2			
Ki	2500			
initHandling	initialize integral			
ts_fact	1			
Outputs				
Out	0	0	...	-0.528
Exp. Out	0	0	...	-0.528
Out (DSP)	0	0	...	-1132797631
Exp. Out (DSP)	0	0	...	-1132797631

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	83
Max CPU cycles	212
Avg CPU cycles	179

Test case: Conversion test OK

Conversion test for Control block PI.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
initHandling	0	0	...	1
sfrb0	31	31	...	31
sfrb1	27	27	...	27
b0	-2362232	-2230997	...	2362232
b1	-1342177280	-1267611876	...	1342177280
Exp. initHandling	0	0	...	1
Exp. sfrb0	31	31	...	31
Exp. sfrb1	27	27	...	27
Exp. b0	-2362232	-2230997	...	2362232
Exp. b1	-1342177280	-1267611876	...	1342177280

Test settings	
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block PI.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
initHandling	0	0	...	1
sfrb0	31	31	...	31
sfrb1	27	27	...	27
b0	-2362232	-2230997	...	2362232
b1	-1342177280	-1267611904	...	1342177280
Exp. initHandling	0	0	...	1
Exp. sfrb0	31	31	...	31
Exp. sfrb1	27	27	...	27
Exp. b0	-2362232	-2230997	...	2362232
Exp. b1	-1342177280	-1267611876	...	1342177280

Test settings	
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±1,0000e+02
Tolerance b1	±1,0000e+02

Test statistics	
Min CPU cycles	2164
Max CPU cycles	2783
Avg CPU cycles	2521

Verification: PI FiP32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for Control block PI.

Test results				
Time step	1	2	...	201
CPU cycles	86	86	...	337
Inputs				
In (DSP)	0	0	...	0
Init (DSP)	236223201	236223201	...	236223201
Enable (DSP)	0	0	...	1
In	0	0	...	0
Init	0.11	0.11	...	0.11
Enable	0	0	...	1
Parameters				
Kp	2			
Ki	2500			
initHandling	initialize integral			
ts_fact	1			
Outputs				
Out	0	0	...	-0.528
Exp. Out	0	0	...	-0.528
Out (DSP)	0	0	...	-1132797631
Exp. Out (DSP)	0	0	...	-1132797631

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	86
Max CPU cycles	349
Avg CPU cycles	302

Test case: Conversion test OK

Conversion test for Control block PI.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
initHandling	0	0	...	1
sfrb0	31	31	...	31
sfrb1	27	27	...	27
b0	-2362232	-2230997	...	2362232
b1	-1342177280	-1267611876	...	1342177280
Exp. initHandling	0	0	...	1
Exp. sfrb0	31	31	...	31
Exp. sfrb1	27	27	...	27
Exp. b0	-2362232	-2230997	...	2362232
Exp. b1	-1342177280	-1267611876	...	1342177280

Test settings	
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block PI.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
initHandling	0	0	...	1
sfrb0	31	31	...	31
sfrb1	27	27	...	27
b0	-2362232	-2230997	...	2362232
b1	-1342177280	-1267611904	...	1342177280
Exp. initHandling	0	0	...	1
Exp. sfrb0	31	31	...	31
Exp. sfrb1	27	27	...	27
Exp. b0	-2362232	-2230997	...	2362232
Exp. b1	-1342177280	-1267611876	...	1342177280

Test settings	
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±1,0000e+02
Tolerance b1	±1,0000e+02

Test statistics	
Min CPU cycles	6085
Max CPU cycles	9969
Avg CPU cycles	8937

Verification: PI FiP32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for Control block PI.

Test results				
Time step	1	2	...	201
CPU cycles	31	31	...	118
Inputs				
In (DSP)	0	0	...	0
Init (DSP)	236223201	236223201	...	236223201
Enable (DSP)	0	0	...	1
In	0	0	...	0
Init	0.11	0.11	...	0.11
Enable	0	0	...	1
Parameters				
Kp	2			
Ki	2500			
initHandling	initialize integral			
ts_fact	1			
Outputs				
Out	0	0	...	-0.528
Exp. Out	0	0	...	-0.528
Out (DSP)	0	0	...	-1132797631
Exp. Out (DSP)	0	0	...	-1132797631

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	31
Max CPU cycles	125
Avg CPU cycles	106

Test case: Conversion test OK

Conversion test for Control block PI.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
initHandling	0	0	...	1
sfrb0	31	31	...	31
sfrb1	27	27	...	27
b0	-2362232	-2230997	...	2362232
b1	-1342177280	-1267611876	...	1342177280
Exp. initHandling	0	0	...	1
Exp. sfrb0	31	31	...	31
Exp. sfrb1	27	27	...	27
Exp. b0	-2362232	-2230997	...	2362232
Exp. b1	-1342177280	-1267611876	...	1342177280

Test settings	
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block PI.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
initHandling	0	0	...	1
sfrb0	31	31	...	31
sfrb1	27	27	...	27
b0	-2362232	-2230997	...	2362232
b1	-1342177280	-1267611904	...	1342177280
Exp. initHandling	0	0	...	1
Exp. sfrb0	31	31	...	31
Exp. sfrb1	27	27	...	27
Exp. b0	-2362232	-2230997	...	2362232
Exp. b1	-1342177280	-1267611876	...	1342177280

Test settings	
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±1,0000e+02
Tolerance b1	±1,0000e+02

Test statistics	
Min CPU cycles	2658
Max CPU cycles	4035
Avg CPU cycles	3626

Verification: PI FiP32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for Control block PI.

Test results				
Time step	1	2	...	201
CPU cycles	82	59	...	151
Inputs				
In (DSP)	0	0	...	0
Init (DSP)	236223201	236223201	...	236223201
Enable (DSP)	0	0	...	1
In	0	0	...	0
Init	0.11	0.11	...	0.11
Enable	0	0	...	1
Parameters				
Kp	2			
Ki	2500			
initHandling	initialize integral			
ts_fact	1			
Outputs				
Out	0	0	...	-0.528
Exp. Out	0	0	...	-0.528
Out (DSP)	0	0	...	-1132797631
Exp. Out (DSP)	0	0	...	-1132797631

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	59
Max CPU cycles	191
Avg CPU cycles	142

Test case: Conversion test OK

Conversion test for Control block PI.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
initHandling	0	0	...	1
sfrb0	31	31	...	31
sfrb1	27	27	...	27
b0	-2362232	-2230997	...	2362232
b1	-1342177280	-1267611876	...	1342177280
Exp. initHandling	0	0	...	1
Exp. sfrb0	31	31	...	31
Exp. sfrb1	27	27	...	27
Exp. b0	-2362232	-2230997	...	2362232
Exp. b1	-1342177280	-1267611876	...	1342177280

Test settings	
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block PI.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
initHandling	0	0	...	1
sfrb0	31	31	...	31
sfrb1	27	27	...	27
b0	-2362232	-2230997	...	2362232
b1	-1342177280	-1267611904	...	1342177280
Exp. initHandling	0	0	...	1
Exp. sfrb0	31	31	...	31
Exp. sfrb1	27	27	...	27
Exp. b0	-2362232	-2230997	...	2362232
Exp. b1	-1342177280	-1267611876	...	1342177280

Test settings	
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±1,0000e+02
Tolerance b1	±1,0000e+02

Test statistics	
Min CPU cycles	1823
Max CPU cycles	2619
Avg CPU cycles	2176

Verification: PI FiP32 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for Control block PI.

Test results				
Time step	1	2	...	201
CPU cycles	67	67	...	216
Inputs				
In (DSP)	0	0	...	0
Init (DSP)	236223201	236223201	...	236223201
Enable (DSP)	0	0	...	1
In	0	0	...	0
Init	0.11	0.11	...	0.11
Enable	0	0	...	1
Parameters				
Kp	2			
Ki	2500			
initHandling	initialize integral			
ts_fact	1			
Outputs				
Out	0	0	...	-0.528
Exp. Out	0	0	...	-0.528
Out (DSP)	0	0	...	-1132797631
Exp. Out (DSP)	0	0	...	-1132797631

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	67
Max CPU cycles	231
Avg CPU cycles	206

Test case: Conversion test OK

Conversion test for Control block PI.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
initHandling	0	0	...	1
sfrb0	31	31	...	31
sfrb1	27	27	...	27
b0	-2362232	-2230997	...	2362232
b1	-1342177280	-1267611876	...	1342177280
Exp. initHandling	0	0	...	1
Exp. sfrb0	31	31	...	31
Exp. sfrb1	27	27	...	27
Exp. b0	-2362232	-2230997	...	2362232
Exp. b1	-1342177280	-1267611876	...	1342177280

Test settings	
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block PI.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
initHandling	0	0	...	1
sfrb0	31	31	...	31
sfrb1	27	27	...	27
b0	-2362232	-2230997	...	2362232
b1	-1342177280	-1267611904	...	1342177280
Exp. initHandling	0	0	...	1
Exp. sfrb0	31	31	...	31
Exp. sfrb1	27	27	...	27
Exp. b0	-2362232	-2230997	...	2362232
Exp. b1	-1342177280	-1267611876	...	1342177280

Test settings	
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±1,0000e+02
Tolerance b1	±1,0000e+02

Test statistics	
Min CPU cycles	2499
Max CPU cycles	4355
Avg CPU cycles	3741

Verification: PI FiP32 CPU dsPIC33EP256MC502

Date of Test	2026-06-23
Target controller	dsPIC33EP256MC502

Test case: Inport test

OK

Inport test for Control block PI.

Test results				
Time step	1	2	...	201
CPU cycles	64	64	...	647
Inputs				
In (DSP)	0	0	...	0
Init (DSP)	236223201	236223201	...	236223201
Enable (DSP)	0	0	...	1
In	0	0	...	0
Init	0.11	0.11	...	0.11
Enable	0	0	...	1
Parameters				
Kp	2			
Ki	2500			
initHandling	initialize integral			
ts_fact	1			
Outputs				
Out	0	0	...	-0.528
Exp. Out	0	0	...	-0.528
Out (DSP)	0	0	...	-1132797631
Exp. Out (DSP)	0	0	...	-1132797631

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	64
Max CPU cycles	666
Avg CPU cycles	604

Test case: Conversion test

OK

Conversion test for Control block PI.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
initHandling	0	0	...	1
sfrb0	31	31	...	31
sfrb1	27	27	...	27
b0	-2362232	-2230997	...	2362232
b1	-1342177280	-1267611876	...	1342177280
Exp. initHandling	0	0	...	1
Exp. sfrb0	31	31	...	31
Exp. sfrb1	27	27	...	27
Exp. b0	-2362232	-2230997	...	2362232
Exp. b1	-1342177280	-1267611876	...	1342177280

Test settings	
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block PI.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
initHandling	0	0	...	1
sfrb0	31	31	...	31
sfrb1	27	27	...	27
b0	-2362232	-2230997	...	2362232
b1	-1342177280	-1267611904	...	1342177280
Exp. initHandling	0	0	...	1
Exp. sfrb0	31	31	...	31
Exp. sfrb1	27	27	...	27
Exp. b0	-2362232	-2230997	...	2362232
Exp. b1	-1342177280	-1267611876	...	1342177280

Test settings	
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±1,0000e+02
Tolerance b1	±1,0000e+02

Test statistics	
Min CPU cycles	7253
Max CPU cycles	15987
Avg CPU cycles	13506

Verification: PI Float32 CPU TMS320F28335

Date of Test 2026-06-19

Target controller TMS320F28335

Test case: Inport test OK

Inport test for Control block PI.

Test results				
Time step	1	2	...	201
CPU cycles	71	71	...	117
Inputs				
In (DSP)	0	0	...	0
Init (DSP)	0.11	0.11	...	0.11
Enable (DSP)	0	0	...	1
In	0	0	...	0
Init	0.11	0.11	...	0.11
Enable	0	0	...	1
Parameters				
Kp	2			
Ki	2500			
initHandling	initialize integral			
ts_fact	1			
Outputs				
Out	0	0	...	-1.84
Exp. Out	0	0	...	-1.84
Out (DSP)	0	0	...	-1.84
Exp. Out (DSP)	0	0	...	-1.84

Test settings	
Tolerance Out	±9,3132e-07 (±2000 LSB)

Test statistics	
Min CPU cycles	71
Max CPU cycles	132
Avg CPU cycles	116

Test case: Conversion test OK

Conversion test for Control block PI.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
initHandling	0	0	...	1
b0	-0.001	-0.001	...	0.001
b1	-10	-9.444	...	10
Exp. initHandling	0	0	...	1
Exp. b0	-0.001	-0.001	...	0.001
Exp. b1	-10	-9.444	...	10

Test settings	
Tolerance initHandling	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block PI.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
initHandling	0	0	...	1
b0	-0.001	-0.001	...	0.001
b1	-10	-9.444	...	10
Exp. initHandling	0	0	...	1
Exp. b0	-0.001	-0.001	...	0.001
Exp. b1	-10	-9.444	...	10

Test settings	
Tolerance initHandling	±0,0000e+00
Tolerance b0	±1,0000e-10
Tolerance b1	±1,0000e-06

Test statistics	
Min CPU cycles	1914
Max CPU cycles	1936
Avg CPU cycles	1914

Verification: PI Float32 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test — OK

Inport test for Control block PI.

Test results				
Time step	1	2	...	201
CPU cycles	41	41	...	87
Inputs				
In (DSP)	0	0	...	0
Init (DSP)	0.11	0.11	...	0.11
Enable (DSP)	0	0	...	1
In	0	0	...	0
Init	0.11	0.11	...	0.11
Enable	0	0	...	1
Parameters				
Kp	2			
Ki	2500			
initHandling	initialize integral			
ts_fact	1			
Outputs				
Out	0	0	...	-1.84
Exp. Out	0	0	...	-1.84
Out (DSP)	0	0	...	-1.84
Exp. Out (DSP)	0	0	...	-1.84

Test settings	
Tolerance Out	±9,3132e-07 (±2000 LSB)

Test statistics	
Min CPU cycles	41
Max CPU cycles	101
Avg CPU cycles	86

Test case: Conversion test — OK

Conversion test for Control block PI.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
initHandling	0	0	...	1
b0	-0.001	-0.001	...	0.001
b1	-10	-9.444	...	10
Exp. initHandling	0	0	...	1
Exp. b0	-0.001	-0.001	...	0.001
Exp. b1	-10	-9.444	...	10

Test settings	
Tolerance initHandling	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block PI.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
initHandling	0	0	...	1
b0	-0.001	-0.001	...	0.001
b1	-10	-9.444	...	10
Exp. initHandling	0	0	...	1
Exp. b0	-0.001	-0.001	...	0.001
Exp. b1	-10	-9.444	...	10

Test settings	
Tolerance initHandling	±0,0000e+00
Tolerance b0	±1,0000e-10
Tolerance b1	±1,0000e-06

Test statistics	
Min CPU cycles	903
Max CPU cycles	903
Avg CPU cycles	903

Verification: PI Float32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for Control block PI.

Test results				
Time step	1	2	...	201
CPU cycles	81	81	...	133
Inputs				
In (DSP)	0	0	...	0
Init (DSP)	0.11	0.11	...	0.11
Enable (DSP)	0	0	...	1
In	0	0	...	0
Init	0.11	0.11	...	0.11
Enable	0	0	...	1
Parameters				
Kp	2			
Ki	2500			
initHandling	initialize integral			
ts_fact	1			
Outputs				
Out	0	0	...	-1.84
Exp. Out	0	0	...	-1.84
Out (DSP)	0	0	...	-1.84
Exp. Out (DSP)	0	0	...	-1.84

Test settings	
Tolerance Out	±9,3132e-07 (±2000 LSB)

Test statistics	
Min CPU cycles	81
Max CPU cycles	148
Avg CPU cycles	132

Test case: Conversion test OK

Conversion test for Control block PI.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
initHandling	0	0	...	1
b0	-0.001	-0.001	...	0.001
b1	-10	-9.444	...	10
Exp. initHandling	0	0	...	1
Exp. b0	-0.001	-0.001	...	0.001
Exp. b1	-10	-9.444	...	10

Test settings	
Tolerance initHandling	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block PI.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
initHandling	0	0	...	1
b0	-0.001	-0.001	...	0.001
b1	-10	-9.444	...	10
Exp. initHandling	0	0	...	1
Exp. b0	-0.001	-0.001	...	0.001
Exp. b1	-10	-9.444	...	10

Test settings	
Tolerance initHandling	±0,0000e+00
Tolerance b0	±1,0000e-10
Tolerance b1	±1,0000e-06

Test statistics	
Min CPU cycles	916
Max CPU cycles	921
Avg CPU cycles	916

Verification: PI Float32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for Control block PI.

Test results				
Time step	1	2	...	201
CPU cycles	81	81	...	676
Inputs				
In (DSP)	0	0	...	0
Init (DSP)	0.11	0.11	...	0.11
Enable (DSP)	0	0	...	1
In	0	0	...	0
Init	0.11	0.11	...	0.11
Enable	0	0	...	1
Parameters				
Kp	2			
Ki	2500			
initHandling	initialize integral			
ts_fact	1			
Outputs				
Out	0	0	...	-1.84
Exp. Out	0	0	...	-1.84
Out (DSP)	0	0	...	-1.84
Exp. Out (DSP)	0	0	...	-1.84

Test settings	
Tolerance Out	±9,3132e-07 (±2000 LSB)

Test statistics	
Min CPU cycles	81
Max CPU cycles	958
Avg CPU cycles	818

Test case: Conversion test OK

Conversion test for Control block PI.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
initHandling	0	0	...	1
b0	-0.001	-0.001	...	0.001
b1	-10	-9.444	...	10
Exp. initHandling	0	0	...	1
Exp. b0	-0.001	-0.001	...	0.001
Exp. b1	-10	-9.444	...	10

Test settings	
Tolerance initHandling	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block PI.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
initHandling	0	0	...	1
b0	-0.001	-0.001	...	0.001
b1	-10	-9.444	...	10
Exp. initHandling	0	0	...	1
Exp. b0	-0.001	-0.001	...	0.001
Exp. b1	-10	-9.444	...	10

Test settings	
Tolerance initHandling	±0,0000e+00
Tolerance b0	±1,0000e-10
Tolerance b1	±1,0000e-06

Test statistics	
Min CPU cycles	2059
Max CPU cycles	2234
Avg CPU cycles	2170

Verification: PI Float32 CPU PIC32MX170F256

Date of Test 2026-06-19

Target controller PIC32MX170F256

Test case: Inport test OK

Inport test for Control block PI.

Test results				
Time step	1	2	...	201
CPU cycles	65	65	...	288
Inputs				
In (DSP)	0	0	...	0
Init (DSP)	0.11	0.11	...	0.11
Enable (DSP)	0	0	...	1
In	0	0	...	0
Init	0.11	0.11	...	0.11
Enable	0	0	...	1
Parameters				
Kp	2			
Ki	2500			
initHandling	initialize integral			
ts_fact	1			
Outputs				
Out	0	0	...	-1.84
Exp. Out	0	0	...	-1.84
Out (DSP)	0	0	...	-1.84
Exp. Out (DSP)	0	0	...	-1.84

Test settings	
Tolerance Out	±9,3132e-07 (±2000 LSB)

Test statistics	
Min CPU cycles	65
Max CPU cycles	386
Avg CPU cycles	346

Test case: Conversion test OK

Conversion test for Control block PI.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
initHandling	0	0	...	1
b0	-0.001	-0.001	...	0.001
b1	-10	-9.444	...	10
Exp. initHandling	0	0	...	1
Exp. b0	-0.001	-0.001	...	0.001
Exp. b1	-10	-9.444	...	10

Test settings	
Tolerance initHandling	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block PI.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
initHandling	0	0	...	1
b0	-0.001	-0.001	...	0.001
b1	-10	-9.444	...	10
Exp. initHandling	0	0	...	1
Exp. b0	-0.001	-0.001	...	0.001
Exp. b1	-10	-9.444	...	10

Test settings	
Tolerance initHandling	±0,0000e+00
Tolerance b0	±1,0000e-10
Tolerance b1	±1,0000e-06

Test statistics	
Min CPU cycles	742
Max CPU cycles	761
Avg CPU cycles	758

Verification: PI Float32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for Control block PI.

Test results				
Time step	1	2	...	201
CPU cycles	81	60	...	104
Inputs				
In (DSP)	0	0	...	0
Init (DSP)	0.11	0.11	...	0.11
Enable (DSP)	0	0	...	1
In	0	0	...	0
Init	0.11	0.11	...	0.11
Enable	0	0	...	1
Parameters				
Kp	2			
Ki	2500			
initHandling	initialize integral			
ts_fact	1			
Outputs				
Out	0	0	...	-1.84
Exp. Out	0	0	...	-1.84
Out (DSP)	0	0	...	-1.84
Exp. Out (DSP)	0	0	...	-1.84

Test settings	
Tolerance Out	±9,3132e-07 (±2000 LSB)

Test statistics	
Min CPU cycles	60
Max CPU cycles	151
Avg CPU cycles	103

Test case: Conversion test OK

Conversion test for Control block PI.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
initHandling	0	0	...	1
b0	-0.001	-0.001	...	0.001
b1	-10	-9.444	...	10
Exp. initHandling	0	0	...	1
Exp. b0	-0.001	-0.001	...	0.001
Exp. b1	-10	-9.444	...	10

Test settings	
Tolerance initHandling	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block PI.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
initHandling	0	0	...	1
b0	-0.001	-0.001	...	0.001
b1	-10	-9.444	...	10
Exp. initHandling	0	0	...	1
Exp. b0	-0.001	-0.001	...	0.001
Exp. b1	-10	-9.444	...	10

Test settings	
Tolerance initHandling	±0,0000e+00
Tolerance b0	±1,0000e-10
Tolerance b1	±1,0000e-06

Test statistics	
Min CPU cycles	843
Max CPU cycles	989
Avg CPU cycles	848

Verification: PI Float32 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for Control block PI.

Test results				
Time step	1	2	...	201
CPU cycles	63	63	...	118
Inputs				
In (DSP)	0	0	...	0
Init (DSP)	0.11	0.11	...	0.11
Enable (DSP)	0	0	...	1
In	0	0	...	0
Init	0.11	0.11	...	0.11
Enable	0	0	...	1
Parameters				
Kp	2			
Ki	2500			
initHandling	initialize integral			
ts_fact	1			
Outputs				
Out	0	0	...	-1.84
Exp. Out	0	0	...	-1.84
Out (DSP)	0	0	...	-1.84
Exp. Out (DSP)	0	0	...	-1.84

Test settings	
Tolerance Out	±9,3132e-07 (±2000 LSB)

Test statistics	
Min CPU cycles	63
Max CPU cycles	137
Avg CPU cycles	117

Test case: Conversion test OK

Conversion test for Control block PI.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
initHandling	0	0	...	1
b0	-0.001	-0.001	...	0.001
b1	-10	-9.444	...	10
Exp. initHandling	0	0	...	1
Exp. b0	-0.001	-0.001	...	0.001
Exp. b1	-10	-9.444	...	10

Test settings	
Tolerance initHandling	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block PI.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
initHandling	0	0	...	1
b0	-0.001	-0.001	...	0.001
b1	-10	-9.444	...	10
Exp. initHandling	0	0	...	1
Exp. b0	-0.001	-0.001	...	0.001
Exp. b1	-10	-9.444	...	10

Test settings	
Tolerance initHandling	±0,0000e+00
Tolerance b0	±1,0000e-10
Tolerance b1	±1,0000e-06

Test statistics	
Min CPU cycles	1429
Max CPU cycles	1451
Avg CPU cycles	1429

Verification: PI Float32 CPU dsPIC33EP256MC502

Date of Test	2026-06-23
Target controller	dsPIC33EP256MC502

Test case: Inport test

OK

Inport test for Control block PI.

Test results				
Time step	1	2	...	201
CPU cycles	64	64	...	750
Inputs				
In (DSP)	0	0	...	0
Init (DSP)	0.11	0.11	...	0.11
Enable (DSP)	0	0	...	1
In	0	0	...	0
Init	0.11	0.11	...	0.11
Enable	0	0	...	1
Parameters				
Kp	2			
Ki	2500			
initHandling	initialize integral			
ts_fact	1			
Outputs				
Out	0	0	...	-1.84
Exp. Out	0	0	...	-1.84
Out (DSP)	0	0	...	-1.84
Exp. Out (DSP)	0	0	...	-1.84

Test settings	
Tolerance Out	±9,3132e-07 (±2000 LSB)

Test statistics	
Min CPU cycles	64
Max CPU cycles	1039
Avg CPU cycles	915

Test case: Conversion test

OK

Conversion test for Control block PI.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
initHandling	0	0	...	1
b0	-0.001	-0.001	...	0.001
b1	-10	-9.444	...	10
Exp. initHandling	0	0	...	1
Exp. b0	-0.001	-0.001	...	0.001
Exp. b1	-10	-9.444	...	10

Test settings	
Tolerance initHandling	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

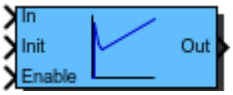
Conversion-on-Target test for Control block PI.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
initHandling	0	0	...	1
b0	-0.001	-0.001	...	0.001
b1	-10	-9.444	...	10
Exp. initHandling	0	0	...	1
Exp. b0	-0.001	-0.001	...	0.001
Exp. b1	-10	-9.444	...	10

Test settings	
Tolerance initHandling	±0,0000e+00
Tolerance b0	±1,0000e-10
Tolerance b1	±1,0000e-06

Test statistics	
Min CPU cycles	2488
Max CPU cycles	3225
Avg CPU cycles	3201

Block: PID



PID controller:
G(s) = Kp + Ki/s + Kd*s/(s/(2*pi*fc) + 1)

Inports	
In	Control error input
Init	Initial value of output Out when enabled
Enable	Enable == 0: Deactivation of block; Out set to 0 Enable 0->1: Preload of integral part Enable == 1: Activation of block

Outports	
Out	Control value

Mask Parameters		
Name	**ID**	**Description**
Kp	1	Proportional Factor
Ki	2	Integral Factor
Kd	3	Derivative Factor
fc	4	Cutoff frequency of realization low pass
initHandling	5	Determines what the signal provided on Init input is used for
ts_fact	6	Multiplication factor of base sampling time (in integer format)

Description:

Preloading Integral
A rising edge at the *Enable* inport enables the controller and preloads the integral.
One may choose from two options how to preload the integral value:

- Preload the integral from the *Init* inport.
- Preload the integral such that the first output of the controller matches the current value at the *Init* inport.
  This option allows controller switching without disturbing the control.

Note: Each fixed point implementation uses the next higher integer data type for the integral value storage variable.
Transfer function (zero-order hold discretization method):
When the block is enabled, the PID controller realizes the following transfer function:

$$G(z) = K_\mathrm{p} + K_\mathrm{i} T_\mathrm{s} \frac{1}{z-1} + K_\mathrm{d} 2\pi f_\mathrm{c} \frac{z-1}{z - e^{-2\pi f_\mathrm{c} T_\mathrm{s}}}$$

FiP8 bug: When using the TI compiler the step response of the derivative part does not return to zero, but generates an overflow at zero crossing if the derivative parameter value is too high.

Developer note: For the fixed point implementations the source code of block *PIDLimit* is used.

Implementations:

FiP8	8 Bit Fixed Point Implementation
FiP16	16 Bit Fixed Point Implementation
FiP32	32 Bit Fixed Point Implementation
Float32	32 Bit Floating Point Implementation
Float64	64 Bit Floating Point Implementation

Implementation: FiP8

8 Bit Fixed Point Implementation

Inports Data Type	
In	int8
Init	int8
Enable	bool

Outports Data Type	
Out	int8

Implementation: FiP16

16 Bit Fixed Point Implementation

Inports Data Type	
In	int16
Init	int16
Enable	bool

Outports Data Type	
Out	int16

Implementation: FiP32

32 Bit Fixed Point Implementation

Inports Data Type	
In	int32
Init	int32
Enable	bool

Outports Data Type	
Out	int32

Implementation: Float32

32 Bit Floating Point Implementation

Inports Data Type	
In	float32
Init	float32
Enable	bool

Outports Data Type	
Out	float32

Implementation: Float64

64 Bit Floating Point Implementation

Inports Data Type	
In	float64
Init	float64
Enable	bool

Outports Data Type	
Out	float64

Verification: PID FiP16 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for Control block PID.

Test results						
Time step	1	2	3	4	...	201
CPU cycles	80	80	80	165	...	175
Inputs						
In (DSP)	0	0	0	0	...	0
Init (DSP)	3604	3604	3604	3604	...	3604
Enable (DSP)	0	0	0	1	...	1
In	0	0	0	0	...	0
Init	0.11	0.11	0.11	0.11	...	0.11
Enable	0	0	0	1	...	1
Parameters						
Kp	2					
Ki	2500					
Kd	0.003					
fc	200					
initHandling	initialize integral					
ts_fact	1					
Outputs						
Out	0	0	0	0.11	...	-0.526
Exp. Out	0	0	0	0.11	...	-0.526
Out (DSP)	0	0	0	3604	...	-17231
Exp. Out (DSP)	0	0	0	3604	...	-17228

Test settings	
Tolerance Out	±3,0518e-04 (±10 LSB)

Test statistics	
Min CPU cycles	80
Max CPU cycles	175
Avg CPU cycles	171

Test case: Conversion test OK

Conversion test for Control block PID.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kp	-10	-9.444	-8.889	-8.333	...	10
Ki	-11	-10.389	-9.778	-9.167	...	11
Kd	-10	-9.444	-8.889	-8.333	...	10
fc	0	13.889	27.778	41.667	...	50
initHandling	initialize integral	initialize integral	initialize integral	initialize integral	...	initialize
ts_fact	1	1	1	1	...	1
Controller parameters						
sfrd	15	5	4	3	...	0
b1d	0	-26374	-24822	-17453	...	314
a0d	-32767	-32483	-32201	-31921	...	-239
b0d	0	26374	24822	17453	...	-314
initHandling	0	0	0	0	...	1
sfrb0	15	15	15	15	...	15
sfrb1	11	11	11	11	...	11
b0	-36	-34	-32	-30	...	36
b1	-20480	-19342	-18204	-17067	...	204
Exp. sfrd	15	5	4	3	...	0
Exp. b1d	0	-26374	-24822	-17453	...	314
Exp. a0d	-32767	-32483	-32201	-31921	...	-239
Exp. b0d	0	26374	24822	17453	...	-314
Exp. initHandling	0	0	0	0	...	1
Exp. sfrb0	15	15	15	15	...	15
Exp. sfrb1	11	11	11	11	...	11
Exp. b0	-36	-34	-32	-30	...	36
Exp. b1	-20480	-19342	-18204	-17067	...	204

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±0,0000e+00
Tolerance a0d	±0,0000e+00
Tolerance b0d	±0,0000e+00
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block PID.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kp	-10	-9.444	-8.889	-8.333	...	10
Ki	-11	-10.389	-9.778	-9.167	...	11
Kd	-10	-9.444	-8.889	-8.333	...	10
fc	0	13.889	27.778	41.667	...	50
initHandling	initialize integral	initialize integral	initialize integral	initialize integral	...	initialize
ts_fact	1	1	1	1	...	1
Controller parameters						
sfrd	15	5	4	3	...	0
b1d	0	-26373	-24822	-17453	...	314
a0d	-32767	-32483	-32201	-31921	...	-239
b0d	0	26373	24822	17453	...	-314
initHandling	0	0	0	0	...	1
sfrb0	15	15	15	15	...	15
sfrb1	11	11	11	11	...	11
b0	-36	-34	-32	-30	...	36
b1	-20480	-19342	-18204	-17066	...	204
Exp. sfrd	15	5	4	3	...	0
Exp. b1d	0	-26374	-24822	-17453	...	314
Exp. a0d	-32767	-32483	-32201	-31921	...	-239
Exp. b0d	0	26374	24822	17453	...	-314
Exp. initHandling	0	0	0	0	...	1
Exp. sfrb0	15	15	15	15	...	15
Exp. sfrb1	11	11	11	11	...	11
Exp. b0	-36	-34	-32	-30	...	36
Exp. b1	-20480	-19342	-18204	-17067	...	204

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±1,0000e+00
Tolerance a0d	±1,0000e+00
Tolerance b0d	±1,0000e+00
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±1,0000e+00
Tolerance b1	±1,0000e+00

Test statistics	
Min CPU cycles	5087
Max CPU cycles	14657
Avg CPU cycles	12746

Verification: PID FiP16 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for Control block PID.

Test results						
Time step	1	2	3	4	...	201
CPU cycles	57	57	57	117	...	125
Inputs						
In (DSP)	0	0	0	0	...	0
Init (DSP)	3604	3604	3604	3604	...	3604
Enable (DSP)	0	0	0	1	...	1
In	0	0	0	0	...	0
Init	0.11	0.11	0.11	0.11	...	0.11
Enable	0	0	0	1	...	1
Parameters						
Kp	2					
Ki	2500					
Kd	0.003					
fc	200					
initHandling	initialize integral					
ts_fact	1					
Outputs						
Out	0	0	0	0.11	...	-0.526
Exp. Out	0	0	0	0.11	...	-0.526
Out (DSP)	0	0	0	3604	...	-17231
Exp. Out (DSP)	0	0	0	3604	...	-17228

Test settings	
Tolerance Out	±3,0518e-04 (±10 LSB)

Test statistics	
Min CPU cycles	57
Max CPU cycles	125
Avg CPU cycles	121

Test case: Conversion test OK

Conversion test for Control block PID.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kp	-10	-9.444	-8.889	-8.333	...	10
Ki	-11	-10.389	-9.778	-9.167	...	11
Kd	-10	-9.444	-8.889	-8.333	...	10
fc	0	13.889	27.778	41.667	...	50
initHandling	initialize integral	initialize integral	initialize integral	initialize integral	...	initialize
ts_fact	1	1	1	1	...	1
Controller parameters						
sfrd	15	5	4	3	...	0
b1d	0	-26374	-24822	-17453	...	314
a0d	-32767	-32483	-32201	-31921	...	-239
b0d	0	26374	24822	17453	...	-314
initHandling	0	0	0	0	...	1
sfrb0	15	15	15	15	...	15
sfrb1	11	11	11	11	...	11
b0	-36	-34	-32	-30	...	36
b1	-20480	-19342	-18204	-17067	...	204
Exp. sfrd	15	5	4	3	...	0
Exp. b1d	0	-26374	-24822	-17453	...	314
Exp. a0d	-32767	-32483	-32201	-31921	...	-239
Exp. b0d	0	26374	24822	17453	...	-314
Exp. initHandling	0	0	0	0	...	1
Exp. sfrb0	15	15	15	15	...	15
Exp. sfrb1	11	11	11	11	...	11
Exp. b0	-36	-34	-32	-30	...	36
Exp. b1	-20480	-19342	-18204	-17067	...	204

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±0,0000e+00
Tolerance a0d	±0,0000e+00
Tolerance b0d	±0,0000e+00
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block PID.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kp	-10	-9.444	-8.889	-8.333	...	10
Ki	-11	-10.389	-9.778	-9.167	...	11
Kd	-10	-9.444	-8.889	-8.333	...	10
fc	0	13.889	27.778	41.667	...	50
initHandling	initialize integral	initialize integral	initialize integral	initialize integral	...	initialize
ts_fact	1	1	1	1	...	1
Controller parameters						
sfrd	15	5	4	3	...	0
b1d	0	-26373	-24822	-17453	...	314
a0d	-32767	-32483	-32201	-31921	...	-239
b0d	0	26373	24822	17453	...	-314
initHandling	0	0	0	0	...	1
sfrb0	15	15	15	15	...	15
sfrb1	11	11	11	11	...	11
b0	-36	-34	-32	-30	...	36
b1	-20480	-19342	-18204	-17066	...	204
Exp. sfrd	15	5	4	3	...	0
Exp. b1d	0	-26374	-24822	-17453	...	314
Exp. a0d	-32767	-32483	-32201	-31921	...	-239
Exp. b0d	0	26374	24822	17453	...	-314
Exp. initHandling	0	0	0	0	...	1
Exp. sfrb0	15	15	15	15	...	15
Exp. sfrb1	11	11	11	11	...	11
Exp. b0	-36	-34	-32	-30	...	36
Exp. b1	-20480	-19342	-18204	-17067	...	204

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±1,0000e+00
Tolerance a0d	±1,0000e+00
Tolerance b0d	±1,0000e+00
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±1,0000e+00
Tolerance b1	±1,0000e+00

Test statistics	
Min CPU cycles	2373
Max CPU cycles	8689
Avg CPU cycles	7188

Verification: PID FiP16 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for Control block PID.

Test results						
Time step	1	2	3	4	...	201
CPU cycles	82	82	82	188	...	188
Inputs						
In (DSP)	0	0	0	0	...	0
Init (DSP)	3604	3604	3604	3604	...	3604
Enable (DSP)	0	0	0	1	...	1
In	0	0	0	0	...	0
Init	0.11	0.11	0.11	0.11	...	0.11
Enable	0	0	0	1	...	1
Parameters						
Kp	2					
Ki	2500					
Kd	0.003					
fc	200					
initHandling	initialize integral					
ts_fact	1					
Outputs						
Out	0	0	0	0.11	...	-0.526
Exp. Out	0	0	0	0.11	...	-0.526
Out (DSP)	0	0	0	3604	...	-17231
Exp. Out (DSP)	0	0	0	3604	...	-17228

Test settings	
Tolerance Out	±3,0518e-04 (±10 LSB)

Test statistics	
Min CPU cycles	82
Max CPU cycles	188
Avg CPU cycles	174

Test case: Conversion test OK

Conversion test for Control block PID.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kp	-10	-9.444	-8.889	-8.333	...	10
Ki	-11	-10.389	-9.778	-9.167	...	11
Kd	-10	-9.444	-8.889	-8.333	...	10
fc	0	13.889	27.778	41.667	...	50
initHandling	initialize integral	initialize integral	initialize integral	initialize integral	...	initialize
ts_fact	1	1	1	1	...	1
Controller parameters						
sfrd	15	5	4	3	...	0
b1d	0	-26374	-24822	-17453	...	314
a0d	-32767	-32483	-32201	-31921	...	-239
b0d	0	26374	24822	17453	...	-314
initHandling	0	0	0	0	...	1
sfrb0	15	15	15	15	...	15
sfrb1	11	11	11	11	...	11
b0	-36	-34	-32	-30	...	36
b1	-20480	-19342	-18204	-17067	...	204
Exp. sfrd	15	5	4	3	...	0
Exp. b1d	0	-26374	-24822	-17453	...	314
Exp. a0d	-32767	-32483	-32201	-31921	...	-239
Exp. b0d	0	26374	24822	17453	...	-314
Exp. initHandling	0	0	0	0	...	1
Exp. sfrb0	15	15	15	15	...	15
Exp. sfrb1	11	11	11	11	...	11
Exp. b0	-36	-34	-32	-30	...	36
Exp. b1	-20480	-19342	-18204	-17067	...	204

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±0,0000e+00
Tolerance a0d	±0,0000e+00
Tolerance b0d	±0,0000e+00
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block PID.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kp	-10	-9.444	-8.889	-8.333	...	10
Ki	-11	-10.389	-9.778	-9.167	...	11
Kd	-10	-9.444	-8.889	-8.333	...	10
fc	0	13.889	27.778	41.667	...	50
initHandling	initialize integral	initialize integral	initialize integral	initialize integral	...	initialize
ts_fact	1	1	1	1	...	1
Controller parameters						
sfrd	15	5	4	3	...	0
b1d	0	-26373	-24822	-17453	...	314
a0d	-32767	-32483	-32201	-31921	...	-239
b0d	0	26373	24822	17453	...	-314
initHandling	0	0	0	0	...	1
sfrb0	15	15	15	15	...	15
sfrb1	11	11	11	11	...	11
b0	-36	-34	-32	-30	...	36
b1	-20480	-19342	-18204	-17066	...	204
Exp. sfrd	15	5	4	3	...	0
Exp. b1d	0	-26374	-24822	-17453	...	314
Exp. a0d	-32767	-32483	-32201	-31921	...	-239
Exp. b0d	0	26374	24822	17453	...	-314
Exp. initHandling	0	0	0	0	...	1
Exp. sfrb0	15	15	15	15	...	15
Exp. sfrb1	11	11	11	11	...	11
Exp. b0	-36	-34	-32	-30	...	36
Exp. b1	-20480	-19342	-18204	-17067	...	204

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±1,0000e+00
Tolerance a0d	±1,0000e+00
Tolerance b0d	±1,0000e+00
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±1,0000e+00
Tolerance b1	±1,0000e+00

Test statistics	
Min CPU cycles	2606
Max CPU cycles	4949
Avg CPU cycles	4396

Verification: PID FiP16 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for Control block PID.

Test results						
Time step	1	2	3	4	...	201
CPU cycles	77	77	77	176	...	189
Inputs						
In (DSP)	0	0	0	0	...	0
Init (DSP)	3604	3604	3604	3604	...	3604
Enable (DSP)	0	0	0	1	...	1
In	0	0	0	0	...	0
Init	0.11	0.11	0.11	0.11	...	0.11
Enable	0	0	0	1	...	1
Parameters						
Kp	2					
Ki	2500					
Kd	0.003					
fc	200					
initHandling	initialize integral					
ts_fact	1					
Outputs						
Out	0	0	0	0.11	...	-0.526
Exp. Out	0	0	0	0.11	...	-0.526
Out (DSP)	0	0	0	3604	...	-17231
Exp. Out (DSP)	0	0	0	3604	...	-17228

Test settings	
Tolerance Out	±3,0518e-04 (±10 LSB)

Test statistics	
Min CPU cycles	77
Max CPU cycles	249
Avg CPU cycles	179

Test case: Conversion test OK

Conversion test for Control block PID.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kp	-10	-9.444	-8.889	-8.333	...	10
Ki	-11	-10.389	-9.778	-9.167	...	11
Kd	-10	-9.444	-8.889	-8.333	...	10
fc	0	13.889	27.778	41.667	...	50
initHandling	initialize integral	initialize integral	initialize integral	initialize integral	...	initialize
ts_fact	1	1	1	1	...	1
Controller parameters						
sfrd	15	5	4	3	...	0
b1d	0	-26374	-24822	-17453	...	314
a0d	-32767	-32483	-32201	-31921	...	-239
b0d	0	26374	24822	17453	...	-314
initHandling	0	0	0	0	...	1
sfrb0	15	15	15	15	...	15
sfrb1	11	11	11	11	...	11
b0	-36	-34	-32	-30	...	36
b1	-20480	-19342	-18204	-17067	...	204
Exp. sfrd	15	5	4	3	...	0
Exp. b1d	0	-26374	-24822	-17453	...	314
Exp. a0d	-32767	-32483	-32201	-31921	...	-239
Exp. b0d	0	26374	24822	17453	...	-314
Exp. initHandling	0	0	0	0	...	1
Exp. sfrb0	15	15	15	15	...	15
Exp. sfrb1	11	11	11	11	...	11
Exp. b0	-36	-34	-32	-30	...	36
Exp. b1	-20480	-19342	-18204	-17067	...	204

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±0,0000e+00
Tolerance a0d	±0,0000e+00
Tolerance b0d	±0,0000e+00
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block PID.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kp	-10	-9.444	-8.889	-8.333	...	10
Ki	-11	-10.389	-9.778	-9.167	...	11
Kd	-10	-9.444	-8.889	-8.333	...	10
fc	0	13.889	27.778	41.667	...	50
initHandling	initialize integral	initialize integral	initialize integral	initialize integral	...	initialize
ts_fact	1	1	1	1	...	1
Controller parameters						
sfrd	15	5	4	3	...	0
b1d	0	-26373	-24822	-17453	...	314
a0d	-32767	-32483	-32201	-31921	...	-239
b0d	0	26373	24822	17453	...	-314
initHandling	0	0	0	0	...	1
sfrb0	15	15	15	15	...	15
sfrb1	11	11	11	11	...	11
b0	-36	-34	-32	-30	...	36
b1	-20480	-19342	-18204	-17066	...	204
Exp. sfrd	15	5	4	3	...	0
Exp. b1d	0	-26374	-24822	-17453	...	314
Exp. a0d	-32767	-32483	-32201	-31921	...	-239
Exp. b0d	0	26374	24822	17453	...	-314
Exp. initHandling	0	0	0	0	...	1
Exp. sfrb0	15	15	15	15	...	15
Exp. sfrb1	11	11	11	11	...	11
Exp. b0	-36	-34	-32	-30	...	36
Exp. b1	-20480	-19342	-18204	-17067	...	204

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±1,0000e+00
Tolerance a0d	±1,0000e+00
Tolerance b0d	±1,0000e+00
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±1,0000e+00
Tolerance b1	±1,0000e+00

Test statistics	
Min CPU cycles	10053
Max CPU cycles	23335
Avg CPU cycles	20428

Verification: PID FiP16 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for Control block PID.

Test results						
Time step	1	2	3	4	...	201
CPU cycles	31	31	31	100	...	111
Inputs						
In (DSP)	0	0	0	0	...	0
Init (DSP)	3604	3604	3604	3604	...	3604
Enable (DSP)	0	0	0	1	...	1
In	0	0	0	0	...	0
Init	0.11	0.11	0.11	0.11	...	0.11
Enable	0	0	0	1	...	1
Parameters						
Kp	2					
Ki	2500					
Kd	0.003					
fc	200					
initHandling	initialize integral					
ts_fact	1					
Outputs						
Out	0	0	0	0.11	...	-0.526
Exp. Out	0	0	0	0.11	...	-0.526
Out (DSP)	0	0	0	3604	...	-17231
Exp. Out (DSP)	0	0	0	3604	...	-17228

Test settings	
Tolerance Out	±3,0518e-04 (±10 LSB)

Test statistics	
Min CPU cycles	31
Max CPU cycles	111
Avg CPU cycles	105

Test case: Conversion test OK

Conversion test for Control block PID.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kp	-10	-9.444	-8.889	-8.333	...	10
Ki	-11	-10.389	-9.778	-9.167	...	11
Kd	-10	-9.444	-8.889	-8.333	...	10
fc	0	13.889	27.778	41.667	...	50
initHandling	initialize integral	initialize integral	initialize integral	initialize integral	...	initialize
ts_fact	1	1	1	1	...	1
Controller parameters						
sfrd	15	5	4	3	...	0
b1d	0	-26374	-24822	-17453	...	314
a0d	-32767	-32483	-32201	-31921	...	-239
b0d	0	26374	24822	17453	...	-314
initHandling	0	0	0	0	...	1
sfrb0	15	15	15	15	...	15
sfrb1	11	11	11	11	...	11
b0	-36	-34	-32	-30	...	36
b1	-20480	-19342	-18204	-17067	...	204
Exp. sfrd	15	5	4	3	...	0
Exp. b1d	0	-26374	-24822	-17453	...	314
Exp. a0d	-32767	-32483	-32201	-31921	...	-239
Exp. b0d	0	26374	24822	17453	...	-314
Exp. initHandling	0	0	0	0	...	1
Exp. sfrb0	15	15	15	15	...	15
Exp. sfrb1	11	11	11	11	...	11
Exp. b0	-36	-34	-32	-30	...	36
Exp. b1	-20480	-19342	-18204	-17067	...	204

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±0,0000e+00
Tolerance a0d	±0,0000e+00
Tolerance b0d	±0,0000e+00
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block PID.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kp	-10	-9.444	-8.889	-8.333	...	10
Ki	-11	-10.389	-9.778	-9.167	...	11
Kd	-10	-9.444	-8.889	-8.333	...	10
fc	0	13.889	27.778	41.667	...	50
initHandling	initialize integral	initialize integral	initialize integral	initialize integral	...	initialize
ts_fact	1	1	1	1	...	1
Controller parameters						
sfrd	15	5	4	3	...	0
b1d	0	-26373	-24822	-17453	...	314
a0d	-32767	-32483	-32201	-31921	...	-239
b0d	0	26373	24822	17453	...	-314
initHandling	0	0	0	0	...	1
sfrb0	15	15	15	15	...	15
sfrb1	11	11	11	11	...	11
b0	-36	-34	-32	-30	...	36
b1	-20480	-19342	-18204	-17066	...	204
Exp. sfrd	15	5	4	3	...	0
Exp. b1d	0	-26374	-24822	-17453	...	314
Exp. a0d	-32767	-32483	-32201	-31921	...	-239
Exp. b0d	0	26374	24822	17453	...	-314
Exp. initHandling	0	0	0	0	...	1
Exp. sfrb0	15	15	15	15	...	15
Exp. sfrb1	11	11	11	11	...	11
Exp. b0	-36	-34	-32	-30	...	36
Exp. b1	-20480	-19342	-18204	-17067	...	204

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±1,0000e+00
Tolerance a0d	±1,0000e+00
Tolerance b0d	±1,0000e+00
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±1,0000e+00
Tolerance b1	±1,0000e+00

Test statistics	
Min CPU cycles	3200
Max CPU cycles	8384
Avg CPU cycles	7391

Verification: PID FiP16 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for Control block PID.

Test results						
Time step	1	2	3	4	...	201
CPU cycles	81	59	59	155	...	142
Inputs						
In (DSP)	0	0	0	0	...	0
Init (DSP)	3604	3604	3604	3604	...	3604
Enable (DSP)	0	0	0	1	...	1
In	0	0	0	0	...	0
Init	0.11	0.11	0.11	0.11	...	0.11
Enable	0	0	0	1	...	1
Parameters						
Kp	2					
Ki	2500					
Kd	0.003					
fc	200					
initHandling	initialize integral					
ts_fact	1					
Outputs						
Out	0	0	0	0.11	...	-0.526
Exp. Out	0	0	0	0.11	...	-0.526
Out (DSP)	0	0	0	3604	...	-17231
Exp. Out (DSP)	0	0	0	3604	...	-17228

Test settings	
Tolerance Out	±3,0518e-04 (±10 LSB)

Test statistics	
Min CPU cycles	59
Max CPU cycles	162
Avg CPU cycles	138

Test case: Conversion test OK

Conversion test for Control block PID.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kp	-10	-9.444	-8.889	-8.333	...	10
Ki	-11	-10.389	-9.778	-9.167	...	11
Kd	-10	-9.444	-8.889	-8.333	...	10
fc	0	13.889	27.778	41.667	...	50
initHandling	initialize integral	initialize integral	initialize integral	initialize integral	...	initialize
ts_fact	1	1	1	1	...	1
Controller parameters						
sfrd	15	5	4	3	...	0
b1d	0	-26374	-24822	-17453	...	314
a0d	-32767	-32483	-32201	-31921	...	-239
b0d	0	26374	24822	17453	...	-314
initHandling	0	0	0	0	...	1
sfrb0	15	15	15	15	...	15
sfrb1	11	11	11	11	...	11
b0	-36	-34	-32	-30	...	36
b1	-20480	-19342	-18204	-17067	...	204
Exp. sfrd	15	5	4	3	...	0
Exp. b1d	0	-26374	-24822	-17453	...	314
Exp. a0d	-32767	-32483	-32201	-31921	...	-239
Exp. b0d	0	26374	24822	17453	...	-314
Exp. initHandling	0	0	0	0	...	1
Exp. sfrb0	15	15	15	15	...	15
Exp. sfrb1	11	11	11	11	...	11
Exp. b0	-36	-34	-32	-30	...	36
Exp. b1	-20480	-19342	-18204	-17067	...	204

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±0,0000e+00
Tolerance a0d	±0,0000e+00
Tolerance b0d	±0,0000e+00
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block PID.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kp	-10	-9.444	-8.889	-8.333	...	10
Ki	-11	-10.389	-9.778	-9.167	...	11
Kd	-10	-9.444	-8.889	-8.333	...	10
fc	0	13.889	27.778	41.667	...	50
initHandling	initialize integral	initialize integral	initialize integral	initialize integral	...	initialize
ts_fact	1	1	1	1	...	1
Controller parameters						
sfrd	15	5	4	3	...	0
b1d	0	-26373	-24822	-17453	...	314
a0d	-32767	-32483	-32201	-31921	...	-239
b0d	0	26373	24822	17453	...	-314
initHandling	0	0	0	0	...	1
sfrb0	15	15	15	15	...	15
sfrb1	11	11	11	11	...	11
b0	-36	-34	-32	-30	...	36
b1	-20480	-19342	-18204	-17066	...	204
Exp. sfrd	15	5	4	3	...	0
Exp. b1d	0	-26374	-24822	-17453	...	314
Exp. a0d	-32767	-32483	-32201	-31921	...	-239
Exp. b0d	0	26374	24822	17453	...	-314
Exp. initHandling	0	0	0	0	...	1
Exp. sfrb0	15	15	15	15	...	15
Exp. sfrb1	11	11	11	11	...	11
Exp. b0	-36	-34	-32	-30	...	36
Exp. b1	-20480	-19342	-18204	-17067	...	204

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±1,0000e+00
Tolerance a0d	±1,0000e+00
Tolerance b0d	±1,0000e+00
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±1,0000e+00
Tolerance b1	±1,0000e+00

Test statistics	
Min CPU cycles	2119
Max CPU cycles	4443
Avg CPU cycles	3912

Verification: PID FiP16 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for Control block PID.

Test results						
Time step	1	2	3	4	...	201
CPU cycles	70	70	70	167	...	177
Inputs						
In (DSP)	0	0	0	0	...	0
Init (DSP)	3604	3604	3604	3604	...	3604
Enable (DSP)	0	0	0	1	...	1
In	0	0	0	0	...	0
Init	0.11	0.11	0.11	0.11	...	0.11
Enable	0	0	0	1	...	1
Parameters						
Kp	2					
Ki	2500					
Kd	0.003					
fc	200					
initHandling	initialize integral					
ts_fact	1					
Outputs						
Out	0	0	0	0.11	...	-0.526
Exp. Out	0	0	0	0.11	...	-0.526
Out (DSP)	0	0	0	3604	...	-17231
Exp. Out (DSP)	0	0	0	3604	...	-17228

Test settings	
Tolerance Out	±3,0518e-04 (±10 LSB)

Test statistics	
Min CPU cycles	70
Max CPU cycles	180
Avg CPU cycles	174

Test case: Conversion test OK

Conversion test for Control block PID.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kp	-10	-9.444	-8.889	-8.333	...	10
Ki	-11	-10.389	-9.778	-9.167	...	11
Kd	-10	-9.444	-8.889	-8.333	...	10
fc	0	13.889	27.778	41.667	...	50
initHandling	initialize integral	initialize integral	initialize integral	initialize integral	...	initialize
ts_fact	1	1	1	1	...	1
Controller parameters						
sfrd	15	5	4	3	...	0
b1d	0	-26374	-24822	-17453	...	314
a0d	-32767	-32483	-32201	-31921	...	-239
b0d	0	26374	24822	17453	...	-314
initHandling	0	0	0	0	...	1
sfrb0	15	15	15	15	...	15
sfrb1	11	11	11	11	...	11
b0	-36	-34	-32	-30	...	36
b1	-20480	-19342	-18204	-17067	...	204
Exp. sfrd	15	5	4	3	...	0
Exp. b1d	0	-26374	-24822	-17453	...	314
Exp. a0d	-32767	-32483	-32201	-31921	...	-239
Exp. b0d	0	26374	24822	17453	...	-314
Exp. initHandling	0	0	0	0	...	1
Exp. sfrb0	15	15	15	15	...	15
Exp. sfrb1	11	11	11	11	...	11
Exp. b0	-36	-34	-32	-30	...	36
Exp. b1	-20480	-19342	-18204	-17067	...	204

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±0,0000e+00
Tolerance a0d	±0,0000e+00
Tolerance b0d	±0,0000e+00
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block PID.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kp	-10	-9.444	-8.889	-8.333	...	10
Ki	-11	-10.389	-9.778	-9.167	...	11
Kd	-10	-9.444	-8.889	-8.333	...	10
fc	0	13.889	27.778	41.667	...	50
initHandling	initialize integral	initialize integral	initialize integral	initialize integral	...	initialize
ts_fact	1	1	1	1	...	1
Controller parameters						
sfrd	15	5	4	3	...	0
b1d	0	-26373	-24822	-17453	...	314
a0d	-32767	-32483	-32201	-31921	...	-239
b0d	0	26373	24822	17453	...	-314
initHandling	0	0	0	0	...	1
sfrb0	15	15	15	15	...	15
sfrb1	11	11	11	11	...	11
b0	-36	-34	-32	-30	...	36
b1	-20480	-19342	-18204	-17066	...	204
Exp. sfrd	15	5	4	3	...	0
Exp. b1d	0	-26374	-24822	-17453	...	314
Exp. a0d	-32767	-32483	-32201	-31921	...	-239
Exp. b0d	0	26374	24822	17453	...	-314
Exp. initHandling	0	0	0	0	...	1
Exp. sfrb0	15	15	15	15	...	15
Exp. sfrb1	11	11	11	11	...	11
Exp. b0	-36	-34	-32	-30	...	36
Exp. b1	-20480	-19342	-18204	-17067	...	204

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±1,0000e+00
Tolerance a0d	±1,0000e+00
Tolerance b0d	±1,0000e+00
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±1,0000e+00
Tolerance b1	±1,0000e+00

Test statistics	
Min CPU cycles	3687
Max CPU cycles	11219
Avg CPU cycles	9710

Verification: PID FiP16 CPU dsPIC33EP256MC502

Date of Test	2026-06-23
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for Control block PID.

Test results						
Time step	1	2	3	4	...	201
CPU cycles	53	53	53	154	...	180
Inputs						
In (DSP)	0	0	0	0	...	0
Init (DSP)	3604	3604	3604	3604	...	3604
Enable (DSP)	0	0	0	1	...	1
In	0	0	0	0	...	0
Init	0.11	0.11	0.11	0.11	...	0.11
Enable	0	0	0	1	...	1
Parameters						
Kp	2					
Ki	2500					
Kd	0.003					
fc	200					
initHandling	initialize integral					
ts_fact	1					
Outputs						
Out	0	0	0	0.11	...	-0.526
Exp. Out	0	0	0	0.11	...	-0.526
Out (DSP)	0	0	0	3604	...	-17231
Exp. Out (DSP)	0	0	0	3604	...	-17228

Test settings	
Tolerance Out	±3,0518e-04 (±10 LSB)

Test statistics	
Min CPU cycles	53
Max CPU cycles	180
Avg CPU cycles	169

Test case: Conversion test OK

Conversion test for Control block PID.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kp	-10	-9.444	-8.889	-8.333	...	10
Ki	-11	-10.389	-9.778	-9.167	...	11
Kd	-10	-9.444	-8.889	-8.333	...	10
fc	0	13.889	27.778	41.667	...	50
initHandling	initialize integral	initialize integral	initialize integral	initialize integral	...	initialize
ts_fact	1	1	1	1	...	1
Controller parameters						
sfrd	15	5	4	3	...	0
b1d	0	-26374	-24822	-17453	...	314
a0d	-32767	-32483	-32201	-31921	...	-239
b0d	0	26374	24822	17453	...	-314
initHandling	0	0	0	0	...	1
sfrb0	15	15	15	15	...	15
sfrb1	11	11	11	11	...	11
b0	-36	-34	-32	-30	...	36
b1	-20480	-19342	-18204	-17067	...	204
Exp. sfrd	15	5	4	3	...	0
Exp. b1d	0	-26374	-24822	-17453	...	314
Exp. a0d	-32767	-32483	-32201	-31921	...	-239
Exp. b0d	0	26374	24822	17453	...	-314
Exp. initHandling	0	0	0	0	...	1
Exp. sfrb0	15	15	15	15	...	15
Exp. sfrb1	11	11	11	11	...	11
Exp. b0	-36	-34	-32	-30	...	36
Exp. b1	-20480	-19342	-18204	-17067	...	204

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±0,0000e+00
Tolerance a0d	±0,0000e+00
Tolerance b0d	±0,0000e+00
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block PID.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kp	-10	-9.444	-8.889	-8.333	...	10
Ki	-11	-10.389	-9.778	-9.167	...	11
Kd	-10	-9.444	-8.889	-8.333	...	10
fc	0	13.889	27.778	41.667	...	50
initHandling	initialize integral	initialize integral	initialize integral	initialize integral	...	initialize
ts_fact	1	1	1	1	...	1
Controller parameters						
sfrd	15	5	4	3	...	0
b1d	0	-26373	-24822	-17453	...	314
a0d	-32767	-32483	-32201	-31921	...	-239
b0d	0	26373	24822	17453	...	-314
initHandling	0	0	0	0	...	1
sfrb0	15	15	15	15	...	15
sfrb1	11	11	11	11	...	11
b0	-36	-34	-32	-30	...	36
b1	-20480	-19342	-18204	-17066	...	204
Exp. sfrd	15	5	4	3	...	0
Exp. b1d	0	-26374	-24822	-17453	...	314
Exp. a0d	-32767	-32483	-32201	-31921	...	-239
Exp. b0d	0	26374	24822	17453	...	-314
Exp. initHandling	0	0	0	0	...	1
Exp. sfrb0	15	15	15	15	...	15
Exp. sfrb1	11	11	11	11	...	11
Exp. b0	-36	-34	-32	-30	...	36
Exp. b1	-20480	-19342	-18204	-17067	...	204

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±1,0000e+00
Tolerance a0d	±1,0000e+00
Tolerance b0d	±1,0000e+00
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±1,0000e+00
Tolerance b1	±1,0000e+00

Test statistics	
Min CPU cycles	14127
Max CPU cycles	48820
Avg CPU cycles	42388

Verification: PID FiP32 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for Control block PID.

Test results				
Time step	1	2	...	201
CPU cycles	84	84	...	425
Inputs				
In (DSP)	0	0	...	0
Init (DSP)	236223201	236223201	...	236223201
Enable (DSP)	0	0	...	1
In	0	0	...	0
Init	0.11	0.11	...	0.11
Enable	0	0	...	1
Parameters				
Kp	2			
Ki	2500			
Kd	0.003			
fc	200			
initHandling	initialize integral			
ts_fact	1			
Outputs				
Out	0	0	...	-0.526
Exp. Out	0	0	...	-0.526
Out (DSP)	0	0	...	-1129025494
Exp. Out (DSP)	0	0	...	-1129025494

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	84
Max CPU cycles	431
Avg CPU cycles	406

Test case: Conversion test OK

Conversion test for Control block PID.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
sfrd	31	21	...	16
b1d	0	-1728437568	...	2058874161
a0d	-2147483647	-2128824851	...	-1568527835
b0d	0	1728437568	...	-2058874161
initHandling	0	0	...	1
sfrb0	31	31	...	31
sfrb1	27	27	...	27
b0	-2362232	-2230997	...	2362232
b1	-1342177280	-1267611876	...	1342177280
Exp. sfrd	31	21	...	16
Exp. b1d	0	-1728437568	...	2058874161
Exp. a0d	-2147483647	-2128824851	...	-1568527835
Exp. b0d	0	1728437568	...	-2058874161
Exp. initHandling	0	0	...	1
Exp. sfrb0	31	31	...	31
Exp. sfrb1	27	27	...	27
Exp. b0	-2362232	-2230997	...	2362232
Exp. b1	-1342177280	-1267611876	...	1342177280

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±0,0000e+00
Tolerance a0d	±0,0000e+00
Tolerance b0d	±0,0000e+00
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block PID.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
sfrd	31	21	...	16
b1d	0	-1728437632	...	2058874240
a0d	-2147483647	-2128824832	...	-1568527872
b0d	0	1728437632	...	-2058874240
initHandling	0	0	...	1
sfrb0	31	31	...	31
sfrb1	27	27	...	27
b0	-2362232	-2230997	...	2362232
b1	-1342177280	-1267611904	...	1342177280
Exp. sfrd	31	21	...	16
Exp. b1d	0	-1728437568	...	2058874161
Exp. a0d	-2147483647	-2128824851	...	-1568527835
Exp. b0d	0	1728437568	...	-2058874161
Exp. initHandling	0	0	...	1
Exp. sfrb0	31	31	...	31
Exp. sfrb1	27	27	...	27
Exp. b0	-2362232	-2230997	...	2362232
Exp. b1	-1342177280	-1267611876	...	1342177280

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±2,0000e+02
Tolerance a0d	±2,0000e+02
Tolerance b0d	±2,0000e+02
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±1,0000e+00
Tolerance b1	±1,0000e+02

Test statistics	
Min CPU cycles	6090
Max CPU cycles	16311
Avg CPU cycles	13994

Verification: PID FiP32 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for Control block PID.

Test results				
Time step	1	2	...	201
CPU cycles	63	63	...	253
Inputs				
In (DSP)	0	0	...	0
Init (DSP)	236223201	236223201	...	236223201
Enable (DSP)	0	0	...	1
In	0	0	...	0
Init	0.11	0.11	...	0.11
Enable	0	0	...	1
Parameters				
Kp	2			
Ki	2500			
Kd	0.003			
fc	200			
initHandling	initialize integral			
ts_fact	1			
Outputs				
Out	0	0	...	-0.526
Exp. Out	0	0	...	-0.526
Out (DSP)	0	0	...	-1129025494
Exp. Out (DSP)	0	0	...	-1129025494

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	63
Max CPU cycles	253
Avg CPU cycles	237

Test case: Conversion test OK

Conversion test for Control block PID.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
sfrd	31	21	...	16
b1d	0	-1728437568	...	2058874161
a0d	-2147483647	-2128824851	...	-1568527835
b0d	0	1728437568	...	-2058874161
initHandling	0	0	...	1
sfrb0	31	31	...	31
sfrb1	27	27	...	27
b0	-2362232	-2230997	...	2362232
b1	-1342177280	-1267611876	...	1342177280
Exp. sfrd	31	21	...	16
Exp. b1d	0	-1728437568	...	2058874161
Exp. a0d	-2147483647	-2128824851	...	-1568527835
Exp. b0d	0	1728437568	...	-2058874161
Exp. initHandling	0	0	...	1
Exp. sfrb0	31	31	...	31
Exp. sfrb1	27	27	...	27
Exp. b0	-2362232	-2230997	...	2362232
Exp. b1	-1342177280	-1267611876	...	1342177280

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±0,0000e+00
Tolerance a0d	±0,0000e+00
Tolerance b0d	±0,0000e+00
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block PID.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
sfrd	31	21	...	16
b1d	0	-1728437632	...	2058874240
a0d	-2147483647	-2128824832	...	-1568527872
b0d	0	1728437632	...	-2058874240
initHandling	0	0	...	1
sfrb0	31	31	...	31
sfrb1	27	27	...	27
b0	-2362232	-2230997	...	2362232
b1	-1342177280	-1267611904	...	1342177280
Exp. sfrd	31	21	...	16
Exp. b1d	0	-1728437568	...	2058874161
Exp. a0d	-2147483647	-2128824851	...	-1568527835
Exp. b0d	0	1728437568	...	-2058874161
Exp. initHandling	0	0	...	1
Exp. sfrb0	31	31	...	31
Exp. sfrb1	27	27	...	27
Exp. b0	-2362232	-2230997	...	2362232
Exp. b1	-1342177280	-1267611876	...	1342177280

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±2,0000e+02
Tolerance a0d	±2,0000e+02
Tolerance b0d	±2,0000e+02
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±1,0000e+00
Tolerance b1	±1,0000e+02

Test statistics	
Min CPU cycles	2341
Max CPU cycles	6943
Avg CPU cycles	5862

Verification: PID FiP32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for Control block PID.

Test results				
Time step	1	2	...	201
CPU cycles	89	89	...	296
Inputs				
In (DSP)	0	0	...	0
Init (DSP)	236223201	236223201	...	236223201
Enable (DSP)	0	0	...	1
In	0	0	...	0
Init	0.11	0.11	...	0.11
Enable	0	0	...	1
Parameters				
Kp	2			
Ki	2500			
Kd	0.003			
fc	200			
initHandling	initialize integral			
ts_fact	1			
Outputs				
Out	0	0	...	-0.526
Exp. Out	0	0	...	-0.526
Out (DSP)	0	0	...	-1129025494
Exp. Out (DSP)	0	0	...	-1129025494

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	89
Max CPU cycles	296
Avg CPU cycles	270

Test case: Conversion test OK

Conversion test for Control block PID.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
sfrd	31	21	...	16
b1d	0	-1728437568	...	2058874161
a0d	-2147483647	-2128824851	...	-1568527835
b0d	0	1728437568	...	-2058874161
initHandling	0	0	...	1
sfrb0	31	31	...	31
sfrb1	27	27	...	27
b0	-2362232	-2230997	...	2362232
b1	-1342177280	-1267611876	...	1342177280
Exp. sfrd	31	21	...	16
Exp. b1d	0	-1728437568	...	2058874161
Exp. a0d	-2147483647	-2128824851	...	-1568527835
Exp. b0d	0	1728437568	...	-2058874161
Exp. initHandling	0	0	...	1
Exp. sfrb0	31	31	...	31
Exp. sfrb1	27	27	...	27
Exp. b0	-2362232	-2230997	...	2362232
Exp. b1	-1342177280	-1267611876	...	1342177280

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±0,0000e+00
Tolerance a0d	±0,0000e+00
Tolerance b0d	±0,0000e+00
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block PID.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
sfrd	31	21	...	16
b1d	0	-1728437632	...	2058874240
a0d	-2147483647	-2128824832	...	-1568527872
b0d	0	1728437632	...	-2058874240
initHandling	0	0	...	1
sfrb0	31	31	...	31
sfrb1	27	27	...	27
b0	-2362232	-2230997	...	2362232
b1	-1342177280	-1267611904	...	1342177280
Exp. sfrd	31	21	...	16
Exp. b1d	0	-1728437568	...	2058874161
Exp. a0d	-2147483647	-2128824851	...	-1568527835
Exp. b0d	0	1728437568	...	-2058874161
Exp. initHandling	0	0	...	1
Exp. sfrb0	31	31	...	31
Exp. sfrb1	27	27	...	27
Exp. b0	-2362232	-2230997	...	2362232
Exp. b1	-1342177280	-1267611876	...	1342177280

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±2,0000e+02
Tolerance a0d	±2,0000e+02
Tolerance b0d	±2,0000e+02
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±1,0000e+00
Tolerance b1	±1,0000e+02

Test statistics	
Min CPU cycles	3836
Max CPU cycles	6293
Avg CPU cycles	5747

Verification: PID FiP32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for Control block PID.

Test results				
Time step	1	2	...	201
CPU cycles	88	88	...	686
Inputs				
In (DSP)	0	0	...	0
Init (DSP)	236223201	236223201	...	236223201
Enable (DSP)	0	0	...	1
In	0	0	...	0
Init	0.11	0.11	...	0.11
Enable	0	0	...	1
Parameters				
Kp	2			
Ki	2500			
Kd	0.003			
fc	200			
initHandling	initialize integral			
ts_fact	1			
Outputs				
Out	0	0	...	-0.526
Exp. Out	0	0	...	-0.526
Out (DSP)	0	0	...	-1129025494
Exp. Out (DSP)	0	0	...	-1129025494

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	88
Max CPU cycles	753
Avg CPU cycles	643

Test case: Conversion test OK

Conversion test for Control block PID.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
sfrd	31	21	...	16
b1d	0	-1728437568	...	2058874161
a0d	-2147483647	-2128824851	...	-1568527835
b0d	0	1728437568	...	-2058874161
initHandling	0	0	...	1
sfrb0	31	31	...	31
sfrb1	27	27	...	27
b0	-2362232	-2230997	...	2362232
b1	-1342177280	-1267611876	...	1342177280
Exp. sfrd	31	21	...	16
Exp. b1d	0	-1728437568	...	2058874161
Exp. a0d	-2147483647	-2128824851	...	-1568527835
Exp. b0d	0	1728437568	...	-2058874161
Exp. initHandling	0	0	...	1
Exp. sfrb0	31	31	...	31
Exp. sfrb1	27	27	...	27
Exp. b0	-2362232	-2230997	...	2362232
Exp. b1	-1342177280	-1267611876	...	1342177280

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±0,0000e+00
Tolerance a0d	±0,0000e+00
Tolerance b0d	±0,0000e+00
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block PID.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
sfrd	31	21	...	16
b1d	0	-1728437632	...	2058874240
a0d	-2147483647	-2128824832	...	-1568527872
b0d	0	1728437632	...	-2058874240
initHandling	0	0	...	1
sfrb0	31	31	...	31
sfrb1	27	27	...	27
b0	-2362232	-2230997	...	2362232
b1	-1342177280	-1267611904	...	1342177280
Exp. sfrd	31	21	...	16
Exp. b1d	0	-1728437568	...	2058874161
Exp. a0d	-2147483647	-2128824851	...	-1568527835
Exp. b0d	0	1728437568	...	-2058874161
Exp. initHandling	0	0	...	1
Exp. sfrb0	31	31	...	31
Exp. sfrb1	27	27	...	27
Exp. b0	-2362232	-2230997	...	2362232
Exp. b1	-1342177280	-1267611876	...	1342177280

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±2,0000e+02
Tolerance a0d	±2,0000e+02
Tolerance b0d	±2,0000e+02
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±1,0000e+00
Tolerance b1	±1,0000e+02

Test statistics	
Min CPU cycles	15408
Max CPU cycles	29718
Avg CPU cycles	26735

Verification: PID FiP32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for Control block PID.

Test results				
Time step	1	2	...	201
CPU cycles	31	31	...	196
Inputs				
In (DSP)	0	0	...	0
Init (DSP)	236223201	236223201	...	236223201
Enable (DSP)	0	0	...	1
In	0	0	...	0
Init	0.11	0.11	...	0.11
Enable	0	0	...	1
Parameters				
Kp	2			
Ki	2500			
Kd	0.003			
fc	200			
initHandling	initialize integral			
ts_fact	1			
Outputs				
Out	0	0	...	-0.526
Exp. Out	0	0	...	-0.526
Out (DSP)	0	0	...	-1129025494
Exp. Out (DSP)	0	0	...	-1129025494

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	31
Max CPU cycles	200
Avg CPU cycles	182

Test case: Conversion test OK

Conversion test for Control block PID.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
sfrd	31	21	...	16
b1d	0	-1728437568	...	2058874161
a0d	-2147483647	-2128824851	...	-1568527835
b0d	0	1728437568	...	-2058874161
initHandling	0	0	...	1
sfrb0	31	31	...	31
sfrb1	27	27	...	27
b0	-2362232	-2230997	...	2362232
b1	-1342177280	-1267611876	...	1342177280
Exp. sfrd	31	21	...	16
Exp. b1d	0	-1728437568	...	2058874161
Exp. a0d	-2147483647	-2128824851	...	-1568527835
Exp. b0d	0	1728437568	...	-2058874161
Exp. initHandling	0	0	...	1
Exp. sfrb0	31	31	...	31
Exp. sfrb1	27	27	...	27
Exp. b0	-2362232	-2230997	...	2362232
Exp. b1	-1342177280	-1267611876	...	1342177280

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±0,0000e+00
Tolerance a0d	±0,0000e+00
Tolerance b0d	±0,0000e+00
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block PID.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
sfrd	31	21	...	16
b1d	0	-1728437632	...	2058874240
a0d	-2147483647	-2128824832	...	-1568527872
b0d	0	1728437632	...	-2058874240
initHandling	0	0	...	1
sfrb0	31	31	...	31
sfrb1	27	27	...	27
b0	-2362232	-2230997	...	2362232
b1	-1342177280	-1267611904	...	1342177280
Exp. sfrd	31	21	...	16
Exp. b1d	0	-1728437568	...	2058874161
Exp. a0d	-2147483647	-2128824851	...	-1568527835
Exp. b0d	0	1728437568	...	-2058874161
Exp. initHandling	0	0	...	1
Exp. sfrb0	31	31	...	31
Exp. sfrb1	27	27	...	27
Exp. b0	-2362232	-2230997	...	2362232
Exp. b1	-1342177280	-1267611876	...	1342177280

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±2,0000e+02
Tolerance a0d	±2,0000e+02
Tolerance b0d	±2,0000e+02
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±1,0000e+00
Tolerance b1	±1,0000e+02

Test statistics	
Min CPU cycles	5332
Max CPU cycles	10879
Avg CPU cycles	9677

Verification: PID FiP32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for Control block PID.

Test results				
Time step	1	2	...	201
CPU cycles	77	59	...	255
Inputs				
In (DSP)	0	0	...	0
Init (DSP)	236223201	236223201	...	236223201
Enable (DSP)	0	0	...	1
In	0	0	...	0
Init	0.11	0.11	...	0.11
Enable	0	0	...	1
Parameters				
Kp	2			
Ki	2500			
Kd	0.003			
fc	200			
initHandling	initialize integral			
ts_fact	1			
Outputs				
Out	0	0	...	-0.526
Exp. Out	0	0	...	-0.526
Out (DSP)	0	0	...	-1129025494
Exp. Out (DSP)	0	0	...	-1129025494

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	59
Max CPU cycles	289
Avg CPU cycles	242

Test case: Conversion test OK

Conversion test for Control block PID.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
sfrd	31	21	...	16
b1d	0	-1728437568	...	2058874161
a0d	-2147483647	-2128824851	...	-1568527835
b0d	0	1728437568	...	-2058874161
initHandling	0	0	...	1
sfrb0	31	31	...	31
sfrb1	27	27	...	27
b0	-2362232	-2230997	...	2362232
b1	-1342177280	-1267611876	...	1342177280
Exp. sfrd	31	21	...	16
Exp. b1d	0	-1728437568	...	2058874161
Exp. a0d	-2147483647	-2128824851	...	-1568527835
Exp. b0d	0	1728437568	...	-2058874161
Exp. initHandling	0	0	...	1
Exp. sfrb0	31	31	...	31
Exp. sfrb1	27	27	...	27
Exp. b0	-2362232	-2230997	...	2362232
Exp. b1	-1342177280	-1267611876	...	1342177280

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±0,0000e+00
Tolerance a0d	±0,0000e+00
Tolerance b0d	±0,0000e+00
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block PID.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
sfrd	31	21	...	16
b1d	0	-1728437632	...	2058874240
a0d	-2147483647	-2128824832	...	-1568527872
b0d	0	1728437632	...	-2058874240
initHandling	0	0	...	1
sfrb0	31	31	...	31
sfrb1	27	27	...	27
b0	-2362232	-2230997	...	2362232
b1	-1342177280	-1267611904	...	1342177280
Exp. sfrd	31	21	...	16
Exp. b1d	0	-1728437568	...	2058874161
Exp. a0d	-2147483647	-2128824851	...	-1568527835
Exp. b0d	0	1728437568	...	-2058874161
Exp. initHandling	0	0	...	1
Exp. sfrb0	31	31	...	31
Exp. sfrb1	27	27	...	27
Exp. b0	-2362232	-2230997	...	2362232
Exp. b1	-1342177280	-1267611876	...	1342177280

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±2,0000e+02
Tolerance a0d	±2,0000e+02
Tolerance b0d	±2,0000e+02
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±1,0000e+00
Tolerance b1	±1,0000e+02

Test statistics	
Min CPU cycles	3528
Max CPU cycles	5903
Avg CPU cycles	5376

Verification: PID FiP32 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for Control block PID.

Test results				
Time step	1	2	...	201
CPU cycles	72	72	...	366
Inputs				
In (DSP)	0	0	...	0
Init (DSP)	236223201	236223201	...	236223201
Enable (DSP)	0	0	...	1
In	0	0	...	0
Init	0.11	0.11	...	0.11
Enable	0	0	...	1
Parameters				
Kp	2			
Ki	2500			
Kd	0.003			
fc	200			
initHandling	initialize integral			
ts_fact	1			
Outputs				
Out	0	0	...	-0.526
Exp. Out	0	0	...	-0.526
Out (DSP)	0	0	...	-1129025494
Exp. Out (DSP)	0	0	...	-1129025494

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	72
Max CPU cycles	376
Avg CPU cycles	352

Test case: Conversion test OK

Conversion test for Control block PID.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
sfrd	31	21	...	16
b1d	0	-1728437568	...	2058874161
a0d	-2147483647	-2128824851	...	-1568527835
b0d	0	1728437568	...	-2058874161
initHandling	0	0	...	1
sfrb0	31	31	...	31
sfrb1	27	27	...	27
b0	-2362232	-2230997	...	2362232
b1	-1342177280	-1267611876	...	1342177280
Exp. sfrd	31	21	...	16
Exp. b1d	0	-1728437568	...	2058874161
Exp. a0d	-2147483647	-2128824851	...	-1568527835
Exp. b0d	0	1728437568	...	-2058874161
Exp. initHandling	0	0	...	1
Exp. sfrb0	31	31	...	31
Exp. sfrb1	27	27	...	27
Exp. b0	-2362232	-2230997	...	2362232
Exp. b1	-1342177280	-1267611876	...	1342177280

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±0,0000e+00
Tolerance a0d	±0,0000e+00
Tolerance b0d	±0,0000e+00
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block PID.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
sfrd	31	21	...	16
b1d	0	-1728437632	...	2058874240
a0d	-2147483647	-2128824832	...	-1568527872
b0d	0	1728437632	...	-2058874240
initHandling	0	0	...	1
sfrb0	31	31	...	31
sfrb1	27	27	...	27
b0	-2362232	-2230997	...	2362232
b1	-1342177280	-1267611904	...	1342177280
Exp. sfrd	31	21	...	16
Exp. b1d	0	-1728437568	...	2058874161
Exp. a0d	-2147483647	-2128824851	...	-1568527835
Exp. b0d	0	1728437568	...	-2058874161
Exp. initHandling	0	0	...	1
Exp. sfrb0	31	31	...	31
Exp. sfrb1	27	27	...	27
Exp. b0	-2362232	-2230997	...	2362232
Exp. b1	-1342177280	-1267611876	...	1342177280

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±2,0000e+02
Tolerance a0d	±2,0000e+02
Tolerance b0d	±2,0000e+02
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±1,0000e+00
Tolerance b1	±1,0000e+02

Test statistics	
Min CPU cycles	4340
Max CPU cycles	12405
Avg CPU cycles	10574

Verification: PID FiP32 CPU dsPIC33EP256MC502

Date of Test	2026-06-23
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for Control block PID.

Test results				
Time step	1	2	...	201
CPU cycles	64	64	...	1348
Inputs				
In (DSP)	0	0	...	0
Init (DSP)	236223201	236223201	...	236223201
Enable (DSP)	0	0	...	1
In	0	0	...	0
Init	0.11	0.11	...	0.11
Enable	0	0	...	1
Parameters				
Kp	2			
Ki	2500			
Kd	0.003			
fc	200			
initHandling	initialize integral			
ts_fact	1			
Outputs				
Out	0	0	...	-0.526
Exp. Out	0	0	...	-0.526
Out (DSP)	0	0	...	-1129025494
Exp. Out (DSP)	0	0	...	-1129025494

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	64
Max CPU cycles	1379
Avg CPU cycles	1296

Test case: Conversion test OK

Conversion test for Control block PID.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
sfrd	31	21	...	16
b1d	0	-1728437568	...	2058874161
a0d	-2147483647	-2128824851	...	-1568527835
b0d	0	1728437568	...	-2058874161
initHandling	0	0	...	1
sfrb0	31	31	...	31
sfrb1	27	27	...	27
b0	-2362232	-2230997	...	2362232
b1	-1342177280	-1267611876	...	1342177280
Exp. sfrd	31	21	...	16
Exp. b1d	0	-1728437568	...	2058874161
Exp. a0d	-2147483647	-2128824851	...	-1568527835
Exp. b0d	0	1728437568	...	-2058874161
Exp. initHandling	0	0	...	1
Exp. sfrb0	31	31	...	31
Exp. sfrb1	27	27	...	27
Exp. b0	-2362232	-2230997	...	2362232
Exp. b1	-1342177280	-1267611876	...	1342177280

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±0,0000e+00
Tolerance a0d	±0,0000e+00
Tolerance b0d	±0,0000e+00
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block PID.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
sfrd	31	21	...	16
b1d	0	-1728437632	...	2058874240
a0d	-2147483647	-2128824832	...	-1568527872
b0d	0	1728437632	...	-2058874240
initHandling	0	0	...	1
sfrb0	31	31	...	31
sfrb1	27	27	...	27
b0	-2362232	-2230997	...	2362232
b1	-1342177280	-1267611904	...	1342177280
Exp. sfrd	31	21	...	16
Exp. b1d	0	-1728437568	...	2058874161
Exp. a0d	-2147483647	-2128824851	...	-1568527835
Exp. b0d	0	1728437568	...	-2058874161
Exp. initHandling	0	0	...	1
Exp. sfrb0	31	31	...	31
Exp. sfrb1	27	27	...	27
Exp. b0	-2362232	-2230997	...	2362232
Exp. b1	-1342177280	-1267611876	...	1342177280

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±2,0000e+02
Tolerance a0d	±2,0000e+02
Tolerance b0d	±2,0000e+02
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±1,0000e+00
Tolerance b1	±1,0000e+02

Test statistics	
Min CPU cycles	15980
Max CPU cycles	50882
Avg CPU cycles	43326

Verification: PID Float32 CPU TMS320F28335

Date of Test 2026-06-19

Target controller TMS320F28335

Test case: Inport test OK

Inport test for Control block PID.

Test results				
Time step	1	2	...	201
CPU cycles	86	86	...	159
Inputs				
In (DSP)	0	0	...	0
Init (DSP)	0.11	0.11	...	0.11
Enable (DSP)	0	0	...	1
In	0	0	...	0
Init	0.11	0.11	...	0.11
Enable	0	0	...	1
Parameters				
Kp	2			
Ki	2500			
Kd	0.003			
fc	200			
initHandling	initialize integral			
ts_fact	1			
Outputs				
Out	0	0	...	-1.838
Exp. Out	0	0	...	-1.838
Out (DSP)	0	0	...	-1.838
Exp. Out (DSP)	0	0	...	-1.838

Test settings	
Tolerance Out	±2,3283e-06 (±5000 LSB)

Test statistics	
Min CPU cycles	86
Max CPU cycles	170
Avg CPU cycles	157

Test case: Conversion test OK

Conversion test for Control block PID.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
b1d	0	-824.183	...	31415.927
a0d	-1	-0.991	...	-0.73
b0d	0	824.183	...	-31415.927
initHandling	0	0	...	1
b0	-0.001	-0.001	...	0.001
b1	-10	-9.444	...	10
Exp. b1d	0	-824.183	...	31415.927
Exp. a0d	-1	-0.991	...	-0.73
Exp. b0d	0	824.183	...	-31415.927
Exp. initHandling	0	0	...	1
Exp. b0	-0.001	-0.001	...	0.001
Exp. b1	-10	-9.444	...	10

Test settings	
Tolerance b1d	±0,0000e+00
Tolerance a0d	±1,0000e-15
Tolerance b0d	±0,0000e+00
Tolerance initHandling	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block PID.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
b1d	0	-824.183	...	31415.928
a0d	-1	-0.991	...	-0.73
b0d	0	824.183	...	-31415.928
initHandling	0	0	...	1
b0	-0.001	-0.001	...	0.001
b1	-10	-9.444	...	10
Exp. b1d	0	-824.183	...	31415.927
Exp. a0d	-1	-0.991	...	-0.73
Exp. b0d	0	824.183	...	-31415.927
Exp. initHandling	0	0	...	1
Exp. b0	-0.001	-0.001	...	0.001
Exp. b1	-10	-9.444	...	10

Test settings	
Tolerance b1d	±3,0000e-03
Tolerance a0d	±1,0000e-07
Tolerance b0d	±3,0000e-03
Tolerance initHandling	±0,0000e+00
Tolerance b0	±1,0000e-10
Tolerance b1	±1,0000e-06

Test statistics	
Min CPU cycles	2955
Max CPU cycles	3320
Avg CPU cycles	3279

Verification: PID Float32 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for Control block PID.

Test results				
Time step	1	2	...	201
CPU cycles	41	41	...	119
Inputs				
In (DSP)	0	0	...	0
Init (DSP)	0.11	0.11	...	0.11
Enable (DSP)	0	0	...	1
In	0	0	...	0
Init	0.11	0.11	...	0.11
Enable	0	0	...	1
Parameters				
Kp	2			
Ki	2500			
Kd	0.003			
fc	200			
initHandling	initialize integral			
ts_fact	1			
Outputs				
Out	0	0	...	-1.838
Exp. Out	0	0	...	-1.838
Out (DSP)	0	0	...	-1.838
Exp. Out (DSP)	0	0	...	-1.838

Test settings	
Tolerance Out	±2,3283e-06 (±5000 LSB)

Test statistics	
Min CPU cycles	41
Max CPU cycles	119
Avg CPU cycles	117

Test case: Conversion test OK

Conversion test for Control block PID.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
b1d	0	-824.183	...	31415.927
a0d	-1	-0.991	...	-0.73
b0d	0	824.183	...	-31415.927
initHandling	0	0	...	1
b0	-0.001	-0.001	...	0.001
b1	-10	-9.444	...	10
Exp. b1d	0	-824.183	...	31415.927
Exp. a0d	-1	-0.991	...	-0.73
Exp. b0d	0	824.183	...	-31415.927
Exp. initHandling	0	0	...	1
Exp. b0	-0.001	-0.001	...	0.001
Exp. b1	-10	-9.444	...	10

Test settings	
Tolerance b1d	±0,0000e+00
Tolerance a0d	±1,0000e-15
Tolerance b0d	±0,0000e+00
Tolerance initHandling	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block PID.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
b1d	0	-824.183	...	31415.928
a0d	-1	-0.991	...	-0.73
b0d	0	824.183	...	-31415.928
initHandling	0	0	...	1
b0	-0.001	-0.001	...	0.001
b1	-10	-9.444	...	10
Exp. b1d	0	-824.183	...	31415.927
Exp. a0d	-1	-0.991	...	-0.73
Exp. b0d	0	824.183	...	-31415.927
Exp. initHandling	0	0	...	1
Exp. b0	-0.001	-0.001	...	0.001
Exp. b1	-10	-9.444	...	10

Test settings	
Tolerance b1d	±3,0000e-03
Tolerance a0d	±1,0000e-07
Tolerance b0d	±3,0000e-03
Tolerance initHandling	±0,0000e+00
Tolerance b0	±1,0000e-10
Tolerance b1	±1,0000e-06

Test statistics	
Min CPU cycles	1309
Max CPU cycles	1355
Avg CPU cycles	1351

Verification: PID Float32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for Control block PID.

Test results				
Time step	1	2	...	201
CPU cycles	73	73	...	173
Inputs				
In (DSP)	0	0	...	0
Init (DSP)	0.11	0.11	...	0.11
Enable (DSP)	0	0	...	1
In	0	0	...	0
Init	0.11	0.11	...	0.11
Enable	0	0	...	1
Parameters				
Kp	2			
Ki	2500			
Kd	0.003			
fc	200			
initHandling	initialize integral			
ts_fact	1			
Outputs				
Out	0	0	...	-1.838
Exp. Out	0	0	...	-1.838
Out (DSP)	0	0	...	-1.838
Exp. Out (DSP)	0	0	...	-1.838

Test settings	
Tolerance Out	±2,3283e-06 (±5000 LSB)

Test statistics	
Min CPU cycles	73
Max CPU cycles	179
Avg CPU cycles	171

Test case: Conversion test OK

Conversion test for Control block PID.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
b1d	0	-824.183	...	31415.927
a0d	-1	-0.991	...	-0.73
b0d	0	824.183	...	-31415.927
initHandling	0	0	...	1
b0	-0.001	-0.001	...	0.001
b1	-10	-9.444	...	10
Exp. b1d	0	-824.183	...	31415.927
Exp. a0d	-1	-0.991	...	-0.73
Exp. b0d	0	824.183	...	-31415.927
Exp. initHandling	0	0	...	1
Exp. b0	-0.001	-0.001	...	0.001
Exp. b1	-10	-9.444	...	10

Test settings	
Tolerance b1d	±0,0000e+00
Tolerance a0d	±1,0000e-15
Tolerance b0d	±0,0000e+00
Tolerance initHandling	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block PID.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
b1d	0	-824.183	...	31415.928
a0d	-1	-0.991	...	-0.73
b0d	0	824.183	...	-31415.928
initHandling	0	0	...	1
b0	-0.001	-0.001	...	0.001
b1	-10	-9.444	...	10
Exp. b1d	0	-824.183	...	31415.927
Exp. a0d	-1	-0.991	...	-0.73
Exp. b0d	0	824.183	...	-31415.927
Exp. initHandling	0	0	...	1
Exp. b0	-0.001	-0.001	...	0.001
Exp. b1	-10	-9.444	...	10

Test settings	
Tolerance b1d	±3,0000e-03
Tolerance a0d	±1,0000e-07
Tolerance b0d	±3,0000e-03
Tolerance initHandling	±0,0000e+00
Tolerance b0	±1,0000e-10
Tolerance b1	±1,0000e-06

Test statistics	
Min CPU cycles	1488
Max CPU cycles	1562
Avg CPU cycles	1556

Verification: PID Float32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for Control block PID.

Test results				
Time step	1	2	...	201
CPU cycles	82	82	...	1440
Inputs				
In (DSP)	0	0	...	0
Init (DSP)	0.11	0.11	...	0.11
Enable (DSP)	0	0	...	1
In	0	0	...	0
Init	0.11	0.11	...	0.11
Enable	0	0	...	1
Parameters				
Kp	2			
Ki	2500			
Kd	0.003			
fc	200			
initHandling	initialize integral			
ts_fact	1			
Outputs				
Out	0	0	...	-1.838
Exp. Out	0	0	...	-1.838
Out (DSP)	0	0	...	-1.838
Exp. Out (DSP)	0	0	...	-1.838

Test settings	
Tolerance Out	±2,3283e-06 (±5000 LSB)

Test statistics	
Min CPU cycles	82
Max CPU cycles	1806
Avg CPU cycles	1621

Test case: Conversion test OK

Conversion test for Control block PID.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
b1d	0	-824.183	...	31415.927
a0d	-1	-0.991	...	-0.73
b0d	0	824.183	...	-31415.927
initHandling	0	0	...	1
b0	-0.001	-0.001	...	0.001
b1	-10	-9.444	...	10
Exp. b1d	0	-824.183	...	31415.927
Exp. a0d	-1	-0.991	...	-0.73
Exp. b0d	0	824.183	...	-31415.927
Exp. initHandling	0	0	...	1
Exp. b0	-0.001	-0.001	...	0.001
Exp. b1	-10	-9.444	...	10

Test settings	
Tolerance b1d	±0,0000e+00
Tolerance a0d	±1,0000e-15
Tolerance b0d	±0,0000e+00
Tolerance initHandling	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block PID.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
b1d	0	-824.183	...	31415.928
a0d	-1	-0.991	...	-0.73
b0d	0	824.183	...	-31415.928
initHandling	0	0	...	1
b0	-0.001	-0.001	...	0.001
b1	-10	-9.444	...	10
Exp. b1d	0	-824.183	...	31415.927
Exp. a0d	-1	-0.991	...	-0.73
Exp. b0d	0	824.183	...	-31415.927
Exp. initHandling	0	0	...	1
Exp. b0	-0.001	-0.001	...	0.001
Exp. b1	-10	-9.444	...	10

Test settings	
Tolerance b1d	±3,0000e-03
Tolerance a0d	±1,0000e-07
Tolerance b0d	±3,0000e-03
Tolerance initHandling	±0,0000e+00
Tolerance b0	±1,0000e-10
Tolerance b1	±1,0000e-06

Test statistics	
Min CPU cycles	4055
Max CPU cycles	7090
Avg CPU cycles	6914

Verification: PID Float32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for Control block PID.

Test results				
Time step	1	2	...	201
CPU cycles	69	69	...	559
Inputs				
In (DSP)	0	0	...	0
Init (DSP)	0.11	0.11	...	0.11
Enable (DSP)	0	0	...	1
In	0	0	...	0
Init	0.11	0.11	...	0.11
Enable	0	0	...	1
Parameters				
Kp	2			
Ki	2500			
Kd	0.003			
fc	200			
initHandling	initialize integral			
ts_fact	1			
Outputs				
Out	0	0	...	-1.838
Exp. Out	0	0	...	-1.838
Out (DSP)	0	0	...	-1.838
Exp. Out (DSP)	0	0	...	-1.838

Test settings	
Tolerance Out	±2,3283e-06 (±5000 LSB)

Test statistics	
Min CPU cycles	69
Max CPU cycles	731
Avg CPU cycles	635

Test case: Conversion test OK

Conversion test for Control block PID.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
b1d	0	-824.183	...	31415.927
a0d	-1	-0.991	...	-0.73
b0d	0	824.183	...	-31415.927
initHandling	0	0	...	1
b0	-0.001	-0.001	...	0.001
b1	-10	-9.444	...	10
Exp. b1d	0	-824.183	...	31415.927
Exp. a0d	-1	-0.991	...	-0.73
Exp. b0d	0	824.183	...	-31415.927
Exp. initHandling	0	0	...	1
Exp. b0	-0.001	-0.001	...	0.001
Exp. b1	-10	-9.444	...	10

Test settings	
Tolerance b1d	±0,0000e+00
Tolerance a0d	±1,0000e-15
Tolerance b0d	±0,0000e+00
Tolerance initHandling	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block PID.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
b1d	0	-824.183	...	31415.928
a0d	-1	-0.991	...	-0.73
b0d	0	824.183	...	-31415.928
initHandling	0	0	...	1
b0	-0.001	-0.001	...	0.001
b1	-10	-9.444	...	10
Exp. b1d	0	-824.183	...	31415.927
Exp. a0d	-1	-0.991	...	-0.73
Exp. b0d	0	824.183	...	-31415.927
Exp. initHandling	0	0	...	1
Exp. b0	-0.001	-0.001	...	0.001
Exp. b1	-10	-9.444	...	10

Test settings	
Tolerance b1d	±3,0000e-03
Tolerance a0d	±1,0000e-07
Tolerance b0d	±3,0000e-03
Tolerance initHandling	±0,0000e+00
Tolerance b0	±1,0000e-10
Tolerance b1	±1,0000e-06

Test statistics	
Min CPU cycles	1304
Max CPU cycles	1551
Avg CPU cycles	1538

Verification: PID Float32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for Control block PID.

Test results				
Time step	1	2	...	201
CPU cycles	78	60	...	136
Inputs				
In (DSP)	0	0	...	0
Init (DSP)	0.11	0.11	...	0.11
Enable (DSP)	0	0	...	1
In	0	0	...	0
Init	0.11	0.11	...	0.11
Enable	0	0	...	1
Parameters				
Kp	2			
Ki	2500			
Kd	0.003			
fc	200			
initHandling	initialize integral			
ts_fact	1			
Outputs				
Out	0	0	...	-1.838
Exp. Out	0	0	...	-1.838
Out (DSP)	0	0	...	-1.838
Exp. Out (DSP)	0	0	...	-1.838

Test settings	
Tolerance Out	±2,3283e-06 (±5000 LSB)

Test statistics	
Min CPU cycles	60
Max CPU cycles	178
Avg CPU cycles	135

Test case: Conversion test OK

Conversion test for Control block PID.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
b1d	0	-824.183	...	31415.927
a0d	-1	-0.991	...	-0.73
b0d	0	824.183	...	-31415.927
initHandling	0	0	...	1
b0	-0.001	-0.001	...	0.001
b1	-10	-9.444	...	10
Exp. b1d	0	-824.183	...	31415.927
Exp. a0d	-1	-0.991	...	-0.73
Exp. b0d	0	824.183	...	-31415.927
Exp. initHandling	0	0	...	1
Exp. b0	-0.001	-0.001	...	0.001
Exp. b1	-10	-9.444	...	10

Test settings	
Tolerance b1d	±0,0000e+00
Tolerance a0d	±1,0000e-15
Tolerance b0d	±0,0000e+00
Tolerance initHandling	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block PID.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
b1d	0	-824.183	...	31415.928
a0d	-1	-0.991	...	-0.73
b0d	0	824.183	...	-31415.928
initHandling	0	0	...	1
b0	-0.001	-0.001	...	0.001
b1	-10	-9.444	...	10
Exp. b1d	0	-824.183	...	31415.927
Exp. a0d	-1	-0.991	...	-0.73
Exp. b0d	0	824.183	...	-31415.927
Exp. initHandling	0	0	...	1
Exp. b0	-0.001	-0.001	...	0.001
Exp. b1	-10	-9.444	...	10

Test settings	
Tolerance b1d	±3,0000e-03
Tolerance a0d	±1,0000e-07
Tolerance b0d	±3,0000e-03
Tolerance initHandling	±0,0000e+00
Tolerance b0	±1,0000e-10
Tolerance b1	±1,0000e-06

Test statistics	
Min CPU cycles	1391
Max CPU cycles	1535
Avg CPU cycles	1398

Verification: PID Float32 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for Control block PID.

Test results				
Time step	1	2	...	201
CPU cycles	72	72	...	150
Inputs				
In (DSP)	0	0	...	0
Init (DSP)	0.11	0.11	...	0.11
Enable (DSP)	0	0	...	1
In	0	0	...	0
Init	0.11	0.11	...	0.11
Enable	0	0	...	1
Parameters				
Kp	2			
Ki	2500			
Kd	0.003			
fc	200			
initHandling	initialize integral			
ts_fact	1			
Outputs				
Out	0	0	...	-1.838
Exp. Out	0	0	...	-1.838
Out (DSP)	0	0	...	-1.838
Exp. Out (DSP)	0	0	...	-1.838

Test settings	
Tolerance Out	±2,3283e-06 (±5000 LSB)

Test statistics	
Min CPU cycles	72
Max CPU cycles	175
Avg CPU cycles	148

Test case: Conversion test OK

Conversion test for Control block PID.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
b1d	0	-824.183	...	31415.927
a0d	-1	-0.991	...	-0.73
b0d	0	824.183	...	-31415.927
initHandling	0	0	...	1
b0	-0.001	-0.001	...	0.001
b1	-10	-9.444	...	10
Exp. b1d	0	-824.183	...	31415.927
Exp. a0d	-1	-0.991	...	-0.73
Exp. b0d	0	824.183	...	-31415.927
Exp. initHandling	0	0	...	1
Exp. b0	-0.001	-0.001	...	0.001
Exp. b1	-10	-9.444	...	10

Test settings	
Tolerance b1d	±0,0000e+00
Tolerance a0d	±1,0000e-15
Tolerance b0d	±0,0000e+00
Tolerance initHandling	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block PID.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
b1d	0	-824.183	...	31415.928
a0d	-1	-0.991	...	-0.73
b0d	0	824.183	...	-31415.928
initHandling	0	0	...	1
b0	-0.001	-0.001	...	0.001
b1	-10	-9.444	...	10
Exp. b1d	0	-824.183	...	31415.927
Exp. a0d	-1	-0.991	...	-0.73
Exp. b0d	0	824.183	...	-31415.927
Exp. initHandling	0	0	...	1
Exp. b0	-0.001	-0.001	...	0.001
Exp. b1	-10	-9.444	...	10

Test settings	
Tolerance b1d	±3,0000e-03
Tolerance a0d	±1,0000e-07
Tolerance b0d	±3,0000e-03
Tolerance initHandling	±0,0000e+00
Tolerance b0	±1,0000e-10
Tolerance b1	±1,0000e-06

Test statistics	
Min CPU cycles	2097
Max CPU cycles	2396
Avg CPU cycles	2356

Verification: PID Float32 CPU dsPIC33EP256MC502

Date of Test	2026-06-23
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for Control block PID.

Test results				
Time step	1	2	...	201
CPU cycles	64	64	...	1692
Inputs				
In (DSP)	0	0	...	0
Init (DSP)	0.11	0.11	...	0.11
Enable (DSP)	0	0	...	1
In	0	0	...	0
Init	0.11	0.11	...	0.11
Enable	0	0	...	1
Parameters				
Kp	2			
Ki	2500			
Kd	0.003			
fc	200			
initHandling	initialize integral			
ts_fact	1			
Outputs				
Out	0	0	...	-1.838
Exp. Out	0	0	...	-1.838
Out (DSP)	0	0	...	-1.838
Exp. Out (DSP)	0	0	...	-1.838

Test settings	
Tolerance Out	±2,3283e-06 (±5000 LSB)

Test statistics	
Min CPU cycles	64
Max CPU cycles	2170
Avg CPU cycles	1876

Test case: Conversion test OK

Conversion test for Control block PID.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
b1d	0	-824.183	...	31415.927
a0d	-1	-0.991	...	-0.73
b0d	0	824.183	...	-31415.927
initHandling	0	0	...	1
b0	-0.001	-0.001	...	0.001
b1	-10	-9.444	...	10
Exp. b1d	0	-824.183	...	31415.927
Exp. a0d	-1	-0.991	...	-0.73
Exp. b0d	0	824.183	...	-31415.927
Exp. initHandling	0	0	...	1
Exp. b0	-0.001	-0.001	...	0.001
Exp. b1	-10	-9.444	...	10

Test settings	
Tolerance b1d	±0,0000e+00
Tolerance a0d	±1,0000e-15
Tolerance b0d	±0,0000e+00
Tolerance initHandling	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

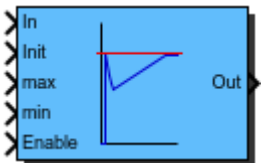
Conversion-on-Target test for Control block PID.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
b1d	0	-824.183	...	31415.928
a0d	-1	-0.991	...	-0.73
b0d	0	824.183	...	-31415.928
initHandling	0	0	...	1
b0	-0.001	-0.001	...	0.001
b1	-10	-9.444	...	10
Exp. b1d	0	-824.183	...	31415.927
Exp. a0d	-1	-0.991	...	-0.73
Exp. b0d	0	824.183	...	-31415.927
Exp. initHandling	0	0	...	1
Exp. b0	-0.001	-0.001	...	0.001
Exp. b1	-10	-9.444	...	10

Test settings	
Tolerance b1d	±3,0000e-03
Tolerance a0d	±1,0000e-07
Tolerance b0d	±3,0000e-03
Tolerance initHandling	±0,0000e+00
Tolerance b0	±1,0000e-10
Tolerance b1	±1,0000e-06

Test statistics	
Min CPU cycles	5102
Max CPU cycles	8863
Avg CPU cycles	8469

Block: PIDLimit



PID Controller with Output Limitation and anti wind-up method clamping:
G(s) = Kp + Ki/s + Kd*s/(s/(2*pi*fc) + 1)

Inports	
In	Control error input
Init	Initial value of output Out when enabled
max	Maximum output value
min	Minimum output value
Enable	Enable == 0: Deactivation of block; Out set to 0 Enable 0->1: Preload of integral part Enable == 1: Activation of block

Outports	
Out	Control value

Mask Parameters		
Name	**ID**	**Description**
Kp	1	Proportional Factor
Ki	2	Integral Factor
Kd	3	Derivative Factor
fc	4	Cutoff frequency of realization low pass
initHandling	5	Determines what the signal provided on Init input is used for
ts_fact	6	Multiplication factor of base sampling time (in integer format)

Description:

Preloading Integral
A rising edge at the *Enable* inport enables the controller and preloads the integral.

One may choose from two options how to preload the integral value:

- Preload the integral from the *Init* inport.
- Preload the integral such that the first output of the controller matches the current value at the *Init* inport.
  This option allows controller switching without disturbing the control.

Note: Each fixed point implementation uses the next higher integer data type for the integral value storage variable.
Transfer function (zero-order hold discretization method):
When the block is enabled, the PID controller realizes the following transfer function:

$$G(z) = K_\mathrm{p} + K_\mathrm{i} T_\mathrm{s} \frac{1}{z-1} + K_\mathrm{d} 2\pi f_\mathrm{c} \frac{z-1}{z - e^{-2\pi f_\mathrm{c} T_\mathrm{s}}}$$

Anti Wind-Up
The implemented anti wind-up method is clamping. If the output signal out exceeds the upper or lower limit value, which is given by the inport max and the inport min, the integrator is clamped if the controller input would increase the saturation even further.

FiP8 bug: When using the TI compiler the step response of the derivative part doesn't return to zero, but generates an overflow at zero crossing if the derivative parameter value is too high.

Developer note: The fixed point implementation source code of this block is used for block *PID*.

Implementations:

FiP8	8 Bit Fixed Point Implementation
FiP16	16 Bit Fixed Point Implementation
FiP32	32 Bit Fixed Point Implementation
Float32	32 Bit Floating Point Implementation
Float64	64 Bit Floating Point Implementation

Implementation: FiP8

8 Bit Fixed Point Implementation

Inports Data Type	
In	int8
Init	int8
max	int8
min	int8
Enable	bool

Outports Data Type	
Out	int8

Implementation: FiP16

16 Bit Fixed Point Implementation

Inports Data Type	
In	int16
Init	int16
max	int16
min	int16
Enable	bool

Outports Data Type	
Out	int16

Implementation: FiP32

32 Bit Fixed Point Implementation

Inports Data Type	
In	int32
Init	int32
max	int32
min	int32
Enable	bool

Outports Data Type	
Out	int32

Implementation: Float32

32 Bit Floating Point Implementation

Inports Data Type	
In	float32
Init	float32
max	float32
min	float32
Enable	bool

Outports Data Type	
Out	float32

Implementation: Float64

64 Bit Floating Point Implementation

Inports Data Type	
In	float64
Init	float64
max	float64
min	float64
Enable	bool

Outports Data Type	
Out	float64

Verification: PIDLimit FiP16 CPU TMS320F28335

Date of Test 2026-06-19

Target controller TMS320F28335

Test case: Inport test OK

Inport test for Control block PIDLimit.

Test results						
Time step	1	2	3	4	...	201
CPU cycles	81	81	81	182	...	182
Inputs						
In (DSP)	0	0	0	0	...	0
Init (DSP)	3604	3604	3604	3604	...	3604
max (DSP)	26214	26214	26214	26214	...	26214
min (DSP)	4915	4915	4915	4915	...	4915
Enable (DSP)	0	0	0	1	...	1
In	0	0	0	0	...	0
Init	0.11	0.11	0.11	0.11	...	0.11
max	0.8	0.8	0.8	0.8	...	0.8
min	0.15	0.15	0.15	0.15	...	0.15
Enable	0	0	0	1	...	1
Parameters						
Kp	2					
Ki	2500					
Kd	0.003					
fc	200					
initHandling	initialize integral					
ts_fact	1					
Outputs						
Out	0	0	0	0.15	...	0.649
Exp. Out	0	0	0	0.15	...	0.649
Out (DSP)	0	0	0	4915	...	21273
Exp. Out (DSP)	0	0	0	4915	...	21275

Test settings	
Tolerance Out	±3,0518e-04 (±10 LSB)

Test statistics	
Min CPU cycles	81
Max CPU cycles	188
Avg CPU cycles	176

Test case: Conversion test OK

Conversion test for Control block PIDLimit.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kp	-10	-9.444	-8.889	-8.333	...	10
Ki	-11	-10.389	-9.778	-9.167	...	11
Kd	-10	-9.444	-8.889	-8.333	...	10
fc	0	13.889	27.778	41.667	...	50
initHandling	initialize integral	initialize integral	initialize integral	initialize integral	...	initialize
ts_fact	1	1	1	1	...	1
Controller parameters						
sfrd	15	5	4	3	...	0
b1d	0	-26374	-24822	-17453	...	314
a0d	-32767	-32483	-32201	-31921	...	-239
b0d	0	26374	24822	17453	...	-314
initHandling	0	0	0	0	...	1
sfrb0	15	15	15	15	...	15
sfrb1	11	11	11	11	...	11
b0	-36	-34	-32	-30	...	36
b1	-20480	-19342	-18204	-17067	...	204
Exp. sfrd	15	5	4	3	...	0
Exp. b1d	0	-26374	-24822	-17453	...	314
Exp. a0d	-32767	-32483	-32201	-31921	...	-239
Exp. b0d	0	26374	24822	17453	...	-314
Exp. initHandling	0	0	0	0	...	1
Exp. sfrb0	15	15	15	15	...	15
Exp. sfrb1	11	11	11	11	...	11
Exp. b0	-36	-34	-32	-30	...	36
Exp. b1	-20480	-19342	-18204	-17067	...	204

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±0,0000e+00
Tolerance a0d	±0,0000e+00
Tolerance b0d	±0,0000e+00
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block PIDLimit.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kp	-10	-9.444	-8.889	-8.333	...	10
Ki	-11	-10.389	-9.778	-9.167	...	11
Kd	-10	-9.444	-8.889	-8.333	...	10
fc	0	13.889	27.778	41.667	...	50
initHandling	initialize integral	initialize integral	initialize integral	initialize integral	...	initialize
ts_fact	1	1	1	1	...	1
Controller parameters						
sfrd	15	5	4	3	...	0
b1d	0	-26373	-24822	-17453	...	314
a0d	-32767	-32483	-32201	-31921	...	-239
b0d	0	26373	24822	17453	...	-314
initHandling	0	0	0	0	...	1
sfrb0	15	15	15	15	...	15
sfrb1	11	11	11	11	...	11
b0	-36	-34	-32	-30	...	36
b1	-20480	-19342	-18204	-17066	...	204
Exp. sfrd	15	5	4	3	...	0
Exp. b1d	0	-26374	-24822	-17453	...	314
Exp. a0d	-32767	-32483	-32201	-31921	...	-239
Exp. b0d	0	26374	24822	17453	...	-314
Exp. initHandling	0	0	0	0	...	1
Exp. sfrb0	15	15	15	15	...	15
Exp. sfrb1	11	11	11	11	...	11
Exp. b0	-36	-34	-32	-30	...	36
Exp. b1	-20480	-19342	-18204	-17067	...	204

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±1,0000e+00
Tolerance a0d	±1,0000e+00
Tolerance b0d	±1,0000e+00
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±1,0000e+00
Tolerance b1	±1,0000e+00

Test statistics	
Min CPU cycles	5082
Max CPU cycles	14652
Avg CPU cycles	12741

Verification: PIDLimit FiP16 CPU TM4C123GH6

Date of Test 2026-06-19

Target controller TM4C123GH6

Test case: Inport test OK

Inport test for Control block PIDLimit.

Test results						
Time step	1	2	3	4	...	201
CPU cycles	57	57	57	131	...	127
Inputs						
In (DSP)	0	0	0	0	...	0
Init (DSP)	3604	3604	3604	3604	...	3604
max (DSP)	26214	26214	26214	26214	...	26214
min (DSP)	4915	4915	4915	4915	...	4915
Enable (DSP)	0	0	0	1	...	1
In	0	0	0	0	...	0
Init	0.11	0.11	0.11	0.11	...	0.11
max	0.8	0.8	0.8	0.8	...	0.8
min	0.15	0.15	0.15	0.15	...	0.15
Enable	0	0	0	1	...	1
Parameters						
Kp	2					
Ki	2500					
Kd	0.003					
fc	200					
initHandling	initialize integral					
ts_fact	1					
Outputs						
Out	0	0	0	0.15	...	0.649
Exp. Out	0	0	0	0.15	...	0.649
Out (DSP)	0	0	0	4915	...	21273
Exp. Out (DSP)	0	0	0	4915	...	21275

Test settings	
Tolerance Out	±3,0518e-04 (±10 LSB)

Test statistics	
Min CPU cycles	57
Max CPU cycles	133
Avg CPU cycles	124

Test case: Conversion test OK

Conversion test for Control block PIDLimit.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kp	-10	-9.444	-8.889	-8.333	...	10
Ki	-11	-10.389	-9.778	-9.167	...	11
Kd	-10	-9.444	-8.889	-8.333	...	10
fc	0	13.889	27.778	41.667	...	50
initHandling	initialize integral	initialize integral	initialize integral	initialize integral	...	initialize
ts_fact	1	1	1	1	...	1
Controller parameters						
sfrd	15	5	4	3	...	0
b1d	0	-26374	-24822	-17453	...	314
a0d	-32767	-32483	-32201	-31921	...	-239
b0d	0	26374	24822	17453	...	-314
initHandling	0	0	0	0	...	1
sfrb0	15	15	15	15	...	15
sfrb1	11	11	11	11	...	11
b0	-36	-34	-32	-30	...	36
b1	-20480	-19342	-18204	-17067	...	204
Exp. sfrd	15	5	4	3	...	0
Exp. b1d	0	-26374	-24822	-17453	...	314
Exp. a0d	-32767	-32483	-32201	-31921	...	-239
Exp. b0d	0	26374	24822	17453	...	-314
Exp. initHandling	0	0	0	0	...	1
Exp. sfrb0	15	15	15	15	...	15
Exp. sfrb1	11	11	11	11	...	11
Exp. b0	-36	-34	-32	-30	...	36
Exp. b1	-20480	-19342	-18204	-17067	...	204

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±0,0000e+00
Tolerance a0d	±0,0000e+00
Tolerance b0d	±0,0000e+00
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block PIDLimit.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kp	-10	-9.444	-8.889	-8.333	...	10
Ki	-11	-10.389	-9.778	-9.167	...	11
Kd	-10	-9.444	-8.889	-8.333	...	10
fc	0	13.889	27.778	41.667	...	50
initHandling	initialize integral	initialize integral	initialize integral	initialize integral	...	initialize
ts_fact	1	1	1	1	...	1
Controller parameters						
sfrd	15	5	4	3	...	0
b1d	0	-26373	-24822	-17453	...	314
a0d	-32767	-32483	-32201	-31921	...	-239
b0d	0	26373	24822	17453	...	-314
initHandling	0	0	0	0	...	1
sfrb0	15	15	15	15	...	15
sfrb1	11	11	11	11	...	11
b0	-36	-34	-32	-30	...	36
b1	-20480	-19342	-18204	-17066	...	204
Exp. sfrd	15	5	4	3	...	0
Exp. b1d	0	-26374	-24822	-17453	...	314
Exp. a0d	-32767	-32483	-32201	-31921	...	-239
Exp. b0d	0	26374	24822	17453	...	-314
Exp. initHandling	0	0	0	0	...	1
Exp. sfrb0	15	15	15	15	...	15
Exp. sfrb1	11	11	11	11	...	11
Exp. b0	-36	-34	-32	-30	...	36
Exp. b1	-20480	-19342	-18204	-17067	...	204

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±1,0000e+00
Tolerance a0d	±1,0000e+00
Tolerance b0d	±1,0000e+00
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±1,0000e+00
Tolerance b1	±1,0000e+00

Test statistics	
Min CPU cycles	2373
Max CPU cycles	8689
Avg CPU cycles	7188

Verification: PIDLimit FiP16 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for Control block PIDLimit.

Test results						
Time step	1	2	3	4	...	201
CPU cycles	82	82	82	198	...	183
Inputs						
In (DSP)	0	0	0	0	...	0
Init (DSP)	3604	3604	3604	3604	...	3604
max (DSP)	26214	26214	26214	26214	...	26214
min (DSP)	4915	4915	4915	4915	...	4915
Enable (DSP)	0	0	0	1	...	1
In	0	0	0	0	...	0
Init	0.11	0.11	0.11	0.11	...	0.11
max	0.8	0.8	0.8	0.8	...	0.8
min	0.15	0.15	0.15	0.15	...	0.15
Enable	0	0	0	1	...	1
Parameters						
Kp	2					
Ki	2500					
Kd	0.003					
fc	200					
initHandling	initialize integral					
ts_fact	1					
Outputs						
Out	0	0	0	0.15	...	0.649
Exp. Out	0	0	0	0.15	...	0.649
Out (DSP)	0	0	0	4915	...	21273
Exp. Out (DSP)	0	0	0	4915	...	21275

Test settings	
Tolerance Out	±3,0518e-04 (±10 LSB)

Test statistics	
Min CPU cycles	82
Max CPU cycles	198
Avg CPU cycles	169

Test case: Conversion test OK

Conversion test for Control block PIDLimit.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kp	-10	-9.444	-8.889	-8.333	...	10
Ki	-11	-10.389	-9.778	-9.167	...	11
Kd	-10	-9.444	-8.889	-8.333	...	10
fc	0	13.889	27.778	41.667	...	50
initHandling	initialize integral	initialize integral	initialize integral	initialize integral	...	initialize
ts_fact	1	1	1	1	...	1
Controller parameters						
sfrd	15	5	4	3	...	0
b1d	0	-26374	-24822	-17453	...	314
a0d	-32767	-32483	-32201	-31921	...	-239
b0d	0	26374	24822	17453	...	-314
initHandling	0	0	0	0	...	1
sfrb0	15	15	15	15	...	15
sfrb1	11	11	11	11	...	11
b0	-36	-34	-32	-30	...	36
b1	-20480	-19342	-18204	-17067	...	204
Exp. sfrd	15	5	4	3	...	0
Exp. b1d	0	-26374	-24822	-17453	...	314
Exp. a0d	-32767	-32483	-32201	-31921	...	-239
Exp. b0d	0	26374	24822	17453	...	-314
Exp. initHandling	0	0	0	0	...	1
Exp. sfrb0	15	15	15	15	...	15
Exp. sfrb1	11	11	11	11	...	11
Exp. b0	-36	-34	-32	-30	...	36
Exp. b1	-20480	-19342	-18204	-17067	...	204

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±0,0000e+00
Tolerance a0d	±0,0000e+00
Tolerance b0d	±0,0000e+00
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block PIDLimit.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kp	-10	-9.444	-8.889	-8.333	...	10
Ki	-11	-10.389	-9.778	-9.167	...	11
Kd	-10	-9.444	-8.889	-8.333	...	10
fc	0	13.889	27.778	41.667	...	50
initHandling	initialize integral	initialize integral	initialize integral	initialize integral	...	initialize
ts_fact	1	1	1	1	...	1
Controller parameters						
sfrd	15	5	4	3	...	0
b1d	0	-26373	-24822	-17453	...	314
a0d	-32767	-32483	-32201	-31921	...	-239
b0d	0	26373	24822	17453	...	-314
initHandling	0	0	0	0	...	1
sfrb0	15	15	15	15	...	15
sfrb1	11	11	11	11	...	11
b0	-36	-34	-32	-30	...	36
b1	-20480	-19342	-18204	-17066	...	204
Exp. sfrd	15	5	4	3	...	0
Exp. b1d	0	-26374	-24822	-17453	...	314
Exp. a0d	-32767	-32483	-32201	-31921	...	-239
Exp. b0d	0	26374	24822	17453	...	-314
Exp. initHandling	0	0	0	0	...	1
Exp. sfrb0	15	15	15	15	...	15
Exp. sfrb1	11	11	11	11	...	11
Exp. b0	-36	-34	-32	-30	...	36
Exp. b1	-20480	-19342	-18204	-17067	...	204

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±1,0000e+00
Tolerance a0d	±1,0000e+00
Tolerance b0d	±1,0000e+00
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±1,0000e+00
Tolerance b1	±1,0000e+00

Test statistics	
Min CPU cycles	2558
Max CPU cycles	4965
Avg CPU cycles	4412

Verification: PIDLimit FiP16 CPU STM32F072RB

Date of Test 2026-06-19

Target controller STM32F072RB

Test case: Inport test OK

Inport test for Control block PIDLimit.

Test results						
Time step	1	2	3	4	...	201
CPU cycles	76	76	76	187	...	185
Inputs						
In (DSP)	0	0	0	0	...	0
Init (DSP)	3604	3604	3604	3604	...	3604
max (DSP)	26214	26214	26214	26214	...	26214
min (DSP)	4915	4915	4915	4915	...	4915
Enable (DSP)	0	0	0	1	...	1
In	0	0	0	0	...	0
Init	0.11	0.11	0.11	0.11	...	0.11
max	0.8	0.8	0.8	0.8	...	0.8
min	0.15	0.15	0.15	0.15	...	0.15
Enable	0	0	0	1	...	1
Parameters						
Kp	2					
Ki	2500					
Kd	0.003					
fc	200					
initHandling	initialize integral					
ts_fact	1					
Outputs						
Out	0	0	0	0.15	...	0.649
Exp. Out	0	0	0	0.15	...	0.649
Out (DSP)	0	0	0	4915	...	21273
Exp. Out (DSP)	0	0	0	4915	...	21275

Test settings	
Tolerance Out	±3,0518e-04 (±10 LSB)

Test statistics	
Min CPU cycles	76
Max CPU cycles	193
Avg CPU cycles	175

Test case: Conversion test OK

Conversion test for Control block PIDLimit.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kp	-10	-9.444	-8.889	-8.333	...	10
Ki	-11	-10.389	-9.778	-9.167	...	11
Kd	-10	-9.444	-8.889	-8.333	...	10
fc	0	13.889	27.778	41.667	...	50
initHandling	initialize integral	initialize integral	initialize integral	initialize integral	...	initialize
ts_fact	1	1	1	1	...	1
Controller parameters						
sfrd	15	5	4	3	...	0
b1d	0	-26374	-24822	-17453	...	314
a0d	-32767	-32483	-32201	-31921	...	-239
b0d	0	26374	24822	17453	...	-314
initHandling	0	0	0	0	...	1
sfrb0	15	15	15	15	...	15
sfrb1	11	11	11	11	...	11
b0	-36	-34	-32	-30	...	36
b1	-20480	-19342	-18204	-17067	...	204
Exp. sfrd	15	5	4	3	...	0
Exp. b1d	0	-26374	-24822	-17453	...	314
Exp. a0d	-32767	-32483	-32201	-31921	...	-239
Exp. b0d	0	26374	24822	17453	...	-314
Exp. initHandling	0	0	0	0	...	1
Exp. sfrb0	15	15	15	15	...	15
Exp. sfrb1	11	11	11	11	...	11
Exp. b0	-36	-34	-32	-30	...	36
Exp. b1	-20480	-19342	-18204	-17067	...	204

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±0,0000e+00
Tolerance a0d	±0,0000e+00
Tolerance b0d	±0,0000e+00
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block PIDLimit.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kp	-10	-9.444	-8.889	-8.333	...	10
Ki	-11	-10.389	-9.778	-9.167	...	11
Kd	-10	-9.444	-8.889	-8.333	...	10
fc	0	13.889	27.778	41.667	...	50
initHandling	initialize integral	initialize integral	initialize integral	initialize integral	...	initialize
ts_fact	1	1	1	1	...	1
Controller parameters						
sfrd	15	5	4	3	...	0
b1d	0	-26373	-24822	-17453	...	314
a0d	-32767	-32483	-32201	-31921	...	-239
b0d	0	26373	24822	17453	...	-314
initHandling	0	0	0	0	...	1
sfrb0	15	15	15	15	...	15
sfrb1	11	11	11	11	...	11
b0	-36	-34	-32	-30	...	36
b1	-20480	-19342	-18204	-17066	...	204
Exp. sfrd	15	5	4	3	...	0
Exp. b1d	0	-26374	-24822	-17453	...	314
Exp. a0d	-32767	-32483	-32201	-31921	...	-239
Exp. b0d	0	26374	24822	17453	...	-314
Exp. initHandling	0	0	0	0	...	1
Exp. sfrb0	15	15	15	15	...	15
Exp. sfrb1	11	11	11	11	...	11
Exp. b0	-36	-34	-32	-30	...	36
Exp. b1	-20480	-19342	-18204	-17067	...	204

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±1,0000e+00
Tolerance a0d	±1,0000e+00
Tolerance b0d	±1,0000e+00
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±1,0000e+00
Tolerance b1	±1,0000e+00

Test statistics	
Min CPU cycles	9997
Max CPU cycles	23339
Avg CPU cycles	20433

Verification: PIDLimit FiP16 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for Control block PIDLimit.

Test results						
Time step	1	2	3	4	...	201
CPU cycles	31	31	31	108	...	115
Inputs						
In (DSP)	0	0	0	0	...	0
Init (DSP)	3604	3604	3604	3604	...	3604
max (DSP)	26214	26214	26214	26214	...	26214
min (DSP)	4915	4915	4915	4915	...	4915
Enable (DSP)	0	0	0	1	...	1
In	0	0	0	0	...	0
Init	0.11	0.11	0.11	0.11	...	0.11
max	0.8	0.8	0.8	0.8	...	0.8
min	0.15	0.15	0.15	0.15	...	0.15
Enable	0	0	0	1	...	1
Parameters						
Kp	2					
Ki	2500					
Kd	0.003					
fc	200					
initHandling	initialize integral					
ts_fact	1					
Outputs						
Out	0	0	0	0.15	...	0.649
Exp. Out	0	0	0	0.15	...	0.649
Out (DSP)	0	0	0	4915	...	21273
Exp. Out (DSP)	0	0	0	4915	...	21275

Test settings	
Tolerance Out	±3,0518e-04 (±10 LSB)

Test statistics	
Min CPU cycles	31
Max CPU cycles	118
Avg CPU cycles	106

Test case: Conversion test OK

Conversion test for Control block PIDLimit.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kp	-10	-9.444	-8.889	-8.333	...	10
Ki	-11	-10.389	-9.778	-9.167	...	11
Kd	-10	-9.444	-8.889	-8.333	...	10
fc	0	13.889	27.778	41.667	...	50
initHandling	initialize integral	initialize integral	initialize integral	initialize integral	...	initialize
ts_fact	1	1	1	1	...	1
Controller parameters						
sfrd	15	5	4	3	...	0
b1d	0	-26374	-24822	-17453	...	314
a0d	-32767	-32483	-32201	-31921	...	-239
b0d	0	26374	24822	17453	...	-314
initHandling	0	0	0	0	...	1
sfrb0	15	15	15	15	...	15
sfrb1	11	11	11	11	...	11
b0	-36	-34	-32	-30	...	36
b1	-20480	-19342	-18204	-17067	...	204
Exp. sfrd	15	5	4	3	...	0
Exp. b1d	0	-26374	-24822	-17453	...	314
Exp. a0d	-32767	-32483	-32201	-31921	...	-239
Exp. b0d	0	26374	24822	17453	...	-314
Exp. initHandling	0	0	0	0	...	1
Exp. sfrb0	15	15	15	15	...	15
Exp. sfrb1	11	11	11	11	...	11
Exp. b0	-36	-34	-32	-30	...	36
Exp. b1	-20480	-19342	-18204	-17067	...	204

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±0,0000e+00
Tolerance a0d	±0,0000e+00
Tolerance b0d	±0,0000e+00
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block PIDLimit.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kp	-10	-9.444	-8.889	-8.333	...	10
Ki	-11	-10.389	-9.778	-9.167	...	11
Kd	-10	-9.444	-8.889	-8.333	...	10
fc	0	13.889	27.778	41.667	...	50
initHandling	initialize integral	initialize integral	initialize integral	initialize integral	...	initialize
ts_fact	1	1	1	1	...	1
Controller parameters						
sfrd	15	5	4	3	...	0
b1d	0	-26373	-24822	-17453	...	314
a0d	-32767	-32483	-32201	-31921	...	-239
b0d	0	26373	24822	17453	...	-314
initHandling	0	0	0	0	...	1
sfrb0	15	15	15	15	...	15
sfrb1	11	11	11	11	...	11
b0	-36	-34	-32	-30	...	36
b1	-20480	-19342	-18204	-17066	...	204
Exp. sfrd	15	5	4	3	...	0
Exp. b1d	0	-26374	-24822	-17453	...	314
Exp. a0d	-32767	-32483	-32201	-31921	...	-239
Exp. b0d	0	26374	24822	17453	...	-314
Exp. initHandling	0	0	0	0	...	1
Exp. sfrb0	15	15	15	15	...	15
Exp. sfrb1	11	11	11	11	...	11
Exp. b0	-36	-34	-32	-30	...	36
Exp. b1	-20480	-19342	-18204	-17067	...	204

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±1,0000e+00
Tolerance a0d	±1,0000e+00
Tolerance b0d	±1,0000e+00
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±1,0000e+00
Tolerance b1	±1,0000e+00

Test statistics	
Min CPU cycles	3200
Max CPU cycles	8384
Avg CPU cycles	7391

Verification: PIDLimit FiP16 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for Control block PIDLimit.

Test results						
Time step	1	2	3	4	...	201
CPU cycles	82	59	59	197	...	156
Inputs						
In (DSP)	0	0	0	0	...	0
Init (DSP)	3604	3604	3604	3604	...	3604
max (DSP)	26214	26214	26214	26214	...	26214
min (DSP)	4915	4915	4915	4915	...	4915
Enable (DSP)	0	0	0	1	...	1
In	0	0	0	0	...	0
Init	0.11	0.11	0.11	0.11	...	0.11
max	0.8	0.8	0.8	0.8	...	0.8
min	0.15	0.15	0.15	0.15	...	0.15
Enable	0	0	0	1	...	1
Parameters						
Kp	2					
Ki	2500					
Kd	0.003					
fc	200					
initHandling	initialize integral					
ts_fact	1					
Outputs						
Out	0	0	0	0.15	...	0.649
Exp. Out	0	0	0	0.15	...	0.649
Out (DSP)	0	0	0	4915	...	21273
Exp. Out (DSP)	0	0	0	4915	...	21275

Test settings	
Tolerance Out	±3,0518e-04 (±10 LSB)

Test statistics	
Min CPU cycles	59
Max CPU cycles	197
Avg CPU cycles	150

Test case: Conversion test OK

Conversion test for Control block PIDLimit.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kp	-10	-9.444	-8.889	-8.333	...	10
Ki	-11	-10.389	-9.778	-9.167	...	11
Kd	-10	-9.444	-8.889	-8.333	...	10
fc	0	13.889	27.778	41.667	...	50
initHandling	initialize integral	initialize integral	initialize integral	initialize integral	...	initialize
ts_fact	1	1	1	1	...	1
Controller parameters						
sfrd	15	5	4	3	...	0
b1d	0	-26374	-24822	-17453	...	314
a0d	-32767	-32483	-32201	-31921	...	-239
b0d	0	26374	24822	17453	...	-314
initHandling	0	0	0	0	...	1
sfrb0	15	15	15	15	...	15
sfrb1	11	11	11	11	...	11
b0	-36	-34	-32	-30	...	36
b1	-20480	-19342	-18204	-17067	...	204
Exp. sfrd	15	5	4	3	...	0
Exp. b1d	0	-26374	-24822	-17453	...	314
Exp. a0d	-32767	-32483	-32201	-31921	...	-239
Exp. b0d	0	26374	24822	17453	...	-314
Exp. initHandling	0	0	0	0	...	1
Exp. sfrb0	15	15	15	15	...	15
Exp. sfrb1	11	11	11	11	...	11
Exp. b0	-36	-34	-32	-30	...	36
Exp. b1	-20480	-19342	-18204	-17067	...	204

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±0,0000e+00
Tolerance a0d	±0,0000e+00
Tolerance b0d	±0,0000e+00
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block PIDLimit.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kp	-10	-9.444	-8.889	-8.333	...	10
Ki	-11	-10.389	-9.778	-9.167	...	11
Kd	-10	-9.444	-8.889	-8.333	...	10
fc	0	13.889	27.778	41.667	...	50
initHandling	initialize integral	initialize integral	initialize integral	initialize integral	...	initialize
ts_fact	1	1	1	1	...	1
Controller parameters						
sfrd	15	5	4	3	...	0
b1d	0	-26373	-24822	-17453	...	314
a0d	-32767	-32483	-32201	-31921	...	-239
b0d	0	26373	24822	17453	...	-314
initHandling	0	0	0	0	...	1
sfrb0	15	15	15	15	...	15
sfrb1	11	11	11	11	...	11
b0	-36	-34	-32	-30	...	36
b1	-20480	-19342	-18204	-17066	...	204
Exp. sfrd	15	5	4	3	...	0
Exp. b1d	0	-26374	-24822	-17453	...	314
Exp. a0d	-32767	-32483	-32201	-31921	...	-239
Exp. b0d	0	26374	24822	17453	...	-314
Exp. initHandling	0	0	0	0	...	1
Exp. sfrb0	15	15	15	15	...	15
Exp. sfrb1	11	11	11	11	...	11
Exp. b0	-36	-34	-32	-30	...	36
Exp. b1	-20480	-19342	-18204	-17067	...	204

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±1,0000e+00
Tolerance a0d	±1,0000e+00
Tolerance b0d	±1,0000e+00
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±1,0000e+00
Tolerance b1	±1,0000e+00

Test statistics	
Min CPU cycles	2203
Max CPU cycles	4527
Avg CPU cycles	3994

Verification: PIDLimit FiP16 CPU TMS320F28379D

Date of Test 2026-06-22

Target controller TMS320F28379D

Test case: Inport test OK

Inport test for Control block PIDLimit.

Test results						
Time step	1	2	3	4	...	201
CPU cycles	75	75	75	185	...	184
Inputs						
In (DSP)	0	0	0	0	...	0
Init (DSP)	3604	3604	3604	3604	...	3604
max (DSP)	26214	26214	26214	26214	...	26214
min (DSP)	4915	4915	4915	4915	...	4915
Enable (DSP)	0	0	0	1	...	1
In	0	0	0	0	...	0
Init	0.11	0.11	0.11	0.11	...	0.11
max	0.8	0.8	0.8	0.8	...	0.8
min	0.15	0.15	0.15	0.15	...	0.15
Enable	0	0	0	1	...	1
Parameters						
Kp	2					
Ki	2500					
Kd	0.003					
fc	200					
initHandling	initialize integral					
ts_fact	1					
Outputs						
Out	0	0	0	0.15	...	0.649
Exp. Out	0	0	0	0.15	...	0.649
Out (DSP)	0	0	0	4915	...	21273
Exp. Out (DSP)	0	0	0	4915	...	21275

Test settings	
Tolerance Out	±3,0518e-04 (±10 LSB)

Test statistics	
Min CPU cycles	75
Max CPU cycles	190
Avg CPU cycles	180

Test case: Conversion test OK

Conversion test for Control block PIDLimit.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kp	-10	-9.444	-8.889	-8.333	...	10
Ki	-11	-10.389	-9.778	-9.167	...	11
Kd	-10	-9.444	-8.889	-8.333	...	10
fc	0	13.889	27.778	41.667	...	50
initHandling	initialize integral	initialize integral	initialize integral	initialize integral	...	initialize
ts_fact	1	1	1	1	...	1
Controller parameters						
sfrd	15	5	4	3	...	0
b1d	0	-26374	-24822	-17453	...	314
a0d	-32767	-32483	-32201	-31921	...	-239
b0d	0	26374	24822	17453	...	-314
initHandling	0	0	0	0	...	1
sfrb0	15	15	15	15	...	15
sfrb1	11	11	11	11	...	11
b0	-36	-34	-32	-30	...	36
b1	-20480	-19342	-18204	-17067	...	204
Exp. sfrd	15	5	4	3	...	0
Exp. b1d	0	-26374	-24822	-17453	...	314
Exp. a0d	-32767	-32483	-32201	-31921	...	-239
Exp. b0d	0	26374	24822	17453	...	-314
Exp. initHandling	0	0	0	0	...	1
Exp. sfrb0	15	15	15	15	...	15
Exp. sfrb1	11	11	11	11	...	11
Exp. b0	-36	-34	-32	-30	...	36
Exp. b1	-20480	-19342	-18204	-17067	...	204

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±0,0000e+00
Tolerance a0d	±0,0000e+00
Tolerance b0d	±0,0000e+00
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block PIDLimit.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kp	-10	-9.444	-8.889	-8.333	...	10
Ki	-11	-10.389	-9.778	-9.167	...	11
Kd	-10	-9.444	-8.889	-8.333	...	10
fc	0	13.889	27.778	41.667	...	50
initHandling	initialize integral	initialize integral	initialize integral	initialize integral	...	initialize
ts_fact	1	1	1	1	...	1
Controller parameters						
sfrd	15	5	4	3	...	0
b1d	0	-26373	-24822	-17453	...	314
a0d	-32767	-32483	-32201	-31921	...	-239
b0d	0	26373	24822	17453	...	-314
initHandling	0	0	0	0	...	1
sfrb0	15	15	15	15	...	15
sfrb1	11	11	11	11	...	11
b0	-36	-34	-32	-30	...	36
b1	-20480	-19342	-18204	-17066	...	204
Exp. sfrd	15	5	4	3	...	0
Exp. b1d	0	-26374	-24822	-17453	...	314
Exp. a0d	-32767	-32483	-32201	-31921	...	-239
Exp. b0d	0	26374	24822	17453	...	-314
Exp. initHandling	0	0	0	0	...	1
Exp. sfrb0	15	15	15	15	...	15
Exp. sfrb1	11	11	11	11	...	11
Exp. b0	-36	-34	-32	-30	...	36
Exp. b1	-20480	-19342	-18204	-17067	...	204

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±1,0000e+00
Tolerance a0d	±1,0000e+00
Tolerance b0d	±1,0000e+00
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±1,0000e+00
Tolerance b1	±1,0000e+00

Test statistics	
Min CPU cycles	3685
Max CPU cycles	11217
Avg CPU cycles	9708

Verification: PIDLimit FiP16 CPU dsPIC33EP256MC502

Date of Test	2026-06-23
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for Control block PIDLimit.

Test results						
Time step	1	2	3	4	...	201
CPU cycles	55	55	55	162	...	188
Inputs						
In (DSP)	0	0	0	0	...	0
Init (DSP)	3604	3604	3604	3604	...	3604
max (DSP)	26214	26214	26214	26214	...	26214
min (DSP)	4915	4915	4915	4915	...	4915
Enable (DSP)	0	0	0	1	...	1
In	0	0	0	0	...	0
Init	0.11	0.11	0.11	0.11	...	0.11
max	0.8	0.8	0.8	0.8	...	0.8
min	0.15	0.15	0.15	0.15	...	0.15
Enable	0	0	0	1	...	1
Parameters						
Kp	2					
Ki	2500					
Kd	0.003					
fc	200					
initHandling	initialize integral					
ts_fact	1					
Outputs						
Out	0	0	0	0.15	...	0.649
Exp. Out	0	0	0	0.15	...	0.649
Out (DSP)	0	0	0	4915	...	21273
Exp. Out (DSP)	0	0	0	4915	...	21275

Test settings	
Tolerance Out	±3,0518e-04 (±10 LSB)

Test statistics	
Min CPU cycles	55
Max CPU cycles	190
Avg CPU cycles	170

Test case: Conversion test OK

Conversion test for Control block PIDLimit.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kp	-10	-9.444	-8.889	-8.333	...	10
Ki	-11	-10.389	-9.778	-9.167	...	11
Kd	-10	-9.444	-8.889	-8.333	...	10
fc	0	13.889	27.778	41.667	...	50
initHandling	initialize integral	initialize integral	initialize integral	initialize integral	...	initialize
ts_fact	1	1	1	1	...	1
Controller parameters						
sfrd	15	5	4	3	...	0
b1d	0	-26374	-24822	-17453	...	314
a0d	-32767	-32483	-32201	-31921	...	-239
b0d	0	26374	24822	17453	...	-314
initHandling	0	0	0	0	...	1
sfrb0	15	15	15	15	...	15
sfrb1	11	11	11	11	...	11
b0	-36	-34	-32	-30	...	36
b1	-20480	-19342	-18204	-17067	...	204
Exp. sfrd	15	5	4	3	...	0
Exp. b1d	0	-26374	-24822	-17453	...	314
Exp. a0d	-32767	-32483	-32201	-31921	...	-239
Exp. b0d	0	26374	24822	17453	...	-314
Exp. initHandling	0	0	0	0	...	1
Exp. sfrb0	15	15	15	15	...	15
Exp. sfrb1	11	11	11	11	...	11
Exp. b0	-36	-34	-32	-30	...	36
Exp. b1	-20480	-19342	-18204	-17067	...	204

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±0,0000e+00
Tolerance a0d	±0,0000e+00
Tolerance b0d	±0,0000e+00
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block PIDLimit.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kp	-10	-9.444	-8.889	-8.333	...	10
Ki	-11	-10.389	-9.778	-9.167	...	11
Kd	-10	-9.444	-8.889	-8.333	...	10
fc	0	13.889	27.778	41.667	...	50
initHandling	initialize integral	initialize integral	initialize integral	initialize integral	...	initialize
ts_fact	1	1	1	1	...	1
Controller parameters						
sfrd	15	5	4	3	...	0
b1d	0	-26373	-24822	-17453	...	314
a0d	-32767	-32483	-32201	-31921	...	-239
b0d	0	26373	24822	17453	...	-314
initHandling	0	0	0	0	...	1
sfrb0	15	15	15	15	...	15
sfrb1	11	11	11	11	...	11
b0	-36	-34	-32	-30	...	36
b1	-20480	-19342	-18204	-17066	...	204
Exp. sfrd	15	5	4	3	...	0
Exp. b1d	0	-26374	-24822	-17453	...	314
Exp. a0d	-32767	-32483	-32201	-31921	...	-239
Exp. b0d	0	26374	24822	17453	...	-314
Exp. initHandling	0	0	0	0	...	1
Exp. sfrb0	15	15	15	15	...	15
Exp. sfrb1	11	11	11	11	...	11
Exp. b0	-36	-34	-32	-30	...	36
Exp. b1	-20480	-19342	-18204	-17067	...	204

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±1,0000e+00
Tolerance a0d	±1,0000e+00
Tolerance b0d	±1,0000e+00
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±1,0000e+00
Tolerance b1	±1,0000e+00

Test statistics	
Min CPU cycles	14127
Max CPU cycles	48820
Avg CPU cycles	42388

Verification: PIDLimit FiP32 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for Control block PIDLimit.

Test results				
Time step	1	2	...	201
CPU cycles	85	85	...	426
Inputs				
In (DSP)	0	0	...	0
Init (DSP)	236223201	236223201	...	236223201
max (DSP)	1717986918	1717986918	...	1717986918
min (DSP)	322122547	322122547	...	322122547
Enable (DSP)	0	0	...	1
In	0	0	...	0
Init	0.11	0.11	...	0.11
max	0.8	0.8	...	0.8
min	0.15	0.15	...	0.15
Enable	0	0	...	1
Parameters				
Kp	2			
Ki	2500			
Kd	0.003			
fc	200			
initHandling	initialize integral			
ts_fact	1			
Outputs				
Out	0	0	...	0.649
Exp. Out	0	0	...	0.649
Out (DSP)	0	0	...	1394267794
Exp. Out (DSP)	0	0	...	1394267794

Test settings	
Tolerance Out	±3,0518e-05 (±65536 LSB)

Test statistics	
Min CPU cycles	85
Max CPU cycles	458
Avg CPU cycles	403

Test case: Conversion test OK

Conversion test for Control block PIDLimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
sfrd	31	21	...	16
b1d	0	-1728437568	...	2058874161
a0d	-2147483647	-2128824851	...	-1568527835
b0d	0	1728437568	...	-2058874161
initHandling	0	0	...	1
sfrb0	31	31	...	31
sfrb1	27	27	...	27
b0	-2362232	-2230997	...	2362232
b1	-1342177280	-1267611876	...	1342177280
Exp. sfrd	31	21	...	16
Exp. b1d	0	-1728437568	...	2058874161
Exp. a0d	-2147483647	-2128824851	...	-1568527835
Exp. b0d	0	1728437568	...	-2058874161
Exp. initHandling	0	0	...	1
Exp. sfrb0	31	31	...	31
Exp. sfrb1	27	27	...	27
Exp. b0	-2362232	-2230997	...	2362232
Exp. b1	-1342177280	-1267611876	...	1342177280

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±0,0000e+00
Tolerance a0d	±0,0000e+00
Tolerance b0d	±0,0000e+00
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block PIDLimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
sfrd	31	21	...	16
b1d	0	-1728437632	...	2058874240
a0d	-2147483647	-2128824832	...	-1568527872
b0d	0	1728437632	...	-2058874240
initHandling	0	0	...	1
sfrb0	31	31	...	31
sfrb1	27	27	...	27
b0	-2362232	-2230997	...	2362232
b1	-1342177280	-1267611904	...	1342177280
Exp. sfrd	31	21	...	16
Exp. b1d	0	-1728437568	...	2058874161
Exp. a0d	-2147483647	-2128824851	...	-1568527835
Exp. b0d	0	1728437568	...	-2058874161
Exp. initHandling	0	0	...	1
Exp. sfrb0	31	31	...	31
Exp. sfrb1	27	27	...	27
Exp. b0	-2362232	-2230997	...	2362232
Exp. b1	-1342177280	-1267611876	...	1342177280

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±2,0000e+02
Tolerance a0d	±2,0000e+02
Tolerance b0d	±2,0000e+02
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±1,0000e+00
Tolerance b1	±1,0000e+02

Test statistics	
Min CPU cycles	6090
Max CPU cycles	16311
Avg CPU cycles	13994

Verification: PIDLimit FiP32 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for Control block PIDLimit.

Test results				
Time step	1	2	...	201
CPU cycles	63	63	...	251
Inputs				
In (DSP)	0	0	...	0
Init (DSP)	236223201	236223201	...	236223201
max (DSP)	1717986918	1717986918	...	1717986918
min (DSP)	322122547	322122547	...	322122547
Enable (DSP)	0	0	...	1
In	0	0	...	0
Init	0.11	0.11	...	0.11
max	0.8	0.8	...	0.8
min	0.15	0.15	...	0.15
Enable	0	0	...	1
Parameters				
Kp	2			
Ki	2500			
Kd	0.003			
fc	200			
initHandling	initialize integral			
ts_fact	1			
Outputs				
Out	0	0	...	0.649
Exp. Out	0	0	...	0.649
Out (DSP)	0	0	...	1394267794
Exp. Out (DSP)	0	0	...	1394267794

Test settings	
Tolerance Out	±3,0518e-05 (±65536 LSB)

Test statistics	
Min CPU cycles	63
Max CPU cycles	251
Avg CPU cycles	228

Test case: Conversion test OK

Conversion test for Control block PIDLimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
sfrd	31	21	...	16
b1d	0	-1728437568	...	2058874161
a0d	-2147483647	-2128824851	...	-1568527835
b0d	0	1728437568	...	-2058874161
initHandling	0	0	...	1
sfrb0	31	31	...	31
sfrb1	27	27	...	27
b0	-2362232	-2230997	...	2362232
b1	-1342177280	-1267611876	...	1342177280
Exp. sfrd	31	21	...	16
Exp. b1d	0	-1728437568	...	2058874161
Exp. a0d	-2147483647	-2128824851	...	-1568527835
Exp. b0d	0	1728437568	...	-2058874161
Exp. initHandling	0	0	...	1
Exp. sfrb0	31	31	...	31
Exp. sfrb1	27	27	...	27
Exp. b0	-2362232	-2230997	...	2362232
Exp. b1	-1342177280	-1267611876	...	1342177280

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±0,0000e+00
Tolerance a0d	±0,0000e+00
Tolerance b0d	±0,0000e+00
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block PIDLimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
sfrd	31	21	...	16
b1d	0	-1728437632	...	2058874240
a0d	-2147483647	-2128824832	...	-1568527872
b0d	0	1728437632	...	-2058874240
initHandling	0	0	...	1
sfrb0	31	31	...	31
sfrb1	27	27	...	27
b0	-2362232	-2230997	...	2362232
b1	-1342177280	-1267611904	...	1342177280
Exp. sfrd	31	21	...	16
Exp. b1d	0	-1728437568	...	2058874161
Exp. a0d	-2147483647	-2128824851	...	-1568527835
Exp. b0d	0	1728437568	...	-2058874161
Exp. initHandling	0	0	...	1
Exp. sfrb0	31	31	...	31
Exp. sfrb1	27	27	...	27
Exp. b0	-2362232	-2230997	...	2362232
Exp. b1	-1342177280	-1267611876	...	1342177280

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±2,0000e+02
Tolerance a0d	±2,0000e+02
Tolerance b0d	±2,0000e+02
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±1,0000e+00
Tolerance b1	±1,0000e+02

Test statistics	
Min CPU cycles	2341
Max CPU cycles	6943
Avg CPU cycles	5862

Verification: PIDLimit FiP32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for Control block PIDLimit.

Test results				
Time step	1	2	...	201
CPU cycles	90	90	...	281
Inputs				
In (DSP)	0	0	...	0
Init (DSP)	236223201	236223201	...	236223201
max (DSP)	1717986918	1717986918	...	1717986918
min (DSP)	322122547	322122547	...	322122547
Enable (DSP)	0	0	...	1
In	0	0	...	0
Init	0.11	0.11	...	0.11
max	0.8	0.8	...	0.8
min	0.15	0.15	...	0.15
Enable	0	0	...	1
Parameters				
Kp	2			
Ki	2500			
Kd	0.003			
fc	200			
initHandling	initialize integral			
ts_fact	1			
Outputs				
Out	0	0	...	0.649
Exp. Out	0	0	...	0.649
Out (DSP)	0	0	...	1394267794
Exp. Out (DSP)	0	0	...	1394267794

Test settings	
Tolerance Out	±3,0518e-05 (±65536 LSB)

Test statistics	
Min CPU cycles	90
Max CPU cycles	334
Avg CPU cycles	253

Test case: Conversion test OK

Conversion test for Control block PIDLimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
sfrd	31	21	...	16
b1d	0	-1728437568	...	2058874161
a0d	-2147483647	-2128824851	...	-1568527835
b0d	0	1728437568	...	-2058874161
initHandling	0	0	...	1
sfrb0	31	31	...	31
sfrb1	27	27	...	27
b0	-2362232	-2230997	...	2362232
b1	-1342177280	-1267611876	...	1342177280
Exp. sfrd	31	21	...	16
Exp. b1d	0	-1728437568	...	2058874161
Exp. a0d	-2147483647	-2128824851	...	-1568527835
Exp. b0d	0	1728437568	...	-2058874161
Exp. initHandling	0	0	...	1
Exp. sfrb0	31	31	...	31
Exp. sfrb1	27	27	...	27
Exp. b0	-2362232	-2230997	...	2362232
Exp. b1	-1342177280	-1267611876	...	1342177280

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±0,0000e+00
Tolerance a0d	±0,0000e+00
Tolerance b0d	±0,0000e+00
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block PIDLimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
sfrd	31	21	...	16
b1d	0	-1728437632	...	2058874240
a0d	-2147483647	-2128824832	...	-1568527872
b0d	0	1728437632	...	-2058874240
initHandling	0	0	...	1
sfrb0	31	31	...	31
sfrb1	27	27	...	27
b0	-2362232	-2230997	...	2362232
b1	-1342177280	-1267611904	...	1342177280
Exp. sfrd	31	21	...	16
Exp. b1d	0	-1728437568	...	2058874161
Exp. a0d	-2147483647	-2128824851	...	-1568527835
Exp. b0d	0	1728437568	...	-2058874161
Exp. initHandling	0	0	...	1
Exp. sfrb0	31	31	...	31
Exp. sfrb1	27	27	...	27
Exp. b0	-2362232	-2230997	...	2362232
Exp. b1	-1342177280	-1267611876	...	1342177280

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±2,0000e+02
Tolerance a0d	±2,0000e+02
Tolerance b0d	±2,0000e+02
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±1,0000e+00
Tolerance b1	±1,0000e+02

Test statistics	
Min CPU cycles	3841
Max CPU cycles	6358
Avg CPU cycles	5749

Verification: PIDLimit FiP32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for Control block PIDLimit.

Test results				
Time step	1	2	...	201
CPU cycles	90	90	...	676
Inputs				
In (DSP)	0	0	...	0
Init (DSP)	236223201	236223201	...	236223201
max (DSP)	1717986918	1717986918	...	1717986918
min (DSP)	322122547	322122547	...	322122547
Enable (DSP)	0	0	...	1
In	0	0	...	0
Init	0.11	0.11	...	0.11
max	0.8	0.8	...	0.8
min	0.15	0.15	...	0.15
Enable	0	0	...	1
Parameters				
Kp	2			
Ki	2500			
Kd	0.003			
fc	200			
initHandling	initialize integral			
ts_fact	1			
Outputs				
Out	0	0	...	0.649
Exp. Out	0	0	...	0.649
Out (DSP)	0	0	...	1394267794
Exp. Out (DSP)	0	0	...	1394267794

Test settings	
Tolerance Out	±3,0518e-05 (±65536 LSB)

Test statistics	
Min CPU cycles	90
Max CPU cycles	735
Avg CPU cycles	609

Test case: Conversion test OK

Conversion test for Control block PIDLimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
sfrd	31	21	...	16
b1d	0	-1728437568	...	2058874161
a0d	-2147483647	-2128824851	...	-1568527835
b0d	0	1728437568	...	-2058874161
initHandling	0	0	...	1
sfrb0	31	31	...	31
sfrb1	27	27	...	27
b0	-2362232	-2230997	...	2362232
b1	-1342177280	-1267611876	...	1342177280
Exp. sfrd	31	21	...	16
Exp. b1d	0	-1728437568	...	2058874161
Exp. a0d	-2147483647	-2128824851	...	-1568527835
Exp. b0d	0	1728437568	...	-2058874161
Exp. initHandling	0	0	...	1
Exp. sfrb0	31	31	...	31
Exp. sfrb1	27	27	...	27
Exp. b0	-2362232	-2230997	...	2362232
Exp. b1	-1342177280	-1267611876	...	1342177280

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±0,0000e+00
Tolerance a0d	±0,0000e+00
Tolerance b0d	±0,0000e+00
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block PIDLimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
sfrd	31	21	...	16
b1d	0	-1728437632	...	2058874240
a0d	-2147483647	-2128824832	...	-1568527872
b0d	0	1728437632	...	-2058874240
initHandling	0	0	...	1
sfrb0	31	31	...	31
sfrb1	27	27	...	27
b0	-2362232	-2230997	...	2362232
b1	-1342177280	-1267611904	...	1342177280
Exp. sfrd	31	21	...	16
Exp. b1d	0	-1728437568	...	2058874161
Exp. a0d	-2147483647	-2128824851	...	-1568527835
Exp. b0d	0	1728437568	...	-2058874161
Exp. initHandling	0	0	...	1
Exp. sfrb0	31	31	...	31
Exp. sfrb1	27	27	...	27
Exp. b0	-2362232	-2230997	...	2362232
Exp. b1	-1342177280	-1267611876	...	1342177280

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±2,0000e+02
Tolerance a0d	±2,0000e+02
Tolerance b0d	±2,0000e+02
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±1,0000e+00
Tolerance b1	±1,0000e+02

Test statistics	
Min CPU cycles	15408
Max CPU cycles	29717
Avg CPU cycles	26731

Verification: PIDLimit FiP32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for Control block PIDLimit.

Test results				
Time step	1	2	...	201
CPU cycles	31	31	...	204
Inputs				
In (DSP)	0	0	...	0
Init (DSP)	236223201	236223201	...	236223201
max (DSP)	1717986918	1717986918	...	1717986918
min (DSP)	322122547	322122547	...	322122547
Enable (DSP)	0	0	...	1
In	0	0	...	0
Init	0.11	0.11	...	0.11
max	0.8	0.8	...	0.8
min	0.15	0.15	...	0.15
Enable	0	0	...	1
Parameters				
Kp	2			
Ki	2500			
Kd	0.003			
fc	200			
initHandling	initialize integral			
ts_fact	1			
Outputs				
Out	0	0	...	0.649
Exp. Out	0	0	...	0.649
Out (DSP)	0	0	...	1394267794
Exp. Out (DSP)	0	0	...	1394267794

Test settings	
Tolerance Out	±3,0518e-05 (±65536 LSB)

Test statistics	
Min CPU cycles	31
Max CPU cycles	204
Avg CPU cycles	182

Test case: Conversion test OK

Conversion test for Control block PIDLimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
sfrd	31	21	...	16
b1d	0	-1728437568	...	2058874161
a0d	-2147483647	-2128824851	...	-1568527835
b0d	0	1728437568	...	-2058874161
initHandling	0	0	...	1
sfrb0	31	31	...	31
sfrb1	27	27	...	27
b0	-2362232	-2230997	...	2362232
b1	-1342177280	-1267611876	...	1342177280
Exp. sfrd	31	21	...	16
Exp. b1d	0	-1728437568	...	2058874161
Exp. a0d	-2147483647	-2128824851	...	-1568527835
Exp. b0d	0	1728437568	...	-2058874161
Exp. initHandling	0	0	...	1
Exp. sfrb0	31	31	...	31
Exp. sfrb1	27	27	...	27
Exp. b0	-2362232	-2230997	...	2362232
Exp. b1	-1342177280	-1267611876	...	1342177280

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±0,0000e+00
Tolerance a0d	±0,0000e+00
Tolerance b0d	±0,0000e+00
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block PIDLimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
sfrd	31	21	...	16
b1d	0	-1728437632	...	2058874240
a0d	-2147483647	-2128824832	...	-1568527872
b0d	0	1728437632	...	-2058874240
initHandling	0	0	...	1
sfrb0	31	31	...	31
sfrb1	27	27	...	27
b0	-2362232	-2230997	...	2362232
b1	-1342177280	-1267611904	...	1342177280
Exp. sfrd	31	21	...	16
Exp. b1d	0	-1728437568	...	2058874161
Exp. a0d	-2147483647	-2128824851	...	-1568527835
Exp. b0d	0	1728437568	...	-2058874161
Exp. initHandling	0	0	...	1
Exp. sfrb0	31	31	...	31
Exp. sfrb1	27	27	...	27
Exp. b0	-2362232	-2230997	...	2362232
Exp. b1	-1342177280	-1267611876	...	1342177280

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±2,0000e+02
Tolerance a0d	±2,0000e+02
Tolerance b0d	±2,0000e+02
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±1,0000e+00
Tolerance b1	±1,0000e+02

Test statistics	
Min CPU cycles	5332
Max CPU cycles	10879
Avg CPU cycles	9677

Verification: PIDLimit FiP32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for Control block PIDLimit.

Test results				
Time step	1	2	...	201
CPU cycles	81	59	...	258
Inputs				
In (DSP)	0	0	...	0
Init (DSP)	236223201	236223201	...	236223201
max (DSP)	1717986918	1717986918	...	1717986918
min (DSP)	322122547	322122547	...	322122547
Enable (DSP)	0	0	...	1
In	0	0	...	0
Init	0.11	0.11	...	0.11
max	0.8	0.8	...	0.8
min	0.15	0.15	...	0.15
Enable	0	0	...	1
Parameters				
Kp	2			
Ki	2500			
Kd	0.003			
fc	200			
initHandling	initialize integral			
ts_fact	1			
Outputs				
Out	0	0	...	0.649
Exp. Out	0	0	...	0.649
Out (DSP)	0	0	...	1394267794
Exp. Out (DSP)	0	0	...	1394267794

Test settings	
Tolerance Out	±3,0518e-05 (±65536 LSB)

Test statistics	
Min CPU cycles	59
Max CPU cycles	291
Avg CPU cycles	242

Test case: Conversion test OK

Conversion test for Control block PIDLimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
sfrd	31	21	...	16
b1d	0	-1728437568	...	2058874161
a0d	-2147483647	-2128824851	...	-1568527835
b0d	0	1728437568	...	-2058874161
initHandling	0	0	...	1
sfrb0	31	31	...	31
sfrb1	27	27	...	27
b0	-2362232	-2230997	...	2362232
b1	-1342177280	-1267611876	...	1342177280
Exp. sfrd	31	21	...	16
Exp. b1d	0	-1728437568	...	2058874161
Exp. a0d	-2147483647	-2128824851	...	-1568527835
Exp. b0d	0	1728437568	...	-2058874161
Exp. initHandling	0	0	...	1
Exp. sfrb0	31	31	...	31
Exp. sfrb1	27	27	...	27
Exp. b0	-2362232	-2230997	...	2362232
Exp. b1	-1342177280	-1267611876	...	1342177280

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±0,0000e+00
Tolerance a0d	±0,0000e+00
Tolerance b0d	±0,0000e+00
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block PIDLimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
sfrd	31	21	...	16
b1d	0	-1728437632	...	2058874240
a0d	-2147483647	-2128824832	...	-1568527872
b0d	0	1728437632	...	-2058874240
initHandling	0	0	...	1
sfrb0	31	31	...	31
sfrb1	27	27	...	27
b0	-2362232	-2230997	...	2362232
b1	-1342177280	-1267611904	...	1342177280
Exp. sfrd	31	21	...	16
Exp. b1d	0	-1728437568	...	2058874161
Exp. a0d	-2147483647	-2128824851	...	-1568527835
Exp. b0d	0	1728437568	...	-2058874161
Exp. initHandling	0	0	...	1
Exp. sfrb0	31	31	...	31
Exp. sfrb1	27	27	...	27
Exp. b0	-2362232	-2230997	...	2362232
Exp. b1	-1342177280	-1267611876	...	1342177280

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±2,0000e+02
Tolerance a0d	±2,0000e+02
Tolerance b0d	±2,0000e+02
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±1,0000e+00
Tolerance b1	±1,0000e+02

Test statistics	
Min CPU cycles	3423
Max CPU cycles	5798
Avg CPU cycles	5275

Verification: PIDLimit FiP32 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for Control block PIDLimit.

Test results				
Time step	1	2	...	201
CPU cycles	73	73	...	370
Inputs				
In (DSP)	0	0	...	0
Init (DSP)	236223201	236223201	...	236223201
max (DSP)	1717986918	1717986918	...	1717986918
min (DSP)	322122547	322122547	...	322122547
Enable (DSP)	0	0	...	1
In	0	0	...	0
Init	0.11	0.11	...	0.11
max	0.8	0.8	...	0.8
min	0.15	0.15	...	0.15
Enable	0	0	...	1
Parameters				
Kp	2			
Ki	2500			
Kd	0.003			
fc	200			
initHandling	initialize integral			
ts_fact	1			
Outputs				
Out	0	0	...	0.649
Exp. Out	0	0	...	0.649
Out (DSP)	0	0	...	1394267794
Exp. Out (DSP)	0	0	...	1394267794

Test settings	
Tolerance Out	±3,0518e-05 (±65536 LSB)

Test statistics	
Min CPU cycles	73
Max CPU cycles	390
Avg CPU cycles	352

Test case: Conversion test OK

Conversion test for Control block PIDLimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
sfrd	31	21	...	16
b1d	0	-1728437568	...	2058874161
a0d	-2147483647	-2128824851	...	-1568527835
b0d	0	1728437568	...	-2058874161
initHandling	0	0	...	1
sfrb0	31	31	...	31
sfrb1	27	27	...	27
b0	-2362232	-2230997	...	2362232
b1	-1342177280	-1267611876	...	1342177280
Exp. sfrd	31	21	...	16
Exp. b1d	0	-1728437568	...	2058874161
Exp. a0d	-2147483647	-2128824851	...	-1568527835
Exp. b0d	0	1728437568	...	-2058874161
Exp. initHandling	0	0	...	1
Exp. sfrb0	31	31	...	31
Exp. sfrb1	27	27	...	27
Exp. b0	-2362232	-2230997	...	2362232
Exp. b1	-1342177280	-1267611876	...	1342177280

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±0,0000e+00
Tolerance a0d	±0,0000e+00
Tolerance b0d	±0,0000e+00
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block PIDLimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
sfrd	31	21	...	16
b1d	0	-1728437632	...	2058874240
a0d	-2147483647	-2128824832	...	-1568527872
b0d	0	1728437632	...	-2058874240
initHandling	0	0	...	1
sfrb0	31	31	...	31
sfrb1	27	27	...	27
b0	-2362232	-2230997	...	2362232
b1	-1342177280	-1267611904	...	1342177280
Exp. sfrd	31	21	...	16
Exp. b1d	0	-1728437568	...	2058874161
Exp. a0d	-2147483647	-2128824851	...	-1568527835
Exp. b0d	0	1728437568	...	-2058874161
Exp. initHandling	0	0	...	1
Exp. sfrb0	31	31	...	31
Exp. sfrb1	27	27	...	27
Exp. b0	-2362232	-2230997	...	2362232
Exp. b1	-1342177280	-1267611876	...	1342177280

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±2,0000e+02
Tolerance a0d	±2,0000e+02
Tolerance b0d	±2,0000e+02
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±1,0000e+00
Tolerance b1	±1,0000e+02

Test statistics	
Min CPU cycles	4343
Max CPU cycles	12410
Avg CPU cycles	10577

Verification: PIDLimit FiP32 CPU dsPIC33EP256MC502

Date of Test	2026-06-23
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for Control block PIDLimit.

Test results				
Time step	1	2	...	201
CPU cycles	64	64	...	1377
Inputs				
In (DSP)	0	0	...	0
Init (DSP)	236223201	236223201	...	236223201
max (DSP)	1717986918	1717986918	...	1717986918
min (DSP)	322122547	322122547	...	322122547
Enable (DSP)	0	0	...	1
In	0	0	...	0
Init	0.11	0.11	...	0.11
max	0.8	0.8	...	0.8
min	0.15	0.15	...	0.15
Enable	0	0	...	1
Parameters				
Kp	2			
Ki	2500			
Kd	0.003			
fc	200			
initHandling	initialize integral			
ts_fact	1			
Outputs				
Out	0	0	...	0.649
Exp. Out	0	0	...	0.649
Out (DSP)	0	0	...	1394267794
Exp. Out (DSP)	0	0	...	1394267794

Test settings	
Tolerance Out	±3,0518e-05 (±65536 LSB)

Test statistics	
Min CPU cycles	64
Max CPU cycles	1400
Avg CPU cycles	1303

Test case: Conversion test OK

Conversion test for Control block PIDLimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
sfrd	31	21	...	16
b1d	0	-1728437568	...	2058874161
a0d	-2147483647	-2128824851	...	-1568527835
b0d	0	1728437568	...	-2058874161
initHandling	0	0	...	1
sfrb0	31	31	...	31
sfrb1	27	27	...	27
b0	-2362232	-2230997	...	2362232
b1	-1342177280	-1267611876	...	1342177280
Exp. sfrd	31	21	...	16
Exp. b1d	0	-1728437568	...	2058874161
Exp. a0d	-2147483647	-2128824851	...	-1568527835
Exp. b0d	0	1728437568	...	-2058874161
Exp. initHandling	0	0	...	1
Exp. sfrb0	31	31	...	31
Exp. sfrb1	27	27	...	27
Exp. b0	-2362232	-2230997	...	2362232
Exp. b1	-1342177280	-1267611876	...	1342177280

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±0,0000e+00
Tolerance a0d	±0,0000e+00
Tolerance b0d	±0,0000e+00
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block PIDLimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
sfrd	31	21	...	16
b1d	0	-1728437632	...	2058874240
a0d	-2147483647	-2128824832	...	-1568527872
b0d	0	1728437632	...	-2058874240
initHandling	0	0	...	1
sfrb0	31	31	...	31
sfrb1	27	27	...	27
b0	-2362232	-2230997	...	2362232
b1	-1342177280	-1267611904	...	1342177280
Exp. sfrd	31	21	...	16
Exp. b1d	0	-1728437568	...	2058874161
Exp. a0d	-2147483647	-2128824851	...	-1568527835
Exp. b0d	0	1728437568	...	-2058874161
Exp. initHandling	0	0	...	1
Exp. sfrb0	31	31	...	31
Exp. sfrb1	27	27	...	27
Exp. b0	-2362232	-2230997	...	2362232
Exp. b1	-1342177280	-1267611876	...	1342177280

Test settings	
Tolerance sfrd	±0,0000e+00
Tolerance b1d	±2,0000e+02
Tolerance a0d	±2,0000e+02
Tolerance b0d	±2,0000e+02
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±1,0000e+00
Tolerance b1	±1,0000e+02

Test statistics	
Min CPU cycles	15980
Max CPU cycles	50882
Avg CPU cycles	43326

Verification: PIDLimit Float32 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for Control block PIDLimit.

Test results				
Time step	1	2	...	201
CPU cycles	87	87	...	168
Inputs				
In (DSP)	0	0	...	0
Init (DSP)	0.11	0.11	...	0.11
max (DSP)	0.8	0.8	...	0.8
min (DSP)	0.15	0.15	...	0.15
Enable (DSP)	0	0	...	1
In	0	0	...	0
Init	0.11	0.11	...	0.11
max	0.8	0.8	...	0.8
min	0.15	0.15	...	0.15
Enable	0	0	...	1
Parameters				
Kp	2			
Ki	2500			
Kd	0.003			
fc	200			
initHandling	initialize integral			
ts_fact	1			
Outputs				
Out	0	0	...	0.649
Exp. Out	0	0	...	0.649
Out (DSP)	0	0	...	0.649
Exp. Out (DSP)	0	0	...	0.649

Test settings	
Tolerance Out	±9,3132e-07 (±2000 LSB)

Test statistics	
Min CPU cycles	87
Max CPU cycles	181
Avg CPU cycles	163

Test case: Conversion test OK

Conversion test for Control block PIDLimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
b1d	0	-824.183	...	31415.927
a0d	-1	-0.991	...	-0.73
b0d	0	824.183	...	-31415.927
initHandling	0	0	...	1
b0	-0.001	-0.001	...	0.001
b1	-10	-9.444	...	10
Exp. b1d	0	-824.183	...	31415.927
Exp. a0d	-1	-0.991	...	-0.73
Exp. b0d	0	824.183	...	-31415.927
Exp. initHandling	0	0	...	1
Exp. b0	-0.001	-0.001	...	0.001
Exp. b1	-10	-9.444	...	10

Test settings	
Tolerance b1d	±0,0000e+00
Tolerance a0d	±1,0000e-15
Tolerance b0d	±0,0000e+00
Tolerance initHandling	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block PIDLimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
b1d	0	-824.183	...	31415.928
a0d	-1	-0.991	...	-0.73
b0d	0	824.183	...	-31415.928
initHandling	0	0	...	1
b0	-0.001	-0.001	...	0.001
b1	-10	-9.444	...	10
Exp. b1d	0	-824.183	...	31415.927
Exp. a0d	-1	-0.991	...	-0.73
Exp. b0d	0	824.183	...	-31415.927
Exp. initHandling	0	0	...	1
Exp. b0	-0.001	-0.001	...	0.001
Exp. b1	-10	-9.444	...	10

Test settings	
Tolerance b1d	±3,0000e-03
Tolerance a0d	±1,0000e-07
Tolerance b0d	±3,0000e-03
Tolerance initHandling	±0,0000e+00
Tolerance b0	±1,0000e-10
Tolerance b1	±1,0000e-06

Test statistics	
Min CPU cycles	2933
Max CPU cycles	3298
Avg CPU cycles	3257

Verification: PIDLimit Float32 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for Control block PIDLimit.

Test results				
Time step	1	2	...	201
CPU cycles	45	45	...	123
Inputs				
In (DSP)	0	0	...	0
Init (DSP)	0.11	0.11	...	0.11
max (DSP)	0.8	0.8	...	0.8
min (DSP)	0.15	0.15	...	0.15
Enable (DSP)	0	0	...	1
In	0	0	...	0
Init	0.11	0.11	...	0.11
max	0.8	0.8	...	0.8
min	0.15	0.15	...	0.15
Enable	0	0	...	1
Parameters				
Kp	2			
Ki	2500			
Kd	0.003			
fc	200			
initHandling	initialize integral			
ts_fact	1			
Outputs				
Out	0	0	...	0.649
Exp. Out	0	0	...	0.649
Out (DSP)	0	0	...	0.649
Exp. Out (DSP)	0	0	...	0.649

Test settings	
Tolerance Out	±9,3132e-07 (±2000 LSB)

Test statistics	
Min CPU cycles	45
Max CPU cycles	131
Avg CPU cycles	118

Test case: Conversion test OK

Conversion test for Control block PIDLimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
b1d	0	-824.183	...	31415.927
a0d	-1	-0.991	...	-0.73
b0d	0	824.183	...	-31415.927
initHandling	0	0	...	1
b0	-0.001	-0.001	...	0.001
b1	-10	-9.444	...	10
Exp. b1d	0	-824.183	...	31415.927
Exp. a0d	-1	-0.991	...	-0.73
Exp. b0d	0	824.183	...	-31415.927
Exp. initHandling	0	0	...	1
Exp. b0	-0.001	-0.001	...	0.001
Exp. b1	-10	-9.444	...	10

Test settings	
Tolerance b1d	±0,0000e+00
Tolerance a0d	±1,0000e-15
Tolerance b0d	±0,0000e+00
Tolerance initHandling	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block PIDLimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
b1d	0	-824.183	...	31415.928
a0d	-1	-0.991	...	-0.73
b0d	0	824.183	...	-31415.928
initHandling	0	0	...	1
b0	-0.001	-0.001	...	0.001
b1	-10	-9.444	...	10
Exp. b1d	0	-824.183	...	31415.927
Exp. a0d	-1	-0.991	...	-0.73
Exp. b0d	0	824.183	...	-31415.927
Exp. initHandling	0	0	...	1
Exp. b0	-0.001	-0.001	...	0.001
Exp. b1	-10	-9.444	...	10

Test settings	
Tolerance b1d	±3,0000e-03
Tolerance a0d	±1,0000e-07
Tolerance b0d	±3,0000e-03
Tolerance initHandling	±0,0000e+00
Tolerance b0	±1,0000e-10
Tolerance b1	±1,0000e-06

Test statistics	
Min CPU cycles	1309
Max CPU cycles	1355
Avg CPU cycles	1351

Verification: PIDLimit Float32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for Control block PIDLimit.

Test results				
Time step	1	2	...	201
CPU cycles	73	73	...	173
Inputs				
In (DSP)	0	0	...	0
Init (DSP)	0.11	0.11	...	0.11
max (DSP)	0.8	0.8	...	0.8
min (DSP)	0.15	0.15	...	0.15
Enable (DSP)	0	0	...	1
In	0	0	...	0
Init	0.11	0.11	...	0.11
max	0.8	0.8	...	0.8
min	0.15	0.15	...	0.15
Enable	0	0	...	1
Parameters				
Kp	2			
Ki	2500			
Kd	0.003			
fc	200			
initHandling	initialize integral			
ts_fact	1			
Outputs				
Out	0	0	...	0.649
Exp. Out	0	0	...	0.649
Out (DSP)	0	0	...	0.649
Exp. Out (DSP)	0	0	...	0.649

Test settings	
Tolerance Out	±9,3132e-07 (±2000 LSB)

Test statistics	
Min CPU cycles	73
Max CPU cycles	174
Avg CPU cycles	155

Test case: Conversion test OK

Conversion test for Control block PIDLimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
b1d	0	-824.183	...	31415.927
a0d	-1	-0.991	...	-0.73
b0d	0	824.183	...	-31415.927
initHandling	0	0	...	1
b0	-0.001	-0.001	...	0.001
b1	-10	-9.444	...	10
Exp. b1d	0	-824.183	...	31415.927
Exp. a0d	-1	-0.991	...	-0.73
Exp. b0d	0	824.183	...	-31415.927
Exp. initHandling	0	0	...	1
Exp. b0	-0.001	-0.001	...	0.001
Exp. b1	-10	-9.444	...	10

Test settings	
Tolerance b1d	±0,0000e+00
Tolerance a0d	±1,0000e-15
Tolerance b0d	±0,0000e+00
Tolerance initHandling	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block PIDLimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
b1d	0	-824.183	...	31415.928
a0d	-1	-0.991	...	-0.73
b0d	0	824.183	...	-31415.928
initHandling	0	0	...	1
b0	-0.001	-0.001	...	0.001
b1	-10	-9.444	...	10
Exp. b1d	0	-824.183	...	31415.927
Exp. a0d	-1	-0.991	...	-0.73
Exp. b0d	0	824.183	...	-31415.927
Exp. initHandling	0	0	...	1
Exp. b0	-0.001	-0.001	...	0.001
Exp. b1	-10	-9.444	...	10

Test settings	
Tolerance b1d	±3,0000e-03
Tolerance a0d	±1,0000e-07
Tolerance b0d	±3,0000e-03
Tolerance initHandling	±0,0000e+00
Tolerance b0	±1,0000e-10
Tolerance b1	±1,0000e-06

Test statistics	
Min CPU cycles	1495
Max CPU cycles	1570
Avg CPU cycles	1563

Verification: PIDLimit Float32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for Control block PIDLimit.

Test results				
Time step	1	2	...	201
CPU cycles	88	88	...	1478
Inputs				
In (DSP)	0	0	...	0
Init (DSP)	0.11	0.11	...	0.11
max (DSP)	0.8	0.8	...	0.8
min (DSP)	0.15	0.15	...	0.15
Enable (DSP)	0	0	...	1
In	0	0	...	0
Init	0.11	0.11	...	0.11
max	0.8	0.8	...	0.8
min	0.15	0.15	...	0.15
Enable	0	0	...	1
Parameters				
Kp	2			
Ki	2500			
Kd	0.003			
fc	200			
initHandling	initialize integral			
ts_fact	1			
Outputs				
Out	0	0	...	0.649
Exp. Out	0	0	...	0.649
Out (DSP)	0	0	...	0.649
Exp. Out (DSP)	0	0	...	0.649

Test settings	
Tolerance Out	±9,3132e-07 (±2000 LSB)

Test statistics	
Min CPU cycles	88
Max CPU cycles	1819
Avg CPU cycles	1527

Test case: Conversion test OK

Conversion test for Control block PIDLimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
b1d	0	-824.183	...	31415.927
a0d	-1	-0.991	...	-0.73
b0d	0	824.183	...	-31415.927
initHandling	0	0	...	1
b0	-0.001	-0.001	...	0.001
b1	-10	-9.444	...	10
Exp. b1d	0	-824.183	...	31415.927
Exp. a0d	-1	-0.991	...	-0.73
Exp. b0d	0	824.183	...	-31415.927
Exp. initHandling	0	0	...	1
Exp. b0	-0.001	-0.001	...	0.001
Exp. b1	-10	-9.444	...	10

Test settings	
Tolerance b1d	±0,0000e+00
Tolerance a0d	±1,0000e-15
Tolerance b0d	±0,0000e+00
Tolerance initHandling	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block PIDLimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
b1d	0	-824.183	...	31415.928
a0d	-1	-0.991	...	-0.73
b0d	0	824.183	...	-31415.928
initHandling	0	0	...	1
b0	-0.001	-0.001	...	0.001
b1	-10	-9.444	...	10
Exp. b1d	0	-824.183	...	31415.927
Exp. a0d	-1	-0.991	...	-0.73
Exp. b0d	0	824.183	...	-31415.927
Exp. initHandling	0	0	...	1
Exp. b0	-0.001	-0.001	...	0.001
Exp. b1	-10	-9.444	...	10

Test settings	
Tolerance b1d	±3,0000e-03
Tolerance a0d	±1,0000e-07
Tolerance b0d	±3,0000e-03
Tolerance initHandling	±0,0000e+00
Tolerance b0	±1,0000e-10
Tolerance b1	±1,0000e-06

Test statistics	
Min CPU cycles	4055
Max CPU cycles	7049
Avg CPU cycles	6909

Verification: PIDLimit Float32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for Control block PIDLimit.

Test results				
Time step	1	2	...	201
CPU cycles	73	73	...	555
Inputs				
In (DSP)	0	0	...	0
Init (DSP)	0.11	0.11	...	0.11
max (DSP)	0.8	0.8	...	0.8
min (DSP)	0.15	0.15	...	0.15
Enable (DSP)	0	0	...	1
In	0	0	...	0
Init	0.11	0.11	...	0.11
max	0.8	0.8	...	0.8
min	0.15	0.15	...	0.15
Enable	0	0	...	1
Parameters				
Kp	2			
Ki	2500			
Kd	0.003			
fc	200			
initHandling	initialize integral			
ts_fact	1			
Outputs				
Out	0	0	...	0.649
Exp. Out	0	0	...	0.649
Out (DSP)	0	0	...	0.649
Exp. Out (DSP)	0	0	...	0.649

Test settings	
Tolerance Out	±9,3132e-07 (±2000 LSB)

Test statistics	
Min CPU cycles	73
Max CPU cycles	699
Avg CPU cycles	595

Test case: Conversion test OK

Conversion test for Control block PIDLimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
b1d	0	-824.183	...	31415.927
a0d	-1	-0.991	...	-0.73
b0d	0	824.183	...	-31415.927
initHandling	0	0	...	1
b0	-0.001	-0.001	...	0.001
b1	-10	-9.444	...	10
Exp. b1d	0	-824.183	...	31415.927
Exp. a0d	-1	-0.991	...	-0.73
Exp. b0d	0	824.183	...	-31415.927
Exp. initHandling	0	0	...	1
Exp. b0	-0.001	-0.001	...	0.001
Exp. b1	-10	-9.444	...	10

Test settings	
Tolerance b1d	±0,0000e+00
Tolerance a0d	±1,0000e-15
Tolerance b0d	±0,0000e+00
Tolerance initHandling	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block PIDLimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
b1d	0	-824.183	...	31415.928
a0d	-1	-0.991	...	-0.73
b0d	0	824.183	...	-31415.928
initHandling	0	0	...	1
b0	-0.001	-0.001	...	0.001
b1	-10	-9.444	...	10
Exp. b1d	0	-824.183	...	31415.927
Exp. a0d	-1	-0.991	...	-0.73
Exp. b0d	0	824.183	...	-31415.927
Exp. initHandling	0	0	...	1
Exp. b0	-0.001	-0.001	...	0.001
Exp. b1	-10	-9.444	...	10

Test settings	
Tolerance b1d	±3,0000e-03
Tolerance a0d	±1,0000e-07
Tolerance b0d	±3,0000e-03
Tolerance initHandling	±0,0000e+00
Tolerance b0	±1,0000e-10
Tolerance b1	±1,0000e-06

Test statistics	
Min CPU cycles	1304
Max CPU cycles	1551
Avg CPU cycles	1538

Verification: PIDLimit Float32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for Control block PIDLimit.

Test results				
Time step	1	2	...	201
CPU cycles	88	60	...	138
Inputs				
In (DSP)	0	0	...	0
Init (DSP)	0.11	0.11	...	0.11
max (DSP)	0.8	0.8	...	0.8
min (DSP)	0.15	0.15	...	0.15
Enable (DSP)	0	0	...	1
In	0	0	...	0
Init	0.11	0.11	...	0.11
max	0.8	0.8	...	0.8
min	0.15	0.15	...	0.15
Enable	0	0	...	1
Parameters				
Kp	2			
Ki	2500			
Kd	0.003			
fc	200			
initHandling	initialize integral			
ts_fact	1			
Outputs				
Out	0	0	...	0.649
Exp. Out	0	0	...	0.649
Out (DSP)	0	0	...	0.649
Exp. Out (DSP)	0	0	...	0.649

Test settings	
Tolerance Out	±9,3132e-07 (±2000 LSB)

Test statistics	
Min CPU cycles	60
Max CPU cycles	193
Avg CPU cycles	133

Test case: Conversion test OK

Conversion test for Control block PIDLimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
b1d	0	-824.183	...	31415.927
a0d	-1	-0.991	...	-0.73
b0d	0	824.183	...	-31415.927
initHandling	0	0	...	1
b0	-0.001	-0.001	...	0.001
b1	-10	-9.444	...	10
Exp. b1d	0	-824.183	...	31415.927
Exp. a0d	-1	-0.991	...	-0.73
Exp. b0d	0	824.183	...	-31415.927
Exp. initHandling	0	0	...	1
Exp. b0	-0.001	-0.001	...	0.001
Exp. b1	-10	-9.444	...	10

Test settings	
Tolerance b1d	±0,0000e+00
Tolerance a0d	±1,0000e-15
Tolerance b0d	±0,0000e+00
Tolerance initHandling	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block PIDLimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
b1d	0	-824.183	...	31415.928
a0d	-1	-0.991	...	-0.73
b0d	0	824.183	...	-31415.928
initHandling	0	0	...	1
b0	-0.001	-0.001	...	0.001
b1	-10	-9.444	...	10
Exp. b1d	0	-824.183	...	31415.927
Exp. a0d	-1	-0.991	...	-0.73
Exp. b0d	0	824.183	...	-31415.927
Exp. initHandling	0	0	...	1
Exp. b0	-0.001	-0.001	...	0.001
Exp. b1	-10	-9.444	...	10

Test settings	
Tolerance b1d	±3,0000e-03
Tolerance a0d	±1,0000e-07
Tolerance b0d	±3,0000e-03
Tolerance initHandling	±0,0000e+00
Tolerance b0	±1,0000e-10
Tolerance b1	±1,0000e-06

Test statistics	
Min CPU cycles	1502
Max CPU cycles	1564
Avg CPU cycles	1508

Verification: PIDLimit Float32 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for Control block PIDLimit.

Test results				
Time step	1	2	...	201
CPU cycles	71	71	...	157
Inputs				
In (DSP)	0	0	...	0
Init (DSP)	0.11	0.11	...	0.11
max (DSP)	0.8	0.8	...	0.8
min (DSP)	0.15	0.15	...	0.15
Enable (DSP)	0	0	...	1
In	0	0	...	0
Init	0.11	0.11	...	0.11
max	0.8	0.8	...	0.8
min	0.15	0.15	...	0.15
Enable	0	0	...	1
Parameters				
Kp	2			
Ki	2500			
Kd	0.003			
fc	200			
initHandling	initialize integral			
ts_fact	1			
Outputs				
Out	0	0	...	0.649
Exp. Out	0	0	...	0.649
Out (DSP)	0	0	...	0.649
Exp. Out (DSP)	0	0	...	0.649

Test settings	
Tolerance Out	±9,3132e-07 (±2000 LSB)

Test statistics	
Min CPU cycles	71
Max CPU cycles	176
Avg CPU cycles	154

Test case: Conversion test OK

Conversion test for Control block PIDLimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
b1d	0	-824.183	...	31415.927
a0d	-1	-0.991	...	-0.73
b0d	0	824.183	...	-31415.927
initHandling	0	0	...	1
b0	-0.001	-0.001	...	0.001
b1	-10	-9.444	...	10
Exp. b1d	0	-824.183	...	31415.927
Exp. a0d	-1	-0.991	...	-0.73
Exp. b0d	0	824.183	...	-31415.927
Exp. initHandling	0	0	...	1
Exp. b0	-0.001	-0.001	...	0.001
Exp. b1	-10	-9.444	...	10

Test settings	
Tolerance b1d	±0,0000e+00
Tolerance a0d	±1,0000e-15
Tolerance b0d	±0,0000e+00
Tolerance initHandling	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block PIDLimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
b1d	0	-824.183	...	31415.928
a0d	-1	-0.991	...	-0.73
b0d	0	824.183	...	-31415.928
initHandling	0	0	...	1
b0	-0.001	-0.001	...	0.001
b1	-10	-9.444	...	10
Exp. b1d	0	-824.183	...	31415.927
Exp. a0d	-1	-0.991	...	-0.73
Exp. b0d	0	824.183	...	-31415.927
Exp. initHandling	0	0	...	1
Exp. b0	-0.001	-0.001	...	0.001
Exp. b1	-10	-9.444	...	10

Test settings	
Tolerance b1d	±3,0000e-03
Tolerance a0d	±1,0000e-07
Tolerance b0d	±3,0000e-03
Tolerance initHandling	±0,0000e+00
Tolerance b0	±1,0000e-10
Tolerance b1	±1,0000e-06

Test statistics	
Min CPU cycles	2092
Max CPU cycles	2391
Avg CPU cycles	2351

Verification: PIDLimit Float32 CPU dsPIC33EP256MC502

Date of Test	2026-06-23
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for Control block PIDLimit.

Test results				
Time step	1	2	...	201
CPU cycles	64	64	...	1684
Inputs				
In (DSP)	0	0	...	0
Init (DSP)	0.11	0.11	...	0.11
max (DSP)	0.8	0.8	...	0.8
min (DSP)	0.15	0.15	...	0.15
Enable (DSP)	0	0	...	1
In	0	0	...	0
Init	0.11	0.11	...	0.11
max	0.8	0.8	...	0.8
min	0.15	0.15	...	0.15
Enable	0	0	...	1
Parameters				
Kp	2			
Ki	2500			
Kd	0.003			
fc	200			
initHandling	initialize integral			
ts_fact	1			
Outputs				
Out	0	0	...	0.649
Exp. Out	0	0	...	0.649
Out (DSP)	0	0	...	0.649
Exp. Out (DSP)	0	0	...	0.649

Test settings	
Tolerance Out	±9,3132e-07 (±2000 LSB)

Test statistics	
Min CPU cycles	64
Max CPU cycles	2045
Avg CPU cycles	1741

Test case: Conversion test OK

Conversion test for Control block PIDLimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
b1d	0	-824.183	...	31415.927
a0d	-1	-0.991	...	-0.73
b0d	0	824.183	...	-31415.927
initHandling	0	0	...	1
b0	-0.001	-0.001	...	0.001
b1	-10	-9.444	...	10
Exp. b1d	0	-824.183	...	31415.927
Exp. a0d	-1	-0.991	...	-0.73
Exp. b0d	0	824.183	...	-31415.927
Exp. initHandling	0	0	...	1
Exp. b0	-0.001	-0.001	...	0.001
Exp. b1	-10	-9.444	...	10

Test settings	
Tolerance b1d	±0,0000e+00
Tolerance a0d	±1,0000e-15
Tolerance b0d	±0,0000e+00
Tolerance initHandling	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

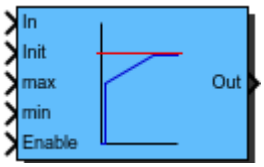
Conversion-on-Target test for Control block PIDLimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
Kd	-10	-9.444	...	10
fc	0	13.889	...	500
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
b1d	0	-824.183	...	31415.928
a0d	-1	-0.991	...	-0.73
b0d	0	824.183	...	-31415.928
initHandling	0	0	...	1
b0	-0.001	-0.001	...	0.001
b1	-10	-9.444	...	10
Exp. b1d	0	-824.183	...	31415.927
Exp. a0d	-1	-0.991	...	-0.73
Exp. b0d	0	824.183	...	-31415.927
Exp. initHandling	0	0	...	1
Exp. b0	-0.001	-0.001	...	0.001
Exp. b1	-10	-9.444	...	10

Test settings	
Tolerance b1d	±3,0000e-03
Tolerance a0d	±1,0000e-07
Tolerance b0d	±3,0000e-03
Tolerance initHandling	±0,0000e+00
Tolerance b0	±1,0000e-10
Tolerance b1	±1,0000e-06

Test statistics	
Min CPU cycles	5102
Max CPU cycles	8863
Avg CPU cycles	8469

Block: PILimit



PI controller with output limitation and anti wind-up method clamping:
G(s) = Kp + Ki/s

Inports	
In	Control error input
Init	Initial value of output Out when enabled
max	Maximum output value
min	Minimum output value
Enable	Enable == 0: Deactivation of block; Out set to 0 Enable 0->1: Preload of integral part Enable == 1: Activation of block

Outports	
Out	Control value

Mask Parameters		
Name	**ID**	**Description**
Kp	1	Proportional Factor
Ki	2	Integral Factor
initHandling	3	Determines what the signal provided on Init input is used for
ts_fact	4	Multiplication factor of base sampling time (in integer format)

Description:

Preloading Integral
A rising edge at the *Enable* inport enables the controller and preloads the integral.

One may choose from two options how to preload the integral value:

- Preload the integral from the *Init* inport.
- Preload the integral such that the first output of the controller matches the current value at the *Init* inport.
  This option allows controller switching without disturbing the control.

Note: Each fixed point implementation uses the next higher integer data type for the integral value storage variable.
Transfer function (zero-order hold discretization method):
When the block is enabled, the PI controller realizes the following transfer function: Transfer

function (zero-order hold discretization method):

$$G(z) = K_\mathrm{p} + K_\mathrm{i} T_\mathrm{s} \frac{1}{z-1}$$

Anti Wind-Up
The implemented anti wind-up method is clamping. If the output signal out exceeds the upper or lower limit value, which is given by the inport max and the inport min, the integrator is clamped if the controller input would increase the saturation even further.

Developer note: The source code of this block is used for block *PI*.

Implementations:

FiP8	8 Bit Fixed Point Implementation
FiP16	16 Bit Fixed Point Implementation
FiP32	32 Bit Fixed Point Implementation
Float32	32 Bit Floating Point Implementation
Float64	64 Bit Floating Point Implementation

Implementation: FiP8

8 Bit Fixed Point Implementation

Inports Data Type	
In	int8
Init	int8
max	int8
min	int8
Enable	bool

Outports Data Type	
Out	int8

Implementation: FiP16

16 Bit Fixed Point Implementation

Inports Data Type	
In	int16
Init	int16
max	int16
min	int16
Enable	bool

Outports Data Type	
Out	int16

Implementation: FiP32

32 Bit Fixed Point Implementation

Inports Data Type	
In	int32
Init	int32
max	int32
min	int32
Enable	bool

Outports Data Type	
Out	int32

Implementation: Float32

32 Bit Floating Point Implementation

Inports Data Type	
In	float32
Init	float32
max	float32
min	float32
Enable	bool

Outports Data Type	
Out	float32

Implementation: Float64

64 Bit Floating Point Implementation

Inports Data Type	
In	float64
Init	float64
max	float64
min	float64
Enable	bool

Outports Data Type	
Out	float64

Verification: PILimit FiP16 CPU TMS320F28335

Date of Test 2026-06-19

Target controller TMS320F28335

Test case: Inport test OK

Inport test for Control block PILimit.

Test results						
Time step	1	2	3	4	...	201
CPU cycles	67	67	67	148	...	129
Inputs						
In (DSP)	0	0	0	0	...	0
Init (DSP)	3604	3604	3604	3604	...	3604
max (DSP)	26214	26214	26214	26214	...	26214
min (DSP)	4915	4915	4915	4915	...	4915
Enable (DSP)	0	0	0	1	...	1
In	0	0	0	0	...	0
Init	0.11	0.11	0.11	0.11	...	0.11
max	0.8	0.8	0.8	0.8	...	0.8
min	0.15	0.15	0.15	0.15	...	0.15
Enable	0	0	0	1	...	1
Parameters						
Kp	2					
Ki	2500					
initHandling	initialize integral					
ts_fact	1					
Outputs						
Out	0	0	0	0.15	...	0.647
Exp. Out	0	0	0	0.15	...	0.647
Out (DSP)	0	0	0	4915	...	21212
Exp. Out (DSP)	0	0	0	4915	...	21217

Test settings	
Tolerance Out	±3,0518e-04 (±10 LSB)

Test statistics	
Min CPU cycles	67
Max CPU cycles	148
Avg CPU cycles	123

Test case: Conversion test OK

Conversion test for Control block PILimit.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kp	-10	-9.444	-8.889	-8.333	...	10
Ki	-11	-10.389	-9.778	-9.167	...	11
initHandling	initialize integral	initialize integral	initialize integral	initialize integral	...	initialize
ts_fact	1	1	1	1	...	1
Controller parameters						
initHandling	0	0	0	0	...	1
sfrb0	15	15	15	15	...	15
sfrb1	11	11	11	11	...	11
b0	-36	-34	-32	-30	...	36
b1	-20480	-19342	-18204	-17067	...	204
Exp. initHandling	0	0	0	0	...	1
Exp. sfrb0	15	15	15	15	...	15
Exp. sfrb1	11	11	11	11	...	11
Exp. b0	-36	-34	-32	-30	...	36
Exp. b1	-20480	-19342	-18204	-17067	...	204

Test settings	
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test OK

Conversion-on-Target test for Control block PILimit.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kp	-10	-9.444	-8.889	-8.333	...	10
Ki	-11	-10.389	-9.778	-9.167	...	11
initHandling	initialize integral	initialize integral	initialize integral	initialize integral	...	initialize
ts_fact	1	1	1	1	...	1
Controller parameters						
initHandling	0	0	0	0	...	1
sfrb0	15	15	15	15	...	15
sfrb1	11	11	11	11	...	11
b0	-36	-34	-32	-30	...	36
b1	-20480	-19342	-18204	-17066	...	204
Exp. initHandling	0	0	0	0	...	1
Exp. sfrb0	15	15	15	15	...	15
Exp. sfrb1	11	11	11	11	...	11
Exp. b0	-36	-34	-32	-30	...	36
Exp. b1	-20480	-19342	-18204	-17067	...	204

Test settings	
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±1,0000e+00

Test statistics	
Min CPU cycles	3071
Max CPU cycles	5316
Avg CPU cycles	4559

Verification: PILimit FiP16 CPU TM4C123GH6

Date of Test 2026-06-19

Target controller TM4C123GH6

Test case: Inport test OK

Inport test for Control block PILimit.

Test results						
Time step	1	2	3	4	...	201
CPU cycles	43	43	43	105	...	83
Inputs						
In (DSP)	0	0	0	0	...	0
Init (DSP)	3604	3604	3604	3604	...	3604
max (DSP)	26214	26214	26214	26214	...	26214
min (DSP)	4915	4915	4915	4915	...	4915
Enable (DSP)	0	0	0	1	...	1
In	0	0	0	0	...	0
Init	0.11	0.11	0.11	0.11	...	0.11
max	0.8	0.8	0.8	0.8	...	0.8
min	0.15	0.15	0.15	0.15	...	0.15
Enable	0	0	0	1	...	1
Parameters						
Kp	2					
Ki	2500					
initHandling	initialize integral					
ts_fact	1					
Outputs						
Out	0	0	0	0.15	...	0.647
Exp. Out	0	0	0	0.15	...	0.647
Out (DSP)	0	0	0	4915	...	21212
Exp. Out (DSP)	0	0	0	4915	...	21217

Test settings	
Tolerance Out	±3,0518e-04 (±10 LSB)

Test statistics	
Min CPU cycles	43
Max CPU cycles	105
Avg CPU cycles	81

Test case: Conversion test OK

Conversion test for Control block PILimit.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kp	-10	-9.444	-8.889	-8.333	...	10
Ki	-11	-10.389	-9.778	-9.167	...	11
initHandling	initialize integral	initialize integral	initialize integral	initialize integral	...	initialize
ts_fact	1	1	1	1	...	1
Controller parameters						
initHandling	0	0	0	0	...	1
sfrb0	15	15	15	15	...	15
sfrb1	11	11	11	11	...	11
b0	-36	-34	-32	-30	...	36
b1	-20480	-19342	-18204	-17067	...	204
Exp. initHandling	0	0	0	0	...	1
Exp. sfrb0	15	15	15	15	...	15
Exp. sfrb1	11	11	11	11	...	11
Exp. b0	-36	-34	-32	-30	...	36
Exp. b1	-20480	-19342	-18204	-17067	...	204

Test settings	
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test OK

Conversion-on-Target test for Control block PILimit.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kp	-10	-9.444	-8.889	-8.333	...	10
Ki	-11	-10.389	-9.778	-9.167	...	11
initHandling	initialize integral	initialize integral	initialize integral	initialize integral	...	initialize
ts_fact	1	1	1	1	...	1
Controller parameters						
initHandling	0	0	0	0	...	1
sfrb0	15	15	15	15	...	15
sfrb1	11	11	11	11	...	11
b0	-36	-34	-32	-30	...	36
b1	-20480	-19342	-18204	-17066	...	204
Exp. initHandling	0	0	0	0	...	1
Exp. sfrb0	15	15	15	15	...	15
Exp. sfrb1	11	11	11	11	...	11
Exp. b0	-36	-34	-32	-30	...	36
Exp. b1	-20480	-19342	-18204	-17067	...	204

Test settings	
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±1,0000e+00

Test statistics	
Min CPU cycles	1563
Max CPU cycles	2889
Avg CPU cycles	2441

Verification: PILimit FiP16 CPU STM32G474RE

Date of Test 2026-06-19

Target controller STM32G474RE

Test case: Inport test OK

Inport test for Control block PILimit.

Test results						
Time step	1	2	3	4	...	201
CPU cycles	73	73	73	137	...	135
Inputs						
In (DSP)	0	0	0	0	...	0
Init (DSP)	3604	3604	3604	3604	...	3604
max (DSP)	26214	26214	26214	26214	...	26214
min (DSP)	4915	4915	4915	4915	...	4915
Enable (DSP)	0	0	0	1	...	1
In	0	0	0	0	...	0
Init	0.11	0.11	0.11	0.11	...	0.11
max	0.8	0.8	0.8	0.8	...	0.8
min	0.15	0.15	0.15	0.15	...	0.15
Enable	0	0	0	1	...	1
Parameters						
Kp	2					
Ki	2500					
initHandling	initialize integral					
ts_fact	1					
Outputs						
Out	0	0	0	0.15	...	0.647
Exp. Out	0	0	0	0.15	...	0.647
Out (DSP)	0	0	0	4915	...	21212
Exp. Out (DSP)	0	0	0	4915	...	21217

Test settings	
Tolerance Out	±3,0518e-04 (±10 LSB)

Test statistics	
Min CPU cycles	73
Max CPU cycles	137
Avg CPU cycles	120

Test case: Conversion test OK

Conversion test for Control block PILimit.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kp	-10	-9.444	-8.889	-8.333	...	10
Ki	-11	-10.389	-9.778	-9.167	...	11
initHandling	initialize integral	initialize integral	initialize integral	initialize integral	...	initialize
ts_fact	1	1	1	1	...	1
Controller parameters						
initHandling	0	0	0	0	...	1
sfrb0	15	15	15	15	...	15
sfrb1	11	11	11	11	...	11
b0	-36	-34	-32	-30	...	36
b1	-20480	-19342	-18204	-17067	...	204
Exp. initHandling	0	0	0	0	...	1
Exp. sfrb0	15	15	15	15	...	15
Exp. sfrb1	11	11	11	11	...	11
Exp. b0	-36	-34	-32	-30	...	36
Exp. b1	-20480	-19342	-18204	-17067	...	204

Test settings	
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test OK

Conversion-on-Target test for Control block PILimit.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kp	-10	-9.444	-8.889	-8.333	...	10
Ki	-11	-10.389	-9.778	-9.167	...	11
initHandling	initialize integral	initialize integral	initialize integral	initialize integral	...	initialize
ts_fact	1	1	1	1	...	1
Controller parameters						
initHandling	0	0	0	0	...	1
sfrb0	15	15	15	15	...	15
sfrb1	11	11	11	11	...	11
b0	-36	-34	-32	-30	...	36
b1	-20480	-19342	-18204	-17066	...	204
Exp. initHandling	0	0	0	0	...	1
Exp. sfrb0	15	15	15	15	...	15
Exp. sfrb1	11	11	11	11	...	11
Exp. b0	-36	-34	-32	-30	...	36
Exp. b1	-20480	-19342	-18204	-17067	...	204

Test settings	
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±1,0000e+00

Test statistics	
Min CPU cycles	1585
Max CPU cycles	2090
Avg CPU cycles	1906

Verification: PILimit FiP16 CPU STM32F072RB

Date of Test 2026-06-19

Target controller STM32F072RB

Test case: Inport test OK

Inport test for Control block PILimit.

Test results						
Time step	1	2	3	4	...	201
CPU cycles	68	68	68	153	...	123
Inputs						
In (DSP)	0	0	0	0	...	0
Init (DSP)	3604	3604	3604	3604	...	3604
max (DSP)	26214	26214	26214	26214	...	26214
min (DSP)	4915	4915	4915	4915	...	4915
Enable (DSP)	0	0	0	1	...	1
In	0	0	0	0	...	0
Init	0.11	0.11	0.11	0.11	...	0.11
max	0.8	0.8	0.8	0.8	...	0.8
min	0.15	0.15	0.15	0.15	...	0.15
Enable	0	0	0	1	...	1
Parameters						
Kp	2					
Ki	2500					
initHandling	initialize integral					
ts_fact	1					
Outputs						
Out	0	0	0	0.15	...	0.647
Exp. Out	0	0	0	0.15	...	0.647
Out (DSP)	0	0	0	4915	...	21212
Exp. Out (DSP)	0	0	0	4915	...	21217

Test settings	
Tolerance Out	±3,0518e-04 (±10 LSB)

Test statistics	
Min CPU cycles	68
Max CPU cycles	183
Avg CPU cycles	113

Test case: Conversion test OK

Conversion test for Control block PILimit.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kp	-10	-9.444	-8.889	-8.333	...	10
Ki	-11	-10.389	-9.778	-9.167	...	11
initHandling	initialize integral	initialize integral	initialize integral	initialize integral	...	initialize
ts_fact	1	1	1	1	...	1
Controller parameters						
initHandling	0	0	0	0	...	1
sfrb0	15	15	15	15	...	15
sfrb1	11	11	11	11	...	11
b0	-36	-34	-32	-30	...	36
b1	-20480	-19342	-18204	-17067	...	204
Exp. initHandling	0	0	0	0	...	1
Exp. sfrb0	15	15	15	15	...	15
Exp. sfrb1	11	11	11	11	...	11
Exp. b0	-36	-34	-32	-30	...	36
Exp. b1	-20480	-19342	-18204	-17067	...	204

Test settings	
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test OK

Conversion-on-Target test for Control block PILimit.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kp	-10	-9.444	-8.889	-8.333	...	10
Ki	-11	-10.389	-9.778	-9.167	...	11
initHandling	initialize integral	initialize integral	initialize integral	initialize integral	...	initialize
ts_fact	1	1	1	1	...	1
Controller parameters						
initHandling	0	0	0	0	...	1
sfrb0	15	15	15	15	...	15
sfrb1	11	11	11	11	...	11
b0	-36	-34	-32	-30	...	36
b1	-20480	-19342	-18204	-17066	...	204
Exp. initHandling	0	0	0	0	...	1
Exp. sfrb0	15	15	15	15	...	15
Exp. sfrb1	11	11	11	11	...	11
Exp. b0	-36	-34	-32	-30	...	36
Exp. b1	-20480	-19342	-18204	-17067	...	204

Test settings	
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±1,0000e+00

Test statistics	
Min CPU cycles	4006
Max CPU cycles	7402
Avg CPU cycles	6391

Verification: PILimit FiP16 CPU PIC32MX170F256

Date of Test 2026-06-19

Target controller PIC32MX170F256

Test case: Inport test OK

Inport test for Control block PILimit.

Test results						
Time step	1	2	3	4	...	201
CPU cycles	31	31	31	92	...	79
Inputs						
In (DSP)	0	0	0	0	...	0
Init (DSP)	3604	3604	3604	3604	...	3604
max (DSP)	26214	26214	26214	26214	...	26214
min (DSP)	4915	4915	4915	4915	...	4915
Enable (DSP)	0	0	0	1	...	1
In	0	0	0	0	...	0
Init	0.11	0.11	0.11	0.11	...	0.11
max	0.8	0.8	0.8	0.8	...	0.8
min	0.15	0.15	0.15	0.15	...	0.15
Enable	0	0	0	1	...	1
Parameters						
Kp	2					
Ki	2500					
initHandling	initialize integral					
ts_fact	1					
Outputs						
Out	0	0	0	0.15	...	0.647
Exp. Out	0	0	0	0.15	...	0.647
Out (DSP)	0	0	0	4915	...	21212
Exp. Out (DSP)	0	0	0	4915	...	21217

Test settings	
Tolerance Out	±3,0518e-04 (±10 LSB)

Test statistics	
Min CPU cycles	31
Max CPU cycles	92
Avg CPU cycles	71

Test case: Conversion test OK

Conversion test for Control block PILimit.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kp	-10	-9.444	-8.889	-8.333	...	10
Ki	-11	-10.389	-9.778	-9.167	...	11
initHandling	initialize integral	initialize integral	initialize integral	initialize integral	...	initialize
ts_fact	1	1	1	1	...	1
Controller parameters						
initHandling	0	0	0	0	...	1
sfrb0	15	15	15	15	...	15
sfrb1	11	11	11	11	...	11
b0	-36	-34	-32	-30	...	36
b1	-20480	-19342	-18204	-17067	...	204
Exp. initHandling	0	0	0	0	...	1
Exp. sfrb0	15	15	15	15	...	15
Exp. sfrb1	11	11	11	11	...	11
Exp. b0	-36	-34	-32	-30	...	36
Exp. b1	-20480	-19342	-18204	-17067	...	204

Test settings	
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test OK

Conversion-on-Target test for Control block PILimit.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kp	-10	-9.444	-8.889	-8.333	...	10
Ki	-11	-10.389	-9.778	-9.167	...	11
initHandling	initialize integral	initialize integral	initialize integral	initialize integral	...	initialize
ts_fact	1	1	1	1	...	1
Controller parameters						
initHandling	0	0	0	0	...	1
sfrb0	15	15	15	15	...	15
sfrb1	11	11	11	11	...	11
b0	-36	-34	-32	-30	...	36
b1	-20480	-19342	-18204	-17066	...	204
Exp. initHandling	0	0	0	0	...	1
Exp. sfrb0	15	15	15	15	...	15
Exp. sfrb1	11	11	11	11	...	11
Exp. b0	-36	-34	-32	-30	...	36
Exp. b1	-20480	-19342	-18204	-17067	...	204

Test settings	
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±1,0000e+00

Test statistics	
Min CPU cycles	1749
Max CPU cycles	3034
Avg CPU cycles	2632

Verification: PILimit FiP16 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for Control block PILimit.

Test results						
Time step	1	2	3	4	...	201
CPU cycles	74	59	59	146	...	104
Inputs						
In (DSP)	0	0	0	0	...	0
Init (DSP)	3604	3604	3604	3604	...	3604
max (DSP)	26214	26214	26214	26214	...	26214
min (DSP)	4915	4915	4915	4915	...	4915
Enable (DSP)	0	0	0	1	...	1
In	0	0	0	0	...	0
Init	0.11	0.11	0.11	0.11	...	0.11
max	0.8	0.8	0.8	0.8	...	0.8
min	0.15	0.15	0.15	0.15	...	0.15
Enable	0	0	0	1	...	1
Parameters						
Kp	2					
Ki	2500					
initHandling	initialize integral					
ts_fact	1					
Outputs						
Out	0	0	0	0.15	...	0.647
Exp. Out	0	0	0	0.15	...	0.647
Out (DSP)	0	0	0	4915	...	21212
Exp. Out (DSP)	0	0	0	4915	...	21217

Test settings	
Tolerance Out	±3,0518e-04 (±10 LSB)

Test statistics	
Min CPU cycles	59
Max CPU cycles	146
Avg CPU cycles	100

Test case: Conversion test OK

Conversion test for Control block PILimit.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kp	-10	-9.444	-8.889	-8.333	...	10
Ki	-11	-10.389	-9.778	-9.167	...	11
initHandling	initialize integral	initialize integral	initialize integral	initialize integral	...	initialize
ts_fact	1	1	1	1	...	1
Controller parameters						
initHandling	0	0	0	0	...	1
sfrb0	15	15	15	15	...	15
sfrb1	11	11	11	11	...	11
b0	-36	-34	-32	-30	...	36
b1	-20480	-19342	-18204	-17067	...	204
Exp. initHandling	0	0	0	0	...	1
Exp. sfrb0	15	15	15	15	...	15
Exp. sfrb1	11	11	11	11	...	11
Exp. b0	-36	-34	-32	-30	...	36
Exp. b1	-20480	-19342	-18204	-17067	...	204

Test settings	
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test OK

Conversion-on-Target test for Control block PILimit.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kp	-10	-9.444	-8.889	-8.333	...	10
Ki	-11	-10.389	-9.778	-9.167	...	11
initHandling	initialize integral	initialize integral	initialize integral	initialize integral	...	initialize
ts_fact	1	1	1	1	...	1
Controller parameters						
initHandling	0	0	0	0	...	1
sfrb0	15	15	15	15	...	15
sfrb1	11	11	11	11	...	11
b0	-36	-34	-32	-30	...	36
b1	-20480	-19342	-18204	-17066	...	204
Exp. initHandling	0	0	0	0	...	1
Exp. sfrb0	15	15	15	15	...	15
Exp. sfrb1	11	11	11	11	...	11
Exp. b0	-36	-34	-32	-30	...	36
Exp. b1	-20480	-19342	-18204	-17067	...	204

Test settings	
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±1,0000e+00

Test statistics	
Min CPU cycles	1365
Max CPU cycles	2005
Avg CPU cycles	1687

Verification: PILimit FiP16 CPU TMS320F28379D

Date of Test 2026-06-22

Target controller TMS320F28379D

Test case: Inport test OK

Inport test for Control block PILimit.

Test results						
Time step	1	2	3	4	...	201
CPU cycles	57	57	57	154	...	129
Inputs						
In (DSP)	0	0	0	0	...	0
Init (DSP)	3604	3604	3604	3604	...	3604
max (DSP)	26214	26214	26214	26214	...	26214
min (DSP)	4915	4915	4915	4915	...	4915
Enable (DSP)	0	0	0	1	...	1
In	0	0	0	0	...	0
Init	0.11	0.11	0.11	0.11	...	0.11
max	0.8	0.8	0.8	0.8	...	0.8
min	0.15	0.15	0.15	0.15	...	0.15
Enable	0	0	0	1	...	1
Parameters						
Kp	2					
Ki	2500					
initHandling	initialize integral					
ts_fact	1					
Outputs						
Out	0	0	0	0.15	...	0.647
Exp. Out	0	0	0	0.15	...	0.647
Out (DSP)	0	0	0	4915	...	21212
Exp. Out (DSP)	0	0	0	4915	...	21217

Test settings	
Tolerance Out	±3,0518e-04 (±10 LSB)

Test statistics	
Min CPU cycles	57
Max CPU cycles	154
Avg CPU cycles	124

Test case: Conversion test OK

Conversion test for Control block PILimit.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kp	-10	-9.444	-8.889	-8.333	...	10
Ki	-11	-10.389	-9.778	-9.167	...	11
initHandling	initialize integral	initialize integral	initialize integral	initialize integral	...	initialize
ts_fact	1	1	1	1	...	1
Controller parameters						
initHandling	0	0	0	0	...	1
sfrb0	15	15	15	15	...	15
sfrb1	11	11	11	11	...	11
b0	-36	-34	-32	-30	...	36
b1	-20480	-19342	-18204	-17067	...	204
Exp. initHandling	0	0	0	0	...	1
Exp. sfrb0	15	15	15	15	...	15
Exp. sfrb1	11	11	11	11	...	11
Exp. b0	-36	-34	-32	-30	...	36
Exp. b1	-20480	-19342	-18204	-17067	...	204

Test settings	
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test OK

Conversion-on-Target test for Control block PILimit.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kp	-10	-9.444	-8.889	-8.333	...	10
Ki	-11	-10.389	-9.778	-9.167	...	11
initHandling	initialize integral	initialize integral	initialize integral	initialize integral	...	initialize
ts_fact	1	1	1	1	...	1
Controller parameters						
initHandling	0	0	0	0	...	1
sfrb0	15	15	15	15	...	15
sfrb1	11	11	11	11	...	11
b0	-36	-34	-32	-30	...	36
b1	-20480	-19342	-18204	-17066	...	204
Exp. initHandling	0	0	0	0	...	1
Exp. sfrb0	15	15	15	15	...	15
Exp. sfrb1	11	11	11	11	...	11
Exp. b0	-36	-34	-32	-30	...	36
Exp. b1	-20480	-19342	-18204	-17067	...	204

Test settings	
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±1,0000e+00

Test statistics	
Min CPU cycles	2294
Max CPU cycles	4061
Avg CPU cycles	3459

Verification: PILimit FiP16 CPU dsPIC33EP256MC502

Date of Test	2026-06-23
Target controller	dsPIC33EP256MC502

Test case: Inport test

OK

Inport test for Control block PILimit.

Test results						
Time step	1	2	3	4	...	201
CPU cycles	49	49	49	131	...	123
Inputs						
In (DSP)	0	0	0	0	...	0
Init (DSP)	3604	3604	3604	3604	...	3604
max (DSP)	26214	26214	26214	26214	...	26214
min (DSP)	4915	4915	4915	4915	...	4915
Enable (DSP)	0	0	0	1	...	1
In	0	0	0	0	...	0
Init	0.11	0.11	0.11	0.11	...	0.11
max	0.8	0.8	0.8	0.8	...	0.8
min	0.15	0.15	0.15	0.15	...	0.15
Enable	0	0	0	1	...	1
Parameters						
Kp	2					
Ki	2500					
initHandling	initialize integral					
ts_fact	1					
Outputs						
Out	0	0	0	0.15	...	0.647
Exp. Out	0	0	0	0.15	...	0.647
Out (DSP)	0	0	0	4915	...	21212
Exp. Out (DSP)	0	0	0	4915	...	21217

Test settings	
Tolerance Out	±3,0518e-04 (±10 LSB)

Test statistics	
Min CPU cycles	49
Max CPU cycles	131
Avg CPU cycles	109

Test case: Conversion test OK

Conversion test for Control block PILimit.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kp	-10	-9.444	-8.889	-8.333	...	10
Ki	-11	-10.389	-9.778	-9.167	...	11
initHandling	initialize integral	initialize integral	initialize integral	initialize integral	...	initialize
ts_fact	1	1	1	1	...	1
Controller parameters						
initHandling	0	0	0	0	...	1
sfrb0	15	15	15	15	...	15
sfrb1	11	11	11	11	...	11
b0	-36	-34	-32	-30	...	36
b1	-20480	-19342	-18204	-17067	...	204
Exp. initHandling	0	0	0	0	...	1
Exp. sfrb0	15	15	15	15	...	15
Exp. sfrb1	11	11	11	11	...	11
Exp. b0	-36	-34	-32	-30	...	36
Exp. b1	-20480	-19342	-18204	-17067	...	204

Test settings	
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test OK

Conversion-on-Target test for Control block PILimit.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kp	-10	-9.444	-8.889	-8.333	...	10
Ki	-11	-10.389	-9.778	-9.167	...	11
initHandling	initialize integral	initialize integral	initialize integral	initialize integral	...	initialize
ts_fact	1	1	1	1	...	1
Controller parameters						
initHandling	0	0	0	0	...	1
sfrb0	15	15	15	15	...	15
sfrb1	11	11	11	11	...	11
b0	-36	-34	-32	-30	...	36
b1	-20480	-19342	-18204	-17066	...	204
Exp. initHandling	0	0	0	0	...	1
Exp. sfrb0	15	15	15	15	...	15
Exp. sfrb1	11	11	11	11	...	11
Exp. b0	-36	-34	-32	-30	...	36
Exp. b1	-20480	-19342	-18204	-17067	...	204

Test settings	
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±1,0000e+00

Test statistics	
Min CPU cycles	6441
Max CPU cycles	15553
Avg CPU cycles	12970

Verification: PILimit FiP32 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for Control block PILimit.

Test results				
Time step	1	2	...	201
CPU cycles	85	85	...	240
Inputs				
In (DSP)	0	0	...	0
Init (DSP)	236223201	236223201	...	236223201
max (DSP)	1717986918	1717986918	...	1717986918
min (DSP)	322122547	322122547	...	322122547
Enable (DSP)	0	0	...	1
In	0	0	...	0
Init	0.11	0.11	...	0.11
max	0.8	0.8	...	0.8
min	0.15	0.15	...	0.15
Enable	0	0	...	1
Parameters				
Kp	2			
Ki	2500			
initHandling	initialize integral			
ts_fact	1			
Outputs				
Out	0	0	...	0.647
Exp. Out	0	0	...	0.647
Out (DSP)	0	0	...	1390495657
Exp. Out (DSP)	0	0	...	1390495657

Test settings	
Tolerance Out	±4,6566e-07 (±1000 LSB)

Test statistics	
Min CPU cycles	85
Max CPU cycles	266
Avg CPU cycles	223

Test case: Conversion test OK

Conversion test for Control block PILimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
initHandling	0	0	...	1
sfrb0	31	31	...	31
sfrb1	27	27	...	27
b0	-2362232	-2230997	...	2362232
b1	-1342177280	-1267611876	...	1342177280
Exp. initHandling	0	0	...	1
Exp. sfrb0	31	31	...	31
Exp. sfrb1	27	27	...	27
Exp. b0	-2362232	-2230997	...	2362232
Exp. b1	-1342177280	-1267611876	...	1342177280

Test settings	
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test OK

Conversion-on-Target test for Control block PILimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
initHandling	0	0	...	1
sfrb0	31	31	...	31
sfrb1	27	27	...	27
b0	-2362232	-2230997	...	2362232
b1	-1342177280	-1267611904	...	1342177280
Exp. initHandling	0	0	...	1
Exp. sfrb0	31	31	...	31
Exp. sfrb1	27	27	...	27
Exp. b0	-2362232	-2230997	...	2362232
Exp. b1	-1342177280	-1267611876	...	1342177280

Test settings	
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±1,0000e+00
Tolerance b1	±1,0000e+02

Test statistics	
Min CPU cycles	3435
Max CPU cycles	5782
Avg CPU cycles	5010

Verification: PILimit FiP32 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for Control block PILimit.

Test results				
Time step	1	2	...	201
CPU cycles	59	59	...	177
Inputs				
In (DSP)	0	0	...	0
Init (DSP)	236223201	236223201	...	236223201
max (DSP)	1717986918	1717986918	...	1717986918
min (DSP)	322122547	322122547	...	322122547
Enable (DSP)	0	0	...	1
In	0	0	...	0
Init	0.11	0.11	...	0.11
max	0.8	0.8	...	0.8
min	0.15	0.15	...	0.15
Enable	0	0	...	1
Parameters				
Kp	2			
Ki	2500			
initHandling	initialize integral			
ts_fact	1			
Outputs				
Out	0	0	...	0.647
Exp. Out	0	0	...	0.647
Out (DSP)	0	0	...	1390495657
Exp. Out (DSP)	0	0	...	1390495657

Test settings	
Tolerance Out	±4,6566e-07 (±1000 LSB)

Test statistics	
Min CPU cycles	59
Max CPU cycles	197
Avg CPU cycles	155

Test case: Conversion test OK

Conversion test for Control block PILimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
initHandling	0	0	...	1
sfrb0	31	31	...	31
sfrb1	27	27	...	27
b0	-2362232	-2230997	...	2362232
b1	-1342177280	-1267611876	...	1342177280
Exp. initHandling	0	0	...	1
Exp. sfrb0	31	31	...	31
Exp. sfrb1	27	27	...	27
Exp. b0	-2362232	-2230997	...	2362232
Exp. b1	-1342177280	-1267611876	...	1342177280

Test settings	
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test OK

Conversion-on-Target test for Control block PILimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
initHandling	0	0	...	1
sfrb0	31	31	...	31
sfrb1	27	27	...	27
b0	-2362232	-2230997	...	2362232
b1	-1342177280	-1267611904	...	1342177280
Exp. initHandling	0	0	...	1
Exp. sfrb0	31	31	...	31
Exp. sfrb1	27	27	...	27
Exp. b0	-2362232	-2230997	...	2362232
Exp. b1	-1342177280	-1267611876	...	1342177280

Test settings	
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±1,0000e+00
Tolerance b1	±1,0000e+02

Test statistics	
Min CPU cycles	1461
Max CPU cycles	2455
Avg CPU cycles	2147

Verification: PILimit FiP32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for Control block PILimit.

Test results				
Time step	1	2	...	201
CPU cycles	84	84	...	191
Inputs				
In (DSP)	0	0	...	0
Init (DSP)	236223201	236223201	...	236223201
max (DSP)	1717986918	1717986918	...	1717986918
min (DSP)	322122547	322122547	...	322122547
Enable (DSP)	0	0	...	1
In	0	0	...	0
Init	0.11	0.11	...	0.11
max	0.8	0.8	...	0.8
min	0.15	0.15	...	0.15
Enable	0	0	...	1
Parameters				
Kp	2			
Ki	2500			
initHandling	initialize integral			
ts_fact	1			
Outputs				
Out	0	0	...	0.647
Exp. Out	0	0	...	0.647
Out (DSP)	0	0	...	1390495657
Exp. Out (DSP)	0	0	...	1390495657

Test settings	
Tolerance Out	±4,6566e-07 (±1000 LSB)

Test statistics	
Min CPU cycles	84
Max CPU cycles	226
Avg CPU cycles	165

Test case: Conversion test OK

Conversion test for Control block PILimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
initHandling	0	0	...	1
sfrb0	31	31	...	31
sfrb1	27	27	...	27
b0	-2362232	-2230997	...	2362232
b1	-1342177280	-1267611876	...	1342177280
Exp. initHandling	0	0	...	1
Exp. sfrb0	31	31	...	31
Exp. sfrb1	27	27	...	27
Exp. b0	-2362232	-2230997	...	2362232
Exp. b1	-1342177280	-1267611876	...	1342177280

Test settings	
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test OK

Conversion-on-Target test for Control block PILimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
initHandling	0	0	...	1
sfrb0	31	31	...	31
sfrb1	27	27	...	27
b0	-2362232	-2230997	...	2362232
b1	-1342177280	-1267611904	...	1342177280
Exp. initHandling	0	0	...	1
Exp. sfrb0	31	31	...	31
Exp. sfrb1	27	27	...	27
Exp. b0	-2362232	-2230997	...	2362232
Exp. b1	-1342177280	-1267611876	...	1342177280

Test settings	
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±1,0000e+00
Tolerance b1	±1,0000e+02

Test statistics	
Min CPU cycles	2164
Max CPU cycles	2721
Avg CPU cycles	2520

Verification: PILimit FiP32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for Control block PILimit.

Test results				
Time step	1	2	...	201
CPU cycles	91	91	...	351
Inputs				
In (DSP)	0	0	...	0
Init (DSP)	236223201	236223201	...	236223201
max (DSP)	1717986918	1717986918	...	1717986918
min (DSP)	322122547	322122547	...	322122547
Enable (DSP)	0	0	...	1
In	0	0	...	0
Init	0.11	0.11	...	0.11
max	0.8	0.8	...	0.8
min	0.15	0.15	...	0.15
Enable	0	0	...	1
Parameters				
Kp	2			
Ki	2500			
initHandling	initialize integral			
ts_fact	1			
Outputs				
Out	0	0	...	0.647
Exp. Out	0	0	...	0.647
Out (DSP)	0	0	...	1390495657
Exp. Out (DSP)	0	0	...	1390495657

Test settings	
Tolerance Out	±4,6566e-07 (±1000 LSB)

Test statistics	
Min CPU cycles	91
Max CPU cycles	373
Avg CPU cycles	295

Test case: Conversion test OK

Conversion test for Control block PILimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
initHandling	0	0	...	1
sfrb0	31	31	...	31
sfrb1	27	27	...	27
b0	-2362232	-2230997	...	2362232
b1	-1342177280	-1267611876	...	1342177280
Exp. initHandling	0	0	...	1
Exp. sfrb0	31	31	...	31
Exp. sfrb1	27	27	...	27
Exp. b0	-2362232	-2230997	...	2362232
Exp. b1	-1342177280	-1267611876	...	1342177280

Test settings	
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test OK

Conversion-on-Target test for Control block PILimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
initHandling	0	0	...	1
sfrb0	31	31	...	31
sfrb1	27	27	...	27
b0	-2362232	-2230997	...	2362232
b1	-1342177280	-1267611904	...	1342177280
Exp. initHandling	0	0	...	1
Exp. sfrb0	31	31	...	31
Exp. sfrb1	27	27	...	27
Exp. b0	-2362232	-2230997	...	2362232
Exp. b1	-1342177280	-1267611876	...	1342177280

Test settings	
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±1,0000e+00
Tolerance b1	±1,0000e+02

Test statistics	
Min CPU cycles	6087
Max CPU cycles	9970
Avg CPU cycles	8951

Verification: PILimit FiP32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for Control block PILimit.

Test results				
Time step	1	2	...	201
CPU cycles	31	31	...	130
Inputs				
In (DSP)	0	0	...	0
Init (DSP)	236223201	236223201	...	236223201
max (DSP)	1717986918	1717986918	...	1717986918
min (DSP)	322122547	322122547	...	322122547
Enable (DSP)	0	0	...	1
In	0	0	...	0
Init	0.11	0.11	...	0.11
max	0.8	0.8	...	0.8
min	0.15	0.15	...	0.15
Enable	0	0	...	1
Parameters				
Kp	2			
Ki	2500			
initHandling	initialize integral			
ts_fact	1			
Outputs				
Out	0	0	...	0.647
Exp. Out	0	0	...	0.647
Out (DSP)	0	0	...	1390495657
Exp. Out (DSP)	0	0	...	1390495657

Test settings	
Tolerance Out	±4,6566e-07 (±1000 LSB)

Test statistics	
Min CPU cycles	31
Max CPU cycles	144
Avg CPU cycles	111

Test case: Conversion test OK

Conversion test for Control block PILimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
initHandling	0	0	...	1
sfrb0	31	31	...	31
sfrb1	27	27	...	27
b0	-2362232	-2230997	...	2362232
b1	-1342177280	-1267611876	...	1342177280
Exp. initHandling	0	0	...	1
Exp. sfrb0	31	31	...	31
Exp. sfrb1	27	27	...	27
Exp. b0	-2362232	-2230997	...	2362232
Exp. b1	-1342177280	-1267611876	...	1342177280

Test settings	
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test OK

Conversion-on-Target test for Control block PILimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
initHandling	0	0	...	1
sfrb0	31	31	...	31
sfrb1	27	27	...	27
b0	-2362232	-2230997	...	2362232
b1	-1342177280	-1267611904	...	1342177280
Exp. initHandling	0	0	...	1
Exp. sfrb0	31	31	...	31
Exp. sfrb1	27	27	...	27
Exp. b0	-2362232	-2230997	...	2362232
Exp. b1	-1342177280	-1267611876	...	1342177280

Test settings	
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±1,0000e+00
Tolerance b1	±1,0000e+02

Test statistics	
Min CPU cycles	2658
Max CPU cycles	4035
Avg CPU cycles	3626

Verification: PILimit FiP32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for Control block PILimit.

Test results				
Time step	1	2	...	201
CPU cycles	83	59	...	164
Inputs				
In (DSP)	0	0	...	0
Init (DSP)	236223201	236223201	...	236223201
max (DSP)	1717986918	1717986918	...	1717986918
min (DSP)	322122547	322122547	...	322122547
Enable (DSP)	0	0	...	1
In	0	0	...	0
Init	0.11	0.11	...	0.11
max	0.8	0.8	...	0.8
min	0.15	0.15	...	0.15
Enable	0	0	...	1
Parameters				
Kp	2			
Ki	2500			
initHandling	initialize integral			
ts_fact	1			
Outputs				
Out	0	0	...	0.647
Exp. Out	0	0	...	0.647
Out (DSP)	0	0	...	1390495657
Exp. Out (DSP)	0	0	...	1390495657

Test settings	
Tolerance Out	±4,6566e-07 (±1000 LSB)

Test statistics	
Min CPU cycles	59
Max CPU cycles	228
Avg CPU cycles	152

Test case: Conversion test OK

Conversion test for Control block PILimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
initHandling	0	0	...	1
sfrb0	31	31	...	31
sfrb1	27	27	...	27
b0	-2362232	-2230997	...	2362232
b1	-1342177280	-1267611876	...	1342177280
Exp. initHandling	0	0	...	1
Exp. sfrb0	31	31	...	31
Exp. sfrb1	27	27	...	27
Exp. b0	-2362232	-2230997	...	2362232
Exp. b1	-1342177280	-1267611876	...	1342177280

Test settings	
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test OK

Conversion-on-Target test for Control block PILimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
initHandling	0	0	...	1
sfrb0	31	31	...	31
sfrb1	27	27	...	27
b0	-2362232	-2230997	...	2362232
b1	-1342177280	-1267611904	...	1342177280
Exp. initHandling	0	0	...	1
Exp. sfrb0	31	31	...	31
Exp. sfrb1	27	27	...	27
Exp. b0	-2362232	-2230997	...	2362232
Exp. b1	-1342177280	-1267611876	...	1342177280

Test settings	
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±1,0000e+00
Tolerance b1	±1,0000e+02

Test statistics	
Min CPU cycles	1859
Max CPU cycles	2570
Avg CPU cycles	2210

Verification: PILimit FiP32 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for Control block PILimit.

Test results				
Time step	1	2	...	201
CPU cycles	68	68	...	215
Inputs				
In (DSP)	0	0	...	0
Init (DSP)	236223201	236223201	...	236223201
max (DSP)	1717986918	1717986918	...	1717986918
min (DSP)	322122547	322122547	...	322122547
Enable (DSP)	0	0	...	1
In	0	0	...	0
Init	0.11	0.11	...	0.11
max	0.8	0.8	...	0.8
min	0.15	0.15	...	0.15
Enable	0	0	...	1
Parameters				
Kp	2			
Ki	2500			
initHandling	initialize integral			
ts_fact	1			
Outputs				
Out	0	0	...	0.647
Exp. Out	0	0	...	0.647
Out (DSP)	0	0	...	1390495657
Exp. Out (DSP)	0	0	...	1390495657

Test settings	
Tolerance Out	±4,6566e-07 (±1000 LSB)

Test statistics	
Min CPU cycles	68
Max CPU cycles	247
Avg CPU cycles	202

Test case: Conversion test OK

Conversion test for Control block PILimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
initHandling	0	0	...	1
sfrb0	31	31	...	31
sfrb1	27	27	...	27
b0	-2362232	-2230997	...	2362232
b1	-1342177280	-1267611876	...	1342177280
Exp. initHandling	0	0	...	1
Exp. sfrb0	31	31	...	31
Exp. sfrb1	27	27	...	27
Exp. b0	-2362232	-2230997	...	2362232
Exp. b1	-1342177280	-1267611876	...	1342177280

Test settings	
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test OK

Conversion-on-Target test for Control block PILimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
initHandling	0	0	...	1
sfrb0	31	31	...	31
sfrb1	27	27	...	27
b0	-2362232	-2230997	...	2362232
b1	-1342177280	-1267611904	...	1342177280
Exp. initHandling	0	0	...	1
Exp. sfrb0	31	31	...	31
Exp. sfrb1	27	27	...	27
Exp. b0	-2362232	-2230997	...	2362232
Exp. b1	-1342177280	-1267611876	...	1342177280

Test settings	
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±1,0000e+00
Tolerance b1	±1,0000e+02

Test statistics	
Min CPU cycles	2500
Max CPU cycles	4353
Avg CPU cycles	3742

Verification: PILimit FiP32 CPU dsPIC33EP256MC502

Date of Test	2026-06-23
Target controller	dsPIC33EP256MC502

Test case: Inport test

OK

Inport test for Control block PILimit.

Test results				
Time step	1	2	...	201
CPU cycles	63	63	...	669
Inputs				
In (DSP)	0	0	...	0
Init (DSP)	236223201	236223201	...	236223201
max (DSP)	1717986918	1717986918	...	1717986918
min (DSP)	322122547	322122547	...	322122547
Enable (DSP)	0	0	...	1
In	0	0	...	0
Init	0.11	0.11	...	0.11
max	0.8	0.8	...	0.8
min	0.15	0.15	...	0.15
Enable	0	0	...	1
Parameters				
Kp	2			
Ki	2500			
initHandling	initialize integral			
ts_fact	1			
Outputs				
Out	0	0	...	0.647
Exp. Out	0	0	...	0.647
Out (DSP)	0	0	...	1390495657
Exp. Out (DSP)	0	0	...	1390495657

Test settings	
Tolerance Out	±4,6566e-07 (±1000 LSB)

Test statistics	
Min CPU cycles	63
Max CPU cycles	699
Avg CPU cycles	604

Test case: Conversion test OK

Conversion test for Control block PILimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
initHandling	0	0	...	1
sfrb0	31	31	...	31
sfrb1	27	27	...	27
b0	-2362232	-2230997	...	2362232
b1	-1342177280	-1267611876	...	1342177280
Exp. initHandling	0	0	...	1
Exp. sfrb0	31	31	...	31
Exp. sfrb1	27	27	...	27
Exp. b0	-2362232	-2230997	...	2362232
Exp. b1	-1342177280	-1267611876	...	1342177280

Test settings	
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test OK

Conversion-on-Target test for Control block PILimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
initHandling	0	0	...	1
sfrb0	31	31	...	31
sfrb1	27	27	...	27
b0	-2362232	-2230997	...	2362232
b1	-1342177280	-1267611904	...	1342177280
Exp. initHandling	0	0	...	1
Exp. sfrb0	31	31	...	31
Exp. sfrb1	27	27	...	27
Exp. b0	-2362232	-2230997	...	2362232
Exp. b1	-1342177280	-1267611876	...	1342177280

Test settings	
Tolerance initHandling	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance b0	±1,0000e+00
Tolerance b1	±1,0000e+02

Test statistics	
Min CPU cycles	7253
Max CPU cycles	15987
Avg CPU cycles	13506

Verification: PILimit Float32 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for Control block PILimit.

Test results				
Time step	1	2	...	201
CPU cycles	73	73	...	128
Inputs				
In (DSP)	0	0	...	0
Init (DSP)	0.11	0.11	...	0.11
max (DSP)	0.8	0.8	...	0.8
min (DSP)	0.15	0.15	...	0.15
Enable (DSP)	0	0	...	1
In	0	0	...	0
Init	0.11	0.11	...	0.11
max	0.8	0.8	...	0.8
min	0.15	0.15	...	0.15
Enable	0	0	...	1
Parameters				
Kp	2			
Ki	2500			
initHandling	initialize integral			
ts_fact	1			
Outputs				
Out	0	0	...	0.647
Exp. Out	0	0	...	0.647
Out (DSP)	0	0	...	0.647
Exp. Out (DSP)	0	0	...	0.647

Test settings	
Tolerance Out	±4,6566e-07 (±1000 LSB)

Test statistics	
Min CPU cycles	73
Max CPU cycles	150
Avg CPU cycles	122

Test case: Conversion test OK

Conversion test for Control block PILimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
initHandling	0	0	...	1
b0	-0.001	-0.001	...	0.001
b1	-10	-9.444	...	10
Exp. initHandling	0	0	...	1
Exp. b0	-0.001	-0.001	...	0.001
Exp. b1	-10	-9.444	...	10

Test settings	
Tolerance initHandling	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test OK

Conversion-on-Target test for Control block PILimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
initHandling	0	0	...	1
b0	-0.001	-0.001	...	0.001
b1	-10	-9.444	...	10
Exp. initHandling	0	0	...	1
Exp. b0	-0.001	-0.001	...	0.001
Exp. b1	-10	-9.444	...	10

Test settings	
Tolerance initHandling	±0,0000e+00
Tolerance b0	±1,0000e-10
Tolerance b1	±1,0000e-06

Test statistics	
Min CPU cycles	1925
Max CPU cycles	1947
Avg CPU cycles	1925

Verification: PILimit Float32 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for Control block PILimit.

Test results				
Time step	1	2	...	201
CPU cycles	45	45	...	93
Inputs				
In (DSP)	0	0	...	0
Init (DSP)	0.11	0.11	...	0.11
max (DSP)	0.8	0.8	...	0.8
min (DSP)	0.15	0.15	...	0.15
Enable (DSP)	0	0	...	1
In	0	0	...	0
Init	0.11	0.11	...	0.11
max	0.8	0.8	...	0.8
min	0.15	0.15	...	0.15
Enable	0	0	...	1
Parameters				
Kp	2			
Ki	2500			
initHandling	initialize integral			
ts_fact	1			
Outputs				
Out	0	0	...	0.647
Exp. Out	0	0	...	0.647
Out (DSP)	0	0	...	0.647
Exp. Out (DSP)	0	0	...	0.647

Test settings	
Tolerance Out	±4,6566e-07 (±1000 LSB)

Test statistics	
Min CPU cycles	45
Max CPU cycles	115
Avg CPU cycles	90

Test case: Conversion test OK

Conversion test for Control block PILimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
initHandling	0	0	...	1
b0	-0.001	-0.001	...	0.001
b1	-10	-9.444	...	10
Exp. initHandling	0	0	...	1
Exp. b0	-0.001	-0.001	...	0.001
Exp. b1	-10	-9.444	...	10

Test settings	
Tolerance initHandling	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test OK

Conversion-on-Target test for Control block PILimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
initHandling	0	0	...	1
b0	-0.001	-0.001	...	0.001
b1	-10	-9.444	...	10
Exp. initHandling	0	0	...	1
Exp. b0	-0.001	-0.001	...	0.001
Exp. b1	-10	-9.444	...	10

Test settings	
Tolerance initHandling	±0,0000e+00
Tolerance b0	±1,0000e-10
Tolerance b1	±1,0000e-06

Test statistics	
Min CPU cycles	903
Max CPU cycles	903
Avg CPU cycles	903

Verification: PILimit Float32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for Control block PILimit.

Test results				
Time step	1	2	...	201
CPU cycles	78	78	...	121
Inputs				
In (DSP)	0	0	...	0
Init (DSP)	0.11	0.11	...	0.11
max (DSP)	0.8	0.8	...	0.8
min (DSP)	0.15	0.15	...	0.15
Enable (DSP)	0	0	...	1
In	0	0	...	0
Init	0.11	0.11	...	0.11
max	0.8	0.8	...	0.8
min	0.15	0.15	...	0.15
Enable	0	0	...	1
Parameters				
Kp	2			
Ki	2500			
initHandling	initialize integral			
ts_fact	1			
Outputs				
Out	0	0	...	0.647
Exp. Out	0	0	...	0.647
Out (DSP)	0	0	...	0.647
Exp. Out (DSP)	0	0	...	0.647

Test settings	
Tolerance Out	±4,6566e-07 (±1000 LSB)

Test statistics	
Min CPU cycles	78
Max CPU cycles	172
Avg CPU cycles	117

Test case: Conversion test OK

Conversion test for Control block PILimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
initHandling	0	0	...	1
b0	-0.001	-0.001	...	0.001
b1	-10	-9.444	...	10
Exp. initHandling	0	0	...	1
Exp. b0	-0.001	-0.001	...	0.001
Exp. b1	-10	-9.444	...	10

Test settings	
Tolerance initHandling	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test OK

Conversion-on-Target test for Control block PILimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
initHandling	0	0	...	1
b0	-0.001	-0.001	...	0.001
b1	-10	-9.444	...	10
Exp. initHandling	0	0	...	1
Exp. b0	-0.001	-0.001	...	0.001
Exp. b1	-10	-9.444	...	10

Test settings	
Tolerance initHandling	±0,0000e+00
Tolerance b0	±1,0000e-10
Tolerance b1	±1,0000e-06

Test statistics	
Min CPU cycles	918
Max CPU cycles	979
Avg CPU cycles	919

Verification: PILimit Float32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for Control block PILimit.

Test results				
Time step	1	2	...	201
CPU cycles	82	82	...	702
Inputs				
In (DSP)	0	0	...	0
Init (DSP)	0.11	0.11	...	0.11
max (DSP)	0.8	0.8	...	0.8
min (DSP)	0.15	0.15	...	0.15
Enable (DSP)	0	0	...	1
In	0	0	...	0
Init	0.11	0.11	...	0.11
max	0.8	0.8	...	0.8
min	0.15	0.15	...	0.15
Enable	0	0	...	1
Parameters				
Kp	2			
Ki	2500			
initHandling	initialize integral			
ts_fact	1			
Outputs				
Out	0	0	...	0.647
Exp. Out	0	0	...	0.647
Out (DSP)	0	0	...	0.647
Exp. Out (DSP)	0	0	...	0.647

Test settings	
Tolerance Out	±4,6566e-07 (±1000 LSB)

Test statistics	
Min CPU cycles	82
Max CPU cycles	976
Avg CPU cycles	720

Test case: Conversion test OK

Conversion test for Control block PILimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
initHandling	0	0	...	1
b0	-0.001	-0.001	...	0.001
b1	-10	-9.444	...	10
Exp. initHandling	0	0	...	1
Exp. b0	-0.001	-0.001	...	0.001
Exp. b1	-10	-9.444	...	10

Test settings	
Tolerance initHandling	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test OK

Conversion-on-Target test for Control block PILimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
initHandling	0	0	...	1
b0	-0.001	-0.001	...	0.001
b1	-10	-9.444	...	10
Exp. initHandling	0	0	...	1
Exp. b0	-0.001	-0.001	...	0.001
Exp. b1	-10	-9.444	...	10

Test settings	
Tolerance initHandling	±0,0000e+00
Tolerance b0	±1,0000e-10
Tolerance b1	±1,0000e-06

Test statistics	
Min CPU cycles	2118
Max CPU cycles	2212
Avg CPU cycles	2170

Verification: PILimit Float32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for Control block PILimit.

Test results				
Time step	1	2	...	201
CPU cycles	69	69	...	290
Inputs				
In (DSP)	0	0	...	0
Init (DSP)	0.11	0.11	...	0.11
max (DSP)	0.8	0.8	...	0.8
min (DSP)	0.15	0.15	...	0.15
Enable (DSP)	0	0	...	1
In	0	0	...	0
Init	0.11	0.11	...	0.11
max	0.8	0.8	...	0.8
min	0.15	0.15	...	0.15
Enable	0	0	...	1
Parameters				
Kp	2			
Ki	2500			
initHandling	initialize integral			
ts_fact	1			
Outputs				
Out	0	0	...	0.647
Exp. Out	0	0	...	0.647
Out (DSP)	0	0	...	0.647
Exp. Out (DSP)	0	0	...	0.647

Test settings	
Tolerance Out	±4,6566e-07 (±1000 LSB)

Test statistics	
Min CPU cycles	69
Max CPU cycles	390
Avg CPU cycles	308

Test case: Conversion test OK

Conversion test for Control block PILimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
initHandling	0	0	...	1
b0	-0.001	-0.001	...	0.001
b1	-10	-9.444	...	10
Exp. initHandling	0	0	...	1
Exp. b0	-0.001	-0.001	...	0.001
Exp. b1	-10	-9.444	...	10

Test settings	
Tolerance initHandling	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test OK

Conversion-on-Target test for Control block PILimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
initHandling	0	0	...	1
b0	-0.001	-0.001	...	0.001
b1	-10	-9.444	...	10
Exp. initHandling	0	0	...	1
Exp. b0	-0.001	-0.001	...	0.001
Exp. b1	-10	-9.444	...	10

Test settings	
Tolerance initHandling	±0,0000e+00
Tolerance b0	±1,0000e-10
Tolerance b1	±1,0000e-06

Test statistics	
Min CPU cycles	742
Max CPU cycles	761
Avg CPU cycles	758

Verification: PILimit Float32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for Control block PILimit.

Test results				
Time step	1	2	...	201
CPU cycles	79	60	...	110
Inputs				
In (DSP)	0	0	...	0
Init (DSP)	0.11	0.11	...	0.11
max (DSP)	0.8	0.8	...	0.8
min (DSP)	0.15	0.15	...	0.15
Enable (DSP)	0	0	...	1
In	0	0	...	0
Init	0.11	0.11	...	0.11
max	0.8	0.8	...	0.8
min	0.15	0.15	...	0.15
Enable	0	0	...	1
Parameters				
Kp	2			
Ki	2500			
initHandling	initialize integral			
ts_fact	1			
Outputs				
Out	0	0	...	0.647
Exp. Out	0	0	...	0.647
Out (DSP)	0	0	...	0.647
Exp. Out (DSP)	0	0	...	0.647

Test settings	
Tolerance Out	±4,6566e-07 (±1000 LSB)

Test statistics	
Min CPU cycles	60
Max CPU cycles	166
Avg CPU cycles	107

Test case: Conversion test OK

Conversion test for Control block PILimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
initHandling	0	0	...	1
b0	-0.001	-0.001	...	0.001
b1	-10	-9.444	...	10
Exp. initHandling	0	0	...	1
Exp. b0	-0.001	-0.001	...	0.001
Exp. b1	-10	-9.444	...	10

Test settings	
Tolerance initHandling	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test OK

Conversion-on-Target test for Control block PILimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
initHandling	0	0	...	1
b0	-0.001	-0.001	...	0.001
b1	-10	-9.444	...	10
Exp. initHandling	0	0	...	1
Exp. b0	-0.001	-0.001	...	0.001
Exp. b1	-10	-9.444	...	10

Test settings	
Tolerance initHandling	±0,0000e+00
Tolerance b0	±1,0000e-10
Tolerance b1	±1,0000e-06

Test statistics	
Min CPU cycles	882
Max CPU cycles	996
Avg CPU cycles	887

Verification: PILimit Float32 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for Control block PILimit.

Test results				
Time step	1	2	...	201
CPU cycles	67	67	...	134
Inputs				
In (DSP)	0	0	...	0
Init (DSP)	0.11	0.11	...	0.11
max (DSP)	0.8	0.8	...	0.8
min (DSP)	0.15	0.15	...	0.15
Enable (DSP)	0	0	...	1
In	0	0	...	0
Init	0.11	0.11	...	0.11
max	0.8	0.8	...	0.8
min	0.15	0.15	...	0.15
Enable	0	0	...	1
Parameters				
Kp	2			
Ki	2500			
initHandling	initialize integral			
ts_fact	1			
Outputs				
Out	0	0	...	0.647
Exp. Out	0	0	...	0.647
Out (DSP)	0	0	...	0.647
Exp. Out (DSP)	0	0	...	0.647

Test settings	
Tolerance Out	±4,6566e-07 (±1000 LSB)

Test statistics	
Min CPU cycles	67
Max CPU cycles	164
Avg CPU cycles	126

Test case: Conversion test OK

Conversion test for Control block PILimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
initHandling	0	0	...	1
b0	-0.001	-0.001	...	0.001
b1	-10	-9.444	...	10
Exp. initHandling	0	0	...	1
Exp. b0	-0.001	-0.001	...	0.001
Exp. b1	-10	-9.444	...	10

Test settings	
Tolerance initHandling	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test OK

Conversion-on-Target test for Control block PILimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
initHandling	0	0	...	1
b0	-0.001	-0.001	...	0.001
b1	-10	-9.444	...	10
Exp. initHandling	0	0	...	1
Exp. b0	-0.001	-0.001	...	0.001
Exp. b1	-10	-9.444	...	10

Test settings	
Tolerance initHandling	±0,0000e+00
Tolerance b0	±1,0000e-10
Tolerance b1	±1,0000e-06

Test statistics	
Min CPU cycles	1427
Max CPU cycles	1449
Avg CPU cycles	1427

Verification: PILimit Float32 CPU dsPIC33EP256MC502

Date of Test	2026-06-23
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for Control block PILimit.

Test results				
Time step	1	2	...	201
CPU cycles	64	64	...	749
Inputs				
In (DSP)	0	0	...	0
Init (DSP)	0.11	0.11	...	0.11
max (DSP)	0.8	0.8	...	0.8
min (DSP)	0.15	0.15	...	0.15
Enable (DSP)	0	0	...	1
In	0	0	...	0
Init	0.11	0.11	...	0.11
max	0.8	0.8	...	0.8
min	0.15	0.15	...	0.15
Enable	0	0	...	1
Parameters				
Kp	2			
Ki	2500			
initHandling	initialize integral			
ts_fact	1			
Outputs				
Out	0	0	...	0.647
Exp. Out	0	0	...	0.647
Out (DSP)	0	0	...	0.647
Exp. Out (DSP)	0	0	...	0.647

Test settings	
Tolerance Out	±4,6566e-07 (±1000 LSB)

Test statistics	
Min CPU cycles	64
Max CPU cycles	1021
Avg CPU cycles	775

Test case: Conversion test OK

Conversion test for Control block PILimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
initHandling	0	0	...	1
b0	-0.001	-0.001	...	0.001
b1	-10	-9.444	...	10
Exp. initHandling	0	0	...	1
Exp. b0	-0.001	-0.001	...	0.001
Exp. b1	-10	-9.444	...	10

Test settings	
Tolerance initHandling	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test OK

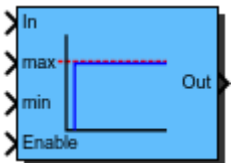
Conversion-on-Target test for Control block PILimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-10	-9.444	...	10
Ki	-11	-10.389	...	11
initHandling	initialize integral	initialize integral	...	initialize output
ts_fact	1	1	...	1
Controller parameters				
initHandling	0	0	...	1
b0	-0.001	-0.001	...	0.001
b1	-10	-9.444	...	10
Exp. initHandling	0	0	...	1
Exp. b0	-0.001	-0.001	...	0.001
Exp. b1	-10	-9.444	...	10

Test settings	
Tolerance initHandling	±0,0000e+00
Tolerance b0	±1,0000e-10
Tolerance b1	±1,0000e-06

Test statistics	
Min CPU cycles	2488
Max CPU cycles	3225
Avg CPU cycles	3201

Block: PLimit



P controller with output limitation:
G(s) = Kp

Inports	
In	Control error input
max	Maximum output value
min	Minimum output value
Enable	Enable == 0: Deactivation of block; Out set to 0 Enable == 1: Activation of block

Outports	
Out	Control value

Mask Parameters		
Name	**ID**	**Description**
Kp	1	Proportional Factor

Description:

Transfer function (zero-order hold discretization method):

$$G(z) = K_\mathrm{p}$$

Developer note: The source code of this block is used for block *P*.

Implementations:

FiP16 16 Bit Fixed Point Implementation
FiP32 32 Bit Fixed Point Implementation
Float32 32 Bit Floating Point Implementation
Float64 64 Bit Floating Point Implementation

Implementation: FiP16

16 Bit Fixed Point Implementation

Inports Data Type	
In	int16
max	int16
min	int16
Enable	bool

Outports Data Type	
Out	int16

Implementation: FiP32

32 Bit Fixed Point Implementation

Inports Data Type	
In	int32
max	int32
min	int32
Enable	bool

Outports Data Type	
Out	int32

Implementation: Float32

32 Bit Floating Point Implementation

Inports Data Type	
In	float32
max	float32
min	float32
Enable	bool

Outports Data Type	
Out	float32

Implementation: Float64

64 Bit Floating Point Implementation

Inports Data Type	
In	float64
max	float64
min	float64
Enable	bool

Outports Data Type	
Out	float64

Verification: PLimit FiP16 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for Control block PLimit.

Test results						
Time step	1	2	3	4	...	201
CPU cycles	64	64	64	90	...	90
Inputs						
In (DSP)	0	0	0	0	...	0
max (DSP)	26214	26214	26214	26214	...	26214
min (DSP)	4915	4915	4915	4915	...	4915
Enable (DSP)	0	0	0	1	...	1
In	0	0	0	0	...	0
max	0.8	0.8	0.8	0.8	...	0.8
min	0.15	0.15	0.15	0.15	...	0.15
Enable	0	0	0	1	...	1
Parameters						
Kp	2					
Outputs						
Out	0	0	0	0.15	...	0.15
Exp. Out	0	0	0	0.15	...	0.15
Out (DSP)	0	0	0	4915	...	4915
Exp. Out (DSP)	0	0	0	4915	...	4915

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	64
Max CPU cycles	90
Avg CPU cycles	89

Test case: Conversion test OK

Conversion test for Control block PLimit.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kp	-11	-10.389	-9.778	-9.167	...	11
Controller parameters						
sfrb1	11	11	11	11	...	11
b1	-22528	-21276	-20025	-18773	...	22528
Exp. sfrb1	11	11	11	11	...	11
Exp. b1	-22528	-21276	-20025	-18773	...	22528

Test settings	
Tolerance sfrb1	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block PLimit.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kp	-11	-10.389	-9.778	-9.167	...	11
Controller parameters						
sfrb1	11	11	11	11	...	11
b1	-22528	-21276	-20024	-18773	...	22528
Exp. sfrb1	11	11	11	11	...	11
Exp. b1	-22528	-21276	-20025	-18773	...	22528

Test settings	
Tolerance sfrb1	±0,0000e+00
Tolerance b1	±1,0000e+00

Test statistics	
Min CPU cycles	1406
Max CPU cycles	3556
Avg CPU cycles	2858

Verification: PLimit FiP16 CPU TM4C123GH6

Date of Test 2026-06-19

Target controller TM4C123GH6

Test case: Inport test OK

Inport test for Control block PLimit.

Test results						
Time step	1	2	3	4	...	201
CPU cycles	37	37	37	53	...	53
Inputs						
In (DSP)	0	0	0	0	...	0
max (DSP)	26214	26214	26214	26214	...	26214
min (DSP)	4915	4915	4915	4915	...	4915
Enable (DSP)	0	0	0	1	...	1
In	0	0	0	0	...	0
max	0.8	0.8	0.8	0.8	...	0.8
min	0.15	0.15	0.15	0.15	...	0.15
Enable	0	0	0	1	...	1
Parameters						
Kp	2					
Outputs						
Out	0	0	0	0.15	...	0.15
Exp. Out	0	0	0	0.15	...	0.15
Out (DSP)	0	0	0	4915	...	4915
Exp. Out (DSP)	0	0	0	4915	...	4915

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	37
Max CPU cycles	53
Avg CPU cycles	52

Test case: Conversion test OK

Conversion test for Control block PLimit.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kp	-11	-10.389	-9.778	-9.167	...	11
Controller parameters						
sfrb1	11	11	11	11	...	11
b1	-22528	-21276	-20025	-18773	...	22528
Exp. sfrb1	11	11	11	11	...	11
Exp. b1	-22528	-21276	-20025	-18773	...	22528

Test settings	
Tolerance sfrb1	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block PLimit.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kp	-11	-10.389	-9.778	-9.167	...	11
Controller parameters						
sfrb1	11	11	11	11	...	11
b1	-22528	-21276	-20024	-18773	...	22528
Exp. sfrb1	11	11	11	11	...	11
Exp. b1	-22528	-21276	-20025	-18773	...	22528

Test settings	
Tolerance sfrb1	±0,0000e+00
Tolerance b1	±1,0000e+00

Test statistics	
Min CPU cycles	727
Max CPU cycles	1979
Avg CPU cycles	1569

Verification: PLimit FiP16 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for Control block PLimit.

Test results						
Time step	1	2	3	4	...	201
CPU cycles	68	68	68	83	...	83
Inputs						
In (DSP)	0	0	0	0	...	0
max (DSP)	26214	26214	26214	26214	...	26214
min (DSP)	4915	4915	4915	4915	...	4915
Enable (DSP)	0	0	0	1	...	1
In	0	0	0	0	...	0
max	0.8	0.8	0.8	0.8	...	0.8
min	0.15	0.15	0.15	0.15	...	0.15
Enable	0	0	0	1	...	1
Parameters						
Kp	2					
Outputs						
Out	0	0	0	0.15	...	0.15
Exp. Out	0	0	0	0.15	...	0.15
Out (DSP)	0	0	0	4915	...	4915
Exp. Out (DSP)	0	0	0	4915	...	4915

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	68
Max CPU cycles	83
Avg CPU cycles	82

Test case: Conversion test OK

Conversion test for Control block PLimit.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kp	-11	-10.389	-9.778	-9.167	...	11
Controller parameters						
sfrb1	11	11	11	11	...	11
b1	-22528	-21276	-20025	-18773	...	22528
Exp. sfrb1	11	11	11	11	...	11
Exp. b1	-22528	-21276	-20025	-18773	...	22528

Test settings	
Tolerance sfrb1	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block PLimit.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kp	-11	-10.389	-9.778	-9.167	...	11
Controller parameters						
sfrb1	11	11	11	11	...	11
b1	-22528	-21276	-20024	-18773	...	22528
Exp. sfrb1	11	11	11	11	...	11
Exp. b1	-22528	-21276	-20025	-18773	...	22528

Test settings	
Tolerance sfrb1	±0,0000e+00
Tolerance b1	±1,0000e+00

Test statistics	
Min CPU cycles	911
Max CPU cycles	1434
Avg CPU cycles	1263

Verification: PLimit FiP16 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for Control block PLimit.

Test results						
Time step	1	2	3	4	...	201
CPU cycles	52	52	52	82	...	82
Inputs						
In (DSP)	0	0	0	0	...	0
max (DSP)	26214	26214	26214	26214	...	26214
min (DSP)	4915	4915	4915	4915	...	4915
Enable (DSP)	0	0	0	1	...	1
In	0	0	0	0	...	0
max	0.8	0.8	0.8	0.8	...	0.8
min	0.15	0.15	0.15	0.15	...	0.15
Enable	0	0	0	1	...	1
Parameters						
Kp	2					
Outputs						
Out	0	0	0	0.15	...	0.15
Exp. Out	0	0	0	0.15	...	0.15
Out (DSP)	0	0	0	4915	...	4915
Exp. Out (DSP)	0	0	0	4915	...	4915

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	52
Max CPU cycles	82
Avg CPU cycles	81

Test case: Conversion test OK

Conversion test for Control block PLimit.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kp	-11	-10.389	-9.778	-9.167	...	11
Controller parameters						
sfrb1	11	11	11	11	...	11
b1	-22528	-21276	-20025	-18773	...	22528
Exp. sfrb1	11	11	11	11	...	11
Exp. b1	-22528	-21276	-20025	-18773	...	22528

Test settings	
Tolerance sfrb1	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block PLimit.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kp	-11	-10.389	-9.778	-9.167	...	11
Controller parameters						
sfrb1	11	11	11	11	...	11
b1	-22528	-21276	-20024	-18773	...	22528
Exp. sfrb1	11	11	11	11	...	11
Exp. b1	-22528	-21276	-20025	-18773	...	22528

Test settings	
Tolerance sfrb1	±0,0000e+00
Tolerance b1	±1,0000e+00

Test statistics	
Min CPU cycles	1640
Max CPU cycles	4611
Avg CPU cycles	3683

Verification: PLimit FiP16 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for Control block PLimit.

Test results						
Time step	1	2	3	4	...	201
CPU cycles	30	30	30	56	...	56
Inputs						
In (DSP)	0	0	0	0	...	0
max (DSP)	26214	26214	26214	26214	...	26214
min (DSP)	4915	4915	4915	4915	...	4915
Enable (DSP)	0	0	0	1	...	1
In	0	0	0	0	...	0
max	0.8	0.8	0.8	0.8	...	0.8
min	0.15	0.15	0.15	0.15	...	0.15
Enable	0	0	0	1	...	1
Parameters						
Kp	2					
Outputs						
Out	0	0	0	0.15	...	0.15
Exp. Out	0	0	0	0.15	...	0.15
Out (DSP)	0	0	0	4915	...	4915
Exp. Out (DSP)	0	0	0	4915	...	4915

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	30
Max CPU cycles	56
Avg CPU cycles	55

Test case: Conversion test OK

Conversion test for Control block PLimit.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kp	-11	-10.389	-9.778	-9.167	...	11
Controller parameters						
sfrb1	11	11	11	11	...	11
b1	-22528	-21276	-20025	-18773	...	22528
Exp. sfrb1	11	11	11	11	...	11
Exp. b1	-22528	-21276	-20025	-18773	...	22528

Test settings	
Tolerance sfrb1	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block PLimit.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kp	-11	-10.389	-9.778	-9.167	...	11
Controller parameters						
sfrb1	11	11	11	11	...	11
b1	-22528	-21276	-20024	-18773	...	22528
Exp. sfrb1	11	11	11	11	...	11
Exp. b1	-22528	-21276	-20025	-18773	...	22528

Test settings	
Tolerance sfrb1	±0,0000e+00
Tolerance b1	±1,0000e+00

Test statistics	
Min CPU cycles	774
Max CPU cycles	1943
Avg CPU cycles	1576

Verification: PLimit FiP16 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test

OK

Inport test for Control block PLimit.

Test results						
Time step	1	2	3	4	...	201
CPU cycles	72	58	58	83	...	83
Inputs						
In (DSP)	0	0	0	0	...	0
max (DSP)	26214	26214	26214	26214	...	26214
min (DSP)	4915	4915	4915	4915	...	4915
Enable (DSP)	0	0	0	1	...	1
In	0	0	0	0	...	0
max	0.8	0.8	0.8	0.8	...	0.8
min	0.15	0.15	0.15	0.15	...	0.15
Enable	0	0	0	1	...	1
Parameters						
Kp	2					
Outputs						
Out	0	0	0	0.15	...	0.15
Exp. Out	0	0	0	0.15	...	0.15
Out (DSP)	0	0	0	4915	...	4915
Exp. Out (DSP)	0	0	0	4915	...	4915

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	58
Max CPU cycles	83
Avg CPU cycles	82

Test case: Conversion test

OK

Conversion test for Control block PLimit.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kp	-11	-10.389	-9.778	-9.167	...	11
Controller parameters						
sfrb1	11	11	11	11	...	11
b1	-22528	-21276	-20025	-18773	...	22528
Exp. sfrb1	11	11	11	11	...	11
Exp. b1	-22528	-21276	-20025	-18773	...	22528

Test settings	
Tolerance sfrb1	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block PLimit.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kp	-11	-10.389	-9.778	-9.167	...	11
Controller parameters						
sfrb1	11	11	11	11	...	11
b1	-22528	-21276	-20024	-18773	...	22528
Exp. sfrb1	11	11	11	11	...	11
Exp. b1	-22528	-21276	-20025	-18773	...	22528

Test settings	
Tolerance sfrb1	±0,0000e+00
Tolerance b1	±1,0000e+00

Test statistics	
Min CPU cycles	667
Max CPU cycles	1218
Avg CPU cycles	992

Verification: PLimit FiP16 CPU TMS320F28379D

Date of Test 2026-06-22

Target controller TMS320F28379D

Test case: Inport test OK

Inport test for Control block PLimit.

Test results						
Time step	1	2	3	4	...	201
CPU cycles	60	60	60	86	...	86
Inputs						
In (DSP)	0	0	0	0	...	0
max (DSP)	26214	26214	26214	26214	...	26214
min (DSP)	4915	4915	4915	4915	...	4915
Enable (DSP)	0	0	0	1	...	1
In	0	0	0	0	...	0
max	0.8	0.8	0.8	0.8	...	0.8
min	0.15	0.15	0.15	0.15	...	0.15
Enable	0	0	0	1	...	1
Parameters						
Kp	2					
Outputs						
Out	0	0	0	0.15	...	0.15
Exp. Out	0	0	0	0.15	...	0.15
Out (DSP)	0	0	0	4915	...	4915
Exp. Out (DSP)	0	0	0	4915	...	4915

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	60
Max CPU cycles	86
Avg CPU cycles	85

Test case: Conversion test OK

Conversion test for Control block PLimit.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kp	-11	-10.389	-9.778	-9.167	...	11
Controller parameters						
sfrb1	11	11	11	11	...	11
b1	-22528	-21276	-20025	-18773	...	22528
Exp. sfrb1	11	11	11	11	...	11
Exp. b1	-22528	-21276	-20025	-18773	...	22528

Test settings	
Tolerance sfrb1	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block PLimit.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kp	-11	-10.389	-9.778	-9.167	...	11
Controller parameters						
sfrb1	11	11	11	11	...	11
b1	-22528	-21276	-20024	-18773	...	22528
Exp. sfrb1	11	11	11	11	...	11
Exp. b1	-22528	-21276	-20025	-18773	...	22528

Test settings	
Tolerance sfrb1	±0,0000e+00
Tolerance b1	±1,0000e+00

Test statistics	
Min CPU cycles	1079
Max CPU cycles	2769
Avg CPU cycles	2219

Verification: PLimit FiP16 CPU dsPIC33EP256MC502

Date of Test	2026-06-23
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for Control block PLimit.

Test results						
Time step	1	2	3	4	...	201
CPU cycles	39	39	39	74	...	74
Inputs						
In (DSP)	0	0	0	0	...	0
max (DSP)	26214	26214	26214	26214	...	26214
min (DSP)	4915	4915	4915	4915	...	4915
Enable (DSP)	0	0	0	1	...	1
In	0	0	0	0	...	0
max	0.8	0.8	0.8	0.8	...	0.8
min	0.15	0.15	0.15	0.15	...	0.15
Enable	0	0	0	1	...	1
Parameters						
Kp	2					
Outputs						
Out	0	0	0	0.15	...	0.15
Exp. Out	0	0	0	0.15	...	0.15
Out (DSP)	0	0	0	4915	...	4915
Exp. Out (DSP)	0	0	0	4915	...	4915

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	39
Max CPU cycles	74
Avg CPU cycles	73

Test case: Conversion test OK

Conversion test for Control block PLimit.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kp	-11	-10.389	-9.778	-9.167	...	11
Controller parameters						
sfrb1	11	11	11	11	...	11
b1	-22528	-21276	-20025	-18773	...	22528
Exp. sfrb1	11	11	11	11	...	11
Exp. b1	-22528	-21276	-20025	-18773	...	22528

Test settings	
Tolerance sfrb1	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block PLimit.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Kp	-11	-10.389	-9.778	-9.167	...	11
Controller parameters						
sfrb1	11	11	11	11	...	11
b1	-22528	-21276	-20024	-18773	...	22528
Exp. sfrb1	11	11	11	11	...	11
Exp. b1	-22528	-21276	-20025	-18773	...	22528

Test settings	
Tolerance sfrb1	±0,0000e+00
Tolerance b1	±1,0000e+00

Test statistics	
Min CPU cycles	2497
Max CPU cycles	10438
Avg CPU cycles	8074

Verification: PLimit FiP32 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for Control block PLimit.

Test results				
Time step	1	2	...	201
CPU cycles	67	67	...	184
Inputs				
In (DSP)	0	0	...	0
max (DSP)	1717986918	1717986918	...	1717986918
min (DSP)	322122547	322122547	...	322122547
Enable (DSP)	0	0	...	1
In	0	0	...	0
max	0.8	0.8	...	0.8
min	0.15	0.15	...	0.15
Enable	0	0	...	1
Parameters				
Kp	2			
Outputs				
Out	0	0	...	0.15
Exp. Out	0	0	...	0.15
Out (DSP)	0	0	...	322122547
Exp. Out (DSP)	0	0	...	322122547

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	67
Max CPU cycles	220
Avg CPU cycles	191

Test case: Conversion test OK

Conversion test for Control block PLimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-11	-10.389	...	11
Controller parameters				
sfrb1	27	27	...	27
b1	-1476395008	-1394373063	...	1476395008
Exp. sfrb1	27	27	...	27
Exp. b1	-1476395008	-1394373063	...	1476395008

Test settings	
Tolerance sfrb1	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block PLimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-11	-10.389	...	11
Controller parameters				
sfrb1	27	27	...	27
b1	-1476395008	-1394373120	...	1476395008
Exp. sfrb1	27	27	...	27
Exp. b1	-1476395008	-1394373063	...	1476395008

Test settings	
Tolerance sfrb1	±0,0000e+00
Tolerance b1	±1,0000e+02

Test statistics	
Min CPU cycles	1586
Max CPU cycles	3784
Avg CPU cycles	3082

Verification: PLimit FiP32 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for Control block PLimit.

Test results				
Time step	1	2	...	201
CPU cycles	43	43	...	87
Inputs				
In (DSP)	0	0	...	0
max (DSP)	1717986918	1717986918	...	1717986918
min (DSP)	322122547	322122547	...	322122547
Enable (DSP)	0	0	...	1
In	0	0	...	0
max	0.8	0.8	...	0.8
min	0.15	0.15	...	0.15
Enable	0	0	...	1
Parameters				
Kp	2			
Outputs				
Out	0	0	...	0.15
Exp. Out	0	0	...	0.15
Out (DSP)	0	0	...	322122547
Exp. Out (DSP)	0	0	...	322122547

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	43
Max CPU cycles	87
Avg CPU cycles	86

Test case: Conversion test OK

Conversion test for Control block PLimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-11	-10.389	...	11
Controller parameters				
sfrb1	27	27	...	27
b1	-1476395008	-1394373063	...	1476395008
Exp. sfrb1	27	27	...	27
Exp. b1	-1476395008	-1394373063	...	1476395008

Test settings	
Tolerance sfrb1	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test OK

Conversion-on-Target test for Control block PLimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-11	-10.389	...	11
Controller parameters				
sfrb1	27	27	...	27
b1	-1476395008	-1394373120	...	1476395008
Exp. sfrb1	27	27	...	27
Exp. b1	-1476395008	-1394373063	...	1476395008

Test settings	
Tolerance sfrb1	±0,0000e+00
Tolerance b1	±1,0000e+02

Test statistics	
Min CPU cycles	689
Max CPU cycles	1585
Avg CPU cycles	1303

Verification: PLimit FiP32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for Control block PLimit.

Test results				
Time step	1	2	...	201
CPU cycles	68	68	...	111
Inputs				
In (DSP)	0	0	...	0
max (DSP)	1717986918	1717986918	...	1717986918
min (DSP)	322122547	322122547	...	322122547
Enable (DSP)	0	0	...	1
In	0	0	...	0
max	0.8	0.8	...	0.8
min	0.15	0.15	...	0.15
Enable	0	0	...	1
Parameters				
Kp	2			
Outputs				
Out	0	0	...	0.15
Exp. Out	0	0	...	0.15
Out (DSP)	0	0	...	322122547
Exp. Out (DSP)	0	0	...	322122547

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	68
Max CPU cycles	111
Avg CPU cycles	110

Test case: Conversion test OK

Conversion test for Control block PLimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-11	-10.389	...	11
Controller parameters				
sfrb1	27	27	...	27
b1	-1476395008	-1394373063	...	1476395008
Exp. sfrb1	27	27	...	27
Exp. b1	-1476395008	-1394373063	...	1476395008

Test settings	
Tolerance sfrb1	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block PLimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-11	-10.389	...	11
Controller parameters				
sfrb1	27	27	...	27
b1	-1476395008	-1394373120	...	1476395008
Exp. sfrb1	27	27	...	27
Exp. b1	-1476395008	-1394373063	...	1476395008

Test settings	
Tolerance sfrb1	±0,0000e+00
Tolerance b1	±1,0000e+02

Test statistics	
Min CPU cycles	1275
Max CPU cycles	1841
Avg CPU cycles	1662

Verification: PLimit FiP32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for Control block PLimit.

Test results				
Time step	1	2	...	201
CPU cycles	64	64	...	189
Inputs				
In (DSP)	0	0	...	0
max (DSP)	1717986918	1717986918	...	1717986918
min (DSP)	322122547	322122547	...	322122547
Enable (DSP)	0	0	...	1
In	0	0	...	0
max	0.8	0.8	...	0.8
min	0.15	0.15	...	0.15
Enable	0	0	...	1
Parameters				
Kp	2			
Outputs				
Out	0	0	...	0.15
Exp. Out	0	0	...	0.15
Out (DSP)	0	0	...	322122547
Exp. Out (DSP)	0	0	...	322122547

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	64
Max CPU cycles	189
Avg CPU cycles	184

Test case: Conversion test OK

Conversion test for Control block PLimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-11	-10.389	...	11
Controller parameters				
sfrb1	27	27	...	27
b1	-1476395008	-1394373063	...	1476395008
Exp. sfrb1	27	27	...	27
Exp. b1	-1476395008	-1394373063	...	1476395008

Test settings	
Tolerance sfrb1	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block PLimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-11	-10.389	...	11
Controller parameters				
sfrb1	27	27	...	27
b1	-1476395008	-1394373120	...	1476395008
Exp. sfrb1	27	27	...	27
Exp. b1	-1476395008	-1394373063	...	1476395008

Test settings	
Tolerance sfrb1	±0,0000e+00
Tolerance b1	±1,0000e+02

Test statistics	
Min CPU cycles	2673
Max CPU cycles	5824
Avg CPU cycles	4950

Verification: PLimit FiP32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for Control block PLimit.

Test results				
Time step	1	2	...	201
CPU cycles	30	30	...	80
Inputs				
In (DSP)	0	0	...	0
max (DSP)	1717986918	1717986918	...	1717986918
min (DSP)	322122547	322122547	...	322122547
Enable (DSP)	0	0	...	1
In	0	0	...	0
max	0.8	0.8	...	0.8
min	0.15	0.15	...	0.15
Enable	0	0	...	1
Parameters				
Kp	2			
Outputs				
Out	0	0	...	0.15
Exp. Out	0	0	...	0.15
Out (DSP)	0	0	...	322122547
Exp. Out (DSP)	0	0	...	322122547

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	30
Max CPU cycles	80
Avg CPU cycles	78

Test case: Conversion test OK

Conversion test for Control block PLimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-11	-10.389	...	11
Controller parameters				
sfrb1	27	27	...	27
b1	-1476395008	-1394373063	...	1476395008
Exp. sfrb1	27	27	...	27
Exp. b1	-1476395008	-1394373063	...	1476395008

Test settings	
Tolerance sfrb1	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test OK

Conversion-on-Target test for Control block PLimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-11	-10.389	...	11
Controller parameters				
sfrb1	27	27	...	27
b1	-1476395008	-1394373120	...	1476395008
Exp. sfrb1	27	27	...	27
Exp. b1	-1476395008	-1394373063	...	1476395008

Test settings	
Tolerance sfrb1	±0,0000e+00
Tolerance b1	±1,0000e+02

Test statistics	
Min CPU cycles	1230
Max CPU cycles	2413
Avg CPU cycles	2045

Verification: PLimit FiP32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for Control block PLimit.

Test results				
Time step	1	2	...	201
CPU cycles	66	58	...	110
Inputs				
In (DSP)	0	0	...	0
max (DSP)	1717986918	1717986918	...	1717986918
min (DSP)	322122547	322122547	...	322122547
Enable (DSP)	0	0	...	1
In	0	0	...	0
max	0.8	0.8	...	0.8
min	0.15	0.15	...	0.15
Enable	0	0	...	1
Parameters				
Kp	2			
Outputs				
Out	0	0	...	0.15
Exp. Out	0	0	...	0.15
Out (DSP)	0	0	...	322122547
Exp. Out (DSP)	0	0	...	322122547

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	58
Max CPU cycles	113
Avg CPU cycles	109

Test case: Conversion test OK

Conversion test for Control block PLimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-11	-10.389	...	11
Controller parameters				
sfrb1	27	27	...	27
b1	-1476395008	-1394373063	...	1476395008
Exp. sfrb1	27	27	...	27
Exp. b1	-1476395008	-1394373063	...	1476395008

Test settings	
Tolerance sfrb1	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block PLimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-11	-10.389	...	11
Controller parameters				
sfrb1	27	27	...	27
b1	-1476395008	-1394373120	...	1476395008
Exp. sfrb1	27	27	...	27
Exp. b1	-1476395008	-1394373063	...	1476395008

Test settings	
Tolerance sfrb1	±0,0000e+00
Tolerance b1	±1,0000e+02

Test statistics	
Min CPU cycles	918
Max CPU cycles	1567
Avg CPU cycles	1252

Verification: PLimit FiP32 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for Control block PLimit.

Test results				
Time step	1	2	...	201
CPU cycles	65	65	...	163
Inputs				
In (DSP)	0	0	...	0
max (DSP)	1717986918	1717986918	...	1717986918
min (DSP)	322122547	322122547	...	322122547
Enable (DSP)	0	0	...	1
In	0	0	...	0
max	0.8	0.8	...	0.8
min	0.15	0.15	...	0.15
Enable	0	0	...	1
Parameters				
Kp	2			
Outputs				
Out	0	0	...	0.15
Exp. Out	0	0	...	0.15
Out (DSP)	0	0	...	322122547
Exp. Out (DSP)	0	0	...	322122547

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	65
Max CPU cycles	183
Avg CPU cycles	166

Test case: Conversion test OK

Conversion test for Control block PLimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-11	-10.389	...	11
Controller parameters				
sfrb1	27	27	...	27
b1	-1476395008	-1394373063	...	1476395008
Exp. sfrb1	27	27	...	27
Exp. b1	-1476395008	-1394373063	...	1476395008

Test settings	
Tolerance sfrb1	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block PLimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-11	-10.389	...	11
Controller parameters				
sfrb1	27	27	...	27
b1	-1476395008	-1394373120	...	1476395008
Exp. sfrb1	27	27	...	27
Exp. b1	-1476395008	-1394373063	...	1476395008

Test settings	
Tolerance sfrb1	±0,0000e+00
Tolerance b1	±1,0000e+02

Test statistics	
Min CPU cycles	1196
Max CPU cycles	2929
Avg CPU cycles	2375

Verification: PLimit FiP32 CPU dsPIC33EP256MC502

Date of Test	2026-06-23
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for Control block PLimit.

Test results				
Time step	1	2	...	201
CPU cycles	53	53	...	496
Inputs				
In (DSP)	0	0	...	0
max (DSP)	1717986918	1717986918	...	1717986918
min (DSP)	322122547	322122547	...	322122547
Enable (DSP)	0	0	...	1
In	0	0	...	0
max	0.8	0.8	...	0.8
min	0.15	0.15	...	0.15
Enable	0	0	...	1
Parameters				
Kp	2			
Outputs				
Out	0	0	...	0.15
Exp. Out	0	0	...	0.15
Out (DSP)	0	0	...	322122547
Exp. Out (DSP)	0	0	...	322122547

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	53
Max CPU cycles	503
Avg CPU cycles	491

Test case: Conversion test OK

Conversion test for Control block PLimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-11	-10.389	...	11
Controller parameters				
sfrb1	27	27	...	27
b1	-1476395008	-1394373063	...	1476395008
Exp. sfrb1	27	27	...	27
Exp. b1	-1476395008	-1394373063	...	1476395008

Test settings	
Tolerance sfrb1	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block PLimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-11	-10.389	...	11
Controller parameters				
sfrb1	27	27	...	27
b1	-1476395008	-1394373120	...	1476395008
Exp. sfrb1	27	27	...	27
Exp. b1	-1476395008	-1394373063	...	1476395008

Test settings	
Tolerance sfrb1	±0,0000e+00
Tolerance b1	±1,0000e+02

Test statistics	
Min CPU cycles	2903
Max CPU cycles	10578
Avg CPU cycles	8305

Verification: PLimit Float32 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test

OK

Inport test for Control block PLimit.

Test results				
Time step	1	2	...	201
CPU cycles	67	67	...	86
Inputs				
In (DSP)	0	0	...	0
max (DSP)	0.8	0.8	...	0.8
min (DSP)	0.15	0.15	...	0.15
Enable (DSP)	0	0	...	1
In	0	0	...	0
max	0.8	0.8	...	0.8
min	0.15	0.15	...	0.15
Enable	0	0	...	1
Parameters				
Kp	2			
Outputs				
Out	0	0	...	0.15
Exp. Out	0	0	...	0.15
Out (DSP)	0	0	...	0.15
Exp. Out (DSP)	0	0	...	0.15

Test settings	
Tolerance Out	±9,3132e-09 (±20 LSB)

Test statistics	
Min CPU cycles	67
Max CPU cycles	86
Avg CPU cycles	85

Test case: Conversion test

OK

Conversion test for Control block PLimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-11	-10.389	...	11
Controller parameters				
b1	-11	-10.389	...	11
Exp. b1	-11	-10.389	...	11

Test settings	
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block PLimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-11	-10.389	...	11
Controller parameters				
b1	-11	-10.389	...	11
Exp. b1	-11	-10.389	...	11

Test settings	
Tolerance b1	±1,0000e-06

Test statistics	
Min CPU cycles	807
Max CPU cycles	818
Avg CPU cycles	807

Verification: PLimit Float32 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for Control block PLimit.

Test results				
Time step	1	2	...	201
CPU cycles	31	31	...	61
Inputs				
In (DSP)	0	0	...	0
max (DSP)	0.8	0.8	...	0.8
min (DSP)	0.15	0.15	...	0.15
Enable (DSP)	0	0	...	1
In	0	0	...	0
max	0.8	0.8	...	0.8
min	0.15	0.15	...	0.15
Enable	0	0	...	1
Parameters				
Kp	2			
Outputs				
Out	0	0	...	0.15
Exp. Out	0	0	...	0.15
Out (DSP)	0	0	...	0.15
Exp. Out (DSP)	0	0	...	0.15

Test settings	
Tolerance Out	±9,3132e-09 (±20 LSB)

Test statistics	
Min CPU cycles	31
Max CPU cycles	61
Avg CPU cycles	60

Test case: Conversion test OK

Conversion test for Control block PLimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-11	-10.389	...	11
Controller parameters				
b1	-11	-10.389	...	11
Exp. b1	-11	-10.389	...	11

Test settings	
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block PLimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-11	-10.389	...	11
Controller parameters				
b1	-11	-10.389	...	11
Exp. b1	-11	-10.389	...	11

Test settings	
Tolerance b1	±1,0000e-06

Test statistics	
Min CPU cycles	397
Max CPU cycles	397
Avg CPU cycles	397

Verification: PLimit Float32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for Control block PLimit.

Test results				
Time step	1	2	...	201
CPU cycles	76	76	...	98
Inputs				
In (DSP)	0	0	...	0
max (DSP)	0.8	0.8	...	0.8
min (DSP)	0.15	0.15	...	0.15
Enable (DSP)	0	0	...	1
In	0	0	...	0
max	0.8	0.8	...	0.8
min	0.15	0.15	...	0.15
Enable	0	0	...	1
Parameters				
Kp	2			
Outputs				
Out	0	0	...	0.15
Exp. Out	0	0	...	0.15
Out (DSP)	0	0	...	0.15
Exp. Out (DSP)	0	0	...	0.15

Test settings	
Tolerance Out	±9,3132e-09 (±20 LSB)

Test statistics	
Min CPU cycles	76
Max CPU cycles	98
Avg CPU cycles	97

Test case: Conversion test OK

Conversion test for Control block PLimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-11	-10.389	...	11
Controller parameters				
b1	-11	-10.389	...	11
Exp. b1	-11	-10.389	...	11

Test settings	
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block PLimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-11	-10.389	...	11
Controller parameters				
b1	-11	-10.389	...	11
Exp. b1	-11	-10.389	...	11

Test settings	
Tolerance b1	±1,0000e-06

Test statistics	
Min CPU cycles	470
Max CPU cycles	470
Avg CPU cycles	470

Verification: PLimit Float32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for Control block PLimit.

Test results				
Time step	1	2	...	201
CPU cycles	64	64	...	352
Inputs				
In (DSP)	0	0	...	0
max (DSP)	0.8	0.8	...	0.8
min (DSP)	0.15	0.15	...	0.15
Enable (DSP)	0	0	...	1
In	0	0	...	0
max	0.8	0.8	...	0.8
min	0.15	0.15	...	0.15
Enable	0	0	...	1
Parameters				
Kp	2			
Outputs				
Out	0	0	...	0.15
Exp. Out	0	0	...	0.15
Out (DSP)	0	0	...	0.15
Exp. Out (DSP)	0	0	...	0.15

Test settings	
Tolerance Out	±9,3132e-09 (±20 LSB)

Test statistics	
Min CPU cycles	64
Max CPU cycles	491
Avg CPU cycles	399

Test case: Conversion test OK

Conversion test for Control block PLimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-11	-10.389	...	11
Controller parameters				
b1	-11	-10.389	...	11
Exp. b1	-11	-10.389	...	11

Test settings	
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block PLimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-11	-10.389	...	11
Controller parameters				
b1	-11	-10.389	...	11
Exp. b1	-11	-10.389	...	11

Test settings	
Tolerance b1	±1,0000e-06

Test statistics	
Min CPU cycles	667
Max CPU cycles	757
Avg CPU cycles	695

Verification: PLimit Float32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for Control block PLimit.

Test results				
Time step	1	2	...	201
CPU cycles	30	30	...	170
Inputs				
In (DSP)	0	0	...	0
max (DSP)	0.8	0.8	...	0.8
min (DSP)	0.15	0.15	...	0.15
Enable (DSP)	0	0	...	1
In	0	0	...	0
max	0.8	0.8	...	0.8
min	0.15	0.15	...	0.15
Enable	0	0	...	1
Parameters				
Kp	2			
Outputs				
Out	0	0	...	0.15
Exp. Out	0	0	...	0.15
Out (DSP)	0	0	...	0.15
Exp. Out (DSP)	0	0	...	0.15

Test settings	
Tolerance Out	±9,3132e-09 (±20 LSB)

Test statistics	
Min CPU cycles	30
Max CPU cycles	190
Avg CPU cycles	181

Test case: Conversion test OK

Conversion test for Control block PLimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-11	-10.389	...	11
Controller parameters				
b1	-11	-10.389	...	11
Exp. b1	-11	-10.389	...	11

Test settings	
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block PLimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-11	-10.389	...	11
Controller parameters				
b1	-11	-10.389	...	11
Exp. b1	-11	-10.389	...	11

Test settings	
Tolerance b1	±1,0000e-06

Test statistics	
Min CPU cycles	277
Max CPU cycles	278
Avg CPU cycles	277

Verification: PLimit Float32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for Control block PLimit.

Test results				
Time step	1	2	...	201
CPU cycles	73	59	...	81
Inputs				
In (DSP)	0	0	...	0
max (DSP)	0.8	0.8	...	0.8
min (DSP)	0.15	0.15	...	0.15
Enable (DSP)	0	0	...	1
In	0	0	...	0
max	0.8	0.8	...	0.8
min	0.15	0.15	...	0.15
Enable	0	0	...	1
Parameters				
Kp	2			
Outputs				
Out	0	0	...	0.15
Exp. Out	0	0	...	0.15
Out (DSP)	0	0	...	0.15
Exp. Out (DSP)	0	0	...	0.15

Test settings	
Tolerance Out	±9,3132e-09 (±20 LSB)

Test statistics	
Min CPU cycles	59
Max CPU cycles	81
Avg CPU cycles	80

Test case: Conversion test OK

Conversion test for Control block PLimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-11	-10.389	...	11
Controller parameters				
b1	-11	-10.389	...	11
Exp. b1	-11	-10.389	...	11

Test settings	
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block PLimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-11	-10.389	...	11
Controller parameters				
b1	-11	-10.389	...	11
Exp. b1	-11	-10.389	...	11

Test settings	
Tolerance b1	±1,0000e-06

Test statistics	
Min CPU cycles	384
Max CPU cycles	416
Avg CPU cycles	385

Verification: PLimit Float32 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test

OK

Inport test for Control block PLimit.

Test results				
Time step	1	2	...	201
CPU cycles	62	62	...	78
Inputs				
In (DSP)	0	0	...	0
max (DSP)	0.8	0.8	...	0.8
min (DSP)	0.15	0.15	...	0.15
Enable (DSP)	0	0	...	1
In	0	0	...	0
max	0.8	0.8	...	0.8
min	0.15	0.15	...	0.15
Enable	0	0	...	1
Parameters				
Kp	2			
Outputs				
Out	0	0	...	0.15
Exp. Out	0	0	...	0.15
Out (DSP)	0	0	...	0.15
Exp. Out (DSP)	0	0	...	0.15

Test settings	
Tolerance Out	±9,3132e-09 (±20 LSB)

Test statistics	
Min CPU cycles	62
Max CPU cycles	78
Avg CPU cycles	77

Test case: Conversion test

OK

Conversion test for Control block PLimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-11	-10.389	...	11
Controller parameters				
b1	-11	-10.389	...	11
Exp. b1	-11	-10.389	...	11

Test settings	
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block PLimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-11	-10.389	...	11
Controller parameters				
b1	-11	-10.389	...	11
Exp. b1	-11	-10.389	...	11

Test settings	
Tolerance b1	±1,0000e-06

Test statistics	
Min CPU cycles	653
Max CPU cycles	664
Avg CPU cycles	653

Verification: PLimit Float32 CPU dsPIC33EP256MC502

Date of Test	2026-06-23
Target controller	dsPIC33EP256MC502

Test case: Inport test

OK

Inport test for Control block PLimit.

Test results				
Time step	1	2	...	201
CPU cycles	55	55	...	386
Inputs				
In (DSP)	0	0	...	0
max (DSP)	0.8	0.8	...	0.8
min (DSP)	0.15	0.15	...	0.15
Enable (DSP)	0	0	...	1
In	0	0	...	0
max	0.8	0.8	...	0.8
min	0.15	0.15	...	0.15
Enable	0	0	...	1
Parameters				
Kp	2			
Outputs				
Out	0	0	...	0.15
Exp. Out	0	0	...	0.15
Out (DSP)	0	0	...	0.15
Exp. Out (DSP)	0	0	...	0.15

Test settings	
Tolerance Out	±9,3132e-09 (±20 LSB)

Test statistics	
Min CPU cycles	55
Max CPU cycles	428
Avg CPU cycles	409

Test case: Conversion test

OK

Conversion test for Control block PLimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-11	-10.389	...	11
Controller parameters				
b1	-11	-10.389	...	11
Exp. b1	-11	-10.389	...	11

Test settings	
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

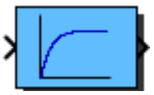
Conversion-on-Target test for Control block PLimit.

Test results				
Time step	1	2	...	37
Mask parameters				
Kp	-11	-10.389	...	11
Controller parameters				
b1	-11	-10.389	...	11
Exp. b1	-11	-10.389	...	11

Test settings	
Tolerance b1	±1,0000e-06

Test statistics	
Min CPU cycles	515
Max CPU cycles	860
Avg CPU cycles	848

Block: PT1



First order low pass:
G(s) = V/(s/w + 1)

Inports	
In	Input In(k)

Outports	
Out	Output Out(k)

Mask Parameters		
Name	**ID**	**Description**
V	1	Gain
fc	2	Cut off frequency of low pass filter
ts_fact	3	Multiplication factor of base sampling time (in integer format)
method	4	Discretization method

Description:

Due to limited value range in the 8 bit fixed point implementation rather high deviations from expected output values may occur.

Developer note: The source code of block *TF1* is used.

Implementations:

FiP8 8 Bit Fixed Point Implementation
FiP16 16 Bit Fixed Point Implementation
FiP32 32 Bit Fixed Point Implementation
Float32 32 Bit Floating Point Implementation
Float64 64 Bit Floating Point Implementation

Implementation: FiP8

8 Bit Fixed Point Implementation

Inports Data Type	
In	int8

Outports Data Type	
Out	int8

Implementation: FiP16

16 Bit Fixed Point Implementation

Inports Data Type	
In	int16

Outports Data Type	
Out	int16

Implementation: FiP32

32 Bit Fixed Point Implementation

Inports Data Type	
In	int32

Outports Data Type	
Out	int32

Implementation: Float32

32 Bit Floating Point Implementation

Inports Data Type	
In	float32

Outports Data Type	
Out	float32

Implementation: Float64

64 Bit Floating Point Implementation

Inports Data Type	
In	float64

Outports Data Type	
Out	float64

Verification: PT1 FiP16 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for Control block PT1.

Test results						
Time step	1	2	3	4	...	105
CPU cycles	88	88	88	88	...	88
Inputs						
In (DSP)	0	0	0	0	...	-9830
In	0	0	0	0	...	-0.3
Parameters						
V	1.1					
fc	230					
ts_fact	1					
method	zoh					
Outputs						
Out	0	0	0	0	...	-0.329
Exp. Out	0	0	0	0	...	-0.329
Out (DSP)	0	0	0	0	...	-10776
Exp. Out (DSP)	0	0	0	0	...	-10780

Test settings	
Tolerance Out	±1,5259e-04 (±5 LSB)

Test statistics	
Min CPU cycles	88
Max CPU cycles	88
Avg CPU cycles	88

Verification: PT1 FiP16 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for Control block PT1.

Test results						
Time step	1	2	3	4	...	105
CPU cycles	69	69	69	69	...	69
Inputs						
In (DSP)	0	0	0	0	...	-9830
In	0	0	0	0	...	-0.3
Parameters						
V	1.1					
fc	230					
ts_fact	1					
method	zoh					
Outputs						
Out	0	0	0	0	...	-0.329
Exp. Out	0	0	0	0	...	-0.329
Out (DSP)	0	0	0	0	...	-10776
Exp. Out (DSP)	0	0	0	0	...	-10780

Test settings	
Tolerance Out	±1,5259e-04 (±5 LSB)

Test statistics	
Min CPU cycles	69
Max CPU cycles	69
Avg CPU cycles	69

Verification: PT1 FiP16 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for Control block PT1.

Test results						
Time step	1	2	3	4	...	105
CPU cycles	104	104	104	104	...	104
Inputs						
In (DSP)	0	0	0	0	...	-9830
In	0	0	0	0	...	-0.3
Parameters						
V	1.1					
fc	230					
ts_fact	1					
method	zoh					
Outputs						
Out	0	0	0	0	...	-0.329
Exp. Out	0	0	0	0	...	-0.329
Out (DSP)	0	0	0	0	...	-10776
Exp. Out (DSP)	0	0	0	0	...	-10780

Test settings	
Tolerance Out	±1,5259e-04 (±5 LSB)

Test statistics	
Min CPU cycles	104
Max CPU cycles	104
Avg CPU cycles	104

Verification: PT1 FiP16 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for Control block PT1.

Test results						
Time step	1	2	3	4	...	105
CPU cycles	96	96	96	96	...	96
Inputs						
In (DSP)	0	0	0	0	...	-9830
In	0	0	0	0	...	-0.3
Parameters						
V	1.1					
fc	230					
ts_fact	1					
method	zoh					
Outputs						
Out	0	0	0	0	...	-0.329
Exp. Out	0	0	0	0	...	-0.329
Out (DSP)	0	0	0	0	...	-10776
Exp. Out (DSP)	0	0	0	0	...	-10780

Test settings	
Tolerance Out	±1,5259e-04 (±5 LSB)

Test statistics	
Min CPU cycles	96
Max CPU cycles	96
Avg CPU cycles	96

Verification: PT1 FiP16 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for Control block PT1.

Test results						
Time step	1	2	3	4	...	105
CPU cycles	59	59	59	59	...	59
Inputs						
In (DSP)	0	0	0	0	...	-9830
In	0	0	0	0	...	-0.3
Parameters						
V	1.1					
fc	230					
ts_fact	1					
method	zoh					
Outputs						
Out	0	0	0	0	...	-0.329
Exp. Out	0	0	0	0	...	-0.329
Out (DSP)	0	0	0	0	...	-10776
Exp. Out (DSP)	0	0	0	0	...	-10780

Test settings	
Tolerance Out	±1,5259e-04 (±5 LSB)

Test statistics	
Min CPU cycles	59
Max CPU cycles	59
Avg CPU cycles	59

Verification: PT1 FiP16 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for Control block PT1.

Test results						
Time step	1	2	3	4	...	105
CPU cycles	118	96	96	96	...	96
Inputs						
In (DSP)	0	0	0	0	...	-9830
In	0	0	0	0	...	-0.3
Parameters						
V	1.1					
fc	230					
ts_fact	1					
method	zoh					
Outputs						
Out	0	0	0	0	...	-0.329
Exp. Out	0	0	0	0	...	-0.329
Out (DSP)	0	0	0	0	...	-10776
Exp. Out (DSP)	0	0	0	0	...	-10780

Test settings	
Tolerance Out	±1,5259e-04 (±5 LSB)

Test statistics	
Min CPU cycles	96
Max CPU cycles	118
Avg CPU cycles	96

Verification: PT1 FiP16 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for Control block PT1.

Test results						
Time step	1	2	3	4	...	105
CPU cycles	85	85	85	85	...	85
Inputs						
In (DSP)	0	0	0	0	...	-9830
In	0	0	0	0	...	-0.3
Parameters						
V	1.1					
fc	230					
ts_fact	1					
method	zoh					
Outputs						
Out	0	0	0	0	...	-0.329
Exp. Out	0	0	0	0	...	-0.329
Out (DSP)	0	0	0	0	...	-10776
Exp. Out (DSP)	0	0	0	0	...	-10780

Test settings	
Tolerance Out	±1,5259e-04 (±5 LSB)

Test statistics	
Min CPU cycles	85
Max CPU cycles	85
Avg CPU cycles	85

Verification: PT1 FiP16 CPU dsPIC33EP256MC502

Date of Test	2026-06-23
Target controller	dsPIC33EP256MC502

Test case: Inport test — OK

Inport test for Control block PT1.

Test results						
Time step	1	2	3	4	...	105
CPU cycles	91	91	91	91	...	91
Inputs						
In (DSP)	0	0	0	0	...	-9830
In	0	0	0	0	...	-0.3
Parameters						
V	1.1					
fc	230					
ts_fact	1					
method	zoh					
Outputs						
Out	0	0	0	0	...	-0.329
Exp. Out	0	0	0	0	...	-0.329
Out (DSP)	0	0	0	0	...	-10776
Exp. Out (DSP)	0	0	0	0	...	-10780

Test settings	
Tolerance Out	±1,5259e-04 (±5 LSB)

Test statistics	
Min CPU cycles	91
Max CPU cycles	91
Avg CPU cycles	91

Verification: PT1 FiP32 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for Control block PT1.

Test results				
Time step	1	2	...	105
CPU cycles	221	221	...	221
Inputs				
In (DSP)	0	0	...	-644245094
In	0	0	...	-0.3
Parameters				
V	1.1			
fc	230			
ts_fact	1			
method	zoh			
Outputs				
Out	0	0	...	-0.329
Exp. Out	0	0	...	-0.329
Out (DSP)	0	0	...	-706485960
Exp. Out (DSP)	0	0	...	-706485964

Test settings	
Tolerance Out	±2,3283e-09 (±5 LSB)

Test statistics	
Min CPU cycles	221
Max CPU cycles	221
Avg CPU cycles	221

Verification: PT1 FiP32 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for Control block PT1.

Test results				
Time step	1	2	...	105
CPU cycles	121	121	...	121
Inputs				
In (DSP)	0	0	...	-644245094
In	0	0	...	-0.3
Parameters				
V	1.1			
fc	230			
ts_fact	1			
method	zoh			
Outputs				
Out	0	0	...	-0.329
Exp. Out	0	0	...	-0.329
Out (DSP)	0	0	...	-706485960
Exp. Out (DSP)	0	0	...	-706485964

Test settings	
Tolerance Out	±2,3283e-09 (±5 LSB)

Test statistics	
Min CPU cycles	121
Max CPU cycles	121
Avg CPU cycles	121

Verification: PT1 FiP32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for Control block PT1.

Test results				
Time step	1	2	...	105
CPU cycles	142	142	...	142
Inputs				
In (DSP)	0	0	...	-644245094
In	0	0	...	-0.3
Parameters				
V	1.1			
fc	230			
ts_fact	1			
method	zoh			
Outputs				
Out	0	0	...	-0.329
Exp. Out	0	0	...	-0.329
Out (DSP)	0	0	...	-706485960
Exp. Out (DSP)	0	0	...	-706485964

Test settings	
Tolerance Out	±2,3283e-09 (±5 LSB)

Test statistics	
Min CPU cycles	142
Max CPU cycles	142
Avg CPU cycles	142

Verification: PT1 FiP32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for Control block PT1.

Test results				
Time step	1	2	...	105
CPU cycles	373	373	...	380
Inputs				
In (DSP)	0	0	...	-644245094
In	0	0	...	-0.3
Parameters				
V	1.1			
fc	230			
ts_fact	1			
method	zoh			
Outputs				
Out	0	0	...	-0.329
Exp. Out	0	0	...	-0.329
Out (DSP)	0	0	...	-706485960
Exp. Out (DSP)	0	0	...	-706485964

Test settings	
Tolerance Out	±2,3283e-09 (±5 LSB)

Test statistics	
Min CPU cycles	373
Max CPU cycles	380
Avg CPU cycles	375

Verification: PT1 FiP32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for Control block PT1.

Test results				
Time step	1	2	...	105
CPU cycles	87	87	...	89
Inputs				
In (DSP)	0	0	...	-644245094
In	0	0	...	-0.3
Parameters				
V	1.1			
fc	230			
ts_fact	1			
method	zoh			
Outputs				
Out	0	0	...	-0.329
Exp. Out	0	0	...	-0.329
Out (DSP)	0	0	...	-706485960
Exp. Out (DSP)	0	0	...	-706485964

Test settings	
Tolerance Out	±2,3283e-09 (±5 LSB)

Test statistics	
Min CPU cycles	87
Max CPU cycles	89
Avg CPU cycles	88

Verification: PT1 FiP32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for Control block PT1.

Test results				
Time step	1	2	...	105
CPU cycles	154	133	...	133
Inputs				
In (DSP)	0	0	...	-644245094
In	0	0	...	-0.3
Parameters				
V	1.1			
fc	230			
ts_fact	1			
method	zoh			
Outputs				
Out	0	0	...	-0.329
Exp. Out	0	0	...	-0.329
Out (DSP)	0	0	...	-706485960
Exp. Out (DSP)	0	0	...	-706485964

Test settings	
Tolerance Out	±2,3283e-09 (±5 LSB)

Test statistics	
Min CPU cycles	133
Max CPU cycles	154
Avg CPU cycles	133

Verification: PT1 FiP32 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for Control block PT1.

Test results				
Time step	1	2	...	105
CPU cycles	188	188	...	188
Inputs				
In (DSP)	0	0	...	-644245094
In	0	0	...	-0.3
Parameters				
V	1.1			
fc	230			
ts_fact	1			
method	zoh			
Outputs				
Out	0	0	...	-0.329
Exp. Out	0	0	...	-0.329
Out (DSP)	0	0	...	-706485960
Exp. Out (DSP)	0	0	...	-706485964

Test settings	
Tolerance Out	±2,3283e-09 (±5 LSB)

Test statistics	
Min CPU cycles	188
Max CPU cycles	188
Avg CPU cycles	188

Verification: PT1 FiP32 CPU dsPIC33EP256MC502

Date of Test	2026-06-23
Target controller	dsPIC33EP256MC502

Test case: Inport test — OK

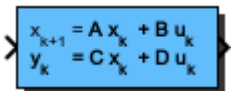
Inport test for Control block PT1.

Test results				
Time step	1	2	...	105
CPU cycles	1038	1038	...	1053
Inputs				
In (DSP)	0	0	...	-644245094
In	0	0	...	-0.3
Parameters				
V	1.1			
fc	230			
ts_fact	1			
method	zoh			
Outputs				
Out	0	0	...	-0.329
Exp. Out	0	0	...	-0.329
Out (DSP)	0	0	...	-706485960
Exp. Out (DSP)	0	0	...	-706485964

Test settings	
Tolerance Out	±2,3283e-09 (±5 LSB)

Test statistics	
Min CPU cycles	1038
Max CPU cycles	1053
Avg CPU cycles	1044

Block: TDSystemO1



1st order time discrete system with one input and one output.

Inports	
In	Input #1

Outports	
Out	Output #1

Mask Parameters		
Name	**ID**	**Description**
A	1	State matrix A
B	2	Input matrix B
C	3	Output matrix C
D	4	Feedthrough matrix D

Description:

Calculation:

$$x_{1,k+1} = a_{1,1}x_{1,k} + b_{1,1}u_{1,k}$$
$$y_{1,k} = c_{1,1}x_{1,k} + d_{1,1}u_{1,k}$$

or short

$$\mathbf{x}_{k+1} = \mathbf{A}\mathbf{x}_k + \mathbf{B}\mathbf{u}_k$$
$$\mathbf{y}_k = \mathbf{C}\mathbf{x}_k + \mathbf{D}\mathbf{u}_k$$

Implementations:

FiP8	8 Bit Fixed Point Implementation
FiP16	16 Bit Fixed Point Implementation
FiP32	32 Bit Fixed Point Implementation
Float32	32 Bit Floating Point Implementation
Float64	64 Bit Floating Point Implementation

Implementation: FiP8

8 Bit Fixed Point Implementation

Inports Data Type	
In	int8

Outports Data Type	
Out	int8

Implementation: FiP16

16 Bit Fixed Point Implementation

Inports Data Type	
In	int16

Outports Data Type	
Out	int16

Implementation: FiP32

32 Bit Fixed Point Implementation

Inports Data Type	
In	int32

Outports Data Type	
Out	int32

Implementation: Float32

32 Bit Floating Point Implementation

Inports Data Type	
In	float32

Outports Data Type	
Out	float32

Implementation: Float64

64 Bit Floating Point Implementation

Inports Data Type	
In	float64

Outports Data Type	
Out	float64

Verification: TDSystemO1 FiP16 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for Control block TDSystemO1.

Test results						
Time step	1	2	3	4	...	174
CPU cycles	120	120	120	120	...	120
Inputs						
In (DSP)	0	-3271	-6510	-9684	...	-19661
In	-0	-0.1	-0.199	-0.296	...	-0.6
Parameters						
A	0.7					
B	0.38					
C	0.33					
D	0.1					
Outputs						
Out	0	-0.01	-0.032	-0.063	...	-0.311
Exp. Out	-0	-0.01	-0.032	-0.063	...	-0.311
Out (DSP)	0	-328	-1063	-2073	...	-10187
Exp. Out (DSP)	0	-327	-1061	-2072	...	-10184

Test settings	
Tolerance Out	±1,2207e-04 (±4 LSB)

Test statistics	
Min CPU cycles	116
Max CPU cycles	120
Avg CPU cycles	119

Test case: Conversion test OK

Conversion test for Control block TDSystemO1.

Test results						
Time step	1	2	3	4	5	6
Mask parameters						
A	0	0.1	1	10	-1	-0.1
B	0	0.1	1	10	-1	-0.1
C	0	0.1	1	10	-1	-0.1
D	0	0.1	1	10	-1	-0.1
Controller parameters						
a11	0	3277	16384	20480	-16384	-3277
c11	0	3277	16384	20480	-16384	-3277
b11	0	3277	16384	20480	-16384	-3277
d11	0	3277	16384	20480	-16384	-3277
sfrd11	15	15	14	11	14	15
sfrc11	15	15	14	11	14	15
sfrb11	15	15	14	11	14	15
sfra11	15	15	14	11	14	15
Exp. a11	0	3277	16384	20480	-16384	-3277
Exp. c11	0	3277	16384	20480	-16384	-3277
Exp. b11	0	3277	16384	20480	-16384	-3277
Exp. d11	0	3277	16384	20480	-16384	-3277
Exp. sfrd11	15	15	14	11	14	15
Exp. sfrc11	15	15	14	11	14	15
Exp. sfrb11	15	15	14	11	14	15
Exp. sfra11	15	15	14	11	14	15

Test settings	
Tolerance a11	±0,0000e+00
Tolerance c11	±0,0000e+00
Tolerance b11	±0,0000e+00
Tolerance d11	±0,0000e+00
Tolerance sfrd11	±0,0000e+00
Tolerance sfrc11	±0,0000e+00
Tolerance sfrb11	±0,0000e+00
Tolerance sfra11	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block TDSystemO1.

Test results						
Time step	1	2	3	4	5	6
Mask parameters						
A	0	0.1	1	10	-1	-0.1
B	0	0.1	1	10	-1	-0.1
C	0	0.1	1	10	-1	-0.1
D	0	0.1	1	10	-1	-0.1
Controller parameters						
a11	0	3276	16384	20480	-16384	-3276
c11	0	3276	16384	20480	-16384	-3276
b11	0	3276	16384	20480	-16384	-3276
d11	0	3276	16384	20480	-16384	-3276
sfrd11	15	15	14	11	14	15
sfrc11	15	15	14	11	14	15
sfrb11	15	15	14	11	14	15
sfra11	15	15	14	11	14	15
Exp. a11	0	3277	16384	20480	-16384	-3277
Exp. c11	0	3277	16384	20480	-16384	-3277
Exp. b11	0	3277	16384	20480	-16384	-3277
Exp. d11	0	3277	16384	20480	-16384	-3277
Exp. sfrd11	15	15	14	11	14	15
Exp. sfrc11	15	15	14	11	14	15
Exp. sfrb11	15	15	14	11	14	15
Exp. sfra11	15	15	14	11	14	15

Test settings	
Tolerance a11	±1,0000e+00
Tolerance c11	±1,0000e+00
Tolerance b11	±1,0000e+00
Tolerance d11	±1,0000e+00
Tolerance sfrd11	±0,0000e+00
Tolerance sfrc11	±0,0000e+00
Tolerance sfrb11	±0,0000e+00
Tolerance sfra11	±0,0000e+00

Test statistics	
Min CPU cycles	4250
Max CPU cycles	12850
Avg CPU cycles	6619

Verification: TDSystemO1 FiP16 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for Control block TDSystemO1.

Test results						
Time step	1	2	3	4	...	174
CPU cycles	85	85	85	85	...	85
Inputs						
In (DSP)	0	-3271	-6510	-9684	...	-19661
In	-0	-0.1	-0.199	-0.296	...	-0.6
Parameters						
A	0.7					
B	0.38					
C	0.33					
D	0.1					
Outputs						
Out	0	-0.01	-0.032	-0.063	...	-0.311
Exp. Out	-0	-0.01	-0.032	-0.063	...	-0.311
Out (DSP)	0	-328	-1063	-2073	...	-10187
Exp. Out (DSP)	0	-327	-1061	-2072	...	-10184

Test settings	
Tolerance Out	±1,2207e-04 (±4 LSB)

Test statistics	
Min CPU cycles	81
Max CPU cycles	87
Avg CPU cycles	84

Test case: Conversion test OK

Conversion test for Control block TDSystemO1.

Test results						
Time step	1	2	3	4	5	6
Mask parameters						
A	0	0.1	1	10	-1	-0.1
B	0	0.1	1	10	-1	-0.1
C	0	0.1	1	10	-1	-0.1
D	0	0.1	1	10	-1	-0.1
Controller parameters						
a11	0	3277	16384	20480	-16384	-3277
c11	0	3277	16384	20480	-16384	-3277
b11	0	3277	16384	20480	-16384	-3277
d11	0	3277	16384	20480	-16384	-3277
sfrd11	15	15	14	11	14	15
sfrc11	15	15	14	11	14	15
sfrb11	15	15	14	11	14	15
sfra11	15	15	14	11	14	15
Exp. a11	0	3277	16384	20480	-16384	-3277
Exp. c11	0	3277	16384	20480	-16384	-3277
Exp. b11	0	3277	16384	20480	-16384	-3277
Exp. d11	0	3277	16384	20480	-16384	-3277
Exp. sfrd11	15	15	14	11	14	15
Exp. sfrc11	15	15	14	11	14	15
Exp. sfrb11	15	15	14	11	14	15
Exp. sfra11	15	15	14	11	14	15

Test settings	
Tolerance a11	±0,0000e+00
Tolerance c11	±0,0000e+00
Tolerance b11	±0,0000e+00
Tolerance d11	±0,0000e+00
Tolerance sfrd11	±0,0000e+00
Tolerance sfrc11	±0,0000e+00
Tolerance sfrb11	±0,0000e+00
Tolerance sfra11	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block TDSystemO1.

Test results						
Time step	1	2	3	4	5	6
Mask parameters						
A	0	0.1	1	10	-1	-0.1
B	0	0.1	1	10	-1	-0.1
C	0	0.1	1	10	-1	-0.1
D	0	0.1	1	10	-1	-0.1
Controller parameters						
a11	0	3276	16384	20480	-16384	-3276
c11	0	3276	16384	20480	-16384	-3276
b11	0	3276	16384	20480	-16384	-3276
d11	0	3276	16384	20480	-16384	-3276
sfrd11	15	15	14	11	14	15
sfrc11	15	15	14	11	14	15
sfrb11	15	15	14	11	14	15
sfra11	15	15	14	11	14	15
Exp. a11	0	3277	16384	20480	-16384	-3277
Exp. c11	0	3277	16384	20480	-16384	-3277
Exp. b11	0	3277	16384	20480	-16384	-3277
Exp. d11	0	3277	16384	20480	-16384	-3277
Exp. sfrd11	15	15	14	11	14	15
Exp. sfrc11	15	15	14	11	14	15
Exp. sfrb11	15	15	14	11	14	15
Exp. sfra11	15	15	14	11	14	15

Test settings	
Tolerance a11	±1,0000e+00
Tolerance c11	±1,0000e+00
Tolerance b11	±1,0000e+00
Tolerance d11	±1,0000e+00
Tolerance sfrd11	±0,0000e+00
Tolerance sfrc11	±0,0000e+00
Tolerance sfrb11	±0,0000e+00
Tolerance sfra11	±0,0000e+00

Test statistics	
Min CPU cycles	2179
Max CPU cycles	7187
Avg CPU cycles	3581

Verification: TDSystemO1 FiP16 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for Control block TDSystemO1.

Test results						
Time step	1	2	3	4	...	174
CPU cycles	120	120	120	120	...	120
Inputs						
In (DSP)	0	-3271	-6510	-9684	...	-19661
In	-0	-0.1	-0.199	-0.296	...	-0.6
Parameters						
A	0.7					
B	0.38					
C	0.33					
D	0.1					
Outputs						
Out	0	-0.01	-0.032	-0.063	...	-0.311
Exp. Out	-0	-0.01	-0.032	-0.063	...	-0.311
Out (DSP)	0	-328	-1063	-2073	...	-10187
Exp. Out (DSP)	0	-327	-1061	-2072	...	-10184

Test settings	
Tolerance Out	±1,2207e-04 (±4 LSB)

Test statistics	
Min CPU cycles	120
Max CPU cycles	120
Avg CPU cycles	120

Test case: Conversion test OK

Conversion test for Control block TDSystemO1.

Test results						
Time step	1	2	3	4	5	6
Mask parameters						
A	0	0.1	1	10	-1	-0.1
B	0	0.1	1	10	-1	-0.1
C	0	0.1	1	10	-1	-0.1
D	0	0.1	1	10	-1	-0.1
Controller parameters						
a11	0	3277	16384	20480	-16384	-3277
c11	0	3277	16384	20480	-16384	-3277
b11	0	3277	16384	20480	-16384	-3277
d11	0	3277	16384	20480	-16384	-3277
sfrd11	15	15	14	11	14	15
sfrc11	15	15	14	11	14	15
sfrb11	15	15	14	11	14	15
sfra11	15	15	14	11	14	15
Exp. a11	0	3277	16384	20480	-16384	-3277
Exp. c11	0	3277	16384	20480	-16384	-3277
Exp. b11	0	3277	16384	20480	-16384	-3277
Exp. d11	0	3277	16384	20480	-16384	-3277
Exp. sfrd11	15	15	14	11	14	15
Exp. sfrc11	15	15	14	11	14	15
Exp. sfrb11	15	15	14	11	14	15
Exp. sfra11	15	15	14	11	14	15

Test settings	
Tolerance a11	±0,0000e+00
Tolerance c11	±0,0000e+00
Tolerance b11	±0,0000e+00
Tolerance d11	±0,0000e+00
Tolerance sfrd11	±0,0000e+00
Tolerance sfrc11	±0,0000e+00
Tolerance sfrb11	±0,0000e+00
Tolerance sfra11	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block TDSystemO1.

Test results						
Time step	1	2	3	4	5	6
Mask parameters						
A	0	0.1	1	10	-1	-0.1
B	0	0.1	1	10	-1	-0.1
C	0	0.1	1	10	-1	-0.1
D	0	0.1	1	10	-1	-0.1
Controller parameters						
a11	0	3276	16384	20480	-16384	-3276
c11	0	3276	16384	20480	-16384	-3276
b11	0	3276	16384	20480	-16384	-3276
d11	0	3276	16384	20480	-16384	-3276
sfrd11	15	15	14	11	14	15
sfrc11	15	15	14	11	14	15
sfrb11	15	15	14	11	14	15
sfra11	15	15	14	11	14	15
Exp. a11	0	3277	16384	20480	-16384	-3277
Exp. c11	0	3277	16384	20480	-16384	-3277
Exp. b11	0	3277	16384	20480	-16384	-3277
Exp. d11	0	3277	16384	20480	-16384	-3277
Exp. sfrd11	15	15	14	11	14	15
Exp. sfrc11	15	15	14	11	14	15
Exp. sfrb11	15	15	14	11	14	15
Exp. sfra11	15	15	14	11	14	15

Test settings	
Tolerance a11	±1,0000e+00
Tolerance c11	±1,0000e+00
Tolerance b11	±1,0000e+00
Tolerance d11	±1,0000e+00
Tolerance sfrd11	±0,0000e+00
Tolerance sfrc11	±0,0000e+00
Tolerance sfrb11	±0,0000e+00
Tolerance sfra11	±0,0000e+00

Test statistics	
Min CPU cycles	2027
Max CPU cycles	4070
Avg CPU cycles	2554

Verification: TDSystemO1 FiP16 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for Control block TDSystemO1.

Test results						
Time step	1	2	3	4	...	174
CPU cycles	121	121	121	121	...	121
Inputs						
In (DSP)	0	-3271	-6510	-9684	...	-19661
In	-0	-0.1	-0.199	-0.296	...	-0.6
Parameters						
A	0.7					
B	0.38					
C	0.33					
D	0.1					
Outputs						
Out	0	-0.01	-0.032	-0.063	...	-0.311
Exp. Out	-0	-0.01	-0.032	-0.063	...	-0.311
Out (DSP)	0	-328	-1063	-2073	...	-10187
Exp. Out (DSP)	0	-327	-1061	-2072	...	-10184

Test settings	
Tolerance Out	±1,2207e-04 (±4 LSB)

Test statistics	
Min CPU cycles	120
Max CPU cycles	122
Avg CPU cycles	120

Test case: Conversion test OK

Conversion test for Control block TDSystemO1.

Test results						
Time step	1	2	3	4	5	6
Mask parameters						
A	0	0.1	1	10	-1	-0.1
B	0	0.1	1	10	-1	-0.1
C	0	0.1	1	10	-1	-0.1
D	0	0.1	1	10	-1	-0.1
Controller parameters						
a11	0	3277	16384	20480	-16384	-3277
c11	0	3277	16384	20480	-16384	-3277
b11	0	3277	16384	20480	-16384	-3277
d11	0	3277	16384	20480	-16384	-3277
sfrd11	15	15	14	11	14	15
sfrc11	15	15	14	11	14	15
sfrb11	15	15	14	11	14	15
sfra11	15	15	14	11	14	15
Exp. a11	0	3277	16384	20480	-16384	-3277
Exp. c11	0	3277	16384	20480	-16384	-3277
Exp. b11	0	3277	16384	20480	-16384	-3277
Exp. d11	0	3277	16384	20480	-16384	-3277
Exp. sfrd11	15	15	14	11	14	15
Exp. sfrc11	15	15	14	11	14	15
Exp. sfrb11	15	15	14	11	14	15
Exp. sfra11	15	15	14	11	14	15

Test settings	
Tolerance a11	±0,0000e+00
Tolerance c11	±0,0000e+00
Tolerance b11	±0,0000e+00
Tolerance d11	±0,0000e+00
Tolerance sfrd11	±0,0000e+00
Tolerance sfrc11	±0,0000e+00
Tolerance sfrb11	±0,0000e+00
Tolerance sfra11	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block TDSystemO1.

Test results						
Time step	1	2	3	4	5	6
Mask parameters						
A	0	0.1	1	10	-1	-0.1
B	0	0.1	1	10	-1	-0.1
C	0	0.1	1	10	-1	-0.1
D	0	0.1	1	10	-1	-0.1
Controller parameters						
a11	0	3276	16384	20480	-16384	-3276
c11	0	3276	16384	20480	-16384	-3276
b11	0	3276	16384	20480	-16384	-3276
d11	0	3276	16384	20480	-16384	-3276
sfrd11	15	15	14	11	14	15
sfrc11	15	15	14	11	14	15
sfrb11	15	15	14	11	14	15
sfra11	15	15	14	11	14	15
Exp. a11	0	3277	16384	20480	-16384	-3277
Exp. c11	0	3277	16384	20480	-16384	-3277
Exp. b11	0	3277	16384	20480	-16384	-3277
Exp. d11	0	3277	16384	20480	-16384	-3277
Exp. sfrd11	15	15	14	11	14	15
Exp. sfrc11	15	15	14	11	14	15
Exp. sfrb11	15	15	14	11	14	15
Exp. sfra11	15	15	14	11	14	15

Test settings	
Tolerance a11	±1,0000e+00
Tolerance c11	±1,0000e+00
Tolerance b11	±1,0000e+00
Tolerance d11	±1,0000e+00
Tolerance sfrd11	±0,0000e+00
Tolerance sfrc11	±0,0000e+00
Tolerance sfrb11	±0,0000e+00
Tolerance sfra11	±0,0000e+00

Test statistics	
Min CPU cycles	5581
Max CPU cycles	17193
Avg CPU cycles	9328

Verification: TDSystemO1 FiP16 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for Control block TDSystemO1.

Test results						
Time step	1	2	3	4	...	174
CPU cycles	70	70	70	70	...	70
Inputs						
In (DSP)	0	-3271	-6510	-9684	...	-19661
In	-0	-0.1	-0.199	-0.296	...	-0.6
Parameters						
A	0.7					
B	0.38					
C	0.33					
D	0.1					
Outputs						
Out	0	-0.01	-0.032	-0.063	...	-0.311
Exp. Out	-0	-0.01	-0.032	-0.063	...	-0.311
Out (DSP)	0	-328	-1063	-2073	...	-10187
Exp. Out (DSP)	0	-327	-1061	-2072	...	-10184

Test settings	
Tolerance Out	±1,2207e-04 (±4 LSB)

Test statistics	
Min CPU cycles	70
Max CPU cycles	70
Avg CPU cycles	70

Test case: Conversion test OK

Conversion test for Control block TDSystemO1.

Test results						
Time step	1	2	3	4	5	6
Mask parameters						
A	0	0.1	1	10	-1	-0.1
B	0	0.1	1	10	-1	-0.1
C	0	0.1	1	10	-1	-0.1
D	0	0.1	1	10	-1	-0.1
Controller parameters						
a11	0	3277	16384	20480	-16384	-3277
c11	0	3277	16384	20480	-16384	-3277
b11	0	3277	16384	20480	-16384	-3277
d11	0	3277	16384	20480	-16384	-3277
sfrd11	15	15	14	11	14	15
sfrc11	15	15	14	11	14	15
sfrb11	15	15	14	11	14	15
sfra11	15	15	14	11	14	15
Exp. a11	0	3277	16384	20480	-16384	-3277
Exp. c11	0	3277	16384	20480	-16384	-3277
Exp. b11	0	3277	16384	20480	-16384	-3277
Exp. d11	0	3277	16384	20480	-16384	-3277
Exp. sfrd11	15	15	14	11	14	15
Exp. sfrc11	15	15	14	11	14	15
Exp. sfrb11	15	15	14	11	14	15
Exp. sfra11	15	15	14	11	14	15

Test settings	
Tolerance a11	±0,0000e+00
Tolerance c11	±0,0000e+00
Tolerance b11	±0,0000e+00
Tolerance d11	±0,0000e+00
Tolerance sfrd11	±0,0000e+00
Tolerance sfrc11	±0,0000e+00
Tolerance sfrb11	±0,0000e+00
Tolerance sfra11	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block TDSystemO1.

Test results						
Time step	1	2	3	4	5	6
Mask parameters						
A	0	0.1	1	10	-1	-0.1
B	0	0.1	1	10	-1	-0.1
C	0	0.1	1	10	-1	-0.1
D	0	0.1	1	10	-1	-0.1
Controller parameters						
a11	0	3276	16384	20480	-16384	-3276
c11	0	3276	16384	20480	-16384	-3276
b11	0	3276	16384	20480	-16384	-3276
d11	0	3276	16384	20480	-16384	-3276
sfrd11	15	15	14	11	14	15
sfrc11	15	15	14	11	14	15
sfrb11	15	15	14	11	14	15
sfra11	15	15	14	11	14	15
Exp. a11	0	3277	16384	20480	-16384	-3277
Exp. c11	0	3277	16384	20480	-16384	-3277
Exp. b11	0	3277	16384	20480	-16384	-3277
Exp. d11	0	3277	16384	20480	-16384	-3277
Exp. sfrd11	15	15	14	11	14	15
Exp. sfrc11	15	15	14	11	14	15
Exp. sfrb11	15	15	14	11	14	15
Exp. sfra11	15	15	14	11	14	15

Test settings	
Tolerance a11	±1,0000e+00
Tolerance c11	±1,0000e+00
Tolerance b11	±1,0000e+00
Tolerance d11	±1,0000e+00
Tolerance sfrd11	±0,0000e+00
Tolerance sfrc11	±0,0000e+00
Tolerance sfrb11	±0,0000e+00
Tolerance sfra11	±0,0000e+00

Test statistics	
Min CPU cycles	2632
Max CPU cycles	7292
Avg CPU cycles	4019

Verification: TDSystemO1 FiP16 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test

OK

Inport test for Control block TDSystemO1.

Test results						
Time step	1	2	3	4	...	174
CPU cycles	145	138	138	138	...	138
Inputs						
In (DSP)	0	-3271	-6510	-9684	...	-19661
In	-0	-0.1	-0.199	-0.296	...	-0.6
Parameters						
A	0.7					
B	0.38					
C	0.33					
D	0.1					
Outputs						
Out	0	-0.01	-0.032	-0.063	...	-0.311
Exp. Out	-0	-0.01	-0.032	-0.063	...	-0.311
Out (DSP)	0	-328	-1063	-2073	...	-10187
Exp. Out (DSP)	0	-327	-1061	-2072	...	-10184

Test settings	
Tolerance Out	±1,2207e-04 (±4 LSB)

Test statistics	
Min CPU cycles	138
Max CPU cycles	145
Avg CPU cycles	138

Test case: Conversion test

OK

Conversion test for Control block TDSystemO1.

Test results						
Time step	1	2	3	4	5	6
Mask parameters						
A	0	0.1	1	10	-1	-0.1
B	0	0.1	1	10	-1	-0.1
C	0	0.1	1	10	-1	-0.1
D	0	0.1	1	10	-1	-0.1
Controller parameters						
a11	0	3277	16384	20480	-16384	-3277
c11	0	3277	16384	20480	-16384	-3277
b11	0	3277	16384	20480	-16384	-3277
d11	0	3277	16384	20480	-16384	-3277
sfrd11	15	15	14	11	14	15
sfrc11	15	15	14	11	14	15
sfrb11	15	15	14	11	14	15
sfra11	15	15	14	11	14	15
Exp. a11	0	3277	16384	20480	-16384	-3277
Exp. c11	0	3277	16384	20480	-16384	-3277
Exp. b11	0	3277	16384	20480	-16384	-3277
Exp. d11	0	3277	16384	20480	-16384	-3277
Exp. sfrd11	15	15	14	11	14	15
Exp. sfrc11	15	15	14	11	14	15
Exp. sfrb11	15	15	14	11	14	15
Exp. sfra11	15	15	14	11	14	15

Test settings	
Tolerance a11	±0,0000e+00
Tolerance c11	±0,0000e+00
Tolerance b11	±0,0000e+00
Tolerance d11	±0,0000e+00
Tolerance sfrd11	±0,0000e+00
Tolerance sfrc11	±0,0000e+00
Tolerance sfrb11	±0,0000e+00
Tolerance sfra11	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block TDSystemO1.

Test results						
Time step	1	2	3	4	5	6
Mask parameters						
A	0	0.1	1	10	-1	-0.1
B	0	0.1	1	10	-1	-0.1
C	0	0.1	1	10	-1	-0.1
D	0	0.1	1	10	-1	-0.1
Controller parameters						
a11	0	3276	16384	20480	-16384	-3276
c11	0	3276	16384	20480	-16384	-3276
b11	0	3276	16384	20480	-16384	-3276
d11	0	3276	16384	20480	-16384	-3276
sfrd11	15	15	14	11	14	15
sfrc11	15	15	14	11	14	15
sfrb11	15	15	14	11	14	15
sfra11	15	15	14	11	14	15
Exp. a11	0	3277	16384	20480	-16384	-3277
Exp. c11	0	3277	16384	20480	-16384	-3277
Exp. b11	0	3277	16384	20480	-16384	-3277
Exp. d11	0	3277	16384	20480	-16384	-3277
Exp. sfrd11	15	15	14	11	14	15
Exp. sfrc11	15	15	14	11	14	15
Exp. sfrb11	15	15	14	11	14	15
Exp. sfra11	15	15	14	11	14	15

Test settings	
Tolerance a11	±1,0000e+00
Tolerance c11	±1,0000e+00
Tolerance b11	±1,0000e+00
Tolerance d11	±1,0000e+00
Tolerance sfrd11	±0,0000e+00
Tolerance sfrc11	±0,0000e+00
Tolerance sfrb11	±0,0000e+00
Tolerance sfra11	±0,0000e+00

Test statistics	
Min CPU cycles	1698
Max CPU cycles	3646
Avg CPU cycles	2247

Verification: TDSystemO1 FiP16 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for Control block TDSystemO1.

Test results						
Time step	1	2	3	4	...	174
CPU cycles	118	118	118	118	...	118
Inputs						
In (DSP)	0	-3271	-6510	-9684	...	-19661
In	-0	-0.1	-0.199	-0.296	...	-0.6
Parameters						
A	0.7					
B	0.38					
C	0.33					
D	0.1					
Outputs						
Out	0	-0.01	-0.032	-0.063	...	-0.311
Exp. Out	-0	-0.01	-0.032	-0.063	...	-0.311
Out (DSP)	0	-328	-1063	-2073	...	-10187
Exp. Out (DSP)	0	-327	-1061	-2072	...	-10184

Test settings	
Tolerance Out	±1,2207e-04 (±4 LSB)

Test statistics	
Min CPU cycles	117
Max CPU cycles	118
Avg CPU cycles	117

Test case: Conversion test OK

Conversion test for Control block TDSystemO1.

Test results						
Time step	1	2	3	4	5	6
Mask parameters						
A	0	0.1	1	10	-1	-0.1
B	0	0.1	1	10	-1	-0.1
C	0	0.1	1	10	-1	-0.1
D	0	0.1	1	10	-1	-0.1
Controller parameters						
a11	0	3277	16384	20480	-16384	-3277
c11	0	3277	16384	20480	-16384	-3277
b11	0	3277	16384	20480	-16384	-3277
d11	0	3277	16384	20480	-16384	-3277
sfrd11	15	15	14	11	14	15
sfrc11	15	15	14	11	14	15
sfrb11	15	15	14	11	14	15
sfra11	15	15	14	11	14	15
Exp. a11	0	3277	16384	20480	-16384	-3277
Exp. c11	0	3277	16384	20480	-16384	-3277
Exp. b11	0	3277	16384	20480	-16384	-3277
Exp. d11	0	3277	16384	20480	-16384	-3277
Exp. sfrd11	15	15	14	11	14	15
Exp. sfrc11	15	15	14	11	14	15
Exp. sfrb11	15	15	14	11	14	15
Exp. sfra11	15	15	14	11	14	15

Test settings	
Tolerance a11	±0,0000e+00
Tolerance c11	±0,0000e+00
Tolerance b11	±0,0000e+00
Tolerance d11	±0,0000e+00
Tolerance sfrd11	±0,0000e+00
Tolerance sfrc11	±0,0000e+00
Tolerance sfrb11	±0,0000e+00
Tolerance sfra11	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block TDSystemO1.

Test results						
Time step	1	2	3	4	5	6
Mask parameters						
A	0	0.1	1	10	-1	-0.1
B	0	0.1	1	10	-1	-0.1
C	0	0.1	1	10	-1	-0.1
D	0	0.1	1	10	-1	-0.1
Controller parameters						
a11	0	3276	16384	20480	-16384	-3276
c11	0	3276	16384	20480	-16384	-3276
b11	0	3276	16384	20480	-16384	-3276
d11	0	3276	16384	20480	-16384	-3276
sfrd11	15	15	14	11	14	15
sfrc11	15	15	14	11	14	15
sfrb11	15	15	14	11	14	15
sfra11	15	15	14	11	14	15
Exp. a11	0	3277	16384	20480	-16384	-3277
Exp. c11	0	3277	16384	20480	-16384	-3277
Exp. b11	0	3277	16384	20480	-16384	-3277
Exp. d11	0	3277	16384	20480	-16384	-3277
Exp. sfrd11	15	15	14	11	14	15
Exp. sfrc11	15	15	14	11	14	15
Exp. sfrb11	15	15	14	11	14	15
Exp. sfra11	15	15	14	11	14	15

Test settings	
Tolerance a11	±1,0000e+00
Tolerance c11	±1,0000e+00
Tolerance b11	±1,0000e+00
Tolerance d11	±1,0000e+00
Tolerance sfrd11	±0,0000e+00
Tolerance sfrc11	±0,0000e+00
Tolerance sfrb11	±0,0000e+00
Tolerance sfra11	±0,0000e+00

Test statistics	
Min CPU cycles	3118
Max CPU cycles	9878
Avg CPU cycles	4971

Verification: TDSystemO1 FiP16 CPU dsPIC33EP256MC502

Date of Test	2026-06-23
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for Control block TDSystemO1.

Test results						
Time step	1	2	3	4	...	174
CPU cycles	129	129	129	129	...	129
Inputs						
In (DSP)	0	-3271	-6510	-9684	...	-19661
In	-0	-0.1	-0.199	-0.296	...	-0.6
Parameters						
A	0.7					
B	0.38					
C	0.33					
D	0.1					
Outputs						
Out	0	-0.01	-0.032	-0.063	...	-0.311
Exp. Out	-0	-0.01	-0.032	-0.063	...	-0.311
Out (DSP)	0	-328	-1063	-2073	...	-10187
Exp. Out (DSP)	0	-327	-1061	-2072	...	-10184

Test settings	
Tolerance Out	±1,2207e-04 (±4 LSB)

Test statistics	
Min CPU cycles	128
Max CPU cycles	129
Avg CPU cycles	128

Test case: Conversion test OK

Conversion test for Control block TDSystemO1.

Test results						
Time step	1	2	3	4	5	6
Mask parameters						
A	0	0.1	1	10	-1	-0.1
B	0	0.1	1	10	-1	-0.1
C	0	0.1	1	10	-1	-0.1
D	0	0.1	1	10	-1	-0.1
Controller parameters						
a11	0	3277	16384	20480	-16384	-3277
c11	0	3277	16384	20480	-16384	-3277
b11	0	3277	16384	20480	-16384	-3277
d11	0	3277	16384	20480	-16384	-3277
sfrd11	15	15	14	11	14	15
sfrc11	15	15	14	11	14	15
sfrb11	15	15	14	11	14	15
sfra11	15	15	14	11	14	15
Exp. a11	0	3277	16384	20480	-16384	-3277
Exp. c11	0	3277	16384	20480	-16384	-3277
Exp. b11	0	3277	16384	20480	-16384	-3277
Exp. d11	0	3277	16384	20480	-16384	-3277
Exp. sfrd11	15	15	14	11	14	15
Exp. sfrc11	15	15	14	11	14	15
Exp. sfrb11	15	15	14	11	14	15
Exp. sfra11	15	15	14	11	14	15

Test settings	
Tolerance a11	±0,0000e+00
Tolerance c11	±0,0000e+00
Tolerance b11	±0,0000e+00
Tolerance d11	±0,0000e+00
Tolerance sfrd11	±0,0000e+00
Tolerance sfrc11	±0,0000e+00
Tolerance sfrb11	±0,0000e+00
Tolerance sfra11	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block TDSystemO1.

Test results						
Time step	1	2	3	4	5	6
Mask parameters						
A	0	0.1	1	10	-1	-0.1
B	0	0.1	1	10	-1	-0.1
C	0	0.1	1	10	-1	-0.1
D	0	0.1	1	10	-1	-0.1
Controller parameters						
a11	0	3276	16384	20480	-16384	-3276
c11	0	3276	16384	20480	-16384	-3276
b11	0	3276	16384	20480	-16384	-3276
d11	0	3276	16384	20480	-16384	-3276
sfrd11	15	15	14	11	14	15
sfrc11	15	15	14	11	14	15
sfrb11	15	15	14	11	14	15
sfra11	15	15	14	11	14	15
Exp. a11	0	3277	16384	20480	-16384	-3277
Exp. c11	0	3277	16384	20480	-16384	-3277
Exp. b11	0	3277	16384	20480	-16384	-3277
Exp. d11	0	3277	16384	20480	-16384	-3277
Exp. sfrd11	15	15	14	11	14	15
Exp. sfrc11	15	15	14	11	14	15
Exp. sfrb11	15	15	14	11	14	15
Exp. sfra11	15	15	14	11	14	15

Test settings	
Tolerance a11	±1,0000e+00
Tolerance c11	±1,0000e+00
Tolerance b11	±1,0000e+00
Tolerance d11	±1,0000e+00
Tolerance sfrd11	±0,0000e+00
Tolerance sfrc11	±0,0000e+00
Tolerance sfrb11	±0,0000e+00
Tolerance sfra11	±0,0000e+00

Test statistics	
Min CPU cycles	9373
Max CPU cycles	41121
Avg CPU cycles	19781

Verification: TDSystemO1 FiP32 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for Control block TDSystemO1.

Test results				
Time step	1	2	...	174
CPU cycles	350	350	...	350
Inputs				
In (DSP)	0	-214390630	...	-1288490189
In	-0	-0.1	...	-0.6
Parameters				
A	0.7			
B	0.38			
C	0.33			
D	0.1			
Outputs				
Out	0	-0.01	...	-0.311
Exp. Out	-0	-0.01	...	-0.311
Out (DSP)	0	-21439064	...	-667434826
Exp. Out (DSP)	0	-21439063	...	-667434823

Test settings	
Tolerance Out	±1,8626e-09 (±4 LSB)

Test statistics	
Min CPU cycles	290
Max CPU cycles	355
Avg CPU cycles	346

Test case: Conversion test OK

Conversion test for Control block TDSystemO1.

Test results				
Time step	1	2	...	6
Mask parameters				
A	0	0.1	...	-0.1
B	0	0.1	...	-0.1
C	0	0.1	...	-0.1
D	0	0.1	...	-0.1
Controller parameters				
a11	0	214748365	...	-214748365
c11	0	214748365	...	-214748365
b11	0	214748365	...	-214748365
d11	0	214748365	...	-214748365
sfrd11	31	31	...	31
sfrc11	31	31	...	31
sfrb11	31	31	...	31
sfra11	31	31	...	31
Exp. a11	0	214748365	...	-214748365
Exp. c11	0	214748365	...	-214748365
Exp. b11	0	214748365	...	-214748365
Exp. d11	0	214748365	...	-214748365
Exp. sfrd11	31	31	...	31
Exp. sfrc11	31	31	...	31
Exp. sfrb11	31	31	...	31
Exp. sfra11	31	31	...	31

Test settings	
Tolerance a11	±0,0000e+00
Tolerance c11	±0,0000e+00
Tolerance b11	±0,0000e+00
Tolerance d11	±0,0000e+00
Tolerance sfrd11	±0,0000e+00
Tolerance sfrc11	±0,0000e+00
Tolerance sfrb11	±0,0000e+00
Tolerance sfra11	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block TDSystemO1.

Test results				
Time step	1	2	...	6
Mask parameters				
A	0	0.1	...	-0.1
B	0	0.1	...	-0.1
C	0	0.1	...	-0.1
D	0	0.1	...	-0.1
Controller parameters				
a11	0	214748368	...	-214748368
c11	0	214748368	...	-214748368
b11	0	214748368	...	-214748368
d11	0	214748368	...	-214748368
sfrd11	31	31	...	31
sfrc11	31	31	...	31
sfrb11	31	31	...	31
sfra11	31	31	...	31
Exp. a11	0	214748365	...	-214748365
Exp. c11	0	214748365	...	-214748365
Exp. b11	0	214748365	...	-214748365
Exp. d11	0	214748365	...	-214748365
Exp. sfrd11	31	31	...	31
Exp. sfrc11	31	31	...	31
Exp. sfrb11	31	31	...	31
Exp. sfra11	31	31	...	31

Test settings	
Tolerance a11	±3,0000e+00
Tolerance c11	±3,0000e+00
Tolerance b11	±3,0000e+00
Tolerance d11	±3,0000e+00
Tolerance sfrd11	±0,0000e+00
Tolerance sfrc11	±0,0000e+00
Tolerance sfrb11	±0,0000e+00
Tolerance sfra11	±0,0000e+00

Test statistics	
Min CPU cycles	4952
Max CPU cycles	13744
Avg CPU cycles	7472

Verification: TDSystemO1 FiP32 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for Control block TDSystemO1.

Test results				
Time step	1	2	...	174
CPU cycles	199	199	...	199
Inputs				
In (DSP)	0	-214390630	...	-1288490189
In	-0	-0.1	...	-0.6
Parameters				
A	0.7			
B	0.38			
C	0.33			
D	0.1			
Outputs				
Out	0	-0.01	...	-0.311
Exp. Out	-0	-0.01	...	-0.311
Out (DSP)	0	-21439064	...	-667434826
Exp. Out (DSP)	0	-21439063	...	-667434823

Test settings	
Tolerance Out	±1,8626e-09 (±4 LSB)

Test statistics	
Min CPU cycles	193
Max CPU cycles	203
Avg CPU cycles	198

Test case: Conversion test OK

Conversion test for Control block TDSystemO1.

Test results				
Time step	1	2	...	6
Mask parameters				
A	0	0.1	...	-0.1
B	0	0.1	...	-0.1
C	0	0.1	...	-0.1
D	0	0.1	...	-0.1
Controller parameters				
a11	0	214748365	...	-214748365
c11	0	214748365	...	-214748365
b11	0	214748365	...	-214748365
d11	0	214748365	...	-214748365
sfrd11	31	31	...	31
sfrc11	31	31	...	31
sfrb11	31	31	...	31
sfra11	31	31	...	31
Exp. a11	0	214748365	...	-214748365
Exp. c11	0	214748365	...	-214748365
Exp. b11	0	214748365	...	-214748365
Exp. d11	0	214748365	...	-214748365
Exp. sfrd11	31	31	...	31
Exp. sfrc11	31	31	...	31
Exp. sfrb11	31	31	...	31
Exp. sfra11	31	31	...	31

Test settings	
Tolerance a11	±0,0000e+00
Tolerance c11	±0,0000e+00
Tolerance b11	±0,0000e+00
Tolerance d11	±0,0000e+00
Tolerance sfrd11	±0,0000e+00
Tolerance sfrc11	±0,0000e+00
Tolerance sfrb11	±0,0000e+00
Tolerance sfra11	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block TDSystemO1.

Test results				
Time step	1	2	...	6
Mask parameters				
A	0	0.1	...	-0.1
B	0	0.1	...	-0.1
C	0	0.1	...	-0.1
D	0	0.1	...	-0.1
Controller parameters				
a11	0	214748368	...	-214748368
c11	0	214748368	...	-214748368
b11	0	214748368	...	-214748368
d11	0	214748368	...	-214748368
sfrd11	31	31	...	31
sfrc11	31	31	...	31
sfrb11	31	31	...	31
sfra11	31	31	...	31
Exp. a11	0	214748365	...	-214748365
Exp. c11	0	214748365	...	-214748365
Exp. b11	0	214748365	...	-214748365
Exp. d11	0	214748365	...	-214748365
Exp. sfrd11	31	31	...	31
Exp. sfrc11	31	31	...	31
Exp. sfrb11	31	31	...	31
Exp. sfra11	31	31	...	31

Test settings	
Tolerance a11	±3,0000e+00
Tolerance c11	±3,0000e+00
Tolerance b11	±3,0000e+00
Tolerance d11	±3,0000e+00
Tolerance sfrd11	±0,0000e+00
Tolerance sfrc11	±0,0000e+00
Tolerance sfrb11	±0,0000e+00
Tolerance sfra11	±0,0000e+00

Test statistics	
Min CPU cycles	1979
Max CPU cycles	5555
Avg CPU cycles	3087

Verification: TDSystemO1 FiP32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for Control block TDSystemO1.

Test results				
Time step	1	2	...	174
CPU cycles	217	217	...	217
Inputs				
In (DSP)	0	-214390630	...	-1288490189
In	-0	-0.1	...	-0.6
Parameters				
A	0.7			
B	0.38			
C	0.33			
D	0.1			
Outputs				
Out	0	-0.01	...	-0.311
Exp. Out	-0	-0.01	...	-0.311
Out (DSP)	0	-21439064	...	-667434826
Exp. Out (DSP)	0	-21439063	...	-667434823

Test settings	
Tolerance Out	±1,8626e-09 (±4 LSB)

Test statistics	
Min CPU cycles	217
Max CPU cycles	217
Avg CPU cycles	217

Test case: Conversion test OK

Conversion test for Control block TDSystemO1.

Test results				
Time step	1	2	...	6
Mask parameters				
A	0	0.1	...	-0.1
B	0	0.1	...	-0.1
C	0	0.1	...	-0.1
D	0	0.1	...	-0.1
Controller parameters				
a11	0	214748365	...	-214748365
c11	0	214748365	...	-214748365
b11	0	214748365	...	-214748365
d11	0	214748365	...	-214748365
sfrd11	31	31	...	31
sfrc11	31	31	...	31
sfrb11	31	31	...	31
sfra11	31	31	...	31
Exp. a11	0	214748365	...	-214748365
Exp. c11	0	214748365	...	-214748365
Exp. b11	0	214748365	...	-214748365
Exp. d11	0	214748365	...	-214748365
Exp. sfrd11	31	31	...	31
Exp. sfrc11	31	31	...	31
Exp. sfrb11	31	31	...	31
Exp. sfra11	31	31	...	31

Test settings	
Tolerance a11	±0,0000e+00
Tolerance c11	±0,0000e+00
Tolerance b11	±0,0000e+00
Tolerance d11	±0,0000e+00
Tolerance sfrd11	±0,0000e+00
Tolerance sfrc11	±0,0000e+00
Tolerance sfrb11	±0,0000e+00
Tolerance sfra11	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block TDSystemO1.

Test results				
Time step	1	2	...	6
Mask parameters				
A	0	0.1	...	-0.1
B	0	0.1	...	-0.1
C	0	0.1	...	-0.1
D	0	0.1	...	-0.1
Controller parameters				
a11	0	214748368	...	-214748368
c11	0	214748368	...	-214748368
b11	0	214748368	...	-214748368
d11	0	214748368	...	-214748368
sfrd11	31	31	...	31
sfrc11	31	31	...	31
sfrb11	31	31	...	31
sfra11	31	31	...	31
Exp. a11	0	214748365	...	-214748365
Exp. c11	0	214748365	...	-214748365
Exp. b11	0	214748365	...	-214748365
Exp. d11	0	214748365	...	-214748365
Exp. sfrd11	31	31	...	31
Exp. sfrc11	31	31	...	31
Exp. sfrb11	31	31	...	31
Exp. sfra11	31	31	...	31

Test settings	
Tolerance a11	±3,0000e+00
Tolerance c11	±3,0000e+00
Tolerance b11	±3,0000e+00
Tolerance d11	±3,0000e+00
Tolerance sfrd11	±0,0000e+00
Tolerance sfrc11	±0,0000e+00
Tolerance sfrb11	±0,0000e+00
Tolerance sfra11	±0,0000e+00

Test statistics	
Min CPU cycles	3032
Max CPU cycles	5129
Avg CPU cycles	3626

Verification: TDSystemO1 FiP32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for Control block TDSystemO1.

Test results				
Time step	1	2	...	174
CPU cycles	523	537	...	537
Inputs				
In (DSP)	0	-214390630	...	-1288490189
In	-0	-0.1	...	-0.6
Parameters				
A	0.7			
B	0.38			
C	0.33			
D	0.1			
Outputs				
Out	0	-0.01	...	-0.311
Exp. Out	-0	-0.01	...	-0.311
Out (DSP)	0	-21439064	...	-667434826
Exp. Out (DSP)	0	-21439063	...	-667434823

Test settings	
Tolerance Out	±1,8626e-09 (±4 LSB)

Test statistics	
Min CPU cycles	523
Max CPU cycles	537
Avg CPU cycles	528

Test case: Conversion test OK

Conversion test for Control block TDSystemO1.

Test results				
Time step	1	2	...	6
Mask parameters				
A	0	0.1	...	-0.1
B	0	0.1	...	-0.1
C	0	0.1	...	-0.1
D	0	0.1	...	-0.1
Controller parameters				
a11	0	214748365	...	-214748365
c11	0	214748365	...	-214748365
b11	0	214748365	...	-214748365
d11	0	214748365	...	-214748365
sfrd11	31	31	...	31
sfrc11	31	31	...	31
sfrb11	31	31	...	31
sfra11	31	31	...	31
Exp. a11	0	214748365	...	-214748365
Exp. c11	0	214748365	...	-214748365
Exp. b11	0	214748365	...	-214748365
Exp. d11	0	214748365	...	-214748365
Exp. sfrd11	31	31	...	31
Exp. sfrc11	31	31	...	31
Exp. sfrb11	31	31	...	31
Exp. sfra11	31	31	...	31

Test settings	
Tolerance a11	±0,0000e+00
Tolerance c11	±0,0000e+00
Tolerance b11	±0,0000e+00
Tolerance d11	±0,0000e+00
Tolerance sfrd11	±0,0000e+00
Tolerance sfrc11	±0,0000e+00
Tolerance sfrb11	±0,0000e+00
Tolerance sfra11	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block TDSystemO1.

Test results				
Time step	1	2	...	6
Mask parameters				
A	0	0.1	...	-0.1
B	0	0.1	...	-0.1
C	0	0.1	...	-0.1
D	0	0.1	...	-0.1
Controller parameters				
a11	0	214748368	...	-214748368
c11	0	214748368	...	-214748368
b11	0	214748368	...	-214748368
d11	0	214748368	...	-214748368
sfrd11	31	31	...	31
sfrc11	31	31	...	31
sfrb11	31	31	...	31
sfra11	31	31	...	31
Exp. a11	0	214748365	...	-214748365
Exp. c11	0	214748365	...	-214748365
Exp. b11	0	214748365	...	-214748365
Exp. d11	0	214748365	...	-214748365
Exp. sfrd11	31	31	...	31
Exp. sfrc11	31	31	...	31
Exp. sfrb11	31	31	...	31
Exp. sfra11	31	31	...	31

Test settings	
Tolerance a11	±3,0000e+00
Tolerance c11	±3,0000e+00
Tolerance b11	±3,0000e+00
Tolerance d11	±3,0000e+00
Tolerance sfrd11	±0,0000e+00
Tolerance sfrc11	±0,0000e+00
Tolerance sfrb11	±0,0000e+00
Tolerance sfra11	±0,0000e+00

Test statistics	
Min CPU cycles	9744
Max CPU cycles	22252
Avg CPU cycles	14298

Verification: TDSystemO1 FiP32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for Control block TDSystemO1.

Test results				
Time step	1	2	...	174
CPU cycles	138	139	...	139
Inputs				
In (DSP)	0	-214390630	...	-1288490189
In	-0	-0.1	...	-0.6
Parameters				
A	0.7			
B	0.38			
C	0.33			
D	0.1			
Outputs				
Out	0	-0.01	...	-0.311
Exp. Out	-0	-0.01	...	-0.311
Out (DSP)	0	-21439064	...	-667434826
Exp. Out (DSP)	0	-21439063	...	-667434823

Test settings	
Tolerance Out	±1,8626e-09 (±4 LSB)

Test statistics	
Min CPU cycles	138
Max CPU cycles	143
Avg CPU cycles	138

Test case: Conversion test OK

Conversion test for Control block TDSystemO1.

Test results				
Time step	1	2	...	6
Mask parameters				
A	0	0.1	...	-0.1
B	0	0.1	...	-0.1
C	0	0.1	...	-0.1
D	0	0.1	...	-0.1
Controller parameters				
a11	0	214748365	...	-214748365
c11	0	214748365	...	-214748365
b11	0	214748365	...	-214748365
d11	0	214748365	...	-214748365
sfrd11	31	31	...	31
sfrc11	31	31	...	31
sfrb11	31	31	...	31
sfra11	31	31	...	31
Exp. a11	0	214748365	...	-214748365
Exp. c11	0	214748365	...	-214748365
Exp. b11	0	214748365	...	-214748365
Exp. d11	0	214748365	...	-214748365
Exp. sfrd11	31	31	...	31
Exp. sfrc11	31	31	...	31
Exp. sfrb11	31	31	...	31
Exp. sfra11	31	31	...	31

Test settings	
Tolerance a11	±0,0000e+00
Tolerance c11	±0,0000e+00
Tolerance b11	±0,0000e+00
Tolerance d11	±0,0000e+00
Tolerance sfrd11	±0,0000e+00
Tolerance sfrc11	±0,0000e+00
Tolerance sfrb11	±0,0000e+00
Tolerance sfra11	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block TDSystemO1.

Test results				
Time step	1	2	...	6
Mask parameters				
A	0	0.1	...	-0.1
B	0	0.1	...	-0.1
C	0	0.1	...	-0.1
D	0	0.1	...	-0.1
Controller parameters				
a11	0	214748368	...	-214748368
c11	0	214748368	...	-214748368
b11	0	214748368	...	-214748368
d11	0	214748368	...	-214748368
sfrd11	31	31	...	31
sfrc11	31	31	...	31
sfrb11	31	31	...	31
sfra11	31	31	...	31
Exp. a11	0	214748365	...	-214748365
Exp. c11	0	214748365	...	-214748365
Exp. b11	0	214748365	...	-214748365
Exp. d11	0	214748365	...	-214748365
Exp. sfrd11	31	31	...	31
Exp. sfrc11	31	31	...	31
Exp. sfrb11	31	31	...	31
Exp. sfra11	31	31	...	31

Test settings	
Tolerance a11	±3,0000e+00
Tolerance c11	±3,0000e+00
Tolerance b11	±3,0000e+00
Tolerance d11	±3,0000e+00
Tolerance sfrd11	±0,0000e+00
Tolerance sfrc11	±0,0000e+00
Tolerance sfrb11	±0,0000e+00
Tolerance sfra11	±0,0000e+00

Test statistics	
Min CPU cycles	4459
Max CPU cycles	9143
Avg CPU cycles	5963

Verification: TDSystemO1 FiP32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for Control block TDSystemO1.

Test results				
Time step	1	2	...	174
CPU cycles	220	179	...	179
Inputs				
In (DSP)	0	-214390630	...	-1288490189
In	-0	-0.1	...	-0.6
Parameters				
A	0.7			
B	0.38			
C	0.33			
D	0.1			
Outputs				
Out	0	-0.01	...	-0.311
Exp. Out	-0	-0.01	...	-0.311
Out (DSP)	0	-21439064	...	-667434826
Exp. Out (DSP)	0	-21439063	...	-667434823

Test settings	
Tolerance Out	±1,8626e-09 (±4 LSB)

Test statistics	
Min CPU cycles	179
Max CPU cycles	220
Avg CPU cycles	179

Test case: Conversion test OK

Conversion test for Control block TDSystemO1.

Test results				
Time step	1	2	...	6
Mask parameters				
A	0	0.1	...	-0.1
B	0	0.1	...	-0.1
C	0	0.1	...	-0.1
D	0	0.1	...	-0.1
Controller parameters				
a11	0	214748365	...	-214748365
c11	0	214748365	...	-214748365
b11	0	214748365	...	-214748365
d11	0	214748365	...	-214748365
sfrd11	31	31	...	31
sfrc11	31	31	...	31
sfrb11	31	31	...	31
sfra11	31	31	...	31
Exp. a11	0	214748365	...	-214748365
Exp. c11	0	214748365	...	-214748365
Exp. b11	0	214748365	...	-214748365
Exp. d11	0	214748365	...	-214748365
Exp. sfrd11	31	31	...	31
Exp. sfrc11	31	31	...	31
Exp. sfrb11	31	31	...	31
Exp. sfra11	31	31	...	31

Test settings	
Tolerance a11	±0,0000e+00
Tolerance c11	±0,0000e+00
Tolerance b11	±0,0000e+00
Tolerance d11	±0,0000e+00
Tolerance sfrd11	±0,0000e+00
Tolerance sfrc11	±0,0000e+00
Tolerance sfrb11	±0,0000e+00
Tolerance sfra11	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block TDSystemO1.

Test results				
Time step	1	2	...	6
Mask parameters				
A	0	0.1	...	-0.1
B	0	0.1	...	-0.1
C	0	0.1	...	-0.1
D	0	0.1	...	-0.1
Controller parameters				
a11	0	214748368	...	-214748368
c11	0	214748368	...	-214748368
b11	0	214748368	...	-214748368
d11	0	214748368	...	-214748368
sfrd11	31	31	...	31
sfrc11	31	31	...	31
sfrb11	31	31	...	31
sfra11	31	31	...	31
Exp. a11	0	214748365	...	-214748365
Exp. c11	0	214748365	...	-214748365
Exp. b11	0	214748365	...	-214748365
Exp. d11	0	214748365	...	-214748365
Exp. sfrd11	31	31	...	31
Exp. sfrc11	31	31	...	31
Exp. sfrb11	31	31	...	31
Exp. sfra11	31	31	...	31

Test settings	
Tolerance a11	±3,0000e+00
Tolerance c11	±3,0000e+00
Tolerance b11	±3,0000e+00
Tolerance d11	±3,0000e+00
Tolerance sfrd11	±0,0000e+00
Tolerance sfrc11	±0,0000e+00
Tolerance sfrb11	±0,0000e+00
Tolerance sfra11	±0,0000e+00

Test statistics	
Min CPU cycles	2871
Max CPU cycles	4838
Avg CPU cycles	3411

Verification: TDSystemO1 FiP32 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for Control block TDSystemO1.

Test results				
Time step	1	2	...	174
CPU cycles	298	298	...	298
Inputs				
In (DSP)	0	-214390630	...	-1288490189
In	-0	-0.1	...	-0.6
Parameters				
A	0.7			
B	0.38			
C	0.33			
D	0.1			
Outputs				
Out	0	-0.01	...	-0.311
Exp. Out	-0	-0.01	...	-0.311
Out (DSP)	0	-21439064	...	-667434826
Exp. Out (DSP)	0	-21439063	...	-667434823

Test settings	
Tolerance Out	±1,8626e-09 (±4 LSB)

Test statistics	
Min CPU cycles	256
Max CPU cycles	307
Avg CPU cycles	296

Test case: Conversion test OK

Conversion test for Control block TDSystemO1.

Test results				
Time step	1	2	...	6
Mask parameters				
A	0	0.1	...	-0.1
B	0	0.1	...	-0.1
C	0	0.1	...	-0.1
D	0	0.1	...	-0.1
Controller parameters				
a11	0	214748365	...	-214748365
c11	0	214748365	...	-214748365
b11	0	214748365	...	-214748365
d11	0	214748365	...	-214748365
sfrd11	31	31	...	31
sfrc11	31	31	...	31
sfrb11	31	31	...	31
sfra11	31	31	...	31
Exp. a11	0	214748365	...	-214748365
Exp. c11	0	214748365	...	-214748365
Exp. b11	0	214748365	...	-214748365
Exp. d11	0	214748365	...	-214748365
Exp. sfrd11	31	31	...	31
Exp. sfrc11	31	31	...	31
Exp. sfrb11	31	31	...	31
Exp. sfra11	31	31	...	31

Test settings	
Tolerance a11	±0,0000e+00
Tolerance c11	±0,0000e+00
Tolerance b11	±0,0000e+00
Tolerance d11	±0,0000e+00
Tolerance sfrd11	±0,0000e+00
Tolerance sfrc11	±0,0000e+00
Tolerance sfrb11	±0,0000e+00
Tolerance sfra11	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block TDSystemO1.

Test results				
Time step	1	2	...	6
Mask parameters				
A	0	0.1	...	-0.1
B	0	0.1	...	-0.1
C	0	0.1	...	-0.1
D	0	0.1	...	-0.1
Controller parameters				
a11	0	214748368	...	-214748368
c11	0	214748368	...	-214748368
b11	0	214748368	...	-214748368
d11	0	214748368	...	-214748368
sfrd11	31	31	...	31
sfrc11	31	31	...	31
sfrb11	31	31	...	31
sfra11	31	31	...	31
Exp. a11	0	214748365	...	-214748365
Exp. c11	0	214748365	...	-214748365
Exp. b11	0	214748365	...	-214748365
Exp. d11	0	214748365	...	-214748365
Exp. sfrd11	31	31	...	31
Exp. sfrc11	31	31	...	31
Exp. sfrb11	31	31	...	31
Exp. sfra11	31	31	...	31

Test settings	
Tolerance a11	±3,0000e+00
Tolerance c11	±3,0000e+00
Tolerance b11	±3,0000e+00
Tolerance d11	±3,0000e+00
Tolerance sfrd11	±0,0000e+00
Tolerance sfrc11	±0,0000e+00
Tolerance sfrb11	±0,0000e+00
Tolerance sfra11	±0,0000e+00

Test statistics	
Min CPU cycles	3528
Max CPU cycles	10460
Avg CPU cycles	5515

Verification: TDSystemO1 FiP32 CPU dsPIC33EP256MC502

Date of Test	2026-06-23
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for Control block TDSystemO1.

Test results				
Time step	1	2	...	174
CPU cycles	1799	1813	...	1827
Inputs				
In (DSP)	0	-214390630	...	-1288490189
In	-0	-0.1	...	-0.6
Parameters				
A	0.7			
B	0.38			
C	0.33			
D	0.1			
Outputs				
Out	0	-0.01	...	-0.311
Exp. Out	-0	-0.01	...	-0.311
Out (DSP)	0	-21439064	...	-667434826
Exp. Out (DSP)	0	-21439063	...	-667434823

Test settings	
Tolerance Out	±1,8626e-09 (±4 LSB)

Test statistics	
Min CPU cycles	1799
Max CPU cycles	1828
Avg CPU cycles	1809

Test case: Conversion test OK

Conversion test for Control block TDSystemO1.

Test results				
Time step	1	2	...	6
Mask parameters				
A	0	0.1	...	-0.1
B	0	0.1	...	-0.1
C	0	0.1	...	-0.1
D	0	0.1	...	-0.1
Controller parameters				
a11	0	214748365	...	-214748365
c11	0	214748365	...	-214748365
b11	0	214748365	...	-214748365
d11	0	214748365	...	-214748365
sfrd11	31	31	...	31
sfrc11	31	31	...	31
sfrb11	31	31	...	31
sfra11	31	31	...	31
Exp. a11	0	214748365	...	-214748365
Exp. c11	0	214748365	...	-214748365
Exp. b11	0	214748365	...	-214748365
Exp. d11	0	214748365	...	-214748365
Exp. sfrd11	31	31	...	31
Exp. sfrc11	31	31	...	31
Exp. sfrb11	31	31	...	31
Exp. sfra11	31	31	...	31

Test settings	
Tolerance a11	±0,0000e+00
Tolerance c11	±0,0000e+00
Tolerance b11	±0,0000e+00
Tolerance d11	±0,0000e+00
Tolerance sfrd11	±0,0000e+00
Tolerance sfrc11	±0,0000e+00
Tolerance sfrb11	±0,0000e+00
Tolerance sfra11	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block TDSystemO1.

Test results				
Time step	1	2	...	6
Mask parameters				
A	0	0.1	...	-0.1
B	0	0.1	...	-0.1
C	0	0.1	...	-0.1
D	0	0.1	...	-0.1
Controller parameters				
a11	0	214748368	...	-214748368
c11	0	214748368	...	-214748368
b11	0	214748368	...	-214748368
d11	0	214748368	...	-214748368
sfrd11	31	31	...	31
sfrc11	31	31	...	31
sfrb11	31	31	...	31
sfra11	31	31	...	31
Exp. a11	0	214748365	...	-214748365
Exp. c11	0	214748365	...	-214748365
Exp. b11	0	214748365	...	-214748365
Exp. d11	0	214748365	...	-214748365
Exp. sfrd11	31	31	...	31
Exp. sfrc11	31	31	...	31
Exp. sfrb11	31	31	...	31
Exp. sfra11	31	31	...	31

Test settings	
Tolerance a11	±3,0000e+00
Tolerance c11	±3,0000e+00
Tolerance b11	±3,0000e+00
Tolerance d11	±3,0000e+00
Tolerance sfrd11	±0,0000e+00
Tolerance sfrc11	±0,0000e+00
Tolerance sfrb11	±0,0000e+00
Tolerance sfra11	±0,0000e+00

Test statistics	
Min CPU cycles	10998
Max CPU cycles	41682
Avg CPU cycles	21084

Verification: TDSystemO1 Float32 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for Control block TDSystemO1.

Test results				
Time step	1	2	...	174
CPU cycles	73	73	...	73
Inputs				
In (DSP)	-0	-0.1	...	-0.6
In	-0	-0.1	...	-0.6
Parameters				
A	0.7			
B	0.38			
C	0.33			
D	0.1			
Outputs				
Out	-0	-0.01	...	-0.311
Exp. Out	-0	-0.01	...	-0.311
Out (DSP)	-0	-0.01	...	-0.311
Exp. Out (DSP)	-0	-0.01	...	-0.311

Test settings	
Tolerance Out	±9,3132e-08 (±200 LSB)

Test statistics	
Min CPU cycles	73
Max CPU cycles	73
Avg CPU cycles	73

Test case: Conversion test OK

Conversion test for Control block TDSystemO1.

Test results				
Time step	1	2	...	6
Mask parameters				
A	0	0.1	...	-0.1
B	0	0.1	...	-0.1
C	0	0.1	...	-0.1
D	0	0.1	...	-0.1
Controller parameters				
a11	0	0.1	...	-0.1
c11	0	0.1	...	-0.1
b11	0	0.1	...	-0.1
d11	0	0.1	...	-0.1
Exp. a11	0	0.1	...	-0.1
Exp. c11	0	0.1	...	-0.1
Exp. b11	0	0.1	...	-0.1
Exp. d11	0	0.1	...	-0.1

Test settings	
Tolerance a11	±0,0000e+00
Tolerance c11	±0,0000e+00
Tolerance b11	±0,0000e+00
Tolerance d11	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block TDSystemO1.

Test results				
Time step	1	2	...	6
Mask parameters				
A	0	0.1	...	-0.1
B	0	0.1	...	-0.1
C	0	0.1	...	-0.1
D	0	0.1	...	-0.1
Controller parameters				
a11	0	0.1	...	-0.1
c11	0	0.1	...	-0.1
b11	0	0.1	...	-0.1
d11	0	0.1	...	-0.1
Exp. a11	0	0.1	...	-0.1
Exp. c11	0	0.1	...	-0.1
Exp. b11	0	0.1	...	-0.1
Exp. d11	0	0.1	...	-0.1

Test settings	
Tolerance a11	±2,0000e-09
Tolerance c11	±2,0000e-09
Tolerance b11	±2,0000e-09
Tolerance d11	±2,0000e-09

Test statistics	
Min CPU cycles	1862
Max CPU cycles	1906
Avg CPU cycles	1869

Verification: TDSystemO1 Float32 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for Control block TDSystemO1.

Test results				
Time step	1	2	...	174
CPU cycles	47	47	...	47
Inputs				
In (DSP)	-0	-0.1	...	-0.6
In	-0	-0.1	...	-0.6
Parameters				
A	0.7			
B	0.38			
C	0.33			
D	0.1			
Outputs				
Out	-0	-0.01	...	-0.311
Exp. Out	-0	-0.01	...	-0.311
Out (DSP)	-0	-0.01	...	-0.311
Exp. Out (DSP)	-0	-0.01	...	-0.311

Test settings	
Tolerance Out	±9,3132e-08 (±200 LSB)

Test statistics	
Min CPU cycles	47
Max CPU cycles	47
Avg CPU cycles	47

Test case: Conversion test OK

Conversion test for Control block TDSystemO1.

Test results				
Time step	1	2	...	6
Mask parameters				
A	0	0.1	...	-0.1
B	0	0.1	...	-0.1
C	0	0.1	...	-0.1
D	0	0.1	...	-0.1
Controller parameters				
a11	0	0.1	...	-0.1
c11	0	0.1	...	-0.1
b11	0	0.1	...	-0.1
d11	0	0.1	...	-0.1
Exp. a11	0	0.1	...	-0.1
Exp. c11	0	0.1	...	-0.1
Exp. b11	0	0.1	...	-0.1
Exp. d11	0	0.1	...	-0.1

Test settings	
Tolerance a11	±0,0000e+00
Tolerance c11	±0,0000e+00
Tolerance b11	±0,0000e+00
Tolerance d11	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block TDSystemO1.

Test results				
Time step	1	2	...	6
Mask parameters				
A	0	0.1	...	-0.1
B	0	0.1	...	-0.1
C	0	0.1	...	-0.1
D	0	0.1	...	-0.1
Controller parameters				
a11	0	0.1	...	-0.1
c11	0	0.1	...	-0.1
b11	0	0.1	...	-0.1
d11	0	0.1	...	-0.1
Exp. a11	0	0.1	...	-0.1
Exp. c11	0	0.1	...	-0.1
Exp. b11	0	0.1	...	-0.1
Exp. d11	0	0.1	...	-0.1

Test settings	
Tolerance a11	±2,0000e-09
Tolerance c11	±2,0000e-09
Tolerance b11	±2,0000e-09
Tolerance d11	±2,0000e-09

Test statistics	
Min CPU cycles	851
Max CPU cycles	851
Avg CPU cycles	851

Verification: TDSystemO1 Float32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for Control block TDSystemO1.

Test results				
Time step	1	2	...	174
CPU cycles	86	86	...	86
Inputs				
In (DSP)	-0	-0.1	...	-0.6
In	-0	-0.1	...	-0.6
Parameters				
A	0.7			
B	0.38			
C	0.33			
D	0.1			
Outputs				
Out	-0	-0.01	...	-0.311
Exp. Out	-0	-0.01	...	-0.311
Out (DSP)	-0	-0.01	...	-0.311
Exp. Out (DSP)	-0	-0.01	...	-0.311

Test settings	
Tolerance Out	±9,3132e-08 (±200 LSB)

Test statistics	
Min CPU cycles	86
Max CPU cycles	86
Avg CPU cycles	86

Test case: Conversion test OK

Conversion test for Control block TDSystemO1.

Test results				
Time step	1	2	...	6
Mask parameters				
A	0	0.1	...	-0.1
B	0	0.1	...	-0.1
C	0	0.1	...	-0.1
D	0	0.1	...	-0.1
Controller parameters				
a11	0	0.1	...	-0.1
c11	0	0.1	...	-0.1
b11	0	0.1	...	-0.1
d11	0	0.1	...	-0.1
Exp. a11	0	0.1	...	-0.1
Exp. c11	0	0.1	...	-0.1
Exp. b11	0	0.1	...	-0.1
Exp. d11	0	0.1	...	-0.1

Test settings	
Tolerance a11	±0,0000e+00
Tolerance c11	±0,0000e+00
Tolerance b11	±0,0000e+00
Tolerance d11	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block TDSystemO1.

Test results				
Time step	1	2	...	6
Mask parameters				
A	0	0.1	...	-0.1
B	0	0.1	...	-0.1
C	0	0.1	...	-0.1
D	0	0.1	...	-0.1
Controller parameters				
a11	0	0.1	...	-0.1
c11	0	0.1	...	-0.1
b11	0	0.1	...	-0.1
d11	0	0.1	...	-0.1
Exp. a11	0	0.1	...	-0.1
Exp. c11	0	0.1	...	-0.1
Exp. b11	0	0.1	...	-0.1
Exp. d11	0	0.1	...	-0.1

Test settings	
Tolerance a11	±2,0000e-09
Tolerance c11	±2,0000e-09
Tolerance b11	±2,0000e-09
Tolerance d11	±2,0000e-09

Test statistics	
Min CPU cycles	810
Max CPU cycles	810
Avg CPU cycles	810

Verification: TDSystemO1 Float32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for Control block TDSystemO1.

Test results				
Time step	1	2	...	174
CPU cycles	817	967	...	1037
Inputs				
In (DSP)	-0	-0.1	...	-0.6
In	-0	-0.1	...	-0.6
Parameters				
A	0.7			
B	0.38			
C	0.33			
D	0.1			
Outputs				
Out	-0	-0.01	...	-0.311
Exp. Out	-0	-0.01	...	-0.311
Out (DSP)	-0	-0.01	...	-0.311
Exp. Out (DSP)	-0	-0.01	...	-0.311

Test settings	
Tolerance Out	±9,3132e-08 (±200 LSB)

Test statistics	
Min CPU cycles	817
Max CPU cycles	1114
Avg CPU cycles	999

Test case: Conversion test OK

Conversion test for Control block TDSystemO1.

Test results				
Time step	1	2	...	6
Mask parameters				
A	0	0.1	...	-0.1
B	0	0.1	...	-0.1
C	0	0.1	...	-0.1
D	0	0.1	...	-0.1
Controller parameters				
a11	0	0.1	...	-0.1
c11	0	0.1	...	-0.1
b11	0	0.1	...	-0.1
d11	0	0.1	...	-0.1
Exp. a11	0	0.1	...	-0.1
Exp. c11	0	0.1	...	-0.1
Exp. b11	0	0.1	...	-0.1
Exp. d11	0	0.1	...	-0.1

Test settings	
Tolerance a11	±0,0000e+00
Tolerance c11	±0,0000e+00
Tolerance b11	±0,0000e+00
Tolerance d11	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block TDSystemO1.

Test results				
Time step	1	2	...	6
Mask parameters				
A	0	0.1	...	-0.1
B	0	0.1	...	-0.1
C	0	0.1	...	-0.1
D	0	0.1	...	-0.1
Controller parameters				
a11	0	0.1	...	-0.1
c11	0	0.1	...	-0.1
b11	0	0.1	...	-0.1
d11	0	0.1	...	-0.1
Exp. a11	0	0.1	...	-0.1
Exp. c11	0	0.1	...	-0.1
Exp. b11	0	0.1	...	-0.1
Exp. d11	0	0.1	...	-0.1

Test settings	
Tolerance a11	±2,0000e-09
Tolerance c11	±2,0000e-09
Tolerance b11	±2,0000e-09
Tolerance d11	±2,0000e-09

Test statistics	
Min CPU cycles	1729
Max CPU cycles	1845
Avg CPU cycles	1807

Verification: TDSystemO1 Float32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for Control block TDSystemO1.

Test results				
Time step	1	2	...	174
CPU cycles	289	363	...	375
Inputs				
In (DSP)	-0	-0.1	...	-0.6
In	-0	-0.1	...	-0.6
Parameters				
A	0.7			
B	0.38			
C	0.33			
D	0.1			
Outputs				
Out	-0	-0.01	...	-0.311
Exp. Out	-0	-0.01	...	-0.311
Out (DSP)	-0	-0.01	...	-0.311
Exp. Out (DSP)	-0	-0.01	...	-0.311

Test settings	
Tolerance Out	±9,3132e-08 (±200 LSB)

Test statistics	
Min CPU cycles	287
Max CPU cycles	395
Avg CPU cycles	359

Test case: Conversion test OK

Conversion test for Control block TDSystemO1.

Test results				
Time step	1	2	...	6
Mask parameters				
A	0	0.1	...	-0.1
B	0	0.1	...	-0.1
C	0	0.1	...	-0.1
D	0	0.1	...	-0.1
Controller parameters				
a11	0	0.1	...	-0.1
c11	0	0.1	...	-0.1
b11	0	0.1	...	-0.1
d11	0	0.1	...	-0.1
Exp. a11	0	0.1	...	-0.1
Exp. c11	0	0.1	...	-0.1
Exp. b11	0	0.1	...	-0.1
Exp. d11	0	0.1	...	-0.1

Test settings	
Tolerance a11	±0,0000e+00
Tolerance c11	±0,0000e+00
Tolerance b11	±0,0000e+00
Tolerance d11	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block TDSystemO1.

Test results				
Time step	1	2	...	6
Mask parameters				
A	0	0.1	...	-0.1
B	0	0.1	...	-0.1
C	0	0.1	...	-0.1
D	0	0.1	...	-0.1
Controller parameters				
a11	0	0.1	...	-0.1
c11	0	0.1	...	-0.1
b11	0	0.1	...	-0.1
d11	0	0.1	...	-0.1
Exp. a11	0	0.1	...	-0.1
Exp. c11	0	0.1	...	-0.1
Exp. b11	0	0.1	...	-0.1
Exp. d11	0	0.1	...	-0.1

Test settings	
Tolerance a11	±2,0000e-09
Tolerance c11	±2,0000e-09
Tolerance b11	±2,0000e-09
Tolerance d11	±2,0000e-09

Test statistics	
Min CPU cycles	647
Max CPU cycles	651
Avg CPU cycles	649

Verification: TDSystemO1 Float32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for Control block TDSystemO1.

Test results				
Time step	1	2	...	174
CPU cycles	92	80	...	80
Inputs				
In (DSP)	-0	-0.1	...	-0.6
In	-0	-0.1	...	-0.6
Parameters				
A	0.7			
B	0.38			
C	0.33			
D	0.1			
Outputs				
Out	-0	-0.01	...	-0.311
Exp. Out	-0	-0.01	...	-0.311
Out (DSP)	-0	-0.01	...	-0.311
Exp. Out (DSP)	-0	-0.01	...	-0.311

Test settings	
Tolerance Out	±9,3132e-08 (±200 LSB)

Test statistics	
Min CPU cycles	80
Max CPU cycles	92
Avg CPU cycles	80

Test case: Conversion test OK

Conversion test for Control block TDSystemO1.

Test results				
Time step	1	2	...	6
Mask parameters				
A	0	0.1	...	-0.1
B	0	0.1	...	-0.1
C	0	0.1	...	-0.1
D	0	0.1	...	-0.1
Controller parameters				
a11	0	0.1	...	-0.1
c11	0	0.1	...	-0.1
b11	0	0.1	...	-0.1
d11	0	0.1	...	-0.1
Exp. a11	0	0.1	...	-0.1
Exp. c11	0	0.1	...	-0.1
Exp. b11	0	0.1	...	-0.1
Exp. d11	0	0.1	...	-0.1

Test settings	
Tolerance a11	±0,0000e+00
Tolerance c11	±0,0000e+00
Tolerance b11	±0,0000e+00
Tolerance d11	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block TDSystemO1.

Test results				
Time step	1	2	...	6
Mask parameters				
A	0	0.1	...	-0.1
B	0	0.1	...	-0.1
C	0	0.1	...	-0.1
D	0	0.1	...	-0.1
Controller parameters				
a11	0	0.1	...	-0.1
c11	0	0.1	...	-0.1
b11	0	0.1	...	-0.1
d11	0	0.1	...	-0.1
Exp. a11	0	0.1	...	-0.1
Exp. c11	0	0.1	...	-0.1
Exp. b11	0	0.1	...	-0.1
Exp. d11	0	0.1	...	-0.1

Test settings	
Tolerance a11	±2,0000e-09
Tolerance c11	±2,0000e-09
Tolerance b11	±2,0000e-09
Tolerance d11	±2,0000e-09

Test statistics	
Min CPU cycles	787
Max CPU cycles	907
Avg CPU cycles	807

Verification: TDSystemO1 Float32 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for Control block TDSystemO1.

Test results				
Time step	1	2	...	174
CPU cycles	63	63	...	63
Inputs				
In (DSP)	-0	-0.1	...	-0.6
In	-0	-0.1	...	-0.6
Parameters				
A	0.7			
B	0.38			
C	0.33			
D	0.1			
Outputs				
Out	-0	-0.01	...	-0.311
Exp. Out	-0	-0.01	...	-0.311
Out (DSP)	-0	-0.01	...	-0.311
Exp. Out (DSP)	-0	-0.01	...	-0.311

Test settings	
Tolerance Out	±9,3132e-08 (±200 LSB)

Test statistics	
Min CPU cycles	63
Max CPU cycles	63
Avg CPU cycles	63

Test case: Conversion test OK

Conversion test for Control block TDSystemO1.

Test results				
Time step	1	2	...	6
Mask parameters				
A	0	0.1	...	-0.1
B	0	0.1	...	-0.1
C	0	0.1	...	-0.1
D	0	0.1	...	-0.1
Controller parameters				
a11	0	0.1	...	-0.1
c11	0	0.1	...	-0.1
b11	0	0.1	...	-0.1
d11	0	0.1	...	-0.1
Exp. a11	0	0.1	...	-0.1
Exp. c11	0	0.1	...	-0.1
Exp. b11	0	0.1	...	-0.1
Exp. d11	0	0.1	...	-0.1

Test settings	
Tolerance a11	±0,0000e+00
Tolerance c11	±0,0000e+00
Tolerance b11	±0,0000e+00
Tolerance d11	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block TDSystemO1.

Test results				
Time step	1	2	...	6
Mask parameters				
A	0	0.1	...	-0.1
B	0	0.1	...	-0.1
C	0	0.1	...	-0.1
D	0	0.1	...	-0.1
Controller parameters				
a11	0	0.1	...	-0.1
c11	0	0.1	...	-0.1
b11	0	0.1	...	-0.1
d11	0	0.1	...	-0.1
Exp. a11	0	0.1	...	-0.1
Exp. c11	0	0.1	...	-0.1
Exp. b11	0	0.1	...	-0.1
Exp. d11	0	0.1	...	-0.1

Test settings	
Tolerance a11	±2,0000e-09
Tolerance c11	±2,0000e-09
Tolerance b11	±2,0000e-09
Tolerance d11	±2,0000e-09

Test statistics	
Min CPU cycles	1362
Max CPU cycles	1406
Avg CPU cycles	1369

Verification: TDSystemO1 Float32 CPU dsPIC33EP256MC502

Date of Test	2026-06-23
Target controller	dsPIC33EP256MC502

Test case: Inport test

OK

Inport test for Control block TDSystemO1.

Test results				
Time step	1	2	...	174
CPU cycles	809	887	...	1027
Inputs				
In (DSP)	-0	-0.1	...	-0.6
In	-0	-0.1	...	-0.6
Parameters				
A	0.7			
B	0.38			
C	0.33			
D	0.1			
Outputs				
Out	-0	-0.01	...	-0.311
Exp. Out	-0	-0.01	...	-0.311
Out (DSP)	-0	-0.01	...	-0.311
Exp. Out (DSP)	-0	-0.01	...	-0.311

Test settings	
Tolerance Out	±9,3132e-08 (±200 LSB)

Test statistics	
Min CPU cycles	803
Max CPU cycles	1370
Avg CPU cycles	976

Test case: Conversion test

OK

Conversion test for Control block TDSystemO1.

Test results				
Time step	1	2	...	6
Mask parameters				
A	0	0.1	...	-0.1
B	0	0.1	...	-0.1
C	0	0.1	...	-0.1
D	0	0.1	...	-0.1
Controller parameters				
a11	0	0.1	...	-0.1
c11	0	0.1	...	-0.1
b11	0	0.1	...	-0.1
d11	0	0.1	...	-0.1
Exp. a11	0	0.1	...	-0.1
Exp. c11	0	0.1	...	-0.1
Exp. b11	0	0.1	...	-0.1
Exp. d11	0	0.1	...	-0.1

Test settings	
Tolerance a11	±0,0000e+00
Tolerance c11	±0,0000e+00
Tolerance b11	±0,0000e+00
Tolerance d11	±0,0000e+00

Test case: Conversion-on-Target test **OK**

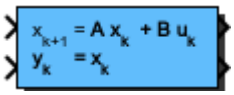
Conversion-on-Target test for Control block TDSystemO1.

Test results				
Time step	1	2	...	6
Mask parameters				
A	0	0.1	...	-0.1
B	0	0.1	...	-0.1
C	0	0.1	...	-0.1
D	0	0.1	...	-0.1
Controller parameters				
a11	0	0.1	...	-0.1
c11	0	0.1	...	-0.1
b11	0	0.1	...	-0.1
d11	0	0.1	...	-0.1
Exp. a11	0	0.1	...	-0.1
Exp. c11	0	0.1	...	-0.1
Exp. b11	0	0.1	...	-0.1
Exp. d11	0	0.1	...	-0.1

Test settings	
Tolerance a11	±2,0000e-09
Tolerance c11	±2,0000e-09
Tolerance b11	±2,0000e-09
Tolerance d11	±2,0000e-09

Test statistics	
Min CPU cycles	1418
Max CPU cycles	2798
Avg CPU cycles	2560

Block: TDSystemO2



2nd order time discrete system with two inputs and two outputs.

Inports	
In1	Input #1
In2	Input #2

Outports	
Out1	Output #1
Out2	Output #2

Mask Parameters		
Name	**ID**	**Description**
A	1	State matrix A
B	2	Input matrix B

Description:

Calculation:

$$\begin{bmatrix} x_{1,k+1} \\ x_{2,k+1} \end{bmatrix} = \begin{bmatrix} a_{1,1} & a_{1,2} \\ a_{2,1} & a_{2,2} \end{bmatrix} \begin{bmatrix} x_{1,k} \\ x_{2,k} \end{bmatrix} + \begin{bmatrix} b_{1,1} & b_{1,2} \\ b_{2,1} & b_{2,2} \end{bmatrix} \begin{bmatrix} u_{1,k} \\ u_{2,k} \end{bmatrix}$$

$$\begin{bmatrix} y_{1,k} \\ y_{2,k} \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} x_{1,k} \\ x_{2,k} \end{bmatrix} + \begin{bmatrix} 0 & 0 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} u_{1,k} \\ u_{2,k} \end{bmatrix}$$

or short

$$\mathbf{x}_{k+1} = \mathbf{A}\mathbf{x}_k + \mathbf{B}\mathbf{u}_k$$
$$\mathbf{y}_k = \mathbf{x}_k$$

Implementations:

FiP8	8 Bit Fixed Point Implementation
FiP16	16 Bit Fixed Point Implementation
FiP32	32 Bit Fixed Point Implementation
Float32	32 Bit Floating Point Implementation
Float64	64 Bit Floating Point Implementation

Implementation: FiP8

8 Bit Fixed Point Implementation

Inports Data Type	
In1	int8
In2	int8

Outports Data Type	
Out1	int8
Out2	int8

Implementation: FiP16

16 Bit Fixed Point Implementation

Inports Data Type	
In1	int16
In2	int16

Outports Data Type	
Out1	int16
Out2	int16

Implementation: FiP32

32 Bit Fixed Point Implementation

Inports Data Type	
In1	int32
In2	int32

Outports Data Type	
Out1	int32
Out2	int32

Implementation: Float32

32 Bit Floating Point Implementation

Inports Data Type	
In1	float32
In2	float32

Outports Data Type	
Out1	float32
Out2	float32

Implementation: Float64

64 Bit Floating Point Implementation

Inports Data Type	
In1	float64
In2	float64

Outports Data Type	
Out1	float64
Out2	float64

Verification: TDSystemO2 FiP16 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for Control block TDSystemO2.

Test results						
Time step	1	2	3	4	...	174
CPU cycles	171	171	171	171	...	171
Inputs						
In1 (DSP)	0	-3271	-6510	-9684	...	-19661
In2 (DSP)	-32768	-32604	-32115	-31304	...	-19661
In1	-0	-0.1	-0.199	-0.296	...	-0.6
In2	-1	-0.995	-0.98	-0.955	...	-0.6
Parameters						
A	[1x4]					
B	[1x4]					
Outputs						
Out1	0	-0.28	-0.44	-0.592	...	-0.898
Out2	0	-0.08	-0.206	-0.252	...	-0.432
Exp. Out1	0	-0.28	-0.44	-0.592	...	-0.898
Exp. Out2	0	-0.08	-0.206	-0.252	...	-0.432
Out1 (DSP)	0	-9175	-14424	-19405	...	-29414
Out2 (DSP)	0	-2621	-6737	-8259	...	-14158
Exp. Out1 (DSP)	0	-9175	-14422	-19402	...	-29410
Exp. Out2 (DSP)	0	-2621	-6736	-8258	...	-14155

Test settings	
Tolerance Out1	±2,4414e-04 (±8 LSB)
Tolerance Out2	±2,4414e-04 (±8 LSB)

Test statistics	
Min CPU cycles	168
Max CPU cycles	171
Avg CPU cycles	170

Test case: Conversion test OK

Conversion test for Control block TDSystemO2.

Test results			
Time step	1	2	3
Mask parameters			
A	[1x4]	[1x4]	[1x4]
B	[1x4]	[1x4]	[1x4]
Controller parameters			
a11	0	0	0
a22	30720	24576	9830
b21	20480	16384	6554
a21	20480	16384	6554
b12	20480	16384	3277
a12	20480	16384	3277
b11	0	0	0
b22	30720	24576	9830
sfrb12	11	14	15
sfra12	11	14	15
sfrb11	15	15	15
sfrb22	10	13	15
sfra11	15	15	15
sfra22	10	13	15
sfrb21	10	13	15
sfra21	10	13	15
Exp. a11	0	0	0
Exp. a22	30720	24576	9830
Exp. b21	20480	16384	6554
Exp. a21	20480	16384	6554
Exp. b12	20480	16384	3277
Exp. a12	20480	16384	3277
Exp. b11	0	0	0
Exp. b22	30720	24576	9830
Exp. sfrb12	11	14	15
Exp. sfra12	11	14	15
Exp. sfrb11	15	15	15
Exp. sfrb22	10	13	15
Exp. sfra11	15	15	15
Exp. sfra22	10	13	15
Exp. sfrb21	10	13	15
Exp. sfra21	10	13	15

Test settings	
Tolerance a11	±0,0000e+00
Tolerance a22	±0,0000e+00
Tolerance b21	±0,0000e+00
Tolerance a21	±0,0000e+00
Tolerance b12	±0,0000e+00
Tolerance a12	±0,0000e+00
Tolerance b11	±0,0000e+00
Tolerance b22	±0,0000e+00
Tolerance sfrb12	±0,0000e+00
Tolerance sfra12	±0,0000e+00
Tolerance sfrb11	±0,0000e+00
Tolerance sfrb22	±0,0000e+00
Tolerance sfra11	±0,0000e+00
Tolerance sfra22	±0,0000e+00
Tolerance sfrb21	±0,0000e+00
Tolerance sfra21	±0,0000e+00

Verification: TDSystemO2 FiP16 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for Control block TDSystemO2.

Test results						
Time step	1	2	3	4	...	174
CPU cycles	129	129	129	129	...	129
Inputs						
In1 (DSP)	0	-3271	-6510	-9684	...	-19661
In2 (DSP)	-32768	-32604	-32115	-31304	...	-19661
In1	-0	-0.1	-0.199	-0.296	...	-0.6
In2	-1	-0.995	-0.98	-0.955	...	-0.6
Parameters						
A	[1x4]					
B	[1x4]					
Outputs						
Out1	0	-0.28	-0.44	-0.592	...	-0.898
Out2	0	-0.08	-0.206	-0.252	...	-0.432
Exp. Out1	0	-0.28	-0.44	-0.592	...	-0.898
Exp. Out2	0	-0.08	-0.206	-0.252	...	-0.432
Out1 (DSP)	0	-9175	-14424	-19405	...	-29414
Out2 (DSP)	0	-2621	-6737	-8259	...	-14158
Exp. Out1 (DSP)	0	-9175	-14422	-19402	...	-29410
Exp. Out2 (DSP)	0	-2621	-6736	-8258	...	-14155

Test settings	
Tolerance Out1	±2,4414e-04 (±8 LSB)
Tolerance Out2	±2,4414e-04 (±8 LSB)

Test statistics	
Min CPU cycles	125
Max CPU cycles	129
Avg CPU cycles	128

Test case: Conversion test OK

Conversion test for Control block TDSystemO2.

Test results			
Time step	1	2	3
Mask parameters			
A	[1x4]	[1x4]	[1x4]
B	[1x4]	[1x4]	[1x4]
Controller parameters			
a11	0	0	0
a22	30720	24576	9830
b21	20480	16384	6554
a21	20480	16384	6554
b12	20480	16384	3277
a12	20480	16384	3277
b11	0	0	0
b22	30720	24576	9830
sfrb12	11	14	15
sfra12	11	14	15
sfrb11	15	15	15
sfrb22	10	13	15
sfra11	15	15	15
sfra22	10	13	15
sfrb21	10	13	15
sfra21	10	13	15
Exp. a11	0	0	0
Exp. a22	30720	24576	9830
Exp. b21	20480	16384	6554
Exp. a21	20480	16384	6554
Exp. b12	20480	16384	3277
Exp. a12	20480	16384	3277
Exp. b11	0	0	0
Exp. b22	30720	24576	9830
Exp. sfrb12	11	14	15
Exp. sfra12	11	14	15
Exp. sfrb11	15	15	15
Exp. sfrb22	10	13	15
Exp. sfra11	15	15	15
Exp. sfra22	10	13	15
Exp. sfrb21	10	13	15
Exp. sfra21	10	13	15

Test settings	
Tolerance a11	±0,0000e+00
Tolerance a22	±0,0000e+00
Tolerance b21	±0,0000e+00
Tolerance a21	±0,0000e+00
Tolerance b12	±0,0000e+00
Tolerance a12	±0,0000e+00
Tolerance b11	±0,0000e+00
Tolerance b22	±0,0000e+00
Tolerance sfrb12	±0,0000e+00
Tolerance sfra12	±0,0000e+00
Tolerance sfrb11	±0,0000e+00
Tolerance sfrb22	±0,0000e+00
Tolerance sfra11	±0,0000e+00
Tolerance sfra22	±0,0000e+00
Tolerance sfrb21	±0,0000e+00
Tolerance sfra21	±0,0000e+00

Verification: TDSystemO2 FiP16 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test

OK

Inport test for Control block TDSystemO2.

Test results						
Time step	1	2	3	4	...	174
CPU cycles	173	173	173	173	...	173
Inputs						
In1 (DSP)	0	-3271	-6510	-9684	...	-19661
In2 (DSP)	-32768	-32604	-32115	-31304	...	-19661
In1	-0	-0.1	-0.199	-0.296	...	-0.6
In2	-1	-0.995	-0.98	-0.955	...	-0.6
Parameters						
A	[1x4]					
B	[1x4]					
Outputs						
Out1	0	-0.28	-0.44	-0.592	...	-0.898
Out2	0	-0.08	-0.206	-0.252	...	-0.432
Exp. Out1	0	-0.28	-0.44	-0.592	...	-0.898
Exp. Out2	0	-0.08	-0.206	-0.252	...	-0.432
Out1 (DSP)	0	-9175	-14424	-19405	...	-29414
Out2 (DSP)	0	-2621	-6737	-8259	...	-14158
Exp. Out1 (DSP)	0	-9175	-14422	-19402	...	-29410
Exp. Out2 (DSP)	0	-2621	-6736	-8258	...	-14155

Test settings	
Tolerance Out1	±2,4414e-04 (±8 LSB)
Tolerance Out2	±2,4414e-04 (±8 LSB)

Test statistics	
Min CPU cycles	173
Max CPU cycles	173
Avg CPU cycles	173

Test case: Conversion test

OK

Conversion test for Control block TDSystemO2.

Test results			
Time step	1	2	3
Mask parameters			
A	[1x4]	[1x4]	[1x4]
B	[1x4]	[1x4]	[1x4]
Controller parameters			
a11	0	0	0
a22	30720	24576	9830
b21	20480	16384	6554
a21	20480	16384	6554
b12	20480	16384	3277
a12	20480	16384	3277
b11	0	0	0
b22	30720	24576	9830
sfrb12	11	14	15
sfra12	11	14	15
sfrb11	15	15	15
sfrb22	10	13	15
sfra11	15	15	15
sfra22	10	13	15
sfrb21	10	13	15
sfra21	10	13	15
Exp. a11	0	0	0
Exp. a22	30720	24576	9830
Exp. b21	20480	16384	6554
Exp. a21	20480	16384	6554
Exp. b12	20480	16384	3277
Exp. a12	20480	16384	3277
Exp. b11	0	0	0
Exp. b22	30720	24576	9830
Exp. sfrb12	11	14	15
Exp. sfra12	11	14	15
Exp. sfrb11	15	15	15
Exp. sfrb22	10	13	15
Exp. sfra11	15	15	15
Exp. sfra22	10	13	15
Exp. sfrb21	10	13	15
Exp. sfra21	10	13	15

Test settings	
Tolerance a11	±0,0000e+00
Tolerance a22	±0,0000e+00
Tolerance b21	±0,0000e+00
Tolerance a21	±0,0000e+00
Tolerance b12	±0,0000e+00
Tolerance a12	±0,0000e+00
Tolerance b11	±0,0000e+00
Tolerance b22	±0,0000e+00
Tolerance sfrb12	±0,0000e+00
Tolerance sfra12	±0,0000e+00
Tolerance sfrb11	±0,0000e+00
Tolerance sfrb22	±0,0000e+00
Tolerance sfra11	±0,0000e+00
Tolerance sfra22	±0,0000e+00
Tolerance sfrb21	±0,0000e+00
Tolerance sfra21	±0,0000e+00

Verification: TDSystemO2 FiP16 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for Control block TDSystemO2.

Test results						
Time step	1	2	3	4	...	174
CPU cycles	172	172	172	172	...	172
Inputs						
In1 (DSP)	0	-3271	-6510	-9684	...	-19661
In2 (DSP)	-32768	-32604	-32115	-31304	...	-19661
In1	-0	-0.1	-0.199	-0.296	...	-0.6
In2	-1	-0.995	-0.98	-0.955	...	-0.6
Parameters						
A	[1x4]					
B	[1x4]					
Outputs						
Out1	0	-0.28	-0.44	-0.592	...	-0.898
Out2	0	-0.08	-0.206	-0.252	...	-0.432
Exp. Out1	0	-0.28	-0.44	-0.592	...	-0.898
Exp. Out2	0	-0.08	-0.206	-0.252	...	-0.432
Out1 (DSP)	0	-9175	-14424	-19405	...	-29414
Out2 (DSP)	0	-2621	-6737	-8259	...	-14158
Exp. Out1 (DSP)	0	-9175	-14422	-19402	...	-29410
Exp. Out2 (DSP)	0	-2621	-6736	-8258	...	-14155

Test settings	
Tolerance Out1	±2,4414e-04 (±8 LSB)
Tolerance Out2	±2,4414e-04 (±8 LSB)

Test statistics	
Min CPU cycles	171
Max CPU cycles	232
Avg CPU cycles	172

Test case: Conversion test OK

Conversion test for Control block TDSystemO2.

Test results			
Time step	1	2	3
Mask parameters			
A	[1x4]	[1x4]	[1x4]
B	[1x4]	[1x4]	[1x4]
Controller parameters			
a11	0	0	0
a22	30720	24576	9830
b21	20480	16384	6554
a21	20480	16384	6554
b12	20480	16384	3277
a12	20480	16384	3277
b11	0	0	0
b22	30720	24576	9830
sfrb12	11	14	15
sfra12	11	14	15
sfrb11	15	15	15
sfrb22	10	13	15
sfra11	15	15	15
sfra22	10	13	15
sfrb21	10	13	15
sfra21	10	13	15
Exp. a11	0	0	0
Exp. a22	30720	24576	9830
Exp. b21	20480	16384	6554
Exp. a21	20480	16384	6554
Exp. b12	20480	16384	3277
Exp. a12	20480	16384	3277
Exp. b11	0	0	0
Exp. b22	30720	24576	9830
Exp. sfrb12	11	14	15
Exp. sfra12	11	14	15
Exp. sfrb11	15	15	15
Exp. sfrb22	10	13	15
Exp. sfra11	15	15	15
Exp. sfra22	10	13	15
Exp. sfrb21	10	13	15
Exp. sfra21	10	13	15

Test settings	
Tolerance a11	±0,0000e+00
Tolerance a22	±0,0000e+00
Tolerance b21	±0,0000e+00
Tolerance a21	±0,0000e+00
Tolerance b12	±0,0000e+00
Tolerance a12	±0,0000e+00
Tolerance b11	±0,0000e+00
Tolerance b22	±0,0000e+00
Tolerance sfrb12	±0,0000e+00
Tolerance sfra12	±0,0000e+00
Tolerance sfrb11	±0,0000e+00
Tolerance sfrb22	±0,0000e+00
Tolerance sfra11	±0,0000e+00
Tolerance sfra22	±0,0000e+00
Tolerance sfrb21	±0,0000e+00
Tolerance sfra21	±0,0000e+00

Verification: TDSystemO2 FiP16 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for Control block TDSystemO2.

Test results						
Time step	1	2	3	4	...	174
CPU cycles	143	143	143	143	...	143
Inputs						
In1 (DSP)	0	-3271	-6510	-9684	...	-19661
In2 (DSP)	-32768	-32604	-32115	-31304	...	-19661
In1	-0	-0.1	-0.199	-0.296	...	-0.6
In2	-1	-0.995	-0.98	-0.955	...	-0.6
Parameters						
A	[1x4]					
B	[1x4]					
Outputs						
Out1	0	-0.28	-0.44	-0.592	...	-0.898
Out2	0	-0.08	-0.206	-0.252	...	-0.432
Exp. Out1	0	-0.28	-0.44	-0.592	...	-0.898
Exp. Out2	0	-0.08	-0.206	-0.252	...	-0.432
Out1 (DSP)	0	-9175	-14424	-19405	...	-29414
Out2 (DSP)	0	-2621	-6737	-8259	...	-14158
Exp. Out1 (DSP)	0	-9175	-14422	-19402	...	-29410
Exp. Out2 (DSP)	0	-2621	-6736	-8258	...	-14155

Test settings	
Tolerance Out1	±2,4414e-04 (±8 LSB)
Tolerance Out2	±2,4414e-04 (±8 LSB)

Test statistics	
Min CPU cycles	143
Max CPU cycles	143
Avg CPU cycles	143

Test case: Conversion test OK

Conversion test for Control block TDSystemO2.

Test results			
Time step	1	2	3
Mask parameters			
A	[1x4]	[1x4]	[1x4]
B	[1x4]	[1x4]	[1x4]
Controller parameters			
a11	0	0	0
a22	30720	24576	9830
b21	20480	16384	6554
a21	20480	16384	6554
b12	20480	16384	3277
a12	20480	16384	3277
b11	0	0	0
b22	30720	24576	9830
sfrb12	11	14	15
sfra12	11	14	15
sfrb11	15	15	15
sfrb22	10	13	15
sfra11	15	15	15
sfra22	10	13	15
sfrb21	10	13	15
sfra21	10	13	15
Exp. a11	0	0	0
Exp. a22	30720	24576	9830
Exp. b21	20480	16384	6554
Exp. a21	20480	16384	6554
Exp. b12	20480	16384	3277
Exp. a12	20480	16384	3277
Exp. b11	0	0	0
Exp. b22	30720	24576	9830
Exp. sfrb12	11	14	15
Exp. sfra12	11	14	15
Exp. sfrb11	15	15	15
Exp. sfrb22	10	13	15
Exp. sfra11	15	15	15
Exp. sfra22	10	13	15
Exp. sfrb21	10	13	15
Exp. sfra21	10	13	15

Test settings	
Tolerance a11	±0,0000e+00
Tolerance a22	±0,0000e+00
Tolerance b21	±0,0000e+00
Tolerance a21	±0,0000e+00
Tolerance b12	±0,0000e+00
Tolerance a12	±0,0000e+00
Tolerance b11	±0,0000e+00
Tolerance b22	±0,0000e+00
Tolerance sfrb12	±0,0000e+00
Tolerance sfra12	±0,0000e+00
Tolerance sfrb11	±0,0000e+00
Tolerance sfrb22	±0,0000e+00
Tolerance sfra11	±0,0000e+00
Tolerance sfra22	±0,0000e+00
Tolerance sfrb21	±0,0000e+00
Tolerance sfra21	±0,0000e+00

Verification: TDSystemO2 FiP16 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test

OK

Inport test for Control block TDSystemO2.

Test results						
Time step	1	2	3	4	...	174
CPU cycles	195	161	161	161	...	161
Inputs						
In1 (DSP)	0	-3271	-6510	-9684	...	-19661
In2 (DSP)	-32768	-32604	-32115	-31304	...	-19661
In1	-0	-0.1	-0.199	-0.296	...	-0.6
In2	-1	-0.995	-0.98	-0.955	...	-0.6
Parameters						
A	[1x4]					
B	[1x4]					
Outputs						
Out1	0	-0.28	-0.44	-0.592	...	-0.898
Out2	0	-0.08	-0.206	-0.252	...	-0.432
Exp. Out1	0	-0.28	-0.44	-0.592	...	-0.898
Exp. Out2	0	-0.08	-0.206	-0.252	...	-0.432
Out1 (DSP)	0	-9175	-14424	-19405	...	-29414
Out2 (DSP)	0	-2621	-6737	-8259	...	-14158
Exp. Out1 (DSP)	0	-9175	-14422	-19402	...	-29410
Exp. Out2 (DSP)	0	-2621	-6736	-8258	...	-14155

Test settings	
Tolerance Out1	±2,4414e-04 (±8 LSB)
Tolerance Out2	±2,4414e-04 (±8 LSB)

Test statistics	
Min CPU cycles	161
Max CPU cycles	195
Avg CPU cycles	161

Test case: Conversion test

OK

Conversion test for Control block TDSystemO2.

Test results			
Time step	1	2	3
Mask parameters			
A	[1x4]	[1x4]	[1x4]
B	[1x4]	[1x4]	[1x4]
Controller parameters			
a11	0	0	0
a22	30720	24576	9830
b21	20480	16384	6554
a21	20480	16384	6554
b12	20480	16384	3277
a12	20480	16384	3277
b11	0	0	0
b22	30720	24576	9830
sfrb12	11	14	15
sfra12	11	14	15
sfrb11	15	15	15
sfrb22	10	13	15
sfra11	15	15	15
sfra22	10	13	15
sfrb21	10	13	15
sfra21	10	13	15
Exp. a11	0	0	0
Exp. a22	30720	24576	9830
Exp. b21	20480	16384	6554
Exp. a21	20480	16384	6554
Exp. b12	20480	16384	3277
Exp. a12	20480	16384	3277
Exp. b11	0	0	0
Exp. b22	30720	24576	9830
Exp. sfrb12	11	14	15
Exp. sfra12	11	14	15
Exp. sfrb11	15	15	15
Exp. sfrb22	10	13	15
Exp. sfra11	15	15	15
Exp. sfra22	10	13	15
Exp. sfrb21	10	13	15
Exp. sfra21	10	13	15

Test settings	
Tolerance a11	±0,0000e+00
Tolerance a22	±0,0000e+00
Tolerance b21	±0,0000e+00
Tolerance a21	±0,0000e+00
Tolerance b12	±0,0000e+00
Tolerance a12	±0,0000e+00
Tolerance b11	±0,0000e+00
Tolerance b22	±0,0000e+00
Tolerance sfrb12	±0,0000e+00
Tolerance sfra12	±0,0000e+00
Tolerance sfrb11	±0,0000e+00
Tolerance sfrb22	±0,0000e+00
Tolerance sfra11	±0,0000e+00
Tolerance sfra22	±0,0000e+00
Tolerance sfrb21	±0,0000e+00
Tolerance sfra21	±0,0000e+00

Verification: TDSystemO2 FiP16 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for Control block TDSystemO2.

Test results						
Time step	1	2	3	4	...	174
CPU cycles	165	165	165	165	...	165
Inputs						
In1 (DSP)	0	-3271	-6510	-9684	...	-19661
In2 (DSP)	-32768	-32604	-32115	-31304	...	-19661
In1	-0	-0.1	-0.199	-0.296	...	-0.6
In2	-1	-0.995	-0.98	-0.955	...	-0.6
Parameters						
A	[1x4]					
B	[1x4]					
Outputs						
Out1	0	-0.28	-0.44	-0.592	...	-0.898
Out2	0	-0.08	-0.206	-0.252	...	-0.432
Exp. Out1	0	-0.28	-0.44	-0.592	...	-0.898
Exp. Out2	0	-0.08	-0.206	-0.252	...	-0.432
Out1 (DSP)	0	-9175	-14424	-19405	...	-29414
Out2 (DSP)	0	-2621	-6737	-8259	...	-14158
Exp. Out1 (DSP)	0	-9175	-14422	-19402	...	-29410
Exp. Out2 (DSP)	0	-2621	-6736	-8258	...	-14155

Test settings	
Tolerance Out1	±2,4414e-04 (±8 LSB)
Tolerance Out2	±2,4414e-04 (±8 LSB)

Test statistics	
Min CPU cycles	165
Max CPU cycles	166
Avg CPU cycles	165

Test case: Conversion test OK

Conversion test for Control block TDSystemO2.

Test results			
Time step	1	2	3
Mask parameters			
A	[1x4]	[1x4]	[1x4]
B	[1x4]	[1x4]	[1x4]
Controller parameters			
a11	0	0	0
a22	30720	24576	9830
b21	20480	16384	6554
a21	20480	16384	6554
b12	20480	16384	3277
a12	20480	16384	3277
b11	0	0	0
b22	30720	24576	9830
sfrb12	11	14	15
sfra12	11	14	15
sfrb11	15	15	15
sfrb22	10	13	15
sfra11	15	15	15
sfra22	10	13	15
sfrb21	10	13	15
sfra21	10	13	15
Exp. a11	0	0	0
Exp. a22	30720	24576	9830
Exp. b21	20480	16384	6554
Exp. a21	20480	16384	6554
Exp. b12	20480	16384	3277
Exp. a12	20480	16384	3277
Exp. b11	0	0	0
Exp. b22	30720	24576	9830
Exp. sfrb12	11	14	15
Exp. sfra12	11	14	15
Exp. sfrb11	15	15	15
Exp. sfrb22	10	13	15
Exp. sfra11	15	15	15
Exp. sfra22	10	13	15
Exp. sfrb21	10	13	15
Exp. sfra21	10	13	15

Test settings	
Tolerance a11	±0,0000e+00
Tolerance a22	±0,0000e+00
Tolerance b21	±0,0000e+00
Tolerance a21	±0,0000e+00
Tolerance b12	±0,0000e+00
Tolerance a12	±0,0000e+00
Tolerance b11	±0,0000e+00
Tolerance b22	±0,0000e+00
Tolerance sfrb12	±0,0000e+00
Tolerance sfra12	±0,0000e+00
Tolerance sfrb11	±0,0000e+00
Tolerance sfrb22	±0,0000e+00
Tolerance sfra11	±0,0000e+00
Tolerance sfra22	±0,0000e+00
Tolerance sfrb21	±0,0000e+00
Tolerance sfra21	±0,0000e+00

Verification: TDSystemO2 FiP16 CPU dsPIC33EP256MC502

Date of Test	2026-06-23
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for Control block TDSystemO2.

Test results						
Time step	1	2	3	4	...	174
CPU cycles	203	203	203	203	...	203
Inputs						
In1 (DSP)	0	-3271	-6510	-9684	...	-19661
In2 (DSP)	-32768	-32604	-32115	-31304	...	-19661
In1	-0	-0.1	-0.199	-0.296	...	-0.6
In2	-1	-0.995	-0.98	-0.955	...	-0.6
Parameters						
A	[1x4]					
B	[1x4]					
Outputs						
Out1	0	-0.28	-0.44	-0.592	...	-0.898
Out2	0	-0.08	-0.206	-0.252	...	-0.432
Exp. Out1	0	-0.28	-0.44	-0.592	...	-0.898
Exp. Out2	0	-0.08	-0.206	-0.252	...	-0.432
Out1 (DSP)	0	-9175	-14424	-19405	...	-29414
Out2 (DSP)	0	-2621	-6737	-8259	...	-14158
Exp. Out1 (DSP)	0	-9175	-14422	-19402	...	-29410
Exp. Out2 (DSP)	0	-2621	-6736	-8258	...	-14155

Test settings	
Tolerance Out1	±2,4414e-04 (±8 LSB)
Tolerance Out2	±2,4414e-04 (±8 LSB)

Test statistics	
Min CPU cycles	202
Max CPU cycles	203
Avg CPU cycles	202

Test case: Conversion test OK

Conversion test for Control block TDSystemO2.

Test results			
Time step	1	2	3
Mask parameters			
A	[1x4]	[1x4]	[1x4]
B	[1x4]	[1x4]	[1x4]
Controller parameters			
a11	0	0	0
a22	30720	24576	9830
b21	20480	16384	6554
a21	20480	16384	6554
b12	20480	16384	3277
a12	20480	16384	3277
b11	0	0	0
b22	30720	24576	9830
sfrb12	11	14	15
sfra12	11	14	15
sfrb11	15	15	15
sfrb22	10	13	15
sfra11	15	15	15
sfra22	10	13	15
sfrb21	10	13	15
sfra21	10	13	15
Exp. a11	0	0	0
Exp. a22	30720	24576	9830
Exp. b21	20480	16384	6554
Exp. a21	20480	16384	6554
Exp. b12	20480	16384	3277
Exp. a12	20480	16384	3277
Exp. b11	0	0	0
Exp. b22	30720	24576	9830
Exp. sfrb12	11	14	15
Exp. sfra12	11	14	15
Exp. sfrb11	15	15	15
Exp. sfrb22	10	13	15
Exp. sfra11	15	15	15
Exp. sfra22	10	13	15
Exp. sfrb21	10	13	15
Exp. sfra21	10	13	15

Test settings	
Tolerance a11	±0,0000e+00
Tolerance a22	±0,0000e+00
Tolerance b21	±0,0000e+00
Tolerance a21	±0,0000e+00
Tolerance b12	±0,0000e+00
Tolerance a12	±0,0000e+00
Tolerance b11	±0,0000e+00
Tolerance b22	±0,0000e+00
Tolerance sfrb12	±0,0000e+00
Tolerance sfra12	±0,0000e+00
Tolerance sfrb11	±0,0000e+00
Tolerance sfrb22	±0,0000e+00
Tolerance sfra11	±0,0000e+00
Tolerance sfra22	±0,0000e+00
Tolerance sfrb21	±0,0000e+00
Tolerance sfra21	±0,0000e+00

Verification: TDSystemO2 FiP32 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for Control block TDSystemO2.

Test results				
Time step	1	2	...	174
CPU cycles	473	473	...	473
Inputs				
In1 (DSP)	0	-214390630	...	-1288490189
In2 (DSP)	-2147483648	-2136755175	...	-1288490189
In1	-0	-0.1	...	-0.6
In2	-1	-0.995	...	-0.6
Parameters				
A	[1x4]			
B	[1x4]			
Outputs				
Out1	0	-0.28	...	-0.898
Out2	0	-0.08	...	-0.432
Exp. Out1	0	-0.28	...	-0.898
Exp. Out2	0	-0.08	...	-0.432
Out1 (DSP)	0	-601295421	...	-1927381242
Out2 (DSP)	0	-171798692	...	-927641873
Exp. Out1 (DSP)	0	-601295421	...	-1927381237
Exp. Out2 (DSP)	0	-171798692	...	-927641869

Test settings	
Tolerance Out1	±3,7253e-09 (±8 LSB)
Tolerance Out2	±3,7253e-09 (±8 LSB)

Test statistics	
Min CPU cycles	411
Max CPU cycles	477
Avg CPU cycles	460

Test case: Conversion test OK

Conversion test for Control block TDSystemO2.

Test results			
Time step	1	2	3
Mask parameters			
A	[1x4]	[1x4]	[1x4]
B	[1x4]	[1x4]	[1x4]
Controller parameters			
a11	0	0	0
a22	2013265920	1610612736	644245094
b21	1342177280	1073741824	429496730
a21	1342177280	1073741824	429496730
b12	1342177280	1073741824	214748365
a12	1342177280	1073741824	214748365
b11	0	0	0
b22	2013265920	1610612736	644245094
sfrb12	27	30	31
sfra12	27	30	31
sfrb11	31	31	31
sfrb22	26	29	31
sfra11	31	31	31
sfra22	26	29	31
sfrb21	26	29	31
sfra21	26	29	31
Exp. a11	0	0	0
Exp. a22	2013265920	1610612736	644245094
Exp. b21	1342177280	1073741824	429496730
Exp. a21	1342177280	1073741824	429496730
Exp. b12	1342177280	1073741824	214748365
Exp. a12	1342177280	1073741824	214748365
Exp. b11	0	0	0
Exp. b22	2013265920	1610612736	644245094
Exp. sfrb12	27	30	31
Exp. sfra12	27	30	31
Exp. sfrb11	31	31	31
Exp. sfrb22	26	29	31
Exp. sfra11	31	31	31
Exp. sfra22	26	29	31
Exp. sfrb21	26	29	31
Exp. sfra21	26	29	31

Test settings	
Tolerance a11	±0,0000e+00
Tolerance a22	±0,0000e+00
Tolerance b21	±0,0000e+00
Tolerance a21	±0,0000e+00
Tolerance b12	±0,0000e+00
Tolerance a12	±0,0000e+00
Tolerance b11	±0,0000e+00
Tolerance b22	±0,0000e+00
Tolerance sfrb12	±0,0000e+00
Tolerance sfra12	±0,0000e+00
Tolerance sfrb11	±0,0000e+00
Tolerance sfrb22	±0,0000e+00
Tolerance sfra11	±0,0000e+00
Tolerance sfra22	±0,0000e+00
Tolerance sfrb21	±0,0000e+00
Tolerance sfra21	±0,0000e+00

Verification: TDSystemO2 FiP32 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for Control block TDSystemO2.

Test results				
Time step	1	2	...	174
CPU cycles	351	351	...	351
Inputs				
In1 (DSP)	0	-214390630	...	-1288490189
In2 (DSP)	-2147483648	-2136755175	...	-1288490189
In1	-0	-0.1	...	-0.6
In2	-1	-0.995	...	-0.6
Parameters				
A	[1x4]			
B	[1x4]			
Outputs				
Out1	0	-0.28	...	-0.898
Out2	0	-0.08	...	-0.432
Exp. Out1	0	-0.28	...	-0.898
Exp. Out2	0	-0.08	...	-0.432
Out1 (DSP)	0	-601295421	...	-1927381242
Out2 (DSP)	0	-171798692	...	-927641873
Exp. Out1 (DSP)	0	-601295421	...	-1927381237
Exp. Out2 (DSP)	0	-171798692	...	-927641869

Test settings	
Tolerance Out1	±3,7253e-09 (±8 LSB)
Tolerance Out2	±3,7253e-09 (±8 LSB)

Test statistics	
Min CPU cycles	345
Max CPU cycles	355
Avg CPU cycles	349

Test case: Conversion test OK

Conversion test for Control block TDSystemO2.

Test results			
Time step	1	2	3
Mask parameters			
A	[1x4]	[1x4]	[1x4]
B	[1x4]	[1x4]	[1x4]
Controller parameters			
a11	0	0	0
a22	2013265920	1610612736	644245094
b21	1342177280	1073741824	429496730
a21	1342177280	1073741824	429496730
b12	1342177280	1073741824	214748365
a12	1342177280	1073741824	214748365
b11	0	0	0
b22	2013265920	1610612736	644245094
sfrb12	27	30	31
sfra12	27	30	31
sfrb11	31	31	31
sfrb22	26	29	31
sfra11	31	31	31
sfra22	26	29	31
sfrb21	26	29	31
sfra21	26	29	31
Exp. a11	0	0	0
Exp. a22	2013265920	1610612736	644245094
Exp. b21	1342177280	1073741824	429496730
Exp. a21	1342177280	1073741824	429496730
Exp. b12	1342177280	1073741824	214748365
Exp. a12	1342177280	1073741824	214748365
Exp. b11	0	0	0
Exp. b22	2013265920	1610612736	644245094
Exp. sfrb12	27	30	31
Exp. sfra12	27	30	31
Exp. sfrb11	31	31	31
Exp. sfrb22	26	29	31
Exp. sfra11	31	31	31
Exp. sfra22	26	29	31
Exp. sfrb21	26	29	31
Exp. sfra21	26	29	31

Test settings	
Tolerance a11	±0,0000e+00
Tolerance a22	±0,0000e+00
Tolerance b21	±0,0000e+00
Tolerance a21	±0,0000e+00
Tolerance b12	±0,0000e+00
Tolerance a12	±0,0000e+00
Tolerance b11	±0,0000e+00
Tolerance b22	±0,0000e+00
Tolerance sfrb12	±0,0000e+00
Tolerance sfra12	±0,0000e+00
Tolerance sfrb11	±0,0000e+00
Tolerance sfrb22	±0,0000e+00
Tolerance sfra11	±0,0000e+00
Tolerance sfra22	±0,0000e+00
Tolerance sfrb21	±0,0000e+00
Tolerance sfra21	±0,0000e+00

Verification: TDSystemO2 FiP32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for Control block TDSystemO2.

Test results				
Time step	1	2	...	174
CPU cycles	341	341	...	341
Inputs				
In1 (DSP)	0	-214390630	...	-1288490189
In2 (DSP)	-2147483648	-2136755175	...	-1288490189
In1	-0	-0.1	...	-0.6
In2	-1	-0.995	...	-0.6
Parameters				
A	[1x4]			
B	[1x4]			
Outputs				
Out1	0	-0.28	...	-0.898
Out2	0	-0.08	...	-0.432
Exp. Out1	0	-0.28	...	-0.898
Exp. Out2	0	-0.08	...	-0.432
Out1 (DSP)	0	-601295421	...	-1927381242
Out2 (DSP)	0	-171798692	...	-927641873
Exp. Out1 (DSP)	0	-601295421	...	-1927381237
Exp. Out2 (DSP)	0	-171798692	...	-927641869

Test settings	
Tolerance Out1	±3,7253e-09 (±8 LSB)
Tolerance Out2	±3,7253e-09 (±8 LSB)

Test statistics	
Min CPU cycles	341
Max CPU cycles	341
Avg CPU cycles	341

Test case: Conversion test OK

Conversion test for Control block TDSystemO2.

Test results			
Time step	1	2	3
Mask parameters			
A	[1x4]	[1x4]	[1x4]
B	[1x4]	[1x4]	[1x4]
Controller parameters			
a11	0	0	0
a22	2013265920	1610612736	644245094
b21	1342177280	1073741824	429496730
a21	1342177280	1073741824	429496730
b12	1342177280	1073741824	214748365
a12	1342177280	1073741824	214748365
b11	0	0	0
b22	2013265920	1610612736	644245094
sfrb12	27	30	31
sfra12	27	30	31
sfrb11	31	31	31
sfrb22	26	29	31
sfra11	31	31	31
sfra22	26	29	31
sfrb21	26	29	31
sfra21	26	29	31
Exp. a11	0	0	0
Exp. a22	2013265920	1610612736	644245094
Exp. b21	1342177280	1073741824	429496730
Exp. a21	1342177280	1073741824	429496730
Exp. b12	1342177280	1073741824	214748365
Exp. a12	1342177280	1073741824	214748365
Exp. b11	0	0	0
Exp. b22	2013265920	1610612736	644245094
Exp. sfrb12	27	30	31
Exp. sfra12	27	30	31
Exp. sfrb11	31	31	31
Exp. sfrb22	26	29	31
Exp. sfra11	31	31	31
Exp. sfra22	26	29	31
Exp. sfrb21	26	29	31
Exp. sfra21	26	29	31

Test settings	
Tolerance a11	±0,0000e+00
Tolerance a22	±0,0000e+00
Tolerance b21	±0,0000e+00
Tolerance a21	±0,0000e+00
Tolerance b12	±0,0000e+00
Tolerance a12	±0,0000e+00
Tolerance b11	±0,0000e+00
Tolerance b22	±0,0000e+00
Tolerance sfrb12	±0,0000e+00
Tolerance sfra12	±0,0000e+00
Tolerance sfrb11	±0,0000e+00
Tolerance sfrb22	±0,0000e+00
Tolerance sfra11	±0,0000e+00
Tolerance sfra22	±0,0000e+00
Tolerance sfrb21	±0,0000e+00
Tolerance sfra21	±0,0000e+00

Verification: TDSystemO2 FiP32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test

OK

Inport test for Control block TDSystemO2.

Test results				
Time step	1	2	...	174
CPU cycles	997	998	...	997
Inputs				
In1 (DSP)	0	-214390630	...	-1288490189
In2 (DSP)	-2147483648	-2136755175	...	-1288490189
In1	-0	-0.1	...	-0.6
In2	-1	-0.995	...	-0.6
Parameters				
A	[1x4]			
B	[1x4]			
Outputs				
Out1	0	-0.28	...	-0.898
Out2	0	-0.08	...	-0.432
Exp. Out1	0	-0.28	...	-0.898
Exp. Out2	0	-0.08	...	-0.432
Out1 (DSP)	0	-601295421	...	-1927381242
Out2 (DSP)	0	-171798692	...	-927641873
Exp. Out1 (DSP)	0	-601295421	...	-1927381237
Exp. Out2 (DSP)	0	-171798692	...	-927641869

Test settings	
Tolerance Out1	±3,7253e-09 (±8 LSB)
Tolerance Out2	±3,7253e-09 (±8 LSB)

Test statistics	
Min CPU cycles	986
Max CPU cycles	1057
Avg CPU cycles	994

Test case: Conversion test

OK

Conversion test for Control block TDSystemO2.

Test results			
Time step	1	2	3
Mask parameters			
A	[1x4]	[1x4]	[1x4]
B	[1x4]	[1x4]	[1x4]
Controller parameters			
a11	0	0	0
a22	2013265920	1610612736	644245094
b21	1342177280	1073741824	429496730
a21	1342177280	1073741824	429496730
b12	1342177280	1073741824	214748365
a12	1342177280	1073741824	214748365
b11	0	0	0
b22	2013265920	1610612736	644245094
sfrb12	27	30	31
sfra12	27	30	31
sfrb11	31	31	31
sfrb22	26	29	31
sfra11	31	31	31
sfra22	26	29	31
sfrb21	26	29	31
sfra21	26	29	31
Exp. a11	0	0	0
Exp. a22	2013265920	1610612736	644245094
Exp. b21	1342177280	1073741824	429496730
Exp. a21	1342177280	1073741824	429496730
Exp. b12	1342177280	1073741824	214748365
Exp. a12	1342177280	1073741824	214748365
Exp. b11	0	0	0
Exp. b22	2013265920	1610612736	644245094
Exp. sfrb12	27	30	31
Exp. sfra12	27	30	31
Exp. sfrb11	31	31	31
Exp. sfrb22	26	29	31
Exp. sfra11	31	31	31
Exp. sfra22	26	29	31
Exp. sfrb21	26	29	31
Exp. sfra21	26	29	31

Test settings	
Tolerance a11	±0,0000e+00
Tolerance a22	±0,0000e+00
Tolerance b21	±0,0000e+00
Tolerance a21	±0,0000e+00
Tolerance b12	±0,0000e+00
Tolerance a12	±0,0000e+00
Tolerance b11	±0,0000e+00
Tolerance b22	±0,0000e+00
Tolerance sfrb12	±0,0000e+00
Tolerance sfra12	±0,0000e+00
Tolerance sfrb11	±0,0000e+00
Tolerance sfrb22	±0,0000e+00
Tolerance sfra11	±0,0000e+00
Tolerance sfra22	±0,0000e+00
Tolerance sfrb21	±0,0000e+00
Tolerance sfra21	±0,0000e+00

Verification: TDSystemO2 FiP32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for Control block TDSystemO2.

Test results				
Time step	1	2	...	174
CPU cycles	274	274	...	274
Inputs				
In1 (DSP)	0	-214390630	...	-1288490189
In2 (DSP)	-2147483648	-2136755175	...	-1288490189
In1	-0	-0.1	...	-0.6
In2	-1	-0.995	...	-0.6
Parameters				
A	[1x4]			
B	[1x4]			
Outputs				
Out1	0	-0.28	...	-0.898
Out2	0	-0.08	...	-0.432
Exp. Out1	0	-0.28	...	-0.898
Exp. Out2	0	-0.08	...	-0.432
Out1 (DSP)	0	-601295421	...	-1927381242
Out2 (DSP)	0	-171798692	...	-927641873
Exp. Out1 (DSP)	0	-601295421	...	-1927381237
Exp. Out2 (DSP)	0	-171798692	...	-927641869

Test settings	
Tolerance Out1	±3,7253e-09 (±8 LSB)
Tolerance Out2	±3,7253e-09 (±8 LSB)

Test statistics	
Min CPU cycles	274
Max CPU cycles	280
Avg CPU cycles	275

Test case: Conversion test OK

Conversion test for Control block TDSystemO2.

Test results			
Time step	1	2	3
Mask parameters			
A	[1x4]	[1x4]	[1x4]
B	[1x4]	[1x4]	[1x4]
Controller parameters			
a11	0	0	0
a22	2013265920	1610612736	644245094
b21	1342177280	1073741824	429496730
a21	1342177280	1073741824	429496730
b12	1342177280	1073741824	214748365
a12	1342177280	1073741824	214748365
b11	0	0	0
b22	2013265920	1610612736	644245094
sfrb12	27	30	31
sfra12	27	30	31
sfrb11	31	31	31
sfrb22	26	29	31
sfra11	31	31	31
sfra22	26	29	31
sfrb21	26	29	31
sfra21	26	29	31
Exp. a11	0	0	0
Exp. a22	2013265920	1610612736	644245094
Exp. b21	1342177280	1073741824	429496730
Exp. a21	1342177280	1073741824	429496730
Exp. b12	1342177280	1073741824	214748365
Exp. a12	1342177280	1073741824	214748365
Exp. b11	0	0	0
Exp. b22	2013265920	1610612736	644245094
Exp. sfrb12	27	30	31
Exp. sfra12	27	30	31
Exp. sfrb11	31	31	31
Exp. sfrb22	26	29	31
Exp. sfra11	31	31	31
Exp. sfra22	26	29	31
Exp. sfrb21	26	29	31
Exp. sfra21	26	29	31

Test settings	
Tolerance a11	±0,0000e+00
Tolerance a22	±0,0000e+00
Tolerance b21	±0,0000e+00
Tolerance a21	±0,0000e+00
Tolerance b12	±0,0000e+00
Tolerance a12	±0,0000e+00
Tolerance b11	±0,0000e+00
Tolerance b22	±0,0000e+00
Tolerance sfrb12	±0,0000e+00
Tolerance sfra12	±0,0000e+00
Tolerance sfrb11	±0,0000e+00
Tolerance sfrb22	±0,0000e+00
Tolerance sfra11	±0,0000e+00
Tolerance sfra22	±0,0000e+00
Tolerance sfrb21	±0,0000e+00
Tolerance sfra21	±0,0000e+00

Verification: TDSystemO2 FiP32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test

OK

Inport test for Control block TDSystemO2.

Test results				
Time step	1	2	...	174
CPU cycles	364	289	...	289
Inputs				
In1 (DSP)	0	-214390630	...	-1288490189
In2 (DSP)	-2147483648	-2136755175	...	-1288490189
In1	-0	-0.1	...	-0.6
In2	-1	-0.995	...	-0.6
Parameters				
A	[1x4]			
B	[1x4]			
Outputs				
Out1	0	-0.28	...	-0.898
Out2	0	-0.08	...	-0.432
Exp. Out1	0	-0.28	...	-0.898
Exp. Out2	0	-0.08	...	-0.432
Out1 (DSP)	0	-601295421	...	-1927381242
Out2 (DSP)	0	-171798692	...	-927641873
Exp. Out1 (DSP)	0	-601295421	...	-1927381237
Exp. Out2 (DSP)	0	-171798692	...	-927641869

Test settings	
Tolerance Out1	±3,7253e-09 (±8 LSB)
Tolerance Out2	±3,7253e-09 (±8 LSB)

Test statistics	
Min CPU cycles	289
Max CPU cycles	364
Avg CPU cycles	289

Test case: Conversion test

OK

Conversion test for Control block TDSystemO2.

Test results			
Time step	1	2	3
Mask parameters			
A	[1x4]	[1x4]	[1x4]
B	[1x4]	[1x4]	[1x4]
Controller parameters			
a11	0	0	0
a22	2013265920	1610612736	644245094
b21	1342177280	1073741824	429496730
a21	1342177280	1073741824	429496730
b12	1342177280	1073741824	214748365
a12	1342177280	1073741824	214748365
b11	0	0	0
b22	2013265920	1610612736	644245094
sfrb12	27	30	31
sfra12	27	30	31
sfrb11	31	31	31
sfrb22	26	29	31
sfra11	31	31	31
sfra22	26	29	31
sfrb21	26	29	31
sfra21	26	29	31
Exp. a11	0	0	0
Exp. a22	2013265920	1610612736	644245094
Exp. b21	1342177280	1073741824	429496730
Exp. a21	1342177280	1073741824	429496730
Exp. b12	1342177280	1073741824	214748365
Exp. a12	1342177280	1073741824	214748365
Exp. b11	0	0	0
Exp. b22	2013265920	1610612736	644245094
Exp. sfrb12	27	30	31
Exp. sfra12	27	30	31
Exp. sfrb11	31	31	31
Exp. sfrb22	26	29	31
Exp. sfra11	31	31	31
Exp. sfra22	26	29	31
Exp. sfrb21	26	29	31
Exp. sfra21	26	29	31

Test settings	
Tolerance a11	±0,0000e+00
Tolerance a22	±0,0000e+00
Tolerance b21	±0,0000e+00
Tolerance a21	±0,0000e+00
Tolerance b12	±0,0000e+00
Tolerance a12	±0,0000e+00
Tolerance b11	±0,0000e+00
Tolerance b22	±0,0000e+00
Tolerance sfrb12	±0,0000e+00
Tolerance sfra12	±0,0000e+00
Tolerance sfrb11	±0,0000e+00
Tolerance sfrb22	±0,0000e+00
Tolerance sfra11	±0,0000e+00
Tolerance sfra22	±0,0000e+00
Tolerance sfrb21	±0,0000e+00
Tolerance sfra21	±0,0000e+00

Verification: TDSystemO2 FiP32 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for Control block TDSystemO2.

Test results				
Time step	1	2	...	174
CPU cycles	417	417	...	417
Inputs				
In1 (DSP)	0	-214390630	...	-1288490189
In2 (DSP)	-2147483648	-2136755175	...	-1288490189
In1	-0	-0.1	...	-0.6
In2	-1	-0.995	...	-0.6
Parameters				
A	[1x4]			
B	[1x4]			
Outputs				
Out1	0	-0.28	...	-0.898
Out2	0	-0.08	...	-0.432
Exp. Out1	0	-0.28	...	-0.898
Exp. Out2	0	-0.08	...	-0.432
Out1 (DSP)	0	-601295421	...	-1927381242
Out2 (DSP)	0	-171798692	...	-927641873
Exp. Out1 (DSP)	0	-601295421	...	-1927381237
Exp. Out2 (DSP)	0	-171798692	...	-927641869

Test settings	
Tolerance Out1	±3,7253e-09 (±8 LSB)
Tolerance Out2	±3,7253e-09 (±8 LSB)

Test statistics	
Min CPU cycles	368
Max CPU cycles	422
Avg CPU cycles	407

Test case: Conversion test OK

Conversion test for Control block TDSystemO2.

Test results			
Time step	1	2	3
Mask parameters			
A	[1x4]	[1x4]	[1x4]
B	[1x4]	[1x4]	[1x4]
Controller parameters			
a11	0	0	0
a22	2013265920	1610612736	644245094
b21	1342177280	1073741824	429496730
a21	1342177280	1073741824	429496730
b12	1342177280	1073741824	214748365
a12	1342177280	1073741824	214748365
b11	0	0	0
b22	2013265920	1610612736	644245094
sfrb12	27	30	31
sfra12	27	30	31
sfrb11	31	31	31
sfrb22	26	29	31
sfra11	31	31	31
sfra22	26	29	31
sfrb21	26	29	31
sfra21	26	29	31
Exp. a11	0	0	0
Exp. a22	2013265920	1610612736	644245094
Exp. b21	1342177280	1073741824	429496730
Exp. a21	1342177280	1073741824	429496730
Exp. b12	1342177280	1073741824	214748365
Exp. a12	1342177280	1073741824	214748365
Exp. b11	0	0	0
Exp. b22	2013265920	1610612736	644245094
Exp. sfrb12	27	30	31
Exp. sfra12	27	30	31
Exp. sfrb11	31	31	31
Exp. sfrb22	26	29	31
Exp. sfra11	31	31	31
Exp. sfra22	26	29	31
Exp. sfrb21	26	29	31
Exp. sfra21	26	29	31

Test settings	
Tolerance a11	±0,0000e+00
Tolerance a22	±0,0000e+00
Tolerance b21	±0,0000e+00
Tolerance a21	±0,0000e+00
Tolerance b12	±0,0000e+00
Tolerance a12	±0,0000e+00
Tolerance b11	±0,0000e+00
Tolerance b22	±0,0000e+00
Tolerance sfrb12	±0,0000e+00
Tolerance sfra12	±0,0000e+00
Tolerance sfrb11	±0,0000e+00
Tolerance sfrb22	±0,0000e+00
Tolerance sfra11	±0,0000e+00
Tolerance sfra22	±0,0000e+00
Tolerance sfrb21	±0,0000e+00
Tolerance sfra21	±0,0000e+00

Verification: TDSystemO2 FiP32 CPU dsPIC33EP256MC502

Date of Test	2026-06-23
Target controller	dsPIC33EP256MC502

Test case: Inport test

OK

Inport test for Control block TDSystemO2.

Test results				
Time step	1	2	...	174
CPU cycles	3572	3608	...	3608
Inputs				
In1 (DSP)	0	-214390630	...	-1288490189
In2 (DSP)	-2147483648	-2136755175	...	-1288490189
In1	-0	-0.1	...	-0.6
In2	-1	-0.995	...	-0.6
Parameters				
A	[1x4]			
B	[1x4]			
Outputs				
Out1	0	-0.28	...	-0.898
Out2	0	-0.08	...	-0.432
Exp. Out1	0	-0.28	...	-0.898
Exp. Out2	0	-0.08	...	-0.432
Out1 (DSP)	0	-601295421	...	-1927381242
Out2 (DSP)	0	-171798692	...	-927641873
Exp. Out1 (DSP)	0	-601295421	...	-1927381237
Exp. Out2 (DSP)	0	-171798692	...	-927641869

Test settings	
Tolerance Out1	±3,7253e-09 (±8 LSB)
Tolerance Out2	±3,7253e-09 (±8 LSB)

Test statistics	
Min CPU cycles	3558
Max CPU cycles	3609
Avg CPU cycles	3585

Test case: Conversion test

OK

Conversion test for Control block TDSystemO2.

Test results			
Time step	1	2	3
Mask parameters			
A	[1x4]	[1x4]	[1x4]
B	[1x4]	[1x4]	[1x4]
Controller parameters			
a11	0	0	0
a22	2013265920	1610612736	644245094
b21	1342177280	1073741824	429496730
a21	1342177280	1073741824	429496730
b12	1342177280	1073741824	214748365
a12	1342177280	1073741824	214748365
b11	0	0	0
b22	2013265920	1610612736	644245094
sfrb12	27	30	31
sfra12	27	30	31
sfrb11	31	31	31
sfrb22	26	29	31
sfra11	31	31	31
sfra22	26	29	31
sfrb21	26	29	31
sfra21	26	29	31
Exp. a11	0	0	0
Exp. a22	2013265920	1610612736	644245094
Exp. b21	1342177280	1073741824	429496730
Exp. a21	1342177280	1073741824	429496730
Exp. b12	1342177280	1073741824	214748365
Exp. a12	1342177280	1073741824	214748365
Exp. b11	0	0	0
Exp. b22	2013265920	1610612736	644245094
Exp. sfrb12	27	30	31
Exp. sfra12	27	30	31
Exp. sfrb11	31	31	31
Exp. sfrb22	26	29	31
Exp. sfra11	31	31	31
Exp. sfra22	26	29	31
Exp. sfrb21	26	29	31
Exp. sfra21	26	29	31

Test settings	
Tolerance a11	±0,0000e+00
Tolerance a22	±0,0000e+00
Tolerance b21	±0,0000e+00
Tolerance a21	±0,0000e+00
Tolerance b12	±0,0000e+00
Tolerance a12	±0,0000e+00
Tolerance b11	±0,0000e+00
Tolerance b22	±0,0000e+00
Tolerance sfrb12	±0,0000e+00
Tolerance sfra12	±0,0000e+00
Tolerance sfrb11	±0,0000e+00
Tolerance sfrb22	±0,0000e+00
Tolerance sfra11	±0,0000e+00
Tolerance sfra22	±0,0000e+00
Tolerance sfrb21	±0,0000e+00
Tolerance sfra21	±0,0000e+00

Verification: TDSystemO2 Float32 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for Control block TDSystemO2.

Test results				
Time step	1	2	...	174
CPU cycles	102	102	...	102
Inputs				
In1 (DSP)	-0	-0.1	...	-0.6
In2 (DSP)	-1	-0.995	...	-0.6
In1	-0	-0.1	...	-0.6
In2	-1	-0.995	...	-0.6
Parameters				
A	[1x4]			
B	[1x4]			
Outputs				
Out1	0	-0.28	...	-0.898
Out2	0	-0.08	...	-0.432
Exp. Out1	0	-0.28	...	-0.898
Exp. Out2	0	-0.08	...	-0.432
Out1 (DSP)	0	-0.28	...	-0.898
Out2 (DSP)	0	-0.08	...	-0.432
Exp. Out1 (DSP)	0	-0.28	...	-0.898
Exp. Out2 (DSP)	0	-0.08	...	-0.432

Test settings	
Tolerance Out1	±2,3283e-07 (±500 LSB)
Tolerance Out2	±2,3283e-07 (±500 LSB)

Test statistics	
Min CPU cycles	102
Max CPU cycles	102
Avg CPU cycles	102

Test case: Conversion test OK

Conversion test for Control block TDSystemO2.

Test results			
Time step	1	2	3
Mask parameters			
A	[1x4]	[1x4]	[1x4]
B	[1x4]	[1x4]	[1x4]
Controller parameters			
a11	0	0	0
a22	30	3	0.3
b21	20	2	0.2
a21	20	2	0.2
b12	10	1	0.1
a12	10	1	0.1
b11	0	0	0
b22	30	3	0.3
Exp. a11	0	0	0
Exp. a22	30	3	0.3
Exp. b21	20	2	0.2
Exp. a21	20	2	0.2
Exp. b12	10	1	0.1
Exp. a12	10	1	0.1
Exp. b11	0	0	0
Exp. b22	30	3	0.3

Test settings	
Tolerance a11	±0,0000e+00
Tolerance a22	±0,0000e+00
Tolerance b21	±0,0000e+00
Tolerance a21	±0,0000e+00
Tolerance b12	±0,0000e+00
Tolerance a12	±0,0000e+00
Tolerance b11	±0,0000e+00
Tolerance b22	±0,0000e+00

Verification: TDSystemO2 Float32 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for Control block TDSystemO2.

Test results				
Time step	1	2	...	174
CPU cycles	71	71	...	71
Inputs				
In1 (DSP)	-0	-0.1	...	-0.6
In2 (DSP)	-1	-0.995	...	-0.6
In1	-0	-0.1	...	-0.6
In2	-1	-0.995	...	-0.6
Parameters				
A	[1x4]			
B	[1x4]			
Outputs				
Out1	0	-0.28	...	-0.898
Out2	0	-0.08	...	-0.432
Exp. Out1	0	-0.28	...	-0.898
Exp. Out2	0	-0.08	...	-0.432
Out1 (DSP)	0	-0.28	...	-0.898
Out2 (DSP)	0	-0.08	...	-0.432
Exp. Out1 (DSP)	0	-0.28	...	-0.898
Exp. Out2 (DSP)	0	-0.08	...	-0.432

Test settings	
Tolerance Out1	±2,3283e-07 (±500 LSB)
Tolerance Out2	±2,3283e-07 (±500 LSB)

Test statistics	
Min CPU cycles	71
Max CPU cycles	71
Avg CPU cycles	71

Test case: Conversion test OK

Conversion test for Control block TDSystemO2.

Test results			
Time step	1	2	3
Mask parameters			
A	[1x4]	[1x4]	[1x4]
B	[1x4]	[1x4]	[1x4]
Controller parameters			
a11	0	0	0
a22	30	3	0.3
b21	20	2	0.2
a21	20	2	0.2
b12	10	1	0.1
a12	10	1	0.1
b11	0	0	0
b22	30	3	0.3
Exp. a11	0	0	0
Exp. a22	30	3	0.3
Exp. b21	20	2	0.2
Exp. a21	20	2	0.2
Exp. b12	10	1	0.1
Exp. a12	10	1	0.1
Exp. b11	0	0	0
Exp. b22	30	3	0.3

Test settings	
Tolerance a11	±0,0000e+00
Tolerance a22	±0,0000e+00
Tolerance b21	±0,0000e+00
Tolerance a21	±0,0000e+00
Tolerance b12	±0,0000e+00
Tolerance a12	±0,0000e+00
Tolerance b11	±0,0000e+00
Tolerance b22	±0,0000e+00

Verification: TDSystemO2 Float32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test

OK

Inport test for Control block TDSystemO2.

Test results				
Time step	1	2	...	174
CPU cycles	113	113	...	113
Inputs				
In1 (DSP)	-0	-0.1	...	-0.6
In2 (DSP)	-1	-0.995	...	-0.6
In1	-0	-0.1	...	-0.6
In2	-1	-0.995	...	-0.6
Parameters				
A	[1x4]			
B	[1x4]			
Outputs				
Out1	0	-0.28	...	-0.898
Out2	0	-0.08	...	-0.432
Exp. Out1	0	-0.28	...	-0.898
Exp. Out2	0	-0.08	...	-0.432
Out1 (DSP)	0	-0.28	...	-0.898
Out2 (DSP)	0	-0.08	...	-0.432
Exp. Out1 (DSP)	0	-0.28	...	-0.898
Exp. Out2 (DSP)	0	-0.08	...	-0.432

Test settings	
Tolerance Out1	±2,3283e-07 (±500 LSB)
Tolerance Out2	±2,3283e-07 (±500 LSB)

Test statistics	
Min CPU cycles	113
Max CPU cycles	113
Avg CPU cycles	113

Test case: Conversion test

OK

Conversion test for Control block TDSystemO2.

Test results			
Time step	1	2	3
Mask parameters			
A	[1x4]	[1x4]	[1x4]
B	[1x4]	[1x4]	[1x4]
Controller parameters			
a11	0	0	0
a22	30	3	0.3
b21	20	2	0.2
a21	20	2	0.2
b12	10	1	0.1
a12	10	1	0.1
b11	0	0	0
b22	30	3	0.3
Exp. a11	0	0	0
Exp. a22	30	3	0.3
Exp. b21	20	2	0.2
Exp. a21	20	2	0.2
Exp. b12	10	1	0.1
Exp. a12	10	1	0.1
Exp. b11	0	0	0
Exp. b22	30	3	0.3

Test settings	
Tolerance a11	±0,0000e+00
Tolerance a22	±0,0000e+00
Tolerance b21	±0,0000e+00
Tolerance a21	±0,0000e+00
Tolerance b12	±0,0000e+00
Tolerance a12	±0,0000e+00
Tolerance b11	±0,0000e+00
Tolerance b22	±0,0000e+00

Verification: TDSystemO2 Float32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for Control block TDSystemO2.

Test results				
Time step	1	2	...	174
CPU cycles	1821	2339	...	2302
Inputs				
In1 (DSP)	-0	-0.1	...	-0.6
In2 (DSP)	-1	-0.995	...	-0.6
In1	-0	-0.1	...	-0.6
In2	-1	-0.995	...	-0.6
Parameters				
A	[1x4]			
B	[1x4]			
Outputs				
Out1	0	-0.28	...	-0.898
Out2	0	-0.08	...	-0.432
Exp. Out1	0	-0.28	...	-0.898
Exp. Out2	0	-0.08	...	-0.432
Out1 (DSP)	0	-0.28	...	-0.898
Out2 (DSP)	0	-0.08	...	-0.432
Exp. Out1 (DSP)	0	-0.28	...	-0.898
Exp. Out2 (DSP)	0	-0.08	...	-0.432

Test settings	
Tolerance Out1	±2,3283e-07 (±500 LSB)
Tolerance Out2	±2,3283e-07 (±500 LSB)

Test statistics	
Min CPU cycles	1821
Max CPU cycles	2444
Avg CPU cycles	2265

Test case: Conversion test OK

Conversion test for Control block TDSystemO2.

Test results			
Time step	1	2	3
Mask parameters			
A	[1x4]	[1x4]	[1x4]
B	[1x4]	[1x4]	[1x4]
Controller parameters			
a11	0	0	0
a22	30	3	0.3
b21	20	2	0.2
a21	20	2	0.2
b12	10	1	0.1
a12	10	1	0.1
b11	0	0	0
b22	30	3	0.3
Exp. a11	0	0	0
Exp. a22	30	3	0.3
Exp. b21	20	2	0.2
Exp. a21	20	2	0.2
Exp. b12	10	1	0.1
Exp. a12	10	1	0.1
Exp. b11	0	0	0
Exp. b22	30	3	0.3

Test settings	
Tolerance a11	±0,0000e+00
Tolerance a22	±0,0000e+00
Tolerance b21	±0,0000e+00
Tolerance a21	±0,0000e+00
Tolerance b12	±0,0000e+00
Tolerance a12	±0,0000e+00
Tolerance b11	±0,0000e+00
Tolerance b22	±0,0000e+00

Verification: TDSystemO2 Float32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for Control block TDSystemO2.

Test results				
Time step	1	2	...	174
CPU cycles	652	848	...	846
Inputs				
In1 (DSP)	-0	-0.1	...	-0.6
In2 (DSP)	-1	-0.995	...	-0.6
In1	-0	-0.1	...	-0.6
In2	-1	-0.995	...	-0.6
Parameters				
A	[1x4]			
B	[1x4]			
Outputs				
Out1	0	-0.28	...	-0.898
Out2	0	-0.08	...	-0.432
Exp. Out1	0	-0.28	...	-0.898
Exp. Out2	0	-0.08	...	-0.432
Out1 (DSP)	0	-0.28	...	-0.898
Out2 (DSP)	0	-0.08	...	-0.432
Exp. Out1 (DSP)	0	-0.28	...	-0.898
Exp. Out2 (DSP)	0	-0.08	...	-0.432

Test settings	
Tolerance Out1	±2,3283e-07 (±500 LSB)
Tolerance Out2	±2,3283e-07 (±500 LSB)

Test statistics	
Min CPU cycles	652
Max CPU cycles	878
Avg CPU cycles	837

Test case: Conversion test OK

Conversion test for Control block TDSystemO2.

Test results			
Time step	1	2	3
Mask parameters			
A	[1x4]	[1x4]	[1x4]
B	[1x4]	[1x4]	[1x4]
Controller parameters			
a11	0	0	0
a22	30	3	0.3
b21	20	2	0.2
a21	20	2	0.2
b12	10	1	0.1
a12	10	1	0.1
b11	0	0	0
b22	30	3	0.3
Exp. a11	0	0	0
Exp. a22	30	3	0.3
Exp. b21	20	2	0.2
Exp. a21	20	2	0.2
Exp. b12	10	1	0.1
Exp. a12	10	1	0.1
Exp. b11	0	0	0
Exp. b22	30	3	0.3

Test settings	
Tolerance a11	±0,0000e+00
Tolerance a22	±0,0000e+00
Tolerance b21	±0,0000e+00
Tolerance a21	±0,0000e+00
Tolerance b12	±0,0000e+00
Tolerance a12	±0,0000e+00
Tolerance b11	±0,0000e+00
Tolerance b22	±0,0000e+00

Verification: TDSystemO2 Float32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test

OK

Inport test for Control block TDSystemO2.

Test results				
Time step	1	2	...	174
CPU cycles	125	108	...	108
Inputs				
In1 (DSP)	-0	-0.1	...	-0.6
In2 (DSP)	-1	-0.995	...	-0.6
In1	-0	-0.1	...	-0.6
In2	-1	-0.995	...	-0.6
Parameters				
A	[1x4]			
B	[1x4]			
Outputs				
Out1	0	-0.28	...	-0.898
Out2	0	-0.08	...	-0.432
Exp. Out1	0	-0.28	...	-0.898
Exp. Out2	0	-0.08	...	-0.432
Out1 (DSP)	0	-0.28	...	-0.898
Out2 (DSP)	0	-0.08	...	-0.432
Exp. Out1 (DSP)	0	-0.28	...	-0.898
Exp. Out2 (DSP)	0	-0.08	...	-0.432

Test settings	
Tolerance Out1	±2,3283e-07 (±500 LSB)
Tolerance Out2	±2,3283e-07 (±500 LSB)

Test statistics	
Min CPU cycles	108
Max CPU cycles	125
Avg CPU cycles	108

Test case: Conversion test

OK

Conversion test for Control block TDSystemO2.

Test results			
Time step	1	2	3
Mask parameters			
A	[1x4]	[1x4]	[1x4]
B	[1x4]	[1x4]	[1x4]
Controller parameters			
a11	0	0	0
a22	30	3	0.3
b21	20	2	0.2
a21	20	2	0.2
b12	10	1	0.1
a12	10	1	0.1
b11	0	0	0
b22	30	3	0.3
Exp. a11	0	0	0
Exp. a22	30	3	0.3
Exp. b21	20	2	0.2
Exp. a21	20	2	0.2
Exp. b12	10	1	0.1
Exp. a12	10	1	0.1
Exp. b11	0	0	0
Exp. b22	30	3	0.3

Test settings	
Tolerance a11	±0,0000e+00
Tolerance a22	±0,0000e+00
Tolerance b21	±0,0000e+00
Tolerance a21	±0,0000e+00
Tolerance b12	±0,0000e+00
Tolerance a12	±0,0000e+00
Tolerance b11	±0,0000e+00
Tolerance b22	±0,0000e+00

Verification: TDSystemO2 Float32 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test

OK

Inport test for Control block TDSystemO2.

Test results				
Time step	1	2	...	174
CPU cycles	90	90	...	90
Inputs				
In1 (DSP)	-0	-0.1	...	-0.6
In2 (DSP)	-1	-0.995	...	-0.6
In1	-0	-0.1	...	-0.6
In2	-1	-0.995	...	-0.6
Parameters				
A	[1x4]			
B	[1x4]			
Outputs				
Out1	0	-0.28	...	-0.898
Out2	0	-0.08	...	-0.432
Exp. Out1	0	-0.28	...	-0.898
Exp. Out2	0	-0.08	...	-0.432
Out1 (DSP)	0	-0.28	...	-0.898
Out2 (DSP)	0	-0.08	...	-0.432
Exp. Out1 (DSP)	0	-0.28	...	-0.898
Exp. Out2 (DSP)	0	-0.08	...	-0.432

Test settings	
Tolerance Out1	±2,3283e-07 (±500 LSB)
Tolerance Out2	±2,3283e-07 (±500 LSB)

Test statistics	
Min CPU cycles	90
Max CPU cycles	90
Avg CPU cycles	90

Test case: Conversion test

OK

Conversion test for Control block TDSystemO2.

Test results			
Time step	1	2	3
Mask parameters			
A	[1x4]	[1x4]	[1x4]
B	[1x4]	[1x4]	[1x4]
Controller parameters			
a11	0	0	0
a22	30	3	0.3
b21	20	2	0.2
a21	20	2	0.2
b12	10	1	0.1
a12	10	1	0.1
b11	0	0	0
b22	30	3	0.3
Exp. a11	0	0	0
Exp. a22	30	3	0.3
Exp. b21	20	2	0.2
Exp. a21	20	2	0.2
Exp. b12	10	1	0.1
Exp. a12	10	1	0.1
Exp. b11	0	0	0
Exp. b22	30	3	0.3

Test settings	
Tolerance a11	±0,0000e+00
Tolerance a22	±0,0000e+00
Tolerance b21	±0,0000e+00
Tolerance a21	±0,0000e+00
Tolerance b12	±0,0000e+00
Tolerance a12	±0,0000e+00
Tolerance b11	±0,0000e+00
Tolerance b22	±0,0000e+00

Verification: TDSystemO2 Float32 CPU dsPIC33EP256MC502

Date of Test	2026-06-23
Target controller	dsPIC33EP256MC502

Test case: Inport test

OK

Inport test for Control block TDSystemO2.

Test results				
Time step	1	2	...	174
CPU cycles	1940	2366	...	2397
Inputs				
In1 (DSP)	-0	-0.1	...	-0.6
In2 (DSP)	-1	-0.995	...	-0.6
In1	-0	-0.1	...	-0.6
In2	-1	-0.995	...	-0.6
Parameters				
A	[1x4]			
B	[1x4]			
Outputs				
Out1	0	-0.28	...	-0.898
Out2	0	-0.08	...	-0.432
Exp. Out1	0	-0.28	...	-0.898
Exp. Out2	0	-0.08	...	-0.432
Out1 (DSP)	0	-0.28	...	-0.898
Out2 (DSP)	0	-0.08	...	-0.432
Exp. Out1 (DSP)	0	-0.28	...	-0.898
Exp. Out2 (DSP)	0	-0.08	...	-0.432

Test settings	
Tolerance Out1	±2,3283e-07 (±500 LSB)
Tolerance Out2	±2,3283e-07 (±500 LSB)

Test statistics	
Min CPU cycles	1940
Max CPU cycles	2469
Avg CPU cycles	2331

Test case: Conversion test

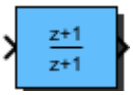
OK

Conversion test for Control block TDSystemO2.

Test results			
Time step	1	2	3
Mask parameters			
A	[1x4]	[1x4]	[1x4]
B	[1x4]	[1x4]	[1x4]
Controller parameters			
a11	0	0	0
a22	30	3	0.3
b21	20	2	0.2
a21	20	2	0.2
b12	10	1	0.1
a12	10	1	0.1
b11	0	0	0
b22	30	3	0.3
Exp. a11	0	0	0
Exp. a22	30	3	0.3
Exp. b21	20	2	0.2
Exp. a21	20	2	0.2
Exp. b12	10	1	0.1
Exp. a12	10	1	0.1
Exp. b11	0	0	0
Exp. b22	30	3	0.3

Test settings	
Tolerance a11	±0,0000e+00
Tolerance a22	±0,0000e+00
Tolerance b21	±0,0000e+00
Tolerance a21	±0,0000e+00
Tolerance b12	±0,0000e+00
Tolerance a12	±0,0000e+00
Tolerance b11	±0,0000e+00
Tolerance b22	±0,0000e+00

Block: TF1



First order transfer function:
G(z) = (b1.z + b0) / (z + a0)

Inports	
In	Input In(k)

Outports	
Out	Output Out(k)

Mask Parameters		
Name	**ID**	**Description**
b1	1	b1
b0	2	b0
a0	3	a0
ts_fact	4	Multiplication factor of base sampling time (in integer format)

Description:

Due to limited value range in the 8 bit fixed point implementation rather high deviations from expected output values may occur.

Developer note: The source code of this block is used for blocks *DT1* and *PT1*.

Implementations:

FiP8 8 Bit Fixed Point Implementation
FiP16 16 Bit Fixed Point Implementation
FiP32 32 Bit Fixed Point Implementation
Float32 32 Bit Floating Point Implementation
Float64 64 Bit Floating Point Implementation

Implementation: FiP8

8 Bit Fixed Point Implementation

Inports Data Type	
In	int8

Outports Data Type	
Out	int8

Implementation: FiP16

16 Bit Fixed Point Implementation

Inports Data Type	
In	int16

Outports Data Type	
Out	int16

Implementation: FiP32

32 Bit Fixed Point Implementation

Inports Data Type	
In	int32

Outports Data Type	
Out	int32

Implementation: Float32

32 Bit Floating Point Implementation

Inports Data Type	
In	float32

Outports Data Type	
Out	float32

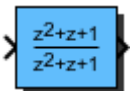
Implementation: Float64

64 Bit Floating Point Implementation

Inports Data Type	
In	float64

Outports Data Type	
Out	float64

Block: TF2



Second order transfer function:
G(z) = (b2.z^2 + b1.z + b0) / (z^2 + a1.z + a0)

Inports	
In	Input In(k)

Outports	
Out	Output Out(k)

Mask Parameters		
Name	**ID**	**Description**
b2	1	b2
b1	2	b1
b0	3	b0
a1	4	a1
a0	5	a0
ts_fact	6	Multiplication factor of base sampling time (in integer format)

Implementations:

FiP16	16 Bit Fixed Point Implementation
FiP8	8 Bit Fixed Point Implementation
FiP32	32 Bit Fixed Point Implementation
Float32	32 Bit Floating Point Implementation
Float64	64 Bit Floating Point Implementation

Implementation: FiP16

16 Bit Fixed Point Implementation

Inports Data Type	
In	int16

Outports Data Type	
Out	int16

Implementation: FiP8

8 Bit Fixed Point Implementation

Inports Data Type	
In	int8

Outports Data Type	
Out	int8

Implementation: FiP32

32 Bit Fixed Point Implementation

Inports Data Type	
In	int32

Outports Data Type	
Out	int32

Implementation: Float32

32 Bit Floating Point Implementation

Inports Data Type	
In	float32

Outports Data Type	
Out	float32

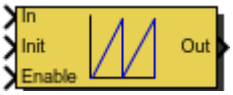
Implementation: Float64

64 Bit Floating Point Implementation

Inports Data Type	
In	float64

Outports Data Type	
Out	float64

Block: ul



Integrator for angle signals:
G(s) = Ki/s = 1/(Ti*s)

Inports	
In	Control error input
Init	Value which is loaded at initialization function call
Enable	Enable == 0: Deactivation of block; Out is set to 0. Enable 0->1: Preload of integral part. Enable == 1: Activation of block

Outports	
Out	Integrator output

Mask Parameters		
Name	**ID**	**Description**
Ki	1	Integral Factor
ts_fact	2	Multiplication factor of base sampling time (in integer format)

Description:

Each fixed point implementation uses the next higher integer datatype for the integrational value storage variable.
A rising flank at the *Enable* inport will preload the integrational part with the value present on the *Init* inport.

Transfer function (zero-order hold discretization method):

$$G(z) = K_{\mathrm{i}} T_{\mathrm{s}} \frac{1}{z-1}$$

Implementations:

FiP8	8 Bit Fixed Point Implementation
FiP16	16 Bit Fixed Point Implementation
FiP32	32 Bit Fixed Point Implementation
Float32	32 Bit Floating Point Implementation
Float64	64 Bit Floating Point Implementation

Implementation: FiP8

8 Bit Fixed Point Implementation

Inports Data Type	
In	int8
Init	int8
Enable	bool

Outports Data Type	
Out	int8

Implementation: FiP16

16 Bit Fixed Point Implementation

Inports Data Type	
In	int16
Init	int16
Enable	bool

Outports Data Type	
Out	int16

Implementation: FiP32

32 Bit Fixed Point Implementation

Inports Data Type	
In	int32
Init	int32
Enable	bool

Outports Data Type	
Out	int32

Implementation: Float32

32 Bit Floating Point Implementation

Inports Data Type	
In	float32
Init	float32
Enable	bool

Outports Data Type	
Out	float32

Implementation: Float64

64 Bit Floating Point Implementation

Inports Data Type	
In	float64
Init	float64
Enable	bool

Outports Data Type	
Out	float64

Verification: ul FiP16 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for Control block ul.

Test results						
Time step	1	2	3	4	...	351
CPU cycles	67	67	67	99	...	94
Inputs						
In (DSP)	0	0	0	0	...	-8192
Init (DSP)	3604	3604	3604	3604	...	3604
Enable (DSP)	0	0	0	1	...	1
In	0	0	0	0	...	-0.25
Init	0.11	0.11	0.11	0.11	...	0.11
Enable	0	0	0	1	...	1
Parameters						
Ki	500					
ts_fact	1					
Outputs						
Out	0	0	0	0.11	...	-0.779
Exp. Out	0	0	0	0.11	...	-0.78
Out (DSP)	0	0	0	3604	...	-25539
Exp. Out (DSP)	0	0	0	3604	...	-25559

Test settings	
Tolerance Out	±7,6294e-04 (±25 LSB)

Test statistics	
Min CPU cycles	67
Max CPU cycles	99
Avg CPU cycles	93

Test case: Conversion test OK

Conversion test for Control block ul.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Ki	-11	-10.389	-9.778	-9.167	...	11
ts_fact	1	2	3	4	...	37
Controller parameters						
b0	-36	-68	-96	-120	...	1334
sfr	15	15	15	15	...	15
Exp. b0	-36	-68	-96	-120	...	1334
Exp. sfr	15	15	15	15	...	15

Test settings	
Tolerance b0	±0,0000e+00
Tolerance sfr	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block ul.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Ki	-11	-10.389	-9.778	-9.167	...	11
ts_fact	1	2	3	4	...	37
Controller parameters						
b0	-36	-68	-96	-120	...	1333
sfr	15	15	15	15	...	15
Exp. b0	-36	-68	-96	-120	...	1334
Exp. sfr	15	15	15	15	...	15

Test settings	
Tolerance b0	±1,0000e+00
Tolerance sfr	±0,0000e+00

Test statistics	
Min CPU cycles	2076
Max CPU cycles	2170
Avg CPU cycles	2160

Verification: ul FiP16 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test

OK

Inport test for Control block ul.

Test results						
Time step	1	2	3	4	...	351
CPU cycles	43	43	43	61	...	59
Inputs						
In (DSP)	0	0	0	0	...	-8192
Init (DSP)	3604	3604	3604	3604	...	3604
Enable (DSP)	0	0	0	1	...	1
In	0	0	0	0	...	-0.25
Init	0.11	0.11	0.11	0.11	...	0.11
Enable	0	0	0	1	...	1
Parameters						
Ki	500					
ts_fact	1					
Outputs						
Out	0	0	0	0.11	...	-0.779
Exp. Out	0	0	0	0.11	...	-0.78
Out (DSP)	0	0	0	3604	...	-25539
Exp. Out (DSP)	0	0	0	3604	...	-25559

Test settings	
Tolerance Out	±7,6294e-04 (±25 LSB)

Test statistics	
Min CPU cycles	43
Max CPU cycles	61
Avg CPU cycles	58

Test case: Conversion test

OK

Conversion test for Control block ul.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Ki	-11	-10.389	-9.778	-9.167	...	11
ts_fact	1	2	3	4	...	37
Controller parameters						
b0	-36	-68	-96	-120	...	1334
sfr	15	15	15	15	...	15
Exp. b0	-36	-68	-96	-120	...	1334
Exp. sfr	15	15	15	15	...	15

Test settings	
Tolerance b0	±0,0000e+00
Tolerance sfr	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block ul.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Ki	-11	-10.389	-9.778	-9.167	...	11
ts_fact	1	2	3	4	...	37
Controller parameters						
b0	-36	-68	-96	-120	...	1333
sfr	15	15	15	15	...	15
Exp. b0	-36	-68	-96	-120	...	1334
Exp. sfr	15	15	15	15	...	15

Test settings	
Tolerance b0	±1,0000e+00
Tolerance sfr	±0,0000e+00

Test statistics	
Min CPU cycles	1071
Max CPU cycles	1141
Avg CPU cycles	1139

Verification: ul FiP16 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test

OK

Inport test for Control block ul.

Test results						
Time step	1	2	3	4	...	351
CPU cycles	68	68	68	98	...	83
Inputs						
In (DSP)	0	0	0	0	...	-8192
Init (DSP)	3604	3604	3604	3604	...	3604
Enable (DSP)	0	0	0	1	...	1
In	0	0	0	0	...	-0.25
Init	0.11	0.11	0.11	0.11	...	0.11
Enable	0	0	0	1	...	1
Parameters						
Ki	500					
ts_fact	1					
Outputs						
Out	0	0	0	0.11	...	-0.779
Exp. Out	0	0	0	0.11	...	-0.78
Out (DSP)	0	0	0	3604	...	-25539
Exp. Out (DSP)	0	0	0	3604	...	-25559

Test settings	
Tolerance Out	±7,6294e-04 (±25 LSB)

Test statistics	
Min CPU cycles	68
Max CPU cycles	98
Avg CPU cycles	82

Test case: Conversion test

OK

Conversion test for Control block ul.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Ki	-11	-10.389	-9.778	-9.167	...	11
ts_fact	1	2	3	4	...	37
Controller parameters						
b0	-36	-68	-96	-120	...	1334
sfr	15	15	15	15	...	15
Exp. b0	-36	-68	-96	-120	...	1334
Exp. sfr	15	15	15	15	...	15

Test settings	
Tolerance b0	±0,0000e+00
Tolerance sfr	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block ul.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Ki	-11	-10.389	-9.778	-9.167	...	11
ts_fact	1	2	3	4	...	37
Controller parameters						
b0	-36	-68	-96	-120	...	1333
sfr	15	15	15	15	...	15
Exp. b0	-36	-68	-96	-120	...	1334
Exp. sfr	15	15	15	15	...	15

Test settings	
Tolerance b0	±1,0000e+00
Tolerance sfr	±0,0000e+00

Test statistics	
Min CPU cycles	1180
Max CPU cycles	1235
Avg CPU cycles	1217

Verification: ul FiP16 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test

OK

Inport test for Control block ul.

Test results						
Time step	1	2	3	4	...	351
CPU cycles	61	61	61	96	...	85
Inputs						
In (DSP)	0	0	0	0	...	-8192
Init (DSP)	3604	3604	3604	3604	...	3604
Enable (DSP)	0	0	0	1	...	1
In	0	0	0	0	...	-0.25
Init	0.11	0.11	0.11	0.11	...	0.11
Enable	0	0	0	1	...	1
Parameters						
Ki	500					
ts_fact	1					
Outputs						
Out	0	0	0	0.11	...	-0.779
Exp. Out	0	0	0	0.11	...	-0.78
Out (DSP)	0	0	0	3604	...	-25539
Exp. Out (DSP)	0	0	0	3604	...	-25559

Test settings	
Tolerance Out	±7,6294e-04 (±25 LSB)

Test statistics	
Min CPU cycles	61
Max CPU cycles	147
Avg CPU cycles	85

Test case: Conversion test

OK

Conversion test for Control block ul.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Ki	-11	-10.389	-9.778	-9.167	...	11
ts_fact	1	2	3	4	...	37
Controller parameters						
b0	-36	-68	-96	-120	...	1334
sfr	15	15	15	15	...	15
Exp. b0	-36	-68	-96	-120	...	1334
Exp. sfr	15	15	15	15	...	15

Test settings	
Tolerance b0	±0,0000e+00
Tolerance sfr	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block ul.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Ki	-11	-10.389	-9.778	-9.167	...	11
ts_fact	1	2	3	4	...	37
Controller parameters						
b0	-36	-68	-96	-120	...	1333
sfr	15	15	15	15	...	15
Exp. b0	-36	-68	-96	-120	...	1334
Exp. sfr	15	15	15	15	...	15

Test settings	
Tolerance b0	±1,0000e+00
Tolerance sfr	±0,0000e+00

Test statistics	
Min CPU cycles	2537
Max CPU cycles	3018
Avg CPU cycles	2948

Verification: ul FiP16 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test

OK

Inport test for Control block ul.

Test results						
Time step	1	2	3	4	...	351
CPU cycles	31	31	31	59	...	55
Inputs						
In (DSP)	0	0	0	0	...	-8192
Init (DSP)	3604	3604	3604	3604	...	3604
Enable (DSP)	0	0	0	1	...	1
In	0	0	0	0	...	-0.25
Init	0.11	0.11	0.11	0.11	...	0.11
Enable	0	0	0	1	...	1
Parameters						
Ki	500					
ts_fact	1					
Outputs						
Out	0	0	0	0.11	...	-0.779
Exp. Out	0	0	0	0.11	...	-0.78
Out (DSP)	0	0	0	3604	...	-25539
Exp. Out (DSP)	0	0	0	3604	...	-25559

Test settings	
Tolerance Out	±7,6294e-04 (±25 LSB)

Test statistics	
Min CPU cycles	31
Max CPU cycles	59
Avg CPU cycles	54

Test case: Conversion test

OK

Conversion test for Control block ul.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Ki	-11	-10.389	-9.778	-9.167	...	11
ts_fact	1	2	3	4	...	37
Controller parameters						
b0	-36	-68	-96	-120	...	1334
sfr	15	15	15	15	...	15
Exp. b0	-36	-68	-96	-120	...	1334
Exp. sfr	15	15	15	15	...	15

Test settings	
Tolerance b0	±0,0000e+00
Tolerance sfr	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block ul.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Ki	-11	-10.389	-9.778	-9.167	...	11
ts_fact	1	2	3	4	...	37
Controller parameters						
b0	-36	-68	-96	-120	...	1333
sfr	15	15	15	15	...	15
Exp. b0	-36	-68	-96	-120	...	1334
Exp. sfr	15	15	15	15	...	15

Test settings	
Tolerance b0	±1,0000e+00
Tolerance sfr	±0,0000e+00

Test statistics	
Min CPU cycles	1072
Max CPU cycles	1188
Avg CPU cycles	1179

Verification: ul FiP16 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test

OK

Inport test for Control block ul.

Test results						
Time step	1	2	3	4	...	351
CPU cycles	72	59	59	86	...	86
Inputs						
In (DSP)	0	0	0	0	...	-8192
Init (DSP)	3604	3604	3604	3604	...	3604
Enable (DSP)	0	0	0	1	...	1
In	0	0	0	0	...	-0.25
Init	0.11	0.11	0.11	0.11	...	0.11
Enable	0	0	0	1	...	1
Parameters						
Ki	500					
ts_fact	1					
Outputs						
Out	0	0	0	0.11	...	-0.779
Exp. Out	0	0	0	0.11	...	-0.78
Out (DSP)	0	0	0	3604	...	-25539
Exp. Out (DSP)	0	0	0	3604	...	-25559

Test settings	
Tolerance Out	±7,6294e-04 (±25 LSB)

Test statistics	
Min CPU cycles	59
Max CPU cycles	86
Avg CPU cycles	85

Test case: Conversion test

OK

Conversion test for Control block ul.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Ki	-11	-10.389	-9.778	-9.167	...	11
ts_fact	1	2	3	4	...	37
Controller parameters						
b0	-36	-68	-96	-120	...	1334
sfr	15	15	15	15	...	15
Exp. b0	-36	-68	-96	-120	...	1334
Exp. sfr	15	15	15	15	...	15

Test settings	
Tolerance b0	±0,0000e+00
Tolerance sfr	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block ul.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Ki	-11	-10.389	-9.778	-9.167	...	11
ts_fact	1	2	3	4	...	37
Controller parameters						
b0	-36	-68	-96	-120	...	1333
sfr	15	15	15	15	...	15
Exp. b0	-36	-68	-96	-120	...	1334
Exp. sfr	15	15	15	15	...	15

Test settings	
Tolerance b0	±1,0000e+00
Tolerance sfr	±0,0000e+00

Test statistics	
Min CPU cycles	857
Max CPU cycles	985
Avg CPU cycles	878

Verification: ul FiP16 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for Control block ul.

Test results						
Time step	1	2	3	4	...	351
CPU cycles	57	57	57	100	...	93
Inputs						
In (DSP)	0	0	0	0	...	-8192
Init (DSP)	3604	3604	3604	3604	...	3604
Enable (DSP)	0	0	0	1	...	1
In	0	0	0	0	...	-0.25
Init	0.11	0.11	0.11	0.11	...	0.11
Enable	0	0	0	1	...	1
Parameters						
Ki	500					
ts_fact	1					
Outputs						
Out	0	0	0	0.11	...	-0.779
Exp. Out	0	0	0	0.11	...	-0.78
Out (DSP)	0	0	0	3604	...	-25539
Exp. Out (DSP)	0	0	0	3604	...	-25559

Test settings	
Tolerance Out	±7,6294e-04 (±25 LSB)

Test statistics	
Min CPU cycles	57
Max CPU cycles	100
Avg CPU cycles	92

Test case: Conversion test OK

Conversion test for Control block ul.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Ki	-11	-10.389	-9.778	-9.167	...	11
ts_fact	1	2	3	4	...	37
Controller parameters						
b0	-36	-68	-96	-120	...	1334
sfr	15	15	15	15	...	15
Exp. b0	-36	-68	-96	-120	...	1334
Exp. sfr	15	15	15	15	...	15

Test settings	
Tolerance b0	±0,0000e+00
Tolerance sfr	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block ul.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Ki	-11	-10.389	-9.778	-9.167	...	11
ts_fact	1	2	3	4	...	37
Controller parameters						
b0	-36	-68	-96	-120	...	1333
sfr	15	15	15	15	...	15
Exp. b0	-36	-68	-96	-120	...	1334
Exp. sfr	15	15	15	15	...	15

Test settings	
Tolerance b0	±1,0000e+00
Tolerance sfr	±0,0000e+00

Test statistics	
Min CPU cycles	1595
Max CPU cycles	1665
Avg CPU cycles	1660

Verification: ul FiP16 CPU dsPIC33EP256MC502

Date of Test	2026-06-23
Target controller	dsPIC33EP256MC502

Test case: Inport test

OK

Inport test for Control block ul.

Test results						
Time step	1	2	3	4	...	351
CPU cycles	48	48	48	80	...	79
Inputs						
In (DSP)	0	0	0	0	...	-8192
Init (DSP)	3604	3604	3604	3604	...	3604
Enable (DSP)	0	0	0	1	...	1
In	0	0	0	0	...	-0.25
Init	0.11	0.11	0.11	0.11	...	0.11
Enable	0	0	0	1	...	1
Parameters						
Ki	500					
ts_fact	1					
Outputs						
Out	0	0	0	0.11	...	-0.779
Exp. Out	0	0	0	0.11	...	-0.78
Out (DSP)	0	0	0	3604	...	-25539
Exp. Out (DSP)	0	0	0	3604	...	-25559

Test settings	
Tolerance Out	±7,6294e-04 (±25 LSB)

Test statistics	
Min CPU cycles	48
Max CPU cycles	80
Avg CPU cycles	78

Test case: Conversion test

OK

Conversion test for Control block ul.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Ki	-11	-10.389	-9.778	-9.167	...	11
ts_fact	1	2	3	4	...	37
Controller parameters						
b0	-36	-68	-96	-120	...	1334
sfr	15	15	15	15	...	15
Exp. b0	-36	-68	-96	-120	...	1334
Exp. sfr	15	15	15	15	...	15

Test settings	
Tolerance b0	±0,0000e+00
Tolerance sfr	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block ul.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Ki	-11	-10.389	-9.778	-9.167	...	11
ts_fact	1	2	3	4	...	37
Controller parameters						
b0	-36	-68	-96	-120	...	1333
sfr	15	15	15	15	...	15
Exp. b0	-36	-68	-96	-120	...	1334
Exp. sfr	15	15	15	15	...	15

Test settings	
Tolerance b0	±1,0000e+00
Tolerance sfr	±0,0000e+00

Test statistics	
Min CPU cycles	4133
Max CPU cycles	5289
Avg CPU cycles	5242

Verification: ul FiP32 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test

OK

Inport test for Control block ul.

Test results				
Time step	1	2	...	351
CPU cycles	74	74	...	124
Inputs				
In (DSP)	0	0	...	-536870912
Init (DSP)	236223201	236223201	...	236223201
Enable (DSP)	0	0	...	1
In	0	0	...	-0.25
Init	0.11	0.11	...	0.11
Enable	0	0	...	1
Parameters				
Ki	500			
ts_fact	1			
Outputs				
Out	0	0	...	-0.78
Exp. Out	0	0	...	-0.78
Out (DSP)	0	0	...	-1675037225
Exp. Out (DSP)	0	0	...	-1675037245

Test settings	
Tolerance Out	±1,1642e-08 (±25 LSB)

Test statistics	
Min CPU cycles	74
Max CPU cycles	131
Avg CPU cycles	123

Test case: Conversion test

OK

Conversion test for Control block ul.

Test results				
Time step	1	2	...	37
Mask parameters				
Ki	-11	-10.389	...	11
ts_fact	1	2	...	37
Controller parameters				
b0	-2362232	-4461994	...	87402584
sfr	31	31	...	31
Exp. b0	-2362232	-4461994	...	87402584
Exp. sfr	31	31	...	31

Test settings	
Tolerance b0	±0,0000e+00
Tolerance sfr	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block ul.

Test results				
Time step	1	2	...	37
Mask parameters				
Ki	-11	-10.389	...	11
ts_fact	1	2	...	37
Controller parameters				
b0	-2362232	-4461994	...	87402584
sfr	31	31	...	31
Exp. b0	-2362232	-4461994	...	87402584
Exp. sfr	31	31	...	31

Test settings	
Tolerance b0	±8,0000e+00
Tolerance sfr	±0,0000e+00

Test statistics	
Min CPU cycles	2254
Max CPU cycles	2396
Avg CPU cycles	2381

Verification: ul FiP32 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for Control block ul.

Test results				
Time step	1	2	...	351
CPU cycles	51	51	...	101
Inputs				
In (DSP)	0	0	...	-536870912
Init (DSP)	236223201	236223201	...	236223201
Enable (DSP)	0	0	...	1
In	0	0	...	-0.25
Init	0.11	0.11	...	0.11
Enable	0	0	...	1
Parameters				
Ki	500			
ts_fact	1			
Outputs				
Out	0	0	...	-0.78
Exp. Out	0	0	...	-0.78
Out (DSP)	0	0	...	-1675037225
Exp. Out (DSP)	0	0	...	-1675037245

Test settings	
Tolerance Out	±1,1642e-08 (±25 LSB)

Test statistics	
Min CPU cycles	51
Max CPU cycles	109
Avg CPU cycles	100

Test case: Conversion test OK

Conversion test for Control block ul.

Test results				
Time step	1	2	...	37
Mask parameters				
Ki	-11	-10.389	...	11
ts_fact	1	2	...	37
Controller parameters				
b0	-2362232	-4461994	...	87402584
sfr	31	31	...	31
Exp. b0	-2362232	-4461994	...	87402584
Exp. sfr	31	31	...	31

Test settings	
Tolerance b0	±0,0000e+00
Tolerance sfr	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block ul.

Test results				
Time step	1	2	...	37
Mask parameters				
Ki	-11	-10.389	...	11
ts_fact	1	2	...	37
Controller parameters				
b0	-2362232	-4461994	...	87402584
sfr	31	31	...	31
Exp. b0	-2362232	-4461994	...	87402584
Exp. sfr	31	31	...	31

Test settings	
Tolerance b0	±8,0000e+00
Tolerance sfr	±0,0000e+00

Test statistics	
Min CPU cycles	1027
Max CPU cycles	1125
Avg CPU cycles	1121

Verification: ul FiP32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for Control block ul.

Test results				
Time step	1	2	...	351
CPU cycles	79	79	...	109
Inputs				
In (DSP)	0	0	...	-536870912
Init (DSP)	236223201	236223201	...	236223201
Enable (DSP)	0	0	...	1
In	0	0	...	-0.25
Init	0.11	0.11	...	0.11
Enable	0	0	...	1
Parameters				
Ki	500			
ts_fact	1			
Outputs				
Out	0	0	...	-0.78
Exp. Out	0	0	...	-0.78
Out (DSP)	0	0	...	-1675037225
Exp. Out (DSP)	0	0	...	-1675037245

Test settings	
Tolerance Out	±1,1642e-08 (±25 LSB)

Test statistics	
Min CPU cycles	79
Max CPU cycles	127
Avg CPU cycles	108

Test case: Conversion test OK

Conversion test for Control block ul.

Test results				
Time step	1	2	...	37
Mask parameters				
Ki	-11	-10.389	...	11
ts_fact	1	2	...	37
Controller parameters				
b0	-2362232	-4461994	...	87402584
sfr	31	31	...	31
Exp. b0	-2362232	-4461994	...	87402584
Exp. sfr	31	31	...	31

Test settings	
Tolerance b0	±0,0000e+00
Tolerance sfr	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block ul.

Test results				
Time step	1	2	...	37
Mask parameters				
Ki	-11	-10.389	...	11
ts_fact	1	2	...	37
Controller parameters				
b0	-2362232	-4461994	...	87402584
sfr	31	31	...	31
Exp. b0	-2362232	-4461994	...	87402584
Exp. sfr	31	31	...	31

Test settings	
Tolerance b0	±8,0000e+00
Tolerance sfr	±0,0000e+00

Test statistics	
Min CPU cycles	1555
Max CPU cycles	1614
Avg CPU cycles	1599

Verification: ul FiP32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for Control block ul.

Test results				
Time step	1	2	...	351
CPU cycles	82	82	...	205
Inputs				
In (DSP)	0	0	...	-536870912
Init (DSP)	236223201	236223201	...	236223201
Enable (DSP)	0	0	...	1
In	0	0	...	-0.25
Init	0.11	0.11	...	0.11
Enable	0	0	...	1
Parameters				
Ki	500			
ts_fact	1			
Outputs				
Out	0	0	...	-0.78
Exp. Out	0	0	...	-0.78
Out (DSP)	0	0	...	-1675037225
Exp. Out (DSP)	0	0	...	-1675037245

Test settings	
Tolerance Out	±1,1642e-08 (±25 LSB)

Test statistics	
Min CPU cycles	82
Max CPU cycles	265
Avg CPU cycles	204

Test case: Conversion test OK

Conversion test for Control block ul.

Test results				
Time step	1	2	...	37
Mask parameters				
Ki	-11	-10.389	...	11
ts_fact	1	2	...	37
Controller parameters				
b0	-2362232	-4461994	...	87402584
sfr	31	31	...	31
Exp. b0	-2362232	-4461994	...	87402584
Exp. sfr	31	31	...	31

Test settings	
Tolerance b0	±0,0000e+00
Tolerance sfr	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block ul.

Test results				
Time step	1	2	...	37
Mask parameters				
Ki	-11	-10.389	...	11
ts_fact	1	2	...	37
Controller parameters				
b0	-2362232	-4461994	...	87402584
sfr	31	31	...	31
Exp. b0	-2362232	-4461994	...	87402584
Exp. sfr	31	31	...	31

Test settings	
Tolerance b0	±8,0000e+00
Tolerance sfr	±0,0000e+00

Test statistics	
Min CPU cycles	3570
Max CPU cycles	4304
Avg CPU cycles	4226

Verification: ul FiP32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test

OK

Inport test for Control block ul.

Test results				
Time step	1	2	...	351
CPU cycles	31	31	...	77
Inputs				
In (DSP)	0	0	...	-536870912
Init (DSP)	236223201	236223201	...	236223201
Enable (DSP)	0	0	...	1
In	0	0	...	-0.25
Init	0.11	0.11	...	0.11
Enable	0	0	...	1
Parameters				
Ki	500			
ts_fact	1			
Outputs				
Out	0	0	...	-0.78
Exp. Out	0	0	...	-0.78
Out (DSP)	0	0	...	-1675037225
Exp. Out (DSP)	0	0	...	-1675037245

Test settings	
Tolerance Out	±1,1642e-08 (±25 LSB)

Test statistics	
Min CPU cycles	31
Max CPU cycles	80
Avg CPU cycles	76

Test case: Conversion test

OK

Conversion test for Control block ul.

Test results				
Time step	1	2	...	37
Mask parameters				
Ki	-11	-10.389	...	11
ts_fact	1	2	...	37
Controller parameters				
b0	-2362232	-4461994	...	87402584
sfr	31	31	...	31
Exp. b0	-2362232	-4461994	...	87402584
Exp. sfr	31	31	...	31

Test settings	
Tolerance b0	±0,0000e+00
Tolerance sfr	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block ul.

Test results				
Time step	1	2	...	37
Mask parameters				
Ki	-11	-10.389	...	11
ts_fact	1	2	...	37
Controller parameters				
b0	-2362232	-4461994	...	87402584
sfr	31	31	...	31
Exp. b0	-2362232	-4461994	...	87402584
Exp. sfr	31	31	...	31

Test settings	
Tolerance b0	±8,0000e+00
Tolerance sfr	±0,0000e+00

Test statistics	
Min CPU cycles	1528
Max CPU cycles	1722
Avg CPU cycles	1707

Verification: ul FiP32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for Control block ul.

Test results				
Time step	1	2	...	351
CPU cycles	77	59	...	113
Inputs				
In (DSP)	0	0	...	-536870912
Init (DSP)	236223201	236223201	...	236223201
Enable (DSP)	0	0	...	1
In	0	0	...	-0.25
Init	0.11	0.11	...	0.11
Enable	0	0	...	1
Parameters				
Ki	500			
ts_fact	1			
Outputs				
Out	0	0	...	-0.78
Exp. Out	0	0	...	-0.78
Out (DSP)	0	0	...	-1675037225
Exp. Out (DSP)	0	0	...	-1675037245

Test settings	
Tolerance Out	±1,1642e-08 (±25 LSB)

Test statistics	
Min CPU cycles	59
Max CPU cycles	119
Avg CPU cycles	112

Test case: Conversion test OK

Conversion test for Control block ul.

Test results				
Time step	1	2	...	37
Mask parameters				
Ki	-11	-10.389	...	11
ts_fact	1	2	...	37
Controller parameters				
b0	-2362232	-4461994	...	87402584
sfr	31	31	...	31
Exp. b0	-2362232	-4461994	...	87402584
Exp. sfr	31	31	...	31

Test settings	
Tolerance b0	±0,0000e+00
Tolerance sfr	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block ul.

Test results				
Time step	1	2	...	37
Mask parameters				
Ki	-11	-10.389	...	11
ts_fact	1	2	...	37
Controller parameters				
b0	-2362232	-4461994	...	87402584
sfr	31	31	...	31
Exp. b0	-2362232	-4461994	...	87402584
Exp. sfr	31	31	...	31

Test settings	
Tolerance b0	±8,0000e+00
Tolerance sfr	±0,0000e+00

Test statistics	
Min CPU cycles	1178
Max CPU cycles	1381
Avg CPU cycles	1209

Verification: ul FiP32 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for Control block ul.

Test results				
Time step	1	2	...	351
CPU cycles	66	66	...	122
Inputs				
In (DSP)	0	0	...	-536870912
Init (DSP)	236223201	236223201	...	236223201
Enable (DSP)	0	0	...	1
In	0	0	...	-0.25
Init	0.11	0.11	...	0.11
Enable	0	0	...	1
Parameters				
Ki	500			
ts_fact	1			
Outputs				
Out	0	0	...	-0.78
Exp. Out	0	0	...	-0.78
Out (DSP)	0	0	...	-1675037225
Exp. Out (DSP)	0	0	...	-1675037245

Test settings	
Tolerance Out	±1,1642e-08 (±25 LSB)

Test statistics	
Min CPU cycles	66
Max CPU cycles	129
Avg CPU cycles	121

Test case: Conversion test OK

Conversion test for Control block ul.

Test results				
Time step	1	2	...	37
Mask parameters				
Ki	-11	-10.389	...	11
ts_fact	1	2	...	37
Controller parameters				
b0	-2362232	-4461994	...	87402584
sfr	31	31	...	31
Exp. b0	-2362232	-4461994	...	87402584
Exp. sfr	31	31	...	31

Test settings	
Tolerance b0	±0,0000e+00
Tolerance sfr	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block ul.

Test results				
Time step	1	2	...	37
Mask parameters				
Ki	-11	-10.389	...	11
ts_fact	1	2	...	37
Controller parameters				
b0	-2362232	-4461994	...	87402584
sfr	31	31	...	31
Exp. b0	-2362232	-4461994	...	87402584
Exp. sfr	31	31	...	31

Test settings	
Tolerance b0	±8,0000e+00
Tolerance sfr	±0,0000e+00

Test statistics	
Min CPU cycles	1691
Max CPU cycles	1804
Avg CPU cycles	1794

Verification: ul FiP32 CPU dsPIC33EP256MC502

Date of Test	2026-06-23
Target controller	dsPIC33EP256MC502

Test case: Inport test

OK

Inport test for Control block ul.

Test results				
Time step	1	2	...	351
CPU cycles	53	53	...	207
Inputs				
In (DSP)	0	0	...	-536870912
Init (DSP)	236223201	236223201	...	236223201
Enable (DSP)	0	0	...	1
In	0	0	...	-0.25
Init	0.11	0.11	...	0.11
Enable	0	0	...	1
Parameters				
Ki	500			
ts_fact	1			
Outputs				
Out	0	0	...	-0.78
Exp. Out	0	0	...	-0.78
Out (DSP)	0	0	...	-1675037225
Exp. Out (DSP)	0	0	...	-1675037245

Test settings	
Tolerance Out	±1,1642e-08 (±25 LSB)

Test statistics	
Min CPU cycles	53
Max CPU cycles	207
Avg CPU cycles	203

Test case: Conversion test

OK

Conversion test for Control block ul.

Test results				
Time step	1	2	...	37
Mask parameters				
Ki	-11	-10.389	...	11
ts_fact	1	2	...	37
Controller parameters				
b0	-2362232	-4461994	...	87402584
sfr	31	31	...	31
Exp. b0	-2362232	-4461994	...	87402584
Exp. sfr	31	31	...	31

Test settings	
Tolerance b0	±0,0000e+00
Tolerance sfr	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block ul.

Test results				
Time step	1	2	...	37
Mask parameters				
Ki	-11	-10.389	...	11
ts_fact	1	2	...	37
Controller parameters				
b0	-2362232	-4461994	...	87402584
sfr	31	31	...	31
Exp. b0	-2362232	-4461994	...	87402584
Exp. sfr	31	31	...	31

Test settings	
Tolerance b0	±8,0000e+00
Tolerance sfr	±0,0000e+00

Test statistics	
Min CPU cycles	4539
Max CPU cycles	5609
Avg CPU cycles	5551

Verification: ul Float32 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test

OK

Inport test for Control block ul.

Test results				
Time step	1	2	...	401
CPU cycles	74	74	...	117
Inputs				
In (DSP)	0	0	...	-0.2
Init (DSP)	0.11	0.11	...	0.11
Enable (DSP)	0	0	...	1
In	0	0	...	-0.2
Init	0.11	0.11	...	0.11
Enable	0	0	...	1
Parameters				
Ki	500			
ts_fact	1			
Outputs				
Out	0	0	...	-1.82
Exp. Out	0	0	...	-1.82
Out (DSP)	0	0	...	-1.82
Exp. Out (DSP)	0	0	...	-1.82

Test settings	
Tolerance Out	±1,3970e-06 (±3000 LSB)

Test statistics	
Min CPU cycles	74
Max CPU cycles	117
Avg CPU cycles	116

Test case: Conversion test

OK

Conversion test for Control block ul.

Test results				
Time step	1	2	...	37
Mask parameters				
Ki	-11	-10.389	...	11
ts_fact	1	2	...	37
Controller parameters				
b0	-0.001	-0.002	...	0.041
Exp. b0	-0.001	-0.002	...	0.041

Test settings	
Tolerance b0	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block ul.

Test results				
Time step	1	2	...	37
Mask parameters				
Ki	-11	-10.389	...	11
ts_fact	1	2	...	37
Controller parameters				
b0	-0.001	-0.002	...	0.041
Exp. b0	-0.001	-0.002	...	0.041

Test settings	
Tolerance b0	±3,0000e-08

Test statistics	
Min CPU cycles	1495
Max CPU cycles	1518
Avg CPU cycles	1500

Verification: ul Float32 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for Control block ul.

Test results				
Time step	1	2	...	401
CPU cycles	41	41	...	79
Inputs				
In (DSP)	0	0	...	-0.2
Init (DSP)	0.11	0.11	...	0.11
Enable (DSP)	0	0	...	1
In	0	0	...	-0.2
Init	0.11	0.11	...	0.11
Enable	0	0	...	1
Parameters				
Ki	500			
ts_fact	1			
Outputs				
Out	0	0	...	-1.82
Exp. Out	0	0	...	-1.82
Out (DSP)	0	0	...	-1.82
Exp. Out (DSP)	0	0	...	-1.82

Test settings	
Tolerance Out	±1,3970e-06 (±3000 LSB)

Test statistics	
Min CPU cycles	41
Max CPU cycles	89
Avg CPU cycles	78

Test case: Conversion test OK

Conversion test for Control block ul.

Test results				
Time step	1	2	...	37
Mask parameters				
Ki	-11	-10.389	...	11
ts_fact	1	2	...	37
Controller parameters				
b0	-0.001	-0.002	...	0.041
Exp. b0	-0.001	-0.002	...	0.041

Test settings	
Tolerance b0	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block ul.

Test results				
Time step	1	2	...	37
Mask parameters				
Ki	-11	-10.389	...	11
ts_fact	1	2	...	37
Controller parameters				
b0	-0.001	-0.002	...	0.041
Exp. b0	-0.001	-0.002	...	0.041

Test settings	
Tolerance b0	±3,0000e-08

Test statistics	
Min CPU cycles	741
Max CPU cycles	741
Avg CPU cycles	741

Verification: ul Float32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for Control block ul.

Test results				
Time step	1	2	...	401
CPU cycles	73	73	...	123
Inputs				
In (DSP)	0	0	...	-0.2
Init (DSP)	0.11	0.11	...	0.11
Enable (DSP)	0	0	...	1
In	0	0	...	-0.2
Init	0.11	0.11	...	0.11
Enable	0	0	...	1
Parameters				
Ki	500			
ts_fact	1			
Outputs				
Out	0	0	...	-1.82
Exp. Out	0	0	...	-1.82
Out (DSP)	0	0	...	-1.82
Exp. Out (DSP)	0	0	...	-1.82

Test settings	
Tolerance Out	±1,3970e-06 (±3000 LSB)

Test statistics	
Min CPU cycles	73
Max CPU cycles	136
Avg CPU cycles	122

Test case: Conversion test OK

Conversion test for Control block ul.

Test results				
Time step	1	2	...	37
Mask parameters				
Ki	-11	-10.389	...	11
ts_fact	1	2	...	37
Controller parameters				
b0	-0.001	-0.002	...	0.041
Exp. b0	-0.001	-0.002	...	0.041

Test settings	
Tolerance b0	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block ul.

Test results				
Time step	1	2	...	37
Mask parameters				
Ki	-11	-10.389	...	11
ts_fact	1	2	...	37
Controller parameters				
b0	-0.001	-0.002	...	0.041
Exp. b0	-0.001	-0.002	...	0.041

Test settings	
Tolerance b0	±3,0000e-08

Test statistics	
Min CPU cycles	789
Max CPU cycles	834
Avg CPU cycles	822

Verification: ul Float32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for Control block ul.

Test results				
Time step	1	2	...	401
CPU cycles	66	66	...	562
Inputs				
In (DSP)	0	0	...	-0.2
Init (DSP)	0.11	0.11	...	0.11
Enable (DSP)	0	0	...	1
In	0	0	...	-0.2
Init	0.11	0.11	...	0.11
Enable	0	0	...	1
Parameters				
Ki	500			
ts_fact	1			
Outputs				
Out	0	0	...	-1.82
Exp. Out	0	0	...	-1.82
Out (DSP)	0	0	...	-1.82
Exp. Out (DSP)	0	0	...	-1.82

Test settings	
Tolerance Out	±1,3970e-06 (±3000 LSB)

Test statistics	
Min CPU cycles	66
Max CPU cycles	628
Avg CPU cycles	560

Test case: Conversion test OK

Conversion test for Control block ul.

Test results				
Time step	1	2	...	37
Mask parameters				
Ki	-11	-10.389	...	11
ts_fact	1	2	...	37
Controller parameters				
b0	-0.001	-0.002	...	0.041
Exp. b0	-0.001	-0.002	...	0.041

Test settings	
Tolerance b0	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block ul.

Test results				
Time step	1	2	...	37
Mask parameters				
Ki	-11	-10.389	...	11
ts_fact	1	2	...	37
Controller parameters				
b0	-0.001	-0.002	...	0.041
Exp. b0	-0.001	-0.002	...	0.041

Test settings	
Tolerance b0	±3,0000e-08

Test statistics	
Min CPU cycles	1589
Max CPU cycles	1724
Avg CPU cycles	1670

Verification: ul Float32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for Control block ul.

Test results				
Time step	1	2	...	401
CPU cycles	57	57	...	256
Inputs				
In (DSP)	0	0	...	-0.2
Init (DSP)	0.11	0.11	...	0.11
Enable (DSP)	0	0	...	1
In	0	0	...	-0.2
Init	0.11	0.11	...	0.11
Enable	0	0	...	1
Parameters				
Ki	500			
ts_fact	1			
Outputs				
Out	0	0	...	-1.82
Exp. Out	0	0	...	-1.82
Out (DSP)	0	0	...	-1.82
Exp. Out (DSP)	0	0	...	-1.82

Test settings	
Tolerance Out	±1,3970e-06 (±3000 LSB)

Test statistics	
Min CPU cycles	57
Max CPU cycles	264
Avg CPU cycles	254

Test case: Conversion test OK

Conversion test for Control block ul.

Test results				
Time step	1	2	...	37
Mask parameters				
Ki	-11	-10.389	...	11
ts_fact	1	2	...	37
Controller parameters				
b0	-0.001	-0.002	...	0.041
Exp. b0	-0.001	-0.002	...	0.041

Test settings	
Tolerance b0	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block ul.

Test results				
Time step	1	2	...	37
Mask parameters				
Ki	-11	-10.389	...	11
ts_fact	1	2	...	37
Controller parameters				
b0	-0.001	-0.002	...	0.041
Exp. b0	-0.001	-0.002	...	0.041

Test settings	
Tolerance b0	±3,0000e-08

Test statistics	
Min CPU cycles	583
Max CPU cycles	602
Avg CPU cycles	597

Verification: ul Float32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for Control block ul.

Test results				
Time step	1	2	...	401
CPU cycles	77	60	...	95
Inputs				
In (DSP)	0	0	...	-0.2
Init (DSP)	0.11	0.11	...	0.11
Enable (DSP)	0	0	...	1
In	0	0	...	-0.2
Init	0.11	0.11	...	0.11
Enable	0	0	...	1
Parameters				
Ki	500			
ts_fact	1			
Outputs				
Out	0	0	...	-1.82
Exp. Out	0	0	...	-1.82
Out (DSP)	0	0	...	-1.82
Exp. Out (DSP)	0	0	...	-1.82

Test settings	
Tolerance Out	±1,3970e-06 (±3000 LSB)

Test statistics	
Min CPU cycles	60
Max CPU cycles	122
Avg CPU cycles	94

Test case: Conversion test OK

Conversion test for Control block ul.

Test results				
Time step	1	2	...	37
Mask parameters				
Ki	-11	-10.389	...	11
ts_fact	1	2	...	37
Controller parameters				
b0	-0.001	-0.002	...	0.041
Exp. b0	-0.001	-0.002	...	0.041

Test settings	
Tolerance b0	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block ul.

Test results				
Time step	1	2	...	37
Mask parameters				
Ki	-11	-10.389	...	11
ts_fact	1	2	...	37
Controller parameters				
b0	-0.001	-0.002	...	0.041
Exp. b0	-0.001	-0.002	...	0.041

Test settings	
Tolerance b0	±3,0000e-08

Test statistics	
Min CPU cycles	595
Max CPU cycles	715
Avg CPU cycles	615

Verification: ul Float32 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for Control block ul.

Test results				
Time step	1	2	...	401
CPU cycles	62	62	...	121
Inputs				
In (DSP)	0	0	...	-0.2
Init (DSP)	0.11	0.11	...	0.11
Enable (DSP)	0	0	...	1
In	0	0	...	-0.2
Init	0.11	0.11	...	0.11
Enable	0	0	...	1
Parameters				
Ki	500			
ts_fact	1			
Outputs				
Out	0	0	...	-1.82
Exp. Out	0	0	...	-1.82
Out (DSP)	0	0	...	-1.82
Exp. Out (DSP)	0	0	...	-1.82

Test settings	
Tolerance Out	±1,3970e-06 (±3000 LSB)

Test statistics	
Min CPU cycles	62
Max CPU cycles	121
Avg CPU cycles	120

Test case: Conversion test OK

Conversion test for Control block ul.

Test results				
Time step	1	2	...	37
Mask parameters				
Ki	-11	-10.389	...	11
ts_fact	1	2	...	37
Controller parameters				
b0	-0.001	-0.002	...	0.041
Exp. b0	-0.001	-0.002	...	0.041

Test settings	
Tolerance b0	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block ul.

Test results				
Time step	1	2	...	37
Mask parameters				
Ki	-11	-10.389	...	11
ts_fact	1	2	...	37
Controller parameters				
b0	-0.001	-0.002	...	0.041
Exp. b0	-0.001	-0.002	...	0.041

Test settings	
Tolerance b0	±3,0000e-08

Test statistics	
Min CPU cycles	1156
Max CPU cycles	1172
Avg CPU cycles	1158

Verification: ul Float32 CPU dsPIC33EP256MC502

Date of Test	2026-06-23
Target controller	dsPIC33EP256MC502

Test case: Inport test

OK

Inport test for Control block ul.

Test results				
Time step	1	2	...	401
CPU cycles	55	55	...	655
Inputs				
In (DSP)	0	0	...	-0.2
Init (DSP)	0.11	0.11	...	0.11
Enable (DSP)	0	0	...	1
In	0	0	...	-0.2
Init	0.11	0.11	...	0.11
Enable	0	0	...	1
Parameters				
Ki	500			
ts_fact	1			
Outputs				
Out	0	0	...	-1.82
Exp. Out	0	0	...	-1.82
Out (DSP)	0	0	...	-1.82
Exp. Out (DSP)	0	0	...	-1.82

Test settings	
Tolerance Out	±1,3970e-06 (±3000 LSB)

Test statistics	
Min CPU cycles	55
Max CPU cycles	803
Avg CPU cycles	639

Test case: Conversion test

OK

Conversion test for Control block ul.

Test results				
Time step	1	2	...	37
Mask parameters				
Ki	-11	-10.389	...	11
ts_fact	1	2	...	37
Controller parameters				
b0	-0.001	-0.002	...	0.041
Exp. b0	-0.001	-0.002	...	0.041

Test settings	
Tolerance b0	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Control block ul.

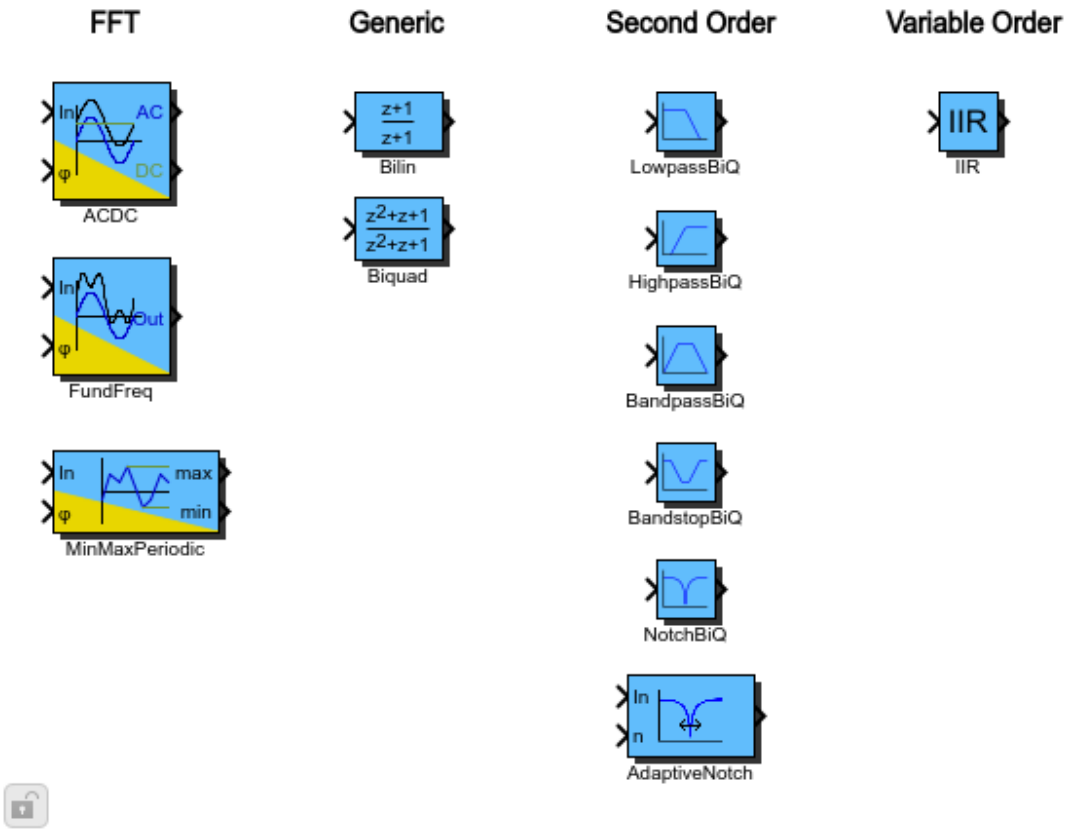
Test results				
Time step	1	2	...	37
Mask parameters				
Ki	-11	-10.389	...	11
ts_fact	1	2	...	37
Controller parameters				
b0	-0.001	-0.002	...	0.041
Exp. b0	-0.001	-0.002	...	0.041

Test settings	
Tolerance b0	±3,0000e-08

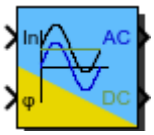
Test statistics	
Min CPU cycles	2155
Max CPU cycles	2551
Avg CPU cycles	2531

4 Filter

Library with various kinds of digital filter blocks.



Block: ACDC



Calculation of AC and DC part of input signal.

Inports	
In	Input signal
phi	Angle signal

Outports	
AC	AC part of input signal
DC	DC part of input signal

Mask Parameters		
Name	**ID**	**Description**
ts_fact	1	Multiplication factor of base sampling time (in integer format)

Implementations:

FiP16	16 Bit Fixed Point Implementation
FiP32	32 Bit Fixed Point Implementation
Float32	32 Bit Floating Point Implementation
Float64	64 Bit Floating Point Implementation

Implementation: FiP16

16 Bit Fixed Point Implementation

Inports Data Type	
In	int16
phi	int16

Outports Data Type	
AC	int16
DC	int16

Implementation: FiP32

32 Bit Fixed Point Implementation

Inports Data Type	
In	int32
phi	int32

Outports Data Type	
AC	int32
DC	int32

Implementation: Float32

32 Bit Floating Point Implementation

Inports Data Type	
In	float32
phi	float32

Outports Data Type	
AC	float32
DC	float32

Implementation: Float64

64 Bit Floating Point Implementation

Inports Data Type	
In	float64
phi	float64

Outports Data Type	
AC	float64
DC	float64

Verification: ACDC FiP16 CPU TMS320F28335

Date of Test 2026-06-25

Target controller TMS320F28335

Test case: Inport test OK

Inport test for Filter block ACDC.

Test results						
Time step	1	2	3	4	...	111
CPU cycles	134	134	134	134	...	134
Inputs						
In (DSP)	9830	7061	4372	1840	...	12599
phi (DSP)	-32768	-30997	-29226	-27454	...	30997
In	0.3	0.215	0.133	0.056	...	0.385
phi	-1	-0.946	-0.892	-0.838	...	0.946
Parameters						
ts_fact	1					
Outputs						
AC	0.3	0.215	0.133	0.056	...	0.085
DC	0	0	0	0	...	0.3
Exp. AC	0.3	0.215	0.133	0.056	...	0.085
Exp. DC	0	0	0	0	...	0.3
AC (DSP)	9830	7061	4372	1840	...	2769
DC (DSP)	0	0	0	0	...	9830
Exp. AC (DSP)	9830	7061	4372	1840	...	2769
Exp. DC (DSP)	0	0	0	0	...	9830

Test settings	
Tolerance AC	±3,0518e-05 (±1 LSB)
Tolerance DC	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	134
Max CPU cycles	228
Avg CPU cycles	135

Verification: ACDC FiP16 CPU TM4C123GH6

Date of Test 2026-06-25

Target controller TM4C123GH6

Test case: Inport test OK

Inport test for Filter block ACDC.

Test results						
Time step	1	2	3	4	...	111
CPU cycles	81	81	81	81	...	81
Inputs						
In (DSP)	9830	7061	4372	1840	...	12599
phi (DSP)	-32768	-30997	-29226	-27454	...	30997
In	0.3	0.215	0.133	0.056	...	0.385
phi	-1	-0.946	-0.892	-0.838	...	0.946
Parameters						
ts_fact	1					
Outputs						
AC	0.3	0.215	0.133	0.056	...	0.085
DC	0	0	0	0	...	0.3
Exp. AC	0.3	0.215	0.133	0.056	...	0.085
Exp. DC	0	0	0	0	...	0.3
AC (DSP)	9830	7061	4372	1840	...	2769
DC (DSP)	0	0	0	0	...	9830
Exp. AC (DSP)	9830	7061	4372	1840	...	2769
Exp. DC (DSP)	0	0	0	0	...	9830

Test settings	
Tolerance AC	±3,0518e-05 (±1 LSB)
Tolerance DC	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	81
Max CPU cycles	101
Avg CPU cycles	81

Verification: ACDC FiP16 CPU STM32G474RE

Date of Test	2026-06-25
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for Filter block ACDC.

Test results						
Time step	1	2	3	4	...	111
CPU cycles	114	114	114	114	...	114
Inputs						
In (DSP)	9830	7061	4372	1840	...	12599
phi (DSP)	-32768	-30997	-29226	-27454	...	30997
In	0.3	0.215	0.133	0.056	...	0.385
phi	-1	-0.946	-0.892	-0.838	...	0.946
Parameters						
ts_fact	1					
Outputs						
AC	0.3	0.215	0.133	0.056	...	0.085
DC	0	0	0	0	...	0.3
Exp. AC	0.3	0.215	0.133	0.056	...	0.085
Exp. DC	0	0	0	0	...	0.3
AC (DSP)	9830	7061	4372	1840	...	2769
DC (DSP)	0	0	0	0	...	9830
Exp. AC (DSP)	9830	7061	4372	1840	...	2769
Exp. DC (DSP)	0	0	0	0	...	9830

Test settings	
Tolerance AC	±3,0518e-05 (±1 LSB)
Tolerance DC	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	114
Max CPU cycles	149
Avg CPU cycles	114

Verification: ACDC FiP16 CPU STM32F072RB

Date of Test 2026-06-25

Target controller STM32F072RB

Test case: Inport test OK

Inport test for Filter block ACDC.

Test results						
Time step	1	2	3	4	...	111
CPU cycles	114	114	114	114	...	114
Inputs						
In (DSP)	9830	7061	4372	1840	...	12599
phi (DSP)	-32768	-30997	-29226	-27454	...	30997
In	0.3	0.215	0.133	0.056	...	0.385
phi	-1	-0.946	-0.892	-0.838	...	0.946
Parameters						
ts_fact	1					
Outputs						
AC	0.3	0.215	0.133	0.056	...	0.085
DC	0	0	0	0	...	0.3
Exp. AC	0.3	0.215	0.133	0.056	...	0.085
Exp. DC	0	0	0	0	...	0.3
AC (DSP)	9830	7061	4372	1840	...	2769
DC (DSP)	0	0	0	0	...	9830
Exp. AC (DSP)	9830	7061	4372	1840	...	2769
Exp. DC (DSP)	0	0	0	0	...	9830

Test settings	
Tolerance AC	±3,0518e-05 (±1 LSB)
Tolerance DC	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	114
Max CPU cycles	268
Avg CPU cycles	117

Verification: ACDC FiP16 CPU PIC32MX170F256

Date of Test 2026-06-25

Target controller PIC32MX170F256

Test case: Inport test OK

Inport test for Filter block ACDC.

Test results						
Time step	1	2	3	4	...	111
CPU cycles	70	70	70	70	...	70
Inputs						
In (DSP)	9830	7061	4372	1840	...	12599
phi (DSP)	-32768	-30997	-29226	-27454	...	30997
In	0.3	0.215	0.133	0.056	...	0.385
phi	-1	-0.946	-0.892	-0.838	...	0.946
Parameters						
ts_fact	1					
Outputs						
AC	0.3	0.215	0.133	0.056	...	0.085
DC	0	0	0	0	...	0.3
Exp. AC	0.3	0.215	0.133	0.056	...	0.085
Exp. DC	0	0	0	0	...	0.3
AC (DSP)	9830	7061	4372	1840	...	2769
DC (DSP)	0	0	0	0	...	9830
Exp. AC (DSP)	9830	7061	4372	1840	...	2769
Exp. DC (DSP)	0	0	0	0	...	9830

Test settings	
Tolerance AC	±3,0518e-05 (±1 LSB)
Tolerance DC	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	70
Max CPU cycles	111
Avg CPU cycles	70

Verification: ACDC FiP16 CPU dsPIC33EP256MC502

Date of Test 2026-06-25

Target controller dsPIC33EP256MC502

Test case: Inport test OK

Inport test for Filter block ACDC.

Test results						
Time step	1	2	3	4	...	111
CPU cycles	106	97	97	97	...	97
Inputs						
In (DSP)	9830	7061	4372	1840	...	12599
phi (DSP)	-32768	-30997	-29226	-27454	...	30997
In	0.3	0.215	0.133	0.056	...	0.385
phi	-1	-0.946	-0.892	-0.838	...	0.946
Parameters						
ts_fact	1					
Outputs						
AC	0.3	0.215	0.133	0.056	...	0.085
DC	0	0	0	0	...	0.3
Exp. AC	0.3	0.215	0.133	0.056	...	0.085
Exp. DC	0	0	0	0	...	0.3
AC (DSP)	9830	7061	4372	1840	...	2769
DC (DSP)	0	0	0	0	...	9830
Exp. AC (DSP)	9830	7061	4372	1840	...	2769
Exp. DC (DSP)	0	0	0	0	...	9830

Test settings	
Tolerance AC	±3,0518e-05 (±1 LSB)
Tolerance DC	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	97
Max CPU cycles	683
Avg CPU cycles	107

Verification: ACDC FiP16 CPU XMC4800-F144K2048

Date of Test	2026-06-25
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for Filter block ACDC.

Test results						
Time step	1	2	3	4	...	111
CPU cycles	115	102	102	102	...	102
Inputs						
In (DSP)	9830	7061	4372	1840	...	12599
phi (DSP)	-32768	-30997	-29226	-27454	...	30997
In	0.3	0.215	0.133	0.056	...	0.385
phi	-1	-0.946	-0.892	-0.838	...	0.946
Parameters						
ts_fact	1					
Outputs						
AC	0.3	0.215	0.133	0.056	...	0.085
DC	0	0	0	0	...	0.3
Exp. AC	0.3	0.215	0.133	0.056	...	0.085
Exp. DC	0	0	0	0	...	0.3
AC (DSP)	9830	7061	4372	1840	...	2769
DC (DSP)	0	0	0	0	...	9830
Exp. AC (DSP)	9830	7061	4372	1840	...	2769
Exp. DC (DSP)	0	0	0	0	...	9830

Test settings	
Tolerance AC	±3,0518e-05 (±1 LSB)
Tolerance DC	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	102
Max CPU cycles	131
Avg CPU cycles	102

Verification: ACDC FiP16 CPU TMS320F28379D

Date of Test 2026-06-25

Target controller TMS320F28379D

Test case: Inport test OK

Inport test for Filter block ACDC.

Test results						
Time step	1	2	3	4	...	111
CPU cycles	140	137	137	137	...	137
Inputs						
In (DSP)	9830	7061	4372	1840	...	12599
phi (DSP)	-32768	-30997	-29226	-27454	...	30997
In	0.3	0.215	0.133	0.056	...	0.385
phi	-1	-0.946	-0.892	-0.838	...	0.946
Parameters						
ts_fact	1					
Outputs						
AC	0.3	0.215	0.133	0.056	...	0.085
DC	0	0	0	0	...	0.3
Exp. AC	0.3	0.215	0.133	0.056	...	0.085
Exp. DC	0	0	0	0	...	0.3
AC (DSP)	9830	7061	4372	1840	...	2769
DC (DSP)	0	0	0	0	...	9830
Exp. AC (DSP)	9830	7061	4372	1840	...	2769
Exp. DC (DSP)	0	0	0	0	...	9830

Test settings	
Tolerance AC	±3,0518e-05 (±1 LSB)
Tolerance DC	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	137
Max CPU cycles	234
Avg CPU cycles	138

Verification: ACDC FiP32 CPU TMS320F28335

Date of Test 2026-06-25

Target controller TMS320F28335

Test case: Inport test OK

Inport test for Filter block ACDC.

Test results				
Time step	1	2	...	111
CPU cycles	290	289	...	289
Inputs				
In (DSP)	644245094	462781845	...	825708343
phi (DSP)	-2147483648	-2031403451	...	2031403451
In	0.3	0.215	...	0.385
phi	-1	-0.946	...	0.946
Parameters				
ts_fact	1			
Outputs				
AC	0.3	0.215	...	0.085
DC	0	0	...	0.3
Exp. AC	0.3	0.215	...	0.085
Exp. DC	0	0	...	0.3
AC (DSP)	644245094	462781845	...	181463249
DC (DSP)	0	0	...	644245094
Exp. AC (DSP)	644245094	462781845	...	181463249
Exp. DC (DSP)	0	0	...	644245094

Test settings	
Tolerance AC	±4,6566e-10 (±1 LSB)
Tolerance DC	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	289
Max CPU cycles	635
Avg CPU cycles	295

Verification: ACDC FiP32 CPU TM4C123GH6

Date of Test	2026-06-25
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for Filter block ACDC.

Test results				
Time step	1	2	...	111
CPU cycles	119	119	...	119
Inputs				
In (DSP)	644245094	462781845	...	825708343
phi (DSP)	-2147483648	-2031403451	...	2031403451
In	0.3	0.215	...	0.385
phi	-1	-0.946	...	0.946
Parameters				
ts_fact	1			
Outputs				
AC	0.3	0.215	...	0.085
DC	0	0	...	0.3
Exp. AC	0.3	0.215	...	0.085
Exp. DC	0	0	...	0.3
AC (DSP)	644245094	462781845	...	181463249
DC (DSP)	0	0	...	644245094
Exp. AC (DSP)	644245094	462781845	...	181463249
Exp. DC (DSP)	0	0	...	644245094

Test settings	
Tolerance AC	±4,6566e-10 (±1 LSB)
Tolerance DC	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	119
Max CPU cycles	641
Avg CPU cycles	128

Verification: ACDC FiP32 CPU STM32G474RE

Date of Test	2026-06-25
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for Filter block ACDC.

Test results				
Time step	1	2	...	111
CPU cycles	138	138	...	138
Inputs				
In (DSP)	644245094	462781845	...	825708343
phi (DSP)	-2147483648	-2031403451	...	2031403451
In	0.3	0.215	...	0.385
phi	-1	-0.946	...	0.946
Parameters				
ts_fact	1			
Outputs				
AC	0.3	0.215	...	0.085
DC	0	0	...	0.3
Exp. AC	0.3	0.215	...	0.085
Exp. DC	0	0	...	0.3
AC (DSP)	644245094	462781845	...	181463249
DC (DSP)	0	0	...	644245094
Exp. AC (DSP)	644245094	462781845	...	181463249
Exp. DC (DSP)	0	0	...	644245094

Test settings	
Tolerance AC	±4,6566e-10 (±1 LSB)
Tolerance DC	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	138
Max CPU cycles	363
Avg CPU cycles	142

Verification: ACDC FiP32 CPU STM32F072RB

Date of Test	2026-06-25
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for Filter block ACDC.

Test results				
Time step	1	2	...	111
CPU cycles	169	169	...	169
Inputs				
In (DSP)	644245094	462781845	...	825708343
phi (DSP)	-2147483648	-2031403451	...	2031403451
In	0.3	0.215	...	0.385
phi	-1	-0.946	...	0.946
Parameters				
ts_fact	1			
Outputs				
AC	0.3	0.215	...	0.085
DC	0	0	...	0.3
Exp. AC	0.3	0.215	...	0.085
Exp. DC	0	0	...	0.3
AC (DSP)	644245094	462781845	...	181463249
DC (DSP)	0	0	...	644245094
Exp. AC (DSP)	644245094	462781845	...	181463249
Exp. DC (DSP)	0	0	...	644245094

Test settings	
Tolerance AC	±4,6566e-10 (±1 LSB)
Tolerance DC	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	169
Max CPU cycles	1092
Avg CPU cycles	188

Verification: ACDC FiP32 CPU PIC32MX170F256

Date of Test 2026-06-25

Target controller PIC32MX170F256

Test case: Inport test OK

Inport test for Filter block ACDC.

Test results				
Time step	1	2	...	111
CPU cycles	118	114	...	114
Inputs				
In (DSP)	644245094	462781845	...	825708343
phi (DSP)	-2147483648	-2031403451	...	2031403451
In	0.3	0.215	...	0.385
phi	-1	-0.946	...	0.946
Parameters				
ts_fact	1			
Outputs				
AC	0.3	0.215	...	0.085
DC	0	0	...	0.3
Exp. AC	0.3	0.215	...	0.085
Exp. DC	0	0	...	0.3
AC (DSP)	644245094	462781845	...	181463249
DC (DSP)	0	0	...	644245094
Exp. AC (DSP)	644245094	462781845	...	181463249
Exp. DC (DSP)	0	0	...	644245094

Test settings	
Tolerance AC	±4,6566e-10 (±1 LSB)
Tolerance DC	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	113
Max CPU cycles	258
Avg CPU cycles	116

Verification: ACDC FiP32 CPU dsPIC33EP256MC502

Date of Test	2026-06-25
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for Filter block ACDC.

Test results				
Time step	1	2	...	111
CPU cycles	148	135	...	135
Inputs				
In (DSP)	644245094	462781845	...	825708343
phi (DSP)	-2147483648	-2031403451	...	2031403451
In	0.3	0.215	...	0.385
phi	-1	-0.946	...	0.946
Parameters				
ts_fact	1			
Outputs				
AC	0.3	0.215	...	0.085
DC	0	0	...	0.3
Exp. AC	0.3	0.215	...	0.085
Exp. DC	0	0	...	0.3
AC (DSP)	644245094	462781845	...	181463249
DC (DSP)	0	0	...	644245094
Exp. AC (DSP)	644245094	462781845	...	181463249
Exp. DC (DSP)	0	0	...	644245094

Test settings	
Tolerance AC	±4,6566e-10 (±1 LSB)
Tolerance DC	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	135
Max CPU cycles	9778
Avg CPU cycles	308

Verification: ACDC FiP32 CPU XMC4800-F144K2048

Date of Test	2026-06-25
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for Filter block ACDC.

Test results				
Time step	1	2	...	111
CPU cycles	173	133	...	133
Inputs				
In (DSP)	644245094	462781845	...	825708343
phi (DSP)	-2147483648	-2031403451	...	2031403451
In	0.3	0.215	...	0.385
phi	-1	-0.946	...	0.946
Parameters				
ts_fact	1			
Outputs				
AC	0.3	0.215	...	0.085
DC	0	0	...	0.3
Exp. AC	0.3	0.215	...	0.085
Exp. DC	0	0	...	0.3
AC (DSP)	644245094	462781845	...	181463249
DC (DSP)	0	0	...	644245094
Exp. AC (DSP)	644245094	462781845	...	181463249
Exp. DC (DSP)	0	0	...	644245094

Test settings	
Tolerance AC	±4,6566e-10 (±1 LSB)
Tolerance DC	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	133
Max CPU cycles	423
Avg CPU cycles	137

Verification: ACDC FiP32 CPU TMS320F28379D

Date of Test	2026-06-25
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for Filter block ACDC.

Test results				
Time step	1	2	...	111
CPU cycles	277	274	...	274
Inputs				
In (DSP)	644245094	462781845	...	825708343
phi (DSP)	-2147483648	-2031403451	...	2031403451
In	0.3	0.215	...	0.385
phi	-1	-0.946	...	0.946
Parameters				
ts_fact	1			
Outputs				
AC	0.3	0.215	...	0.085
DC	0	0	...	0.3
Exp. AC	0.3	0.215	...	0.085
Exp. DC	0	0	...	0.3
AC (DSP)	644245094	462781845	...	181463249
DC (DSP)	0	0	...	644245094
Exp. AC (DSP)	644245094	462781845	...	181463249
Exp. DC (DSP)	0	0	...	644245094

Test settings	
Tolerance AC	±4,6566e-10 (±1 LSB)
Tolerance DC	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	274
Max CPU cycles	581
Avg CPU cycles	279

Verification: ACDC Float32 CPU TMS320F28335

Date of Test	2026-06-25
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for Filter block ACDC.

Test results				
Time step	1	2	...	111
CPU cycles	112	112	...	112
Inputs				
In (DSP)	1.59	1.142	...	2.038
phi (DSP)	-3.142	-2.972	...	2.972
In	1.59	1.142	...	2.038
phi	-3.142	-2.972	...	2.972
Parameters				
ts_fact	1			
Outputs				
AC	1.59	1.142	...	0.448
DC	0	0	...	1.59
Exp. AC	1.59	1.142	...	0.448
Exp. DC	0	0	...	1.59
AC (DSP)	1.59	1.142	...	0.448
DC (DSP)	0	0	...	1.59
Exp. AC (DSP)	1.59	1.142	...	0.448
Exp. DC (DSP)	0	0	...	1.59

Test settings	
Tolerance AC	±4,6566e-07 (±1000 LSB)
Tolerance DC	±2,3283e-07 (±500 LSB)

Test statistics	
Min CPU cycles	112
Max CPU cycles	377
Avg CPU cycles	116

Verification: ACDC Float32 CPU TM4C123GH6

Date of Test	2026-06-25
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for Filter block ACDC.

Test results				
Time step	1	2	...	111
CPU cycles	81	81	...	81
Inputs				
In (DSP)	1.59	1.142	...	2.038
phi (DSP)	-3.142	-2.972	...	2.972
In	1.59	1.142	...	2.038
phi	-3.142	-2.972	...	2.972
Parameters				
ts_fact	1			
Outputs				
AC	1.59	1.142	...	0.448
DC	0	0	...	1.59
Exp. AC	1.59	1.142	...	0.448
Exp. DC	0	0	...	1.59
AC (DSP)	1.59	1.142	...	0.448
DC (DSP)	0	0	...	1.59
Exp. AC (DSP)	1.59	1.142	...	0.448
Exp. DC (DSP)	0	0	...	1.59

Test settings	
Tolerance AC	±4,6566e-07 (±1000 LSB)
Tolerance DC	±2,3283e-07 (±500 LSB)

Test statistics	
Min CPU cycles	81
Max CPU cycles	101
Avg CPU cycles	81

Verification: ACDC Float32 CPU STM32G474RE

Date of Test	2026-06-25
Target controller	STM32G474RE

Test case: Inport test

OK

Inport test for Filter block ACDC.

Test results				
Time step	1	2	...	111
CPU cycles	113	113	...	113
Inputs				
In (DSP)	1.59	1.142	...	2.038
phi (DSP)	-3.142	-2.972	...	2.972
In	1.59	1.142	...	2.038
phi	-3.142	-2.972	...	2.972
Parameters				
ts_fact	1			
Outputs				
AC	1.59	1.142	...	0.448
DC	0	0	...	1.59
Exp. AC	1.59	1.142	...	0.448
Exp. DC	0	0	...	1.59
AC (DSP)	1.59	1.142	...	0.448
DC (DSP)	0	0	...	1.59
Exp. AC (DSP)	1.59	1.142	...	0.448
Exp. DC (DSP)	0	0	...	1.59

Test settings	
Tolerance AC	±4,6566e-07 (±1000 LSB)
Tolerance DC	±2,3283e-07 (±500 LSB)

Test statistics	
Min CPU cycles	113
Max CPU cycles	143
Avg CPU cycles	113

Verification: ACDC Float32 CPU STM32F072RB

Date of Test	2026-06-25
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for Filter block ACDC.

Test results				
Time step	1	2	...	111
CPU cycles	525	612	...	696
Inputs				
In (DSP)	1.59	1.142	...	2.038
phi (DSP)	-3.142	-2.972	...	2.972
In	1.59	1.142	...	2.038
phi	-3.142	-2.972	...	2.972
Parameters				
ts_fact	1			
Outputs				
AC	1.59	1.142	...	0.448
DC	0	0	...	1.59
Exp. AC	1.59	1.142	...	0.448
Exp. DC	0	0	...	1.59
AC (DSP)	1.59	1.142	...	0.448
DC (DSP)	0	0	...	1.59
Exp. AC (DSP)	1.59	1.142	...	0.448
Exp. DC (DSP)	0	0	...	1.59

Test settings	
Tolerance AC	±4,6566e-07 (±1000 LSB)
Tolerance DC	±2,3283e-07 (±500 LSB)

Test statistics	
Min CPU cycles	525
Max CPU cycles	1298
Avg CPU cycles	684

Verification: ACDC Float32 CPU PIC32MX170F256

Date of Test	2026-06-25
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for Filter block ACDC.

Test results				
Time step	1	2	...	111
CPU cycles	242	301	...	320
Inputs				
In (DSP)	1.59	1.142	...	2.038
phi (DSP)	-3.142	-2.972	...	2.972
In	1.59	1.142	...	2.038
phi	-3.142	-2.972	...	2.972
Parameters				
ts_fact	1			
Outputs				
AC	1.59	1.142	...	0.448
DC	0	0	...	1.59
Exp. AC	1.59	1.142	...	0.448
Exp. DC	0	0	...	1.59
AC (DSP)	1.59	1.142	...	0.448
DC (DSP)	0	0	...	1.59
Exp. AC (DSP)	1.59	1.142	...	0.448
Exp. DC (DSP)	0	0	...	1.59

Test settings	
Tolerance AC	±4,6566e-07 (±1000 LSB)
Tolerance DC	±2,3283e-07 (±500 LSB)

Test statistics	
Min CPU cycles	242
Max CPU cycles	514
Avg CPU cycles	318

Verification: ACDC Float32 CPU dsPIC33EP256MC502

Date of Test	2026-06-25
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for Filter block ACDC.

Test results				
Time step	1	2	...	111
CPU cycles	640	781	...	911
Inputs				
In (DSP)	1.59	1.142	...	2.038
phi (DSP)	-3.142	-2.972	...	2.972
In	1.59	1.142	...	2.038
phi	-3.142	-2.972	...	2.972
Parameters				
ts_fact	1			
Outputs				
AC	1.59	1.142	...	0.448
DC	0	0	...	1.59
Exp. AC	1.59	1.142	...	0.448
Exp. DC	0	0	...	1.59
AC (DSP)	1.59	1.142	...	0.448
DC (DSP)	0	0	...	1.59
Exp. AC (DSP)	1.59	1.142	...	0.448
Exp. DC (DSP)	0	0	...	1.59

Test settings	
Tolerance AC	±4,6566e-07 (±1000 LSB)
Tolerance DC	±2,3283e-07 (±500 LSB)

Test statistics	
Min CPU cycles	640
Max CPU cycles	1870
Avg CPU cycles	852

Verification: ACDC Float32 CPU XMC4800-F144K2048

Date of Test	2026-06-25
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for Filter block ACDC.

Test results				
Time step	1	2	...	111
CPU cycles	126	104	...	104
Inputs				
In (DSP)	1.59	1.142	...	2.038
phi (DSP)	-3.142	-2.972	...	2.972
In	1.59	1.142	...	2.038
phi	-3.142	-2.972	...	2.972
Parameters				
ts_fact	1			
Outputs				
AC	1.59	1.142	...	0.448
DC	0	0	...	1.59
Exp. AC	1.59	1.142	...	0.448
Exp. DC	0	0	...	1.59
AC (DSP)	1.59	1.142	...	0.448
DC (DSP)	0	0	...	1.59
Exp. AC (DSP)	1.59	1.142	...	0.448
Exp. DC (DSP)	0	0	...	1.59

Test settings	
Tolerance AC	±4,6566e-07 (±1000 LSB)
Tolerance DC	±2,3283e-07 (±500 LSB)

Test statistics	
Min CPU cycles	104
Max CPU cycles	126
Avg CPU cycles	104

Verification: ACDC Float32 CPU TMS320F28379D

Date of Test	2026-06-25
Target controller	TMS320F28379D

Test case: Inport test OK

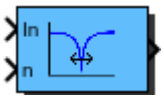
Inport test for Filter block ACDC.

Test results				
Time step	1	2	...	111
CPU cycles	114	114	...	114
Inputs				
In (DSP)	1.59	1.142	...	2.038
phi (DSP)	-3.142	-2.972	...	2.972
In	1.59	1.142	...	2.038
phi	-3.142	-2.972	...	2.972
Parameters				
ts_fact	1			
Outputs				
AC	1.59	1.142	...	0.448
DC	0	0	...	1.59
Exp. AC	1.59	1.142	...	0.448
Exp. DC	0	0	...	1.59
AC (DSP)	1.59	1.142	...	0.448
DC (DSP)	0	0	...	1.59
Exp. AC (DSP)	1.59	1.142	...	0.448
Exp. DC (DSP)	0	0	...	1.59

Test settings	
Tolerance AC	±4,6566e-07 (±1000 LSB)
Tolerance DC	±2,3283e-07 (±500 LSB)

Test statistics	
Min CPU cycles	114
Max CPU cycles	361
Avg CPU cycles	118

Block: AdaptiveNotch



Notch filter with variable notch frequency

Inports	
In	Input signal
n	Speed input = notch frequency

Outports	
Out	Filtered output signal

Mask Parameters		
Name	**ID**	**Description**
Q	1	Q-Factor of the notch filter
n_thresh	2	Speed threshold for activating the filter
n_max	3	Maximum revolutions per minute (Not used in floating point implementations)
p	4	Number of pole pairs
ts_fact	5	Multiplication factor of base sampling time (in integer format)
method	6	Discretization method

Description:

Calculation:

$$\mathrm{Out(k)} = \begin{cases} \mathrm{In(k)} & \mathrm{n(k)} \leq \mathrm{n_{thresh}} \\ \mathrm{In(k)} \cdot \mathrm{H(z)} & \mathrm{n(k)} > \mathrm{n_{thresh}} \end{cases}$$

The transfer function H(z) of the filter is

$$H(z) = \frac{b_0 + b_1 z^{-1} + b_2 z^{-2}}{1 + a_1 z^{-1} + a_2 z^{-2}}$$

with coefficients derived from the transfer function

$$H(s) = \frac{s^2 + \omega_0^2}{s^2 + \frac{\omega_0}{Q} + \omega_0^2}$$

by a matched Z-transformation.

Implementations:

FiP16	16 Bit Fixed Point Implementation
FiP32	32 Bit Fixed Point Implementation
Float32	32 Bit Floating Point Implementation
Float64	64 Bit Floating Point Implementation

Implementation: FiP16

16 Bit Fixed Point Implementation

Inports Data Type	
In	int16
n	int16

Outports Data Type	
Out	int16

Implementation: FiP32

32 Bit Fixed Point Implementation

Inports Data Type	
In	int32
n	int32

Outports Data Type	
Out	int32

Implementation: Float32

32 Bit Floating Point Implementation

Inports Data Type	
In	float32
n	float32

Outports Data Type	
Out	float32

Implementation: Float64

64 Bit Floating Point Implementation

Inports Data Type	
In	float64
n	float64

Outports Data Type	
Out	float64

Block: BandpassBiQ



Calculates the filter coefficients for a second order bandpass and performs filtering on input signal.
Second order transfer function used:
H(z) = (b0.z^2 + b1.z + b2) / (z^2 + a1.z + a2)

Inports	
In	Input In(k)

Outports	
Out	Output Out(k)

Mask Parameters		
Name	**ID**	**Description**
characteristic	1	The filter characteristic is one of Butterworth (=Bessel) or Chebyshev
fc1	2	Lower cut-off frequency in Hz
fc2	3	Upper cut-off frequency in Hz
rc	4	Attenuation at cut-off frequencies
ts_fact	5	Multiplication factor of base sampling time (in integer format)

Description:

Butterworth

- center frequency f_c
  - center frequency f_c is given by ${f_c}^2 = {f_{c1}}^2 * {f_{c2}}^2$
  - zero phaseshift @center frequency f_c
- @lower cut-off frequency f_{c1}
  - -3dB attenuation
  - 45 degree phaseshift
- @upper cut-off frequency f_{c2}
  - -3dB attenuation
  - -45 degree phaseshift
- stopband
  - monotonic -20dB decline per decade
  - roll-off dynamics are constant and not adjustable

E.g.:
The cut-off frequencies are $f_{c1} = 10$Hz and $f_{c2} = 100$Hz.
The bodeplot is shown in the figure 1 below.

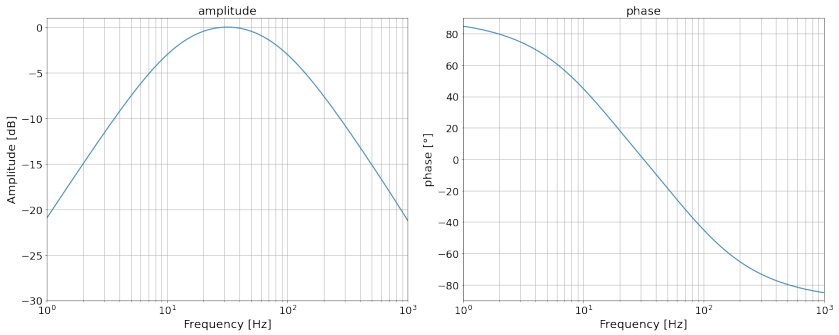


Figure 1: Bodeplot Butterworth bandpass.

Chebyshev
Note: A second order Chebyshev I bandpass has the same bodeplot as a second order Chebyshev II bandpass. Hence, only the 'Chebyshev' option is given.

- center frequency f_c
  - center frequency f_c is given by ${f_c}^2 = {f_{c1}}^2 * {f_{c2}}^2$
  - zero phaseshift @center frequency f_c
- @lower cut-off frequency f_{c1}
  - $-rc$dB attenuation
  - phaseshift proportional to rc
- @upper cut-off frequency f_{c2}
  - $-rc$dB attenuation
  - -phaseshift proportional to rc
- stopband
  - monotonic -20dB decline per decade
  - roll-off dynamics are adjustable using parameter rc

E.g.:
The cut-off frequencies are $f_{c1} = 10$Hz and $f_{c2} = 100$Hz.
The parameter rc is set to 10dB.
The bodeplot is shown in the figure 2 below.
Bessel
Note: A second order Bessel bandpass behaves exactly like a second order Butterworth bandpass. Hence, no 'Bessel' option is given.

Implementations:

FiP16	16 Bit Fixed Point Implementation
FiP32	32 Bit Fixed Point Implementation
Float32	32 Bit Floating Point Implementation
Float64	64 Bit Floating Point Implementation

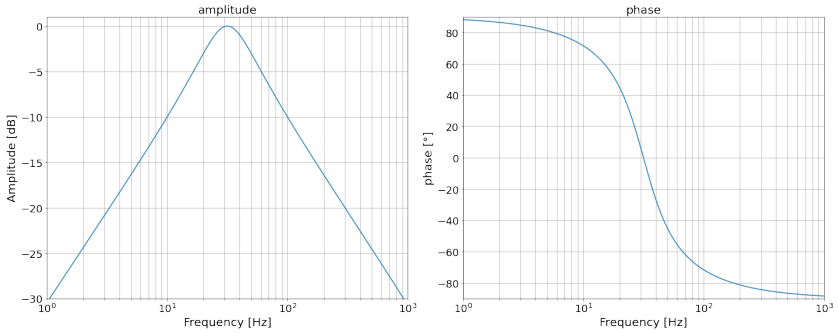


Figure 2: Bodeplot Chebyshev bandpass. $rc = 10$dB

Implementation: FiP16

16 Bit Fixed Point Implementation

Inports Data Type	
In	int16

Outports Data Type	
Out	int16

Implementation: FiP32

32 Bit Fixed Point Implementation

Inports Data Type	
In	int32

Outports Data Type	
Out	int32

Implementation: Float32

32 Bit Floating Point Implementation

Inports Data Type	
In	float32

Outports Data Type	
Out	float32

Implementation: Float64

64 Bit Floating Point Implementation

Inports Data Type	
In	float64

Outports Data Type	
Out	float64

Block: BandstopBiQ



Calculates the filter coefficients for a second order bandstop and performs filtering on input signal.
Second order transfer function used:
H(z) = (b0.z^2 + b1.z + b2) / (z^2 + a1.z + a2)

Inports	
In	Input In(k)

Outports	
Out	Output Out(k)

Mask Parameters		
Name	**ID**	**Description**
characteristic	1	The filter characteristic is one of Butterworth (=Bessel) or Chebyshev
fc1	2	Lower cut-off frequency in Hz
fc2	3	Upper cut-off frequency in Hz
rc	4	Attenuation at cut-off frequencies
ts_fact	5	Multiplication factor of base sampling time (in integer format)

Description:

Butterworth

- center frequency f_c
  - center frequency f_c is given by ${f_c}^2 = {f_{c1}}^2 * {f_{c2}}^2$
  - phase discontinuity @center frequency f_c
- @lower cut-off frequency f_{c1}
  - -3dB attenuation
  - -45 degree phaseshift
- @upper cut-off frequency f_{c2}
  - -3dB attenuation
  - 45 degree phaseshift
- passband
  - roll-off dynamics are constant and not adjustable

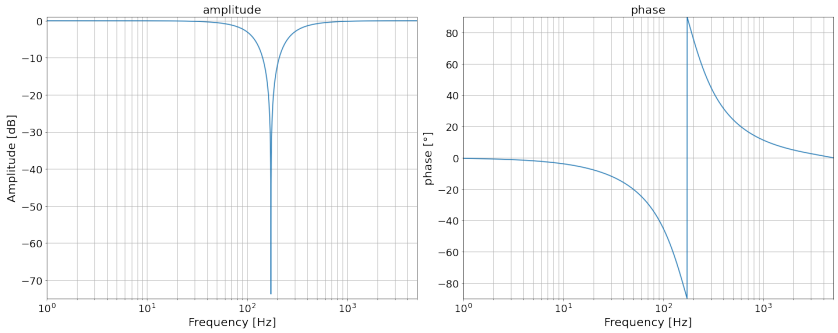


Figure 3: Bodeplot Butterworth bandstop.

E.g.:
The cut-off frequencies are $f_{c1} = 100$Hz and $f_{c2} = 300$Hz.
The bodeplot is shown in the figure 3 below.

Chebyshev

Note: A second order Chebyshev I bandstop has the same bodeplot as a second order Chebyshev II bandstop. Hence, only the 'Chebyshev' option is given.

- center frequency f_c
  - center frequency f_c is given by ${f_c}^2 = {f_{c1}}^2 * {f_{c2}}^2$
  - phase discontinuity @center frequency f_c
- @lower cut-off frequency f_{c1}
  - $-rc$dB attenuation
  - -phaseshift proportional to rc
- @upper cut-off frequency f_{c2}
  - $-rc$dB attenuation
  - phaseshift proportional to rc
- passband
  - roll-off dynamics are adjustable using parameter rc

E.g.:
The cut-off frequencies are $f_{c1} = 100$Hz and $f_{c2} = 300$Hz.
The parameter rc is set to 10dB.
The bodeplot is shown in the figure 4 below.

Bessel

Note: A second order Bessel bandstop behaves exactly like a second order Butterworth bandstop. Hence, no 'Bessel' option is given.

Implementations:

FiP16	16 Bit Fixed Point Implementation
FiP32	32 Bit Fixed Point Implementation
Float32	32 Bit Floating Point Implementation
Float64	64 Bit Floating Point Implementation

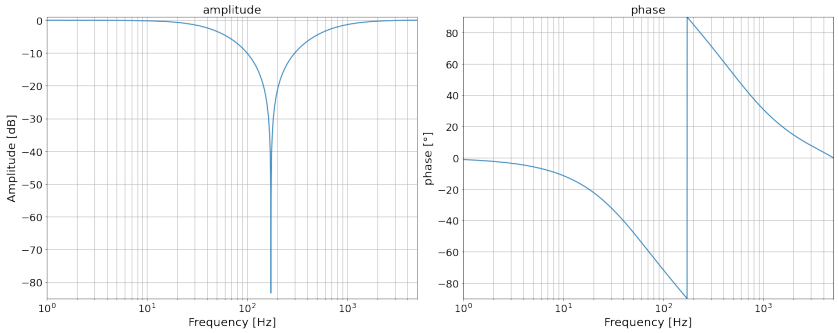


Figure 4: Bodeplot Chebyshev bandstop. $rc = 10$dB

Implementation: FiP16

16 Bit Fixed Point Implementation

Inports Data Type	
In	int16

Outports Data Type	
Out	int16

Implementation: FiP32

32 Bit Fixed Point Implementation

Inports Data Type	
In	int32

Outports Data Type	
Out	int32

Implementation: Float32

32 Bit Floating Point Implementation

Inports Data Type	
In	float32

Outports Data Type	
Out	float32

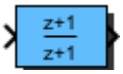
Implementation: Float64

64 Bit Floating Point Implementation

Inports Data Type	
In	float64

Outports Data Type	
Out	float64

Block: Bilin



First order transfer function:
H(z) = (b0.z + b1) / (a0.z + a1)

Inports	
In	Input In(k)

Outports	
Out	Output Out(k)

Mask Parameters		
Name	**ID**	**Description**
b0	1	Filter coefficient b0
b1	2	Filter coefficient b1
a0	3	Filter coefficient a0
a1	4	Filter coefficient a1
ts_fact	5	Multiplication factor of base sampling time (in integer format)

Description:

Alternative representation of the same transfer function:

$$H(z) = \frac{b_0 + b_1 z^{-1}}{a_0 + a_1 z^{-1}}$$

Implementations:

FiP16 16 Bit Fixed Point Implementation
FiP32 32 Bit Fixed Point Implementation
Float32 32 Bit Floating Point Implementation
Float64 64 Bit Floating Point Implementation

Implementation: FiP16

16 Bit Fixed Point Implementation

Inports Data Type	
In	int16

Outports Data Type	
Out	int16

Implementation: FiP32

32 Bit Fixed Point Implementation

Inports Data Type	
In	int32

Outports Data Type	
Out	int32

Implementation: Float32

32 Bit Floating Point Implementation

Inports Data Type	
In	float32

Outports Data Type	
Out	float32

Implementation: Float64

64 Bit Floating Point Implementation

Inports Data Type	
In	float64

Outports Data Type	
Out	float64

Verification: Bilin FiP16 CPU TMS320F28335

Date of Test	2026-06-25
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for Filter block Bilin.

Test results						
Time step	1	2	3	4	...	73
CPU cycles	87	87	87	87	...	87
Inputs						
In (DSP)	-1842	-679	5729	7954	...	15256
In	-0.056	-0.021	0.175	0.243	...	0.466
Parameters						
b0	0.2					
b1	0.1					
a0	1.1					
a1	-0.7					
ts_fact	1					
Outputs						
Out	-0.01	-0.015	0.02	0.073	...	0.338
Exp. Out	-0.01	-0.015	0.02	0.073	...	0.338
Out (DSP)	-335	-505	658	2385	...	11070
Exp. Out (DSP)	-335	-504	659	2387	...	11073

Test settings	
Tolerance Out	±1,5259e-04 (±5 LSB)

Test statistics	
Min CPU cycles	87
Max CPU cycles	87
Avg CPU cycles	87

Test case: Conversion test OK

Conversion test for Filter block Bilin.

Test results						
Time step	1	2	3	4	...	8
Mask parameters						
b0	0	0.1	0.2	0.5	...	10
b1	0	0.1	0.2	0.5	...	10
a0	0.1	0.1	0.1	1	...	1
a1	0	0.1	0.2	0.5	...	10
ts_fact	1	1	1	1	...	1
Controller parameters						
a1	0	16384	16384	16384	...	20480
sfrb0	15	14	13	15	...	11
sfrb1	15	14	13	15	...	11
sfra1	15	14	13	15	...	11
b0	0	16384	16384	16384	...	20480
b1	0	16384	16384	16384	...	20480
Exp. a1	0	16384	16384	16384	...	20480
Exp. sfrb0	15	14	13	15	...	11
Exp. sfrb1	15	14	13	15	...	11
Exp. sfra1	15	14	13	15	...	11
Exp. b0	0	16384	16384	16384	...	20480
Exp. b1	0	16384	16384	16384	...	20480

Test settings	
Tolerance a1	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance sfra1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Filter block Bilin.

Test results						
Time step	1	2	3	4	...	8
Mask parameters						
b0	0	0.1	0.2	0.5	...	10
b1	0	0.1	0.2	0.5	...	10
a0	0.1	0.1	0.1	1	...	1
a1	0	0.1	0.2	0.5	...	10
ts_fact	1	1	1	1	...	1
Controller parameters						
a1	0	16384	16384	16384	...	20480
sfrb0	15	14	13	15	...	11
sfrb1	15	14	13	15	...	11
sfra1	15	14	13	15	...	11
b0	0	16384	16384	16384	...	20480
b1	0	16384	16384	16384	...	20480
Exp. a1	0	16384	16384	16384	...	20480
Exp. sfrb0	15	14	13	15	...	11
Exp. sfrb1	15	14	13	15	...	11
Exp. sfra1	15	14	13	15	...	11
Exp. b0	0	16384	16384	16384	...	20480
Exp. b1	0	16384	16384	16384	...	20480

Test settings	
Tolerance a1	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance sfra1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test statistics	
Min CPU cycles	4658
Max CPU cycles	18605
Avg CPU cycles	10505

Verification: Bilin FiP16 CPU TM4C123GH6

Date of Test	2026-06-25
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for Filter block Bilin.

Test results						
Time step	1	2	3	4	...	73
CPU cycles	71	71	71	71	...	71
Inputs						
In (DSP)	-1842	-679	5729	7954	...	15256
In	-0.056	-0.021	0.175	0.243	...	0.466
Parameters						
b0	0.2					
b1	0.1					
a0	1.1					
a1	-0.7					
ts_fact	1					
Outputs						
Out	-0.01	-0.015	0.02	0.073	...	0.338
Exp. Out	-0.01	-0.015	0.02	0.073	...	0.338
Out (DSP)	-335	-505	658	2385	...	11070
Exp. Out (DSP)	-335	-504	659	2387	...	11073

Test settings	
Tolerance Out	±1,5259e-04 (±5 LSB)

Test statistics	
Min CPU cycles	71
Max CPU cycles	71
Avg CPU cycles	71

Test case: Conversion test OK

Conversion test for Filter block Bilin.

Test results						
Time step	1	2	3	4	...	8
Mask parameters						
b0	0	0.1	0.2	0.5	...	10
b1	0	0.1	0.2	0.5	...	10
a0	0.1	0.1	0.1	1	...	1
a1	0	0.1	0.2	0.5	...	10
ts_fact	1	1	1	1	...	1
Controller parameters						
a1	0	16384	16384	16384	...	20480
sfrb0	15	14	13	15	...	11
sfrb1	15	14	13	15	...	11
sfra1	15	14	13	15	...	11
b0	0	16384	16384	16384	...	20480
b1	0	16384	16384	16384	...	20480
Exp. a1	0	16384	16384	16384	...	20480
Exp. sfrb0	15	14	13	15	...	11
Exp. sfrb1	15	14	13	15	...	11
Exp. sfra1	15	14	13	15	...	11
Exp. b0	0	16384	16384	16384	...	20480
Exp. b1	0	16384	16384	16384	...	20480

Test settings	
Tolerance a1	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance sfra1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Filter block Bilin.

Test results						
Time step	1	2	3	4	...	8
Mask parameters						
b0	0	0.1	0.2	0.5	...	10
b1	0	0.1	0.2	0.5	...	10
a0	0.1	0.1	0.1	1	...	1
a1	0	0.1	0.2	0.5	...	10
ts_fact	1	1	1	1	...	1
Controller parameters						
a1	0	16384	16384	16384	...	20480
sfrb0	15	14	13	15	...	11
sfrb1	15	14	13	15	...	11
sfra1	15	14	13	15	...	11
b0	0	16384	16384	16384	...	20480
b1	0	16384	16384	16384	...	20480
Exp. a1	0	16384	16384	16384	...	20480
Exp. sfrb0	15	14	13	15	...	11
Exp. sfrb1	15	14	13	15	...	11
Exp. sfra1	15	14	13	15	...	11
Exp. b0	0	16384	16384	16384	...	20480
Exp. b1	0	16384	16384	16384	...	20480

Test settings	
Tolerance a1	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance sfra1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test statistics	
Min CPU cycles	2383
Max CPU cycles	8683
Avg CPU cycles	5255

Verification: Bilin FiP16 CPU STM32G474RE

Date of Test	2026-06-25
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for Filter block Bilin.

Test results						
Time step	1	2	3	4	...	73
CPU cycles	112	112	112	112	...	112
Inputs						
In (DSP)	-1842	-679	5729	7954	...	15256
In	-0.056	-0.021	0.175	0.243	...	0.466
Parameters						
b0	0.2					
b1	0.1					
a0	1.1					
a1	-0.7					
ts_fact	1					
Outputs						
Out	-0.01	-0.015	0.02	0.073	...	0.338
Exp. Out	-0.01	-0.015	0.02	0.073	...	0.338
Out (DSP)	-335	-505	658	2385	...	11070
Exp. Out (DSP)	-335	-504	659	2387	...	11073

Test settings	
Tolerance Out	±1,5259e-04 (±5 LSB)

Test statistics	
Min CPU cycles	112
Max CPU cycles	112
Avg CPU cycles	112

Test case: Conversion test OK

Conversion test for Filter block Bilin.

Test results						
Time step	1	2	3	4	...	8
Mask parameters						
b0	0	0.1	0.2	0.5	...	10
b1	0	0.1	0.2	0.5	...	10
a0	0.1	0.1	0.1	1	...	1
a1	0	0.1	0.2	0.5	...	10
ts_fact	1	1	1	1	...	1
Controller parameters						
a1	0	16384	16384	16384	...	20480
sfrb0	15	14	13	15	...	11
sfrb1	15	14	13	15	...	11
sfra1	15	14	13	15	...	11
b0	0	16384	16384	16384	...	20480
b1	0	16384	16384	16384	...	20480
Exp. a1	0	16384	16384	16384	...	20480
Exp. sfrb0	15	14	13	15	...	11
Exp. sfrb1	15	14	13	15	...	11
Exp. sfra1	15	14	13	15	...	11
Exp. b0	0	16384	16384	16384	...	20480
Exp. b1	0	16384	16384	16384	...	20480

Test settings	
Tolerance a1	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance sfra1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Filter block Bilin.

Test results						
Time step	1	2	3	4	...	8
Mask parameters						
b0	0	0.1	0.2	0.5	...	10
b1	0	0.1	0.2	0.5	...	10
a0	0.1	0.1	0.1	1	...	1
a1	0	0.1	0.2	0.5	...	10
ts_fact	1	1	1	1	...	1
Controller parameters						
a1	0	16384	16384	16384	...	20480
sfrb0	15	14	13	15	...	11
sfrb1	15	14	13	15	...	11
sfra1	15	14	13	15	...	11
b0	0	16384	16384	16384	...	20480
b1	0	16384	16384	16384	...	20480
Exp. a1	0	16384	16384	16384	...	20480
Exp. sfrb0	15	14	13	15	...	11
Exp. sfrb1	15	14	13	15	...	11
Exp. sfra1	15	14	13	15	...	11
Exp. b0	0	16384	16384	16384	...	20480
Exp. b1	0	16384	16384	16384	...	20480

Test settings	
Tolerance a1	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance sfra1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test statistics	
Min CPU cycles	2150
Max CPU cycles	4735
Avg CPU cycles	3228

Verification: Bilin FiP16 CPU STM32F072RB

Date of Test	2026-06-25
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for Filter block Bilin.

Test results						
Time step	1	2	3	4	...	73
CPU cycles	99	99	99	99	...	99
Inputs						
In (DSP)	-1842	-679	5729	7954	...	15256
In	-0.056	-0.021	0.175	0.243	...	0.466
Parameters						
b0	0.2					
b1	0.1					
a0	1.1					
a1	-0.7					
ts_fact	1					
Outputs						
Out	-0.01	-0.015	0.02	0.073	...	0.338
Exp. Out	-0.01	-0.015	0.02	0.073	...	0.338
Out (DSP)	-335	-505	658	2385	...	11070
Exp. Out (DSP)	-335	-504	659	2387	...	11073

Test settings	
Tolerance Out	±1,5259e-04 (±5 LSB)

Test statistics	
Min CPU cycles	99
Max CPU cycles	99
Avg CPU cycles	99

Test case: Conversion test OK

Conversion test for Filter block Bilin.

Test results						
Time step	1	2	3	4	...	8
Mask parameters						
b0	0	0.1	0.2	0.5	...	10
b1	0	0.1	0.2	0.5	...	10
a0	0.1	0.1	0.1	1	...	1
a1	0	0.1	0.2	0.5	...	10
ts_fact	1	1	1	1	...	1
Controller parameters						
a1	0	16384	16384	16384	...	20480
sfrb0	15	14	13	15	...	11
sfrb1	15	14	13	15	...	11
sfra1	15	14	13	15	...	11
b0	0	16384	16384	16384	...	20480
b1	0	16384	16384	16384	...	20480
Exp. a1	0	16384	16384	16384	...	20480
Exp. sfrb0	15	14	13	15	...	11
Exp. sfrb1	15	14	13	15	...	11
Exp. sfra1	15	14	13	15	...	11
Exp. b0	0	16384	16384	16384	...	20480
Exp. b1	0	16384	16384	16384	...	20480

Test settings	
Tolerance a1	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance sfra1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Filter block Bilin.

Test results						
Time step	1	2	3	4	...	8
Mask parameters						
b0	0	0.1	0.2	0.5	...	10
b1	0	0.1	0.2	0.5	...	10
a0	0.1	0.1	0.1	1	...	1
a1	0	0.1	0.2	0.5	...	10
ts_fact	1	1	1	1	...	1
Controller parameters						
a1	0	16384	16384	16384	...	20480
sfrb0	15	14	13	15	...	11
sfrb1	15	14	13	15	...	11
sfra1	15	14	13	15	...	11
b0	0	16384	16384	16384	...	20480
b1	0	16384	16384	16384	...	20480
Exp. a1	0	16384	16384	16384	...	20480
Exp. sfrb0	15	14	13	15	...	11
Exp. sfrb1	15	14	13	15	...	11
Exp. sfra1	15	14	13	15	...	11
Exp. b0	0	16384	16384	16384	...	20480
Exp. b1	0	16384	16384	16384	...	20480

Test settings	
Tolerance a1	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance sfra1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test statistics	
Min CPU cycles	5338
Max CPU cycles	15205
Avg CPU cycles	10684

Verification: Bilin FiP16 CPU PIC32MX170F256

Date of Test	2026-06-25
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for Filter block Bilin.

Test results						
Time step	1	2	3	4	...	73
CPU cycles	60	60	60	60	...	60
Inputs						
In (DSP)	-1842	-679	5729	7954	...	15256
In	-0.056	-0.021	0.175	0.243	...	0.466
Parameters						
b0	0.2					
b1	0.1					
a0	1.1					
a1	-0.7					
ts_fact	1					
Outputs						
Out	-0.01	-0.015	0.02	0.073	...	0.338
Exp. Out	-0.01	-0.015	0.02	0.073	...	0.338
Out (DSP)	-335	-505	658	2385	...	11070
Exp. Out (DSP)	-335	-504	659	2387	...	11073

Test settings	
Tolerance Out	±1,5259e-04 (±5 LSB)

Test statistics	
Min CPU cycles	60
Max CPU cycles	60
Avg CPU cycles	60

Test case: Conversion test OK

Conversion test for Filter block Bilin.

Test results						
Time step	1	2	3	4	...	8
Mask parameters						
b0	0	0.1	0.2	0.5	...	10
b1	0	0.1	0.2	0.5	...	10
a0	0.1	0.1	0.1	1	...	1
a1	0	0.1	0.2	0.5	...	10
ts_fact	1	1	1	1	...	1
Controller parameters						
a1	0	16384	16384	16384	...	20480
sfrb0	15	14	13	15	...	11
sfrb1	15	14	13	15	...	11
sfra1	15	14	13	15	...	11
b0	0	16384	16384	16384	...	20480
b1	0	16384	16384	16384	...	20480
Exp. a1	0	16384	16384	16384	...	20480
Exp. sfrb0	15	14	13	15	...	11
Exp. sfrb1	15	14	13	15	...	11
Exp. sfra1	15	14	13	15	...	11
Exp. b0	0	16384	16384	16384	...	20480
Exp. b1	0	16384	16384	16384	...	20480

Test settings	
Tolerance a1	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance sfra1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Filter block Bilin.

Test results						
Time step	1	2	3	4	...	8
Mask parameters						
b0	0	0.1	0.2	0.5	...	10
b1	0	0.1	0.2	0.5	...	10
a0	0.1	0.1	0.1	1	...	1
a1	0	0.1	0.2	0.5	...	10
ts_fact	1	1	1	1	...	1
Controller parameters						
a1	0	16384	16384	16384	...	20480
sfrb0	15	14	13	15	...	11
sfrb1	15	14	13	15	...	11
sfra1	15	14	13	15	...	11
b0	0	16384	16384	16384	...	20480
b1	0	16384	16384	16384	...	20480
Exp. a1	0	16384	16384	16384	...	20480
Exp. sfrb0	15	14	13	15	...	11
Exp. sfrb1	15	14	13	15	...	11
Exp. sfra1	15	14	13	15	...	11
Exp. b0	0	16384	16384	16384	...	20480
Exp. b1	0	16384	16384	16384	...	20480

Test settings	
Tolerance a1	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance sfra1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test statistics	
Min CPU cycles	2432
Max CPU cycles	6430
Avg CPU cycles	4480

Verification: Bilin FiP16 CPU dsPIC33EP256MC502

Date of Test	2026-06-25
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for Filter block Bilin.

Test results						
Time step	1	2	3	4	...	73
CPU cycles	110	110	110	110	...	110
Inputs						
In (DSP)	-1842	-679	5729	7954	...	15256
In	-0.056	-0.021	0.175	0.243	...	0.466
Parameters						
b0	0.2					
b1	0.1					
a0	1.1					
a1	-0.7					
ts_fact	1					
Outputs						
Out	-0.01	-0.015	0.02	0.073	...	0.338
Exp. Out	-0.01	-0.015	0.02	0.073	...	0.338
Out (DSP)	-335	-505	658	2385	...	11070
Exp. Out (DSP)	-335	-504	659	2387	...	11073

Test settings	
Tolerance Out	±1,5259e-04 (±5 LSB)

Test statistics	
Min CPU cycles	110
Max CPU cycles	110
Avg CPU cycles	110

Test case: Conversion test OK

Conversion test for Filter block Bilin.

Test results						
Time step	1	2	3	4	...	8
Mask parameters						
b0	0	0.1	0.2	0.5	...	10
b1	0	0.1	0.2	0.5	...	10
a0	0.1	0.1	0.1	1	...	1
a1	0	0.1	0.2	0.5	...	10
ts_fact	1	1	1	1	...	1
Controller parameters						
a1	0	16384	16384	16384	...	20480
sfrb0	15	14	13	15	...	11
sfrb1	15	14	13	15	...	11
sfra1	15	14	13	15	...	11
b0	0	16384	16384	16384	...	20480
b1	0	16384	16384	16384	...	20480
Exp. a1	0	16384	16384	16384	...	20480
Exp. sfrb0	15	14	13	15	...	11
Exp. sfrb1	15	14	13	15	...	11
Exp. sfra1	15	14	13	15	...	11
Exp. b0	0	16384	16384	16384	...	20480
Exp. b1	0	16384	16384	16384	...	20480

Test settings	
Tolerance a1	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance sfra1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Filter block Bilin.

Test results						
Time step	1	2	3	4	...	8
Mask parameters						
b0	0	0.1	0.2	0.5	...	10
b1	0	0.1	0.2	0.5	...	10
a0	0.1	0.1	0.1	1	...	1
a1	0	0.1	0.2	0.5	...	10
ts_fact	1	1	1	1	...	1
Controller parameters						
a1	0	16384	16384	16384	...	20480
sfrb0	15	14	13	15	...	11
sfrb1	15	14	13	15	...	11
sfra1	15	14	13	15	...	11
b0	0	16384	16384	16384	...	20480
b1	0	16384	16384	16384	...	20480
Exp. a1	0	16384	16384	16384	...	20480
Exp. sfrb0	15	14	13	15	...	11
Exp. sfrb1	15	14	13	15	...	11
Exp. sfra1	15	14	13	15	...	11
Exp. b0	0	16384	16384	16384	...	20480
Exp. b1	0	16384	16384	16384	...	20480

Test settings	
Tolerance a1	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance sfra1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test statistics	
Min CPU cycles	8952
Max CPU cycles	36527
Avg CPU cycles	23341

Verification: Bilin FiP16 CPU XMC4800-F144K2048

Date of Test	2026-06-25
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for Filter block Bilin.

Test results						
Time step	1	2	3	4	...	73
CPU cycles	119	102	102	102	...	102
Inputs						
In (DSP)	-1842	-679	5729	7954	...	15256
In	-0.056	-0.021	0.175	0.243	...	0.466
Parameters						
b0	0.2					
b1	0.1					
a0	1.1					
a1	-0.7					
ts_fact	1					
Outputs						
Out	-0.01	-0.015	0.02	0.073	...	0.338
Exp. Out	-0.01	-0.015	0.02	0.073	...	0.338
Out (DSP)	-335	-505	658	2385	...	11070
Exp. Out (DSP)	-335	-504	659	2387	...	11073

Test settings	
Tolerance Out	±1,5259e-04 (±5 LSB)

Test statistics	
Min CPU cycles	102
Max CPU cycles	119
Avg CPU cycles	102

Test case: Conversion test OK

Conversion test for Filter block Bilin.

Test results						
Time step	1	2	3	4	...	8
Mask parameters						
b0	0	0.1	0.2	0.5	...	10
b1	0	0.1	0.2	0.5	...	10
a0	0.1	0.1	0.1	1	...	1
a1	0	0.1	0.2	0.5	...	10
ts_fact	1	1	1	1	...	1
Controller parameters						
a1	0	16384	16384	16384	...	20480
sfrb0	15	14	13	15	...	11
sfrb1	15	14	13	15	...	11
sfra1	15	14	13	15	...	11
b0	0	16384	16384	16384	...	20480
b1	0	16384	16384	16384	...	20480
Exp. a1	0	16384	16384	16384	...	20480
Exp. sfrb0	15	14	13	15	...	11
Exp. sfrb1	15	14	13	15	...	11
Exp. sfra1	15	14	13	15	...	11
Exp. b0	0	16384	16384	16384	...	20480
Exp. b1	0	16384	16384	16384	...	20480

Test settings	
Tolerance a1	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance sfra1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Filter block Bilin.

Test results						
Time step	1	2	3	4	...	8
Mask parameters						
b0	0	0.1	0.2	0.5	...	10
b1	0	0.1	0.2	0.5	...	10
a0	0.1	0.1	0.1	1	...	1
a1	0	0.1	0.2	0.5	...	10
ts_fact	1	1	1	1	...	1
Controller parameters						
a1	0	16384	16384	16384	...	20480
sfrb0	15	14	13	15	...	11
sfrb1	15	14	13	15	...	11
sfra1	15	14	13	15	...	11
b0	0	16384	16384	16384	...	20480
b1	0	16384	16384	16384	...	20480
Exp. a1	0	16384	16384	16384	...	20480
Exp. sfrb0	15	14	13	15	...	11
Exp. sfrb1	15	14	13	15	...	11
Exp. sfra1	15	14	13	15	...	11
Exp. b0	0	16384	16384	16384	...	20480
Exp. b1	0	16384	16384	16384	...	20480

Test settings	
Tolerance a1	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance sfra1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test statistics	
Min CPU cycles	1804
Max CPU cycles	4279
Avg CPU cycles	2888

Verification: Bilin FiP16 CPU TMS320F28379D

Date of Test	2026-06-25
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for Filter block Bilin.

Test results						
Time step	1	2	3	4	...	73
CPU cycles	86	86	86	86	...	86
Inputs						
In (DSP)	-1842	-679	5729	7954	...	15256
In	-0.056	-0.021	0.175	0.243	...	0.466
Parameters						
b0	0.2					
b1	0.1					
a0	1.1					
a1	-0.7					
ts_fact	1					
Outputs						
Out	-0.01	-0.015	0.02	0.073	...	0.338
Exp. Out	-0.01	-0.015	0.02	0.073	...	0.338
Out (DSP)	-335	-505	658	2385	...	11070
Exp. Out (DSP)	-335	-504	659	2387	...	11073

Test settings	
Tolerance Out	±1,5259e-04 (±5 LSB)

Test statistics	
Min CPU cycles	86
Max CPU cycles	86
Avg CPU cycles	86

Test case: Conversion test OK

Conversion test for Filter block Bilin.

Test results						
Time step	1	2	3	4	...	8
Mask parameters						
b0	0	0.1	0.2	0.5	...	10
b1	0	0.1	0.2	0.5	...	10
a0	0.1	0.1	0.1	1	...	1
a1	0	0.1	0.2	0.5	...	10
ts_fact	1	1	1	1	...	1
Controller parameters						
a1	0	16384	16384	16384	...	20480
sfrb0	15	14	13	15	...	11
sfrb1	15	14	13	15	...	11
sfra1	15	14	13	15	...	11
b0	0	16384	16384	16384	...	20480
b1	0	16384	16384	16384	...	20480
Exp. a1	0	16384	16384	16384	...	20480
Exp. sfrb0	15	14	13	15	...	11
Exp. sfrb1	15	14	13	15	...	11
Exp. sfra1	15	14	13	15	...	11
Exp. b0	0	16384	16384	16384	...	20480
Exp. b1	0	16384	16384	16384	...	20480

Test settings	
Tolerance a1	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance sfra1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Filter block Bilin.

Test results						
Time step	1	2	3	4	...	8
Mask parameters						
b0	0	0.1	0.2	0.5	...	10
b1	0	0.1	0.2	0.5	...	10
a0	0.1	0.1	0.1	1	...	1
a1	0	0.1	0.2	0.5	...	10
ts_fact	1	1	1	1	...	1
Controller parameters						
a1	0	16384	16384	16384	...	20480
sfrb0	15	14	13	15	...	11
sfrb1	15	14	13	15	...	11
sfra1	15	14	13	15	...	11
b0	0	16384	16384	16384	...	20480
b1	0	16384	16384	16384	...	20480
Exp. a1	0	16384	16384	16384	...	20480
Exp. sfrb0	15	14	13	15	...	11
Exp. sfrb1	15	14	13	15	...	11
Exp. sfra1	15	14	13	15	...	11
Exp. b0	0	16384	16384	16384	...	20480
Exp. b1	0	16384	16384	16384	...	20480

Test settings	
Tolerance a1	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance sfra1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test statistics	
Min CPU cycles	3363
Max CPU cycles	13695
Avg CPU cycles	7751

Verification: Bilin FiP32 CPU TMS320F28335

Date of Test	2026-06-25
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for Filter block Bilin.

Test results				
Time step	1	2	...	73
CPU cycles	216	216	...	216
Inputs				
In (DSP)	-120706110	-44469415	...	999834674
In	-0.056	-0.021	...	0.466
Parameters				
b0	0.2			
b1	0.1			
a0	1.1			
a1	-0.7			
ts_fact	1			
Outputs				
Out	-0.01	-0.015	...	0.338
Exp. Out	-0.01	-0.015	...	0.338
Out (DSP)	-21946566	-33024628	...	725708721
Exp. Out (DSP)	-21946566	-33024627	...	725708723

Test settings	
Tolerance Out	±2,3283e-09 (±5 LSB)

Test statistics	
Min CPU cycles	216
Max CPU cycles	216
Avg CPU cycles	216

Test case: Conversion test OK

Conversion test for Filter block Bilin.

Test results				
Time step	1	2	...	8
Mask parameters				
b0	0	0.1	...	10
b1	0	0.1	...	10
a0	0.1	0.1	...	1
a1	0	0.1	...	10
ts_fact	1	1	...	1
Controller parameters				
a1	0	1073741824	...	1342177280
sfrb0	31	30	...	27
sfrb1	31	30	...	27
sfra1	31	30	...	27
b0	0	1073741824	...	1342177280
b1	0	1073741824	...	1342177280
Exp. a1	0	1073741824	...	1342177280
Exp. sfrb0	31	30	...	27
Exp. sfrb1	31	30	...	27
Exp. sfra1	31	30	...	27
Exp. b0	0	1073741824	...	1342177280
Exp. b1	0	1073741824	...	1342177280

Test settings	
Tolerance a1	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance sfra1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Filter block Bilin.

Test results				
Time step	1	2	...	8
Mask parameters				
b0	0	0.1	...	10
b1	0	0.1	...	10
a0	0.1	0.1	...	1
a1	0	0.1	...	10
ts_fact	1	1	...	1
Controller parameters				
a1	0	1073741824	...	1342177280
sfrb0	31	30	...	27
sfrb1	31	30	...	27
sfra1	31	30	...	27
b0	0	1073741824	...	1342177280
b1	0	1073741824	...	1342177280
Exp. a1	0	1073741824	...	1342177280
Exp. sfrb0	31	30	...	27
Exp. sfrb1	31	30	...	27
Exp. sfra1	31	30	...	27
Exp. b0	0	1073741824	...	1342177280
Exp. b1	0	1073741824	...	1342177280

Test settings	
Tolerance a1	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance sfra1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test statistics	
Min CPU cycles	5170
Max CPU cycles	19264
Avg CPU cycles	11146

Verification: Bilin FiP32 CPU TM4C123GH6

Date of Test	2026-06-25
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for Filter block Bilin.

Test results				
Time step	1	2	...	73
CPU cycles	155	155	...	155
Inputs				
In (DSP)	-120706110	-44469415	...	999834674
In	-0.056	-0.021	...	0.466
Parameters				
b0	0.2			
b1	0.1			
a0	1.1			
a1	-0.7			
ts_fact	1			
Outputs				
Out	-0.01	-0.015	...	0.338
Exp. Out	-0.01	-0.015	...	0.338
Out (DSP)	-21946566	-33024628	...	725708721
Exp. Out (DSP)	-21946566	-33024627	...	725708723

Test settings	
Tolerance Out	±2,3283e-09 (±5 LSB)

Test statistics	
Min CPU cycles	155
Max CPU cycles	155
Avg CPU cycles	155

Test case: Conversion test OK

Conversion test for Filter block Bilin.

Test results				
Time step	1	2	...	8
Mask parameters				
b0	0	0.1	...	10
b1	0	0.1	...	10
a0	0.1	0.1	...	1
a1	0	0.1	...	10
ts_fact	1	1	...	1
Controller parameters				
a1	0	1073741824	...	1342177280
sfrb0	31	30	...	27
sfrb1	31	30	...	27
sfra1	31	30	...	27
b0	0	1073741824	...	1342177280
b1	0	1073741824	...	1342177280
Exp. a1	0	1073741824	...	1342177280
Exp. sfrb0	31	30	...	27
Exp. sfrb1	31	30	...	27
Exp. sfra1	31	30	...	27
Exp. b0	0	1073741824	...	1342177280
Exp. b1	0	1073741824	...	1342177280

Test settings	
Tolerance a1	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance sfra1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Filter block Bilin.

Test results				
Time step	1	2	...	8
Mask parameters				
b0	0	0.1	...	10
b1	0	0.1	...	10
a0	0.1	0.1	...	1
a1	0	0.1	...	10
ts_fact	1	1	...	1
Controller parameters				
a1	0	1073741824	...	1342177280
sfrb0	31	30	...	27
sfrb1	31	30	...	27
sfra1	31	30	...	27
b0	0	1073741824	...	1342177280
b1	0	1073741824	...	1342177280
Exp. a1	0	1073741824	...	1342177280
Exp. sfrb0	31	30	...	27
Exp. sfrb1	31	30	...	27
Exp. sfra1	31	30	...	27
Exp. b0	0	1073741824	...	1342177280
Exp. b1	0	1073741824	...	1342177280

Test settings	
Tolerance a1	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance sfra1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test statistics	
Min CPU cycles	2229
Max CPU cycles	8031
Avg CPU cycles	4701

Verification: Bilin FiP32 CPU STM32G474RE

Date of Test	2026-06-25
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for Filter block Bilin.

Test results				
Time step	1	2	...	73
CPU cycles	167	167	...	167
Inputs				
In (DSP)	-120706110	-44469415	...	999834674
In	-0.056	-0.021	...	0.466
Parameters				
b0	0.2			
b1	0.1			
a0	1.1			
a1	-0.7			
ts_fact	1			
Outputs				
Out	-0.01	-0.015	...	0.338
Exp. Out	-0.01	-0.015	...	0.338
Out (DSP)	-21946566	-33024628	...	725708721
Exp. Out (DSP)	-21946566	-33024627	...	725708723

Test settings	
Tolerance Out	±2,3283e-09 (±5 LSB)

Test statistics	
Min CPU cycles	167
Max CPU cycles	167
Avg CPU cycles	167

Test case: Conversion test OK

Conversion test for Filter block Bilin.

Test results				
Time step	1	2	...	8
Mask parameters				
b0	0	0.1	...	10
b1	0	0.1	...	10
a0	0.1	0.1	...	1
a1	0	0.1	...	10
ts_fact	1	1	...	1
Controller parameters				
a1	0	1073741824	...	1342177280
sfrb0	31	30	...	27
sfrb1	31	30	...	27
sfra1	31	30	...	27
b0	0	1073741824	...	1342177280
b1	0	1073741824	...	1342177280
Exp. a1	0	1073741824	...	1342177280
Exp. sfrb0	31	30	...	27
Exp. sfrb1	31	30	...	27
Exp. sfra1	31	30	...	27
Exp. b0	0	1073741824	...	1342177280
Exp. b1	0	1073741824	...	1342177280

Test settings	
Tolerance a1	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance sfra1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Filter block Bilin.

Test results				
Time step	1	2	...	8
Mask parameters				
b0	0	0.1	...	10
b1	0	0.1	...	10
a0	0.1	0.1	...	1
a1	0	0.1	...	10
ts_fact	1	1	...	1
Controller parameters				
a1	0	1073741824	...	1342177280
sfrb0	31	30	...	27
sfrb1	31	30	...	27
sfra1	31	30	...	27
b0	0	1073741824	...	1342177280
b1	0	1073741824	...	1342177280
Exp. a1	0	1073741824	...	1342177280
Exp. sfrb0	31	30	...	27
Exp. sfrb1	31	30	...	27
Exp. sfra1	31	30	...	27
Exp. b0	0	1073741824	...	1342177280
Exp. b1	0	1073741824	...	1342177280

Test settings	
Tolerance a1	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance sfra1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test statistics	
Min CPU cycles	2931
Max CPU cycles	5516
Avg CPU cycles	4004

Verification: Bilin FiP32 CPU STM32F072RB

Date of Test	2026-06-25
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for Filter block Bilin.

Test results				
Time step	1	2	...	73
CPU cycles	410	410	...	405
Inputs				
In (DSP)	-120706110	-44469415	...	999834674
In	-0.056	-0.021	...	0.466
Parameters				
b0	0.2			
b1	0.1			
a0	1.1			
a1	-0.7			
ts_fact	1			
Outputs				
Out	-0.01	-0.015	...	0.338
Exp. Out	-0.01	-0.015	...	0.338
Out (DSP)	-21946566	-33024628	...	725708721
Exp. Out (DSP)	-21946566	-33024627	...	725708723

Test settings	
Tolerance Out	±2,3283e-09 (±5 LSB)

Test statistics	
Min CPU cycles	405
Max CPU cycles	411
Avg CPU cycles	407

Test case: Conversion test OK

Conversion test for Filter block Bilin.

Test results				
Time step	1	2	...	8
Mask parameters				
b0	0	0.1	...	10
b1	0	0.1	...	10
a0	0.1	0.1	...	1
a1	0	0.1	...	10
ts_fact	1	1	...	1
Controller parameters				
a1	0	1073741824	...	1342177280
sfrb0	31	30	...	27
sfrb1	31	30	...	27
sfra1	31	30	...	27
b0	0	1073741824	...	1342177280
b1	0	1073741824	...	1342177280
Exp. a1	0	1073741824	...	1342177280
Exp. sfrb0	31	30	...	27
Exp. sfrb1	31	30	...	27
Exp. sfra1	31	30	...	27
Exp. b0	0	1073741824	...	1342177280
Exp. b1	0	1073741824	...	1342177280

Test settings	
Tolerance a1	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance sfra1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Filter block Bilin.

Test results				
Time step	1	2	...	8
Mask parameters				
b0	0	0.1	...	10
b1	0	0.1	...	10
a0	0.1	0.1	...	1
a1	0	0.1	...	10
ts_fact	1	1	...	1
Controller parameters				
a1	0	1073741824	...	1342177280
sfrb0	31	30	...	27
sfrb1	31	30	...	27
sfra1	31	30	...	27
b0	0	1073741824	...	1342177280
b1	0	1073741824	...	1342177280
Exp. a1	0	1073741824	...	1342177280
Exp. sfrb0	31	30	...	27
Exp. sfrb1	31	30	...	27
Exp. sfra1	31	30	...	27
Exp. b0	0	1073741824	...	1342177280
Exp. b1	0	1073741824	...	1342177280

Test settings	
Tolerance a1	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance sfra1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test statistics	
Min CPU cycles	8462
Max CPU cycles	19060
Avg CPU cycles	14421

Verification: Bilin FiP32 CPU PIC32MX170F256

Date of Test	2026-06-25
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for Filter block Bilin.

Test results				
Time step	1	2	...	73
CPU cycles	121	121	...	123
Inputs				
In (DSP)	-120706110	-44469415	...	999834674
In	-0.056	-0.021	...	0.466
Parameters				
b0	0.2			
b1	0.1			
a0	1.1			
a1	-0.7			
ts_fact	1			
Outputs				
Out	-0.01	-0.015	...	0.338
Exp. Out	-0.01	-0.015	...	0.338
Out (DSP)	-21946566	-33024628	...	725708721
Exp. Out (DSP)	-21946566	-33024627	...	725708723

Test settings	
Tolerance Out	±2,3283e-09 (±5 LSB)

Test statistics	
Min CPU cycles	121
Max CPU cycles	123
Avg CPU cycles	122

Test case: Conversion test OK

Conversion test for Filter block Bilin.

Test results				
Time step	1	2	...	8
Mask parameters				
b0	0	0.1	...	10
b1	0	0.1	...	10
a0	0.1	0.1	...	1
a1	0	0.1	...	10
ts_fact	1	1	...	1
Controller parameters				
a1	0	1073741824	...	1342177280
sfrb0	31	30	...	27
sfrb1	31	30	...	27
sfra1	31	30	...	27
b0	0	1073741824	...	1342177280
b1	0	1073741824	...	1342177280
Exp. a1	0	1073741824	...	1342177280
Exp. sfrb0	31	30	...	27
Exp. sfrb1	31	30	...	27
Exp. sfra1	31	30	...	27
Exp. b0	0	1073741824	...	1342177280
Exp. b1	0	1073741824	...	1342177280

Test settings	
Tolerance a1	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance sfra1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Filter block Bilin.

Test results				
Time step	1	2	...	8
Mask parameters				
b0	0	0.1	...	10
b1	0	0.1	...	10
a0	0.1	0.1	...	1
a1	0	0.1	...	10
ts_fact	1	1	...	1
Controller parameters				
a1	0	1073741824	...	1342177280
sfrb0	31	30	...	27
sfrb1	31	30	...	27
sfra1	31	30	...	27
b0	0	1073741824	...	1342177280
b1	0	1073741824	...	1342177280
Exp. a1	0	1073741824	...	1342177280
Exp. sfrb0	31	30	...	27
Exp. sfrb1	31	30	...	27
Exp. sfra1	31	30	...	27
Exp. b0	0	1073741824	...	1342177280
Exp. b1	0	1073741824	...	1342177280

Test settings	
Tolerance a1	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance sfra1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test statistics	
Min CPU cycles	3804
Max CPU cycles	7820
Avg CPU cycles	5893

Verification: Bilin FiP32 CPU dsPIC33EP256MC502

Date of Test	2026-06-25
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for Filter block Bilin.

Test results				
Time step	1	2	...	73
CPU cycles	1378	1386	...	1371
Inputs				
In (DSP)	-120706110	-44469415	...	999834674
In	-0.056	-0.021	...	0.466
Parameters				
b0	0.2			
b1	0.1			
a0	1.1			
a1	-0.7			
ts_fact	1			
Outputs				
Out	-0.01	-0.015	...	0.338
Exp. Out	-0.01	-0.015	...	0.338
Out (DSP)	-21946566	-33024628	...	725708721
Exp. Out (DSP)	-21946566	-33024627	...	725708723

Test settings	
Tolerance Out	±2,3283e-09 (±5 LSB)

Test statistics	
Min CPU cycles	1371
Max CPU cycles	1386
Avg CPU cycles	1377

Test case: Conversion test OK

Conversion test for Filter block Bilin.

Test results				
Time step	1	2	...	8
Mask parameters				
b0	0	0.1	...	10
b1	0	0.1	...	10
a0	0.1	0.1	...	1
a1	0	0.1	...	10
ts_fact	1	1	...	1
Controller parameters				
a1	0	1073741824	...	1342177280
sfrb0	31	30	...	27
sfrb1	31	30	...	27
sfra1	31	30	...	27
b0	0	1073741824	...	1342177280
b1	0	1073741824	...	1342177280
Exp. a1	0	1073741824	...	1342177280
Exp. sfrb0	31	30	...	27
Exp. sfrb1	31	30	...	27
Exp. sfra1	31	30	...	27
Exp. b0	0	1073741824	...	1342177280
Exp. b1	0	1073741824	...	1342177280

Test settings	
Tolerance a1	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance sfra1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Filter block Bilin.

Test results				
Time step	1	2	...	8
Mask parameters				
b0	0	0.1	...	10
b1	0	0.1	...	10
a0	0.1	0.1	...	1
a1	0	0.1	...	10
ts_fact	1	1	...	1
Controller parameters				
a1	0	1073741824	...	1342177280
sfrb0	31	30	...	27
sfrb1	31	30	...	27
sfra1	31	30	...	27
b0	0	1073741824	...	1342177280
b1	0	1073741824	...	1342177280
Exp. a1	0	1073741824	...	1342177280
Exp. sfrb0	31	30	...	27
Exp. sfrb1	31	30	...	27
Exp. sfra1	31	30	...	27
Exp. b0	0	1073741824	...	1342177280
Exp. b1	0	1073741824	...	1342177280

Test settings	
Tolerance a1	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance sfra1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test statistics	
Min CPU cycles	10170
Max CPU cycles	36947
Avg CPU cycles	24237

Verification: Bilin FiP32 CPU XMC4800-F144K2048

Date of Test	2026-06-25
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for Filter block Bilin.

Test results				
Time step	1	2	...	73
CPU cycles	164	142	...	142
Inputs				
In (DSP)	-120706110	-44469415	...	999834674
In	-0.056	-0.021	...	0.466
Parameters				
b0	0.2			
b1	0.1			
a0	1.1			
a1	-0.7			
ts_fact	1			
Outputs				
Out	-0.01	-0.015	...	0.338
Exp. Out	-0.01	-0.015	...	0.338
Out (DSP)	-21946566	-33024628	...	725708721
Exp. Out (DSP)	-21946566	-33024627	...	725708723

Test settings	
Tolerance Out	±2,3283e-09 (±5 LSB)

Test statistics	
Min CPU cycles	142
Max CPU cycles	164
Avg CPU cycles	142

Test case: Conversion test OK

Conversion test for Filter block Bilin.

Test results				
Time step	1	2	...	8
Mask parameters				
b0	0	0.1	...	10
b1	0	0.1	...	10
a0	0.1	0.1	...	1
a1	0	0.1	...	10
ts_fact	1	1	...	1
Controller parameters				
a1	0	1073741824	...	1342177280
sfrb0	31	30	...	27
sfrb1	31	30	...	27
sfra1	31	30	...	27
b0	0	1073741824	...	1342177280
b1	0	1073741824	...	1342177280
Exp. a1	0	1073741824	...	1342177280
Exp. sfrb0	31	30	...	27
Exp. sfrb1	31	30	...	27
Exp. sfra1	31	30	...	27
Exp. b0	0	1073741824	...	1342177280
Exp. b1	0	1073741824	...	1342177280

Test settings	
Tolerance a1	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance sfra1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Filter block Bilin.

Test results				
Time step	1	2	...	8
Mask parameters				
b0	0	0.1	...	10
b1	0	0.1	...	10
a0	0.1	0.1	...	1
a1	0	0.1	...	10
ts_fact	1	1	...	1
Controller parameters				
a1	0	1073741824	...	1342177280
sfrb0	31	30	...	27
sfrb1	31	30	...	27
sfra1	31	30	...	27
b0	0	1073741824	...	1342177280
b1	0	1073741824	...	1342177280
Exp. a1	0	1073741824	...	1342177280
Exp. sfrb0	31	30	...	27
Exp. sfrb1	31	30	...	27
Exp. sfra1	31	30	...	27
Exp. b0	0	1073741824	...	1342177280
Exp. b1	0	1073741824	...	1342177280

Test settings	
Tolerance a1	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance sfra1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test statistics	
Min CPU cycles	2588
Max CPU cycles	5130
Avg CPU cycles	3663

Verification: Bilin FiP32 CPU TMS320F28379D

Date of Test	2026-06-25
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for Filter block Bilin.

Test results				
Time step	1	2	...	73
CPU cycles	193	193	...	193
Inputs				
In (DSP)	-120706110	-44469415	...	999834674
In	-0.056	-0.021	...	0.466
Parameters				
b0	0.2			
b1	0.1			
a0	1.1			
a1	-0.7			
ts_fact	1			
Outputs				
Out	-0.01	-0.015	...	0.338
Exp. Out	-0.01	-0.015	...	0.338
Out (DSP)	-21946566	-33024628	...	725708721
Exp. Out (DSP)	-21946566	-33024627	...	725708723

Test settings	
Tolerance Out	±2,3283e-09 (±5 LSB)

Test statistics	
Min CPU cycles	193
Max CPU cycles	193
Avg CPU cycles	193

Test case: Conversion test OK

Conversion test for Filter block Bilin.

Test results				
Time step	1	2	...	8
Mask parameters				
b0	0	0.1	...	10
b1	0	0.1	...	10
a0	0.1	0.1	...	1
a1	0	0.1	...	10
ts_fact	1	1	...	1
Controller parameters				
a1	0	1073741824	...	1342177280
sfrb0	31	30	...	27
sfrb1	31	30	...	27
sfra1	31	30	...	27
b0	0	1073741824	...	1342177280
b1	0	1073741824	...	1342177280
Exp. a1	0	1073741824	...	1342177280
Exp. sfrb0	31	30	...	27
Exp. sfrb1	31	30	...	27
Exp. sfra1	31	30	...	27
Exp. b0	0	1073741824	...	1342177280
Exp. b1	0	1073741824	...	1342177280

Test settings	
Tolerance a1	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance sfra1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Filter block Bilin.

Test results				
Time step	1	2	...	8
Mask parameters				
b0	0	0.1	...	10
b1	0	0.1	...	10
a0	0.1	0.1	...	1
a1	0	0.1	...	10
ts_fact	1	1	...	1
Controller parameters				
a1	0	1073741824	...	1342177280
sfrb0	31	30	...	27
sfrb1	31	30	...	27
sfra1	31	30	...	27
b0	0	1073741824	...	1342177280
b1	0	1073741824	...	1342177280
Exp. a1	0	1073741824	...	1342177280
Exp. sfrb0	31	30	...	27
Exp. sfrb1	31	30	...	27
Exp. sfra1	31	30	...	27
Exp. b0	0	1073741824	...	1342177280
Exp. b1	0	1073741824	...	1342177280

Test settings	
Tolerance a1	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance sfra1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test statistics	
Min CPU cycles	3707
Max CPU cycles	14159
Avg CPU cycles	8200

Verification: Bilin Float32 CPU TMS320F28335

Date of Test	2026-06-25
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for Filter block Bilin.

Test results				
Time step	1	2	...	73
CPU cycles	65	65	...	65
Inputs				
In (DSP)	-0.056	-0.021	...	0.466
In	-0.056	-0.021	...	0.466
Parameters				
b0	0.2			
b1	0.1			
a0	1.1			
a1	-0.7			
ts_fact	1			
Outputs				
Out	-0.01	-0.015	...	0.338
Exp. Out	-0.01	-0.015	...	0.338
Out (DSP)	-0.01	-0.015	...	0.338
Exp. Out (DSP)	-0.01	-0.015	...	0.338

Test settings	
Tolerance Out	±9,3132e-08 (±200 LSB)

Test statistics	
Min CPU cycles	65
Max CPU cycles	65
Avg CPU cycles	65

Test case: Conversion test OK

Conversion test for Filter block Bilin.

Test results				
Time step	1	2	...	8
Mask parameters				
b0	0	0.1	...	10
b1	0	0.1	...	10
a0	0.1	0.1	...	1
a1	0	0.1	...	10
ts_fact	1	1	...	1
Controller parameters				
a1	0	1	...	10
b0	0	1	...	10
b1	0	1	...	10
Exp. a1	0	1	...	10
Exp. b0	0	1	...	10
Exp. b1	0	1	...	10

Test settings	
Tolerance a1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Filter block Bilin.

Test results				
Time step	1	2	...	8
Mask parameters				
b0	0	0.1	...	10
b1	0	0.1	...	10
a0	0.1	0.1	...	1
a1	0	0.1	...	10
ts_fact	1	1	...	1
Controller parameters				
a1	0	1	...	10
b0	0	1	...	10
b1	0	1	...	10
Exp. a1	0	1	...	10
Exp. b0	0	1	...	10
Exp. b1	0	1	...	10

Test settings	
Tolerance a1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test statistics	
Min CPU cycles	2974
Max CPU cycles	13480
Avg CPU cycles	6004

Verification: Bilin Float32 CPU TM4C123GH6

Date of Test	2026-06-25
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for Filter block Bilin.

Test results				
Time step	1	2	...	73
CPU cycles	41	41	...	41
Inputs				
In (DSP)	-0.056	-0.021	...	0.466
In	-0.056	-0.021	...	0.466
Parameters				
b0	0.2			
b1	0.1			
a0	1.1			
a1	-0.7			
ts_fact	1			
Outputs				
Out	-0.01	-0.015	...	0.338
Exp. Out	-0.01	-0.015	...	0.338
Out (DSP)	-0.01	-0.015	...	0.338
Exp. Out (DSP)	-0.01	-0.015	...	0.338

Test settings	
Tolerance Out	±9,3132e-08 (±200 LSB)

Test statistics	
Min CPU cycles	41
Max CPU cycles	41
Avg CPU cycles	41

Test case: Conversion test OK

Conversion test for Filter block Bilin.

Test results				
Time step	1	2	...	8
Mask parameters				
b0	0	0.1	...	10
b1	0	0.1	...	10
a0	0.1	0.1	...	1
a1	0	0.1	...	10
ts_fact	1	1	...	1
Controller parameters				
a1	0	1	...	10
b0	0	1	...	10
b1	0	1	...	10
Exp. a1	0	1	...	10
Exp. b0	0	1	...	10
Exp. b1	0	1	...	10

Test settings	
Tolerance a1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Filter block Bilin.

Test results				
Time step	1	2	...	8
Mask parameters				
b0	0	0.1	...	10
b1	0	0.1	...	10
a0	0.1	0.1	...	1
a1	0	0.1	...	10
ts_fact	1	1	...	1
Controller parameters				
a1	0	1	...	10
b0	0	1	...	10
b1	0	1	...	10
Exp. a1	0	1	...	10
Exp. b0	0	1	...	10
Exp. b1	0	1	...	10

Test settings	
Tolerance a1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test statistics	
Min CPU cycles	1381
Max CPU cycles	5719
Avg CPU cycles	2632

Verification: Bilin Float32 CPU STM32G474RE

Date of Test	2026-06-25
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for Filter block Bilin.

Test results				
Time step	1	2	...	73
CPU cycles	82	82	...	82
Inputs				
In (DSP)	-0.056	-0.021	...	0.466
In	-0.056	-0.021	...	0.466
Parameters				
b0	0.2			
b1	0.1			
a0	1.1			
a1	-0.7			
ts_fact	1			
Outputs				
Out	-0.01	-0.015	...	0.338
Exp. Out	-0.01	-0.015	...	0.338
Out (DSP)	-0.01	-0.015	...	0.338
Exp. Out (DSP)	-0.01	-0.015	...	0.338

Test settings	
Tolerance Out	±9,3132e-08 (±200 LSB)

Test statistics	
Min CPU cycles	82
Max CPU cycles	82
Avg CPU cycles	82

Test case: Conversion test OK

Conversion test for Filter block Bilin.

Test results				
Time step	1	2	...	8
Mask parameters				
b0	0	0.1	...	10
b1	0	0.1	...	10
a0	0.1	0.1	...	1
a1	0	0.1	...	10
ts_fact	1	1	...	1
Controller parameters				
a1	0	1	...	10
b0	0	1	...	10
b1	0	1	...	10
Exp. a1	0	1	...	10
Exp. b0	0	1	...	10
Exp. b1	0	1	...	10

Test settings	
Tolerance a1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Filter block Bilin.

Test results				
Time step	1	2	...	8
Mask parameters				
b0	0	0.1	...	10
b1	0	0.1	...	10
a0	0.1	0.1	...	1
a1	0	0.1	...	10
ts_fact	1	1	...	1
Controller parameters				
a1	0	1	...	10
b0	0	1	...	10
b1	0	1	...	10
Exp. a1	0	1	...	10
Exp. b0	0	1	...	10
Exp. b1	0	1	...	10

Test settings	
Tolerance a1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test statistics	
Min CPU cycles	1165
Max CPU cycles	2994
Avg CPU cycles	1633

Verification: Bilin Float32 CPU STM32F072RB

Date of Test	2026-06-25
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for Filter block Bilin.

Test results				
Time step	1	2	...	73
CPU cycles	650	859	...	836
Inputs				
In (DSP)	-0.056	-0.021	...	0.466
In	-0.056	-0.021	...	0.466
Parameters				
b0	0.2			
b1	0.1			
a0	1.1			
a1	-0.7			
ts_fact	1			
Outputs				
Out	-0.01	-0.015	...	0.338
Exp. Out	-0.01	-0.015	...	0.338
Out (DSP)	-0.01	-0.015	...	0.338
Exp. Out (DSP)	-0.01	-0.015	...	0.338

Test settings	
Tolerance Out	±9,3132e-08 (±200 LSB)

Test statistics	
Min CPU cycles	650
Max CPU cycles	912
Avg CPU cycles	848

Test case: Conversion test OK

Conversion test for Filter block Bilin.

Test results				
Time step	1	2	...	8
Mask parameters				
b0	0	0.1	...	10
b1	0	0.1	...	10
a0	0.1	0.1	...	1
a1	0	0.1	...	10
ts_fact	1	1	...	1
Controller parameters				
a1	0	1	...	10
b0	0	1	...	10
b1	0	1	...	10
Exp. a1	0	1	...	10
Exp. b0	0	1	...	10
Exp. b1	0	1	...	10

Test settings	
Tolerance a1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Filter block Bilin.

Test results				
Time step	1	2	...	8
Mask parameters				
b0	0	0.1	...	10
b1	0	0.1	...	10
a0	0.1	0.1	...	1
a1	0	0.1	...	10
ts_fact	1	1	...	1
Controller parameters				
a1	0	1	...	10
b0	0	1	...	10
b1	0	1	...	10
Exp. a1	0	1	...	10
Exp. b0	0	1	...	10
Exp. b1	0	1	...	10

Test settings	
Tolerance a1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test statistics	
Min CPU cycles	2424
Max CPU cycles	4811
Avg CPU cycles	3781

Verification: Bilin Float32 CPU PIC32MX170F256

Date of Test	2026-06-25
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for Filter block Bilin.

Test results				
Time step	1	2	...	73
CPU cycles	230	328	...	334
Inputs				
In (DSP)	-0.056	-0.021	...	0.466
In	-0.056	-0.021	...	0.466
Parameters				
b0	0.2			
b1	0.1			
a0	1.1			
a1	-0.7			
ts_fact	1			
Outputs				
Out	-0.01	-0.015	...	0.338
Exp. Out	-0.01	-0.015	...	0.338
Out (DSP)	-0.01	-0.015	...	0.338
Exp. Out (DSP)	-0.01	-0.015	...	0.338

Test settings	
Tolerance Out	±9,3132e-08 (±200 LSB)

Test statistics	
Min CPU cycles	230
Max CPU cycles	338
Avg CPU cycles	326

Test case: Conversion test OK

Conversion test for Filter block Bilin.

Test results				
Time step	1	2	...	8
Mask parameters				
b0	0	0.1	...	10
b1	0	0.1	...	10
a0	0.1	0.1	...	1
a1	0	0.1	...	10
ts_fact	1	1	...	1
Controller parameters				
a1	0	1	...	10
b0	0	1	...	10
b1	0	1	...	10
Exp. a1	0	1	...	10
Exp. b0	0	1	...	10
Exp. b1	0	1	...	10

Test settings	
Tolerance a1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Filter block Bilin.

Test results				
Time step	1	2	...	8
Mask parameters				
b0	0	0.1	...	10
b1	0	0.1	...	10
a0	0.1	0.1	...	1
a1	0	0.1	...	10
ts_fact	1	1	...	1
Controller parameters				
a1	0	1	...	10
b0	0	1	...	10
b1	0	1	...	10
Exp. a1	0	1	...	10
Exp. b0	0	1	...	10
Exp. b1	0	1	...	10

Test settings	
Tolerance a1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test statistics	
Min CPU cycles	930
Max CPU cycles	1659
Avg CPU cycles	1424

Verification: Bilin Float32 CPU dsPIC33EP256MC502

Date of Test	2026-06-25
Target controller	dsPIC33EP256MC502

Test case: Inport test — OK

Inport test for Filter block Bilin.

Test results				
Time step	1	2	...	73
CPU cycles	668	861	...	854
Inputs				
In (DSP)	-0.056	-0.021	...	0.466
In	-0.056	-0.021	...	0.466
Parameters				
b0	0.2			
b1	0.1			
a0	1.1			
a1	-0.7			
ts_fact	1			
Outputs				
Out	-0.01	-0.015	...	0.338
Exp. Out	-0.01	-0.015	...	0.338
Out (DSP)	-0.01	-0.015	...	0.338
Exp. Out (DSP)	-0.01	-0.015	...	0.338

Test settings	
Tolerance Out	±9,3132e-08 (±200 LSB)

Test statistics	
Min CPU cycles	668
Max CPU cycles	958
Avg CPU cycles	868

Test case: Conversion test — OK

Conversion test for Filter block Bilin.

Test results				
Time step	1	2	...	8
Mask parameters				
b0	0	0.1	...	10
b1	0	0.1	...	10
a0	0.1	0.1	...	1
a1	0	0.1	...	10
ts_fact	1	1	...	1
Controller parameters				
a1	0	1	...	10
b0	0	1	...	10
b1	0	1	...	10
Exp. a1	0	1	...	10
Exp. b0	0	1	...	10
Exp. b1	0	1	...	10

Test settings	
Tolerance a1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Filter block Bilin.

Test results				
Time step	1	2	...	8
Mask parameters				
b0	0	0.1	...	10
b1	0	0.1	...	10
a0	0.1	0.1	...	1
a1	0	0.1	...	10
ts_fact	1	1	...	1
Controller parameters				
a1	0	1	...	10
b0	0	1	...	10
b1	0	1	...	10
Exp. a1	0	1	...	10
Exp. b0	0	1	...	10
Exp. b1	0	1	...	10

Test settings	
Tolerance a1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test statistics	
Min CPU cycles	2988
Max CPU cycles	7784
Avg CPU cycles	7124

Verification: Bilin Float32 CPU XMC4800-F144K2048

Date of Test	2026-06-25
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for Filter block Bilin.

Test results				
Time step	1	2	...	73
CPU cycles	88	76	...	76
Inputs				
In (DSP)	-0.056	-0.021	...	0.466
In	-0.056	-0.021	...	0.466
Parameters				
b0	0.2			
b1	0.1			
a0	1.1			
a1	-0.7			
ts_fact	1			
Outputs				
Out	-0.01	-0.015	...	0.338
Exp. Out	-0.01	-0.015	...	0.338
Out (DSP)	-0.01	-0.015	...	0.338
Exp. Out (DSP)	-0.01	-0.015	...	0.338

Test settings	
Tolerance Out	±9,3132e-08 (±200 LSB)

Test statistics	
Min CPU cycles	76
Max CPU cycles	88
Avg CPU cycles	76

Test case: Conversion test OK

Conversion test for Filter block Bilin.

Test results				
Time step	1	2	...	8
Mask parameters				
b0	0	0.1	...	10
b1	0	0.1	...	10
a0	0.1	0.1	...	1
a1	0	0.1	...	10
ts_fact	1	1	...	1
Controller parameters				
a1	0	1	...	10
b0	0	1	...	10
b1	0	1	...	10
Exp. a1	0	1	...	10
Exp. b0	0	1	...	10
Exp. b1	0	1	...	10

Test settings	
Tolerance a1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Filter block Bilin.

Test results				
Time step	1	2	...	8
Mask parameters				
b0	0	0.1	...	10
b1	0	0.1	...	10
a0	0.1	0.1	...	1
a1	0	0.1	...	10
ts_fact	1	1	...	1
Controller parameters				
a1	0	1	...	10
b0	0	1	...	10
b1	0	1	...	10
Exp. a1	0	1	...	10
Exp. b0	0	1	...	10
Exp. b1	0	1	...	10

Test settings	
Tolerance a1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test statistics	
Min CPU cycles	1037
Max CPU cycles	2847
Avg CPU cycles	1512

Verification: Bilin Float32 CPU TMS320F28379D

Date of Test	2026-06-25
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for Filter block Bilin.

Test results				
Time step	1	2	...	73
CPU cycles	58	58	...	58
Inputs				
In (DSP)	-0.056	-0.021	...	0.466
In	-0.056	-0.021	...	0.466
Parameters				
b0	0.2			
b1	0.1			
a0	1.1			
a1	-0.7			
ts_fact	1			
Outputs				
Out	-0.01	-0.015	...	0.338
Exp. Out	-0.01	-0.015	...	0.338
Out (DSP)	-0.01	-0.015	...	0.338
Exp. Out (DSP)	-0.01	-0.015	...	0.338

Test settings	
Tolerance Out	±9,3132e-08 (±200 LSB)

Test statistics	
Min CPU cycles	58
Max CPU cycles	58
Avg CPU cycles	58

Test case: Conversion test OK

Conversion test for Filter block Bilin.

Test results				
Time step	1	2	...	8
Mask parameters				
b0	0	0.1	...	10
b1	0	0.1	...	10
a0	0.1	0.1	...	1
a1	0	0.1	...	10
ts_fact	1	1	...	1
Controller parameters				
a1	0	1	...	10
b0	0	1	...	10
b1	0	1	...	10
Exp. a1	0	1	...	10
Exp. b0	0	1	...	10
Exp. b1	0	1	...	10

Test settings	
Tolerance a1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

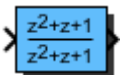
Conversion-on-Target test for Filter block Bilin.

Test results				
Time step	1	2	...	8
Mask parameters				
b0	0	0.1	...	10
b1	0	0.1	...	10
a0	0.1	0.1	...	1
a1	0	0.1	...	10
ts_fact	1	1	...	1
Controller parameters				
a1	0	1	...	10
b0	0	1	...	10
b1	0	1	...	10
Exp. a1	0	1	...	10
Exp. b0	0	1	...	10
Exp. b1	0	1	...	10

Test settings	
Tolerance a1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test statistics	
Min CPU cycles	2123
Max CPU cycles	9827
Avg CPU cycles	4360

Block: Biquad



Second order transfer function:
H(z) = (b0.z^2 + b1.z + b2) / (a0.z^2 + a1.z + a2)

Inports	
In	Input In(k)

Outports	
Out	Output Out(k)

Mask Parameters		
Name	**ID**	**Description**
b0	1	Filter coefficient b0
b1	2	Filter coefficient b1
b2	3	Filter coefficient b2
a0	4	Filter coefficient a0
a1	5	Filter coefficient a1
a2	6	Filter coefficient a2
ts_fact	7	Multiplication factor of base sampling time (in integer format)

Description:

Alternative representation of the same transfer function:

$$H(z) = \frac{b_0 + b_1 z^{-1} + b_2 z^{-2}}{a_0 + a_1 z^{-1} + a_2 z^{-2}}$$

Implementations:

FiP16 16 Bit Fixed Point Implementation
FiP32 32 Bit Fixed Point Implementation
Float32 32 Bit Floating Point Implementation
Float64 64 Bit Floating Point Implementation

Implementation: FiP16

16 Bit Fixed Point Implementation

Inports Data Type	
In	int16

Outports Data Type	
Out	int16

Implementation: FiP32

32 Bit Fixed Point Implementation

Inports Data Type	
In	int32

Outports Data Type	
Out	int32

Implementation: Float32

32 Bit Floating Point Implementation

Inports Data Type	
In	float32

Outports Data Type	
Out	float32

Implementation: Float64

64 Bit Floating Point Implementation

Inports Data Type	
In	float64

Outports Data Type	
Out	float64

Verification: Biquad FiP16 CPU TMS320F28335

Date of Test	2026-06-25
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for Filter block Biquad.

Test results						
Time step	1	2	3	4	...	73
CPU cycles	116	116	116	116	...	116
Inputs						
In (DSP)	-1842	-679	5729	7954	...	15256
In	-0.056	-0.021	0.175	0.243	...	0.466
Parameters						
b0	0.2					
b1	0.1					
b2	0.3					
a0	1.1					
a1	-0.7					
a2	0.8					
ts_fact	1					
Outputs						
Out	-0.01	-0.015	0.012	0.073	...	0.257
Exp. Out	-0.01	-0.015	0.012	0.073	...	0.257
Out (DSP)	-335	-505	399	2402	...	8434
Exp. Out (DSP)	-335	-504	401	2403	...	8434

Test settings	
Tolerance Out	±1,5259e-04 (±5 LSB)

Test statistics	
Min CPU cycles	116
Max CPU cycles	116
Avg CPU cycles	116

Test case: Conversion test OK

Conversion test for Filter block Biquad.

Test results						
Time step	1	2	3	4	...	8
Mask parameters						
b0	0	0.1	0.2	0.5	...	10
b1	0	0.1	0.2	0.5	...	10
b2	0	0.1	0.2	0.5	...	10
a0	0.1	0.1	0.1	1	...	1
a1	0	0.1	0.2	0.5	...	10
a2	0	0.1	0.2	0.5	...	10
ts_fact	1	1	1	1	...	1
Controller parameters						
b2	0	16384	16384	16384	...	20480
a1	0	16384	16384	16384	...	20480
a2	0	16384	16384	16384	...	20480
sfra2	15	14	13	15	...	11
sfrb0	15	14	13	15	...	11
sfrb1	15	14	13	15	...	11
sfrb2	15	14	13	15	...	11
sfra1	15	14	13	15	...	11
b0	0	16384	16384	16384	...	20480
b1	0	16384	16384	16384	...	20480
Exp. b2	0	16384	16384	16384	...	20480
Exp. a1	0	16384	16384	16384	...	20480
Exp. a2	0	16384	16384	16384	...	20480
Exp. sfra2	15	14	13	15	...	11
Exp. sfrb0	15	14	13	15	...	11
Exp. sfrb1	15	14	13	15	...	11
Exp. sfrb2	15	14	13	15	...	11
Exp. sfra1	15	14	13	15	...	11
Exp. b0	0	16384	16384	16384	...	20480
Exp. b1	0	16384	16384	16384	...	20480

Test settings	
Tolerance b2	±0,0000e+00
Tolerance a1	±0,0000e+00
Tolerance a2	±0,0000e+00
Tolerance sfra2	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance sfrb2	±0,0000e+00
Tolerance sfra1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Filter block Biquad.

Test results						
Time step	1	2	3	4	...	8
Mask parameters						
b0	0	0.1	0.2	0.5	...	10
b1	0	0.1	0.2	0.5	...	10
b2	0	0.1	0.2	0.5	...	10
a0	0.1	0.1	0.1	1	...	1
a1	0	0.1	0.2	0.5	...	10
a2	0	0.1	0.2	0.5	...	10
ts_fact	1	1	1	1	...	1
Controller parameters						
b2	0	16384	16384	16384	...	20480
a1	0	16384	16384	16384	...	20480
a2	0	16384	16384	16384	...	20480
sfra2	15	14	13	15	...	11
sfrb0	15	14	13	15	...	11
sfrb1	15	14	13	15	...	11
sfrb2	15	14	13	15	...	11
sfra1	15	14	13	15	...	11
b0	0	16384	16384	16384	...	20480
b1	0	16384	16384	16384	...	20480
Exp. b2	0	16384	16384	16384	...	20480
Exp. a1	0	16384	16384	16384	...	20480
Exp. a2	0	16384	16384	16384	...	20480
Exp. sfra2	15	14	13	15	...	11
Exp. sfrb0	15	14	13	15	...	11
Exp. sfrb1	15	14	13	15	...	11
Exp. sfrb2	15	14	13	15	...	11
Exp. sfra1	15	14	13	15	...	11
Exp. b0	0	16384	16384	16384	...	20480
Exp. b1	0	16384	16384	16384	...	20480

Test settings	
Tolerance b2	±0,0000e+00
Tolerance a1	±0,0000e+00
Tolerance a2	±0,0000e+00
Tolerance sfra2	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance sfrb2	±0,0000e+00
Tolerance sfra1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test statistics	
Min CPU cycles	6789
Max CPU cycles	30034
Avg CPU cycles	16535

Verification: Biquad FiP16 CPU TM4C123GH6

Date of Test	2026-06-25
Target controller	TM4C123GH6

Test case: Inport test — OK

Inport test for Filter block Biquad.

Test results						
Time step	1	2	3	4	...	73
CPU cycles	93	93	93	93	...	93
Inputs						
In (DSP)	-1842	-679	5729	7954	...	15256
In	-0.056	-0.021	0.175	0.243	...	0.466
Parameters						
b0	0.2					
b1	0.1					
b2	0.3					
a0	1.1					
a1	-0.7					
a2	0.8					
ts_fact	1					
Outputs						
Out	-0.01	-0.015	0.012	0.073	...	0.257
Exp. Out	-0.01	-0.015	0.012	0.073	...	0.257
Out (DSP)	-335	-505	399	2402	...	8434
Exp. Out (DSP)	-335	-504	401	2403	...	8434

Test settings	
Tolerance Out	±1,5259e-04 (±5 LSB)

Test statistics	
Min CPU cycles	93
Max CPU cycles	93
Avg CPU cycles	93

Test case: Conversion test — OK

Conversion test for Filter block Biquad.

Test results						
Time step	1	2	3	4	...	8
Mask parameters						
b0	0	0.1	0.2	0.5	...	10
b1	0	0.1	0.2	0.5	...	10
b2	0	0.1	0.2	0.5	...	10
a0	0.1	0.1	0.1	1	...	1
a1	0	0.1	0.2	0.5	...	10
a2	0	0.1	0.2	0.5	...	10
ts_fact	1	1	1	1	...	1
Controller parameters						
b2	0	16384	16384	16384	...	20480
a1	0	16384	16384	16384	...	20480
a2	0	16384	16384	16384	...	20480
sfra2	15	14	13	15	...	11
sfrb0	15	14	13	15	...	11
sfrb1	15	14	13	15	...	11
sfrb2	15	14	13	15	...	11
sfra1	15	14	13	15	...	11
b0	0	16384	16384	16384	...	20480
b1	0	16384	16384	16384	...	20480
Exp. b2	0	16384	16384	16384	...	20480
Exp. a1	0	16384	16384	16384	...	20480
Exp. a2	0	16384	16384	16384	...	20480
Exp. sfra2	15	14	13	15	...	11
Exp. sfrb0	15	14	13	15	...	11
Exp. sfrb1	15	14	13	15	...	11
Exp. sfrb2	15	14	13	15	...	11
Exp. sfra1	15	14	13	15	...	11
Exp. b0	0	16384	16384	16384	...	20480
Exp. b1	0	16384	16384	16384	...	20480

Test settings	
Tolerance b2	±0,0000e+00
Tolerance a1	±0,0000e+00
Tolerance a2	±0,0000e+00
Tolerance sfra2	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance sfrb2	±0,0000e+00
Tolerance sfra1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Filter block Biquad.

Test results						
Time step	1	2	3	4	...	8
Mask parameters						
b0	0	0.1	0.2	0.5	...	10
b1	0	0.1	0.2	0.5	...	10
b2	0	0.1	0.2	0.5	...	10
a0	0.1	0.1	0.1	1	...	1
a1	0	0.1	0.2	0.5	...	10
a2	0	0.1	0.2	0.5	...	10
ts_fact	1	1	1	1	...	1
Controller parameters						
b2	0	16384	16384	16384	...	20480
a1	0	16384	16384	16384	...	20480
a2	0	16384	16384	16384	...	20480
sfra2	15	14	13	15	...	11
sfrb0	15	14	13	15	...	11
sfrb1	15	14	13	15	...	11
sfrb2	15	14	13	15	...	11
sfra1	15	14	13	15	...	11
b0	0	16384	16384	16384	...	20480
b1	0	16384	16384	16384	...	20480
Exp. b2	0	16384	16384	16384	...	20480
Exp. a1	0	16384	16384	16384	...	20480
Exp. a2	0	16384	16384	16384	...	20480
Exp. sfra2	15	14	13	15	...	11
Exp. sfrb0	15	14	13	15	...	11
Exp. sfrb1	15	14	13	15	...	11
Exp. sfrb2	15	14	13	15	...	11
Exp. sfra1	15	14	13	15	...	11
Exp. b0	0	16384	16384	16384	...	20480
Exp. b1	0	16384	16384	16384	...	20480

Test settings	
Tolerance b2	±0,0000e+00
Tolerance a1	±0,0000e+00
Tolerance a2	±0,0000e+00
Tolerance sfra2	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance sfrb2	±0,0000e+00
Tolerance sfra1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test statistics	
Min CPU cycles	3473
Max CPU cycles	13973
Avg CPU cycles	8260

Verification: Biquad FiP16 CPU STM32G474RE

Date of Test	2026-06-25
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for Filter block Biquad.

Test results						
Time step	1	2	3	4	...	73
CPU cycles	147	147	147	147	...	147
Inputs						
In (DSP)	-1842	-679	5729	7954	...	15256
In	-0.056	-0.021	0.175	0.243	...	0.466
Parameters						
b0	0.2					
b1	0.1					
b2	0.3					
a0	1.1					
a1	-0.7					
a2	0.8					
ts_fact	1					
Outputs						
Out	-0.01	-0.015	0.012	0.073	...	0.257
Exp. Out	-0.01	-0.015	0.012	0.073	...	0.257
Out (DSP)	-335	-505	399	2402	...	8434
Exp. Out (DSP)	-335	-504	401	2403	...	8434

Test settings	
Tolerance Out	±1,5259e-04 (±5 LSB)

Test statistics	
Min CPU cycles	147
Max CPU cycles	147
Avg CPU cycles	147

Test case: Conversion test OK

Conversion test for Filter block Biquad.

Test results						
Time step	1	2	3	4	...	8
Mask parameters						
b0	0	0.1	0.2	0.5	...	10
b1	0	0.1	0.2	0.5	...	10
b2	0	0.1	0.2	0.5	...	10
a0	0.1	0.1	0.1	1	...	1
a1	0	0.1	0.2	0.5	...	10
a2	0	0.1	0.2	0.5	...	10
ts_fact	1	1	1	1	...	1
Controller parameters						
b2	0	16384	16384	16384	...	20480
a1	0	16384	16384	16384	...	20480
a2	0	16384	16384	16384	...	20480
sfra2	15	14	13	15	...	11
sfrb0	15	14	13	15	...	11
sfrb1	15	14	13	15	...	11
sfrb2	15	14	13	15	...	11
sfra1	15	14	13	15	...	11
b0	0	16384	16384	16384	...	20480
b1	0	16384	16384	16384	...	20480
Exp. b2	0	16384	16384	16384	...	20480
Exp. a1	0	16384	16384	16384	...	20480
Exp. a2	0	16384	16384	16384	...	20480
Exp. sfra2	15	14	13	15	...	11
Exp. sfrb0	15	14	13	15	...	11
Exp. sfrb1	15	14	13	15	...	11
Exp. sfrb2	15	14	13	15	...	11
Exp. sfra1	15	14	13	15	...	11
Exp. b0	0	16384	16384	16384	...	20480
Exp. b1	0	16384	16384	16384	...	20480

Test settings	
Tolerance b2	±0,0000e+00
Tolerance a1	±0,0000e+00
Tolerance a2	±0,0000e+00
Tolerance sfra2	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance sfrb2	±0,0000e+00
Tolerance sfra1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Filter block Biquad.

Test results						
Time step	1	2	3	4	...	8
Mask parameters						
b0	0	0.1	0.2	0.5	...	10
b1	0	0.1	0.2	0.5	...	10
b2	0	0.1	0.2	0.5	...	10
a0	0.1	0.1	0.1	1	...	1
a1	0	0.1	0.2	0.5	...	10
a2	0	0.1	0.2	0.5	...	10
ts_fact	1	1	1	1	...	1
Controller parameters						
b2	0	16384	16384	16384	...	20480
a1	0	16384	16384	16384	...	20480
a2	0	16384	16384	16384	...	20480
sfra2	15	14	13	15	...	11
sfrb0	15	14	13	15	...	11
sfrb1	15	14	13	15	...	11
sfrb2	15	14	13	15	...	11
sfra1	15	14	13	15	...	11
b0	0	16384	16384	16384	...	20480
b1	0	16384	16384	16384	...	20480
Exp. b2	0	16384	16384	16384	...	20480
Exp. a1	0	16384	16384	16384	...	20480
Exp. a2	0	16384	16384	16384	...	20480
Exp. sfra2	15	14	13	15	...	11
Exp. sfrb0	15	14	13	15	...	11
Exp. sfrb1	15	14	13	15	...	11
Exp. sfrb2	15	14	13	15	...	11
Exp. sfra1	15	14	13	15	...	11
Exp. b0	0	16384	16384	16384	...	20480
Exp. b1	0	16384	16384	16384	...	20480

Test settings	
Tolerance b2	±0,0000e+00
Tolerance a1	±0,0000e+00
Tolerance a2	±0,0000e+00
Tolerance sfra2	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance sfrb2	±0,0000e+00
Tolerance sfra1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test statistics	
Min CPU cycles	2955
Max CPU cycles	7208
Avg CPU cycles	4737

Verification: Biquad FiP16 CPU STM32F072RB

Date of Test	2026-06-25
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for Filter block Biquad.

Test results						
Time step	1	2	3	4	...	73
CPU cycles	133	133	133	133	...	133
Inputs						
In (DSP)	-1842	-679	5729	7954	...	15256
In	-0.056	-0.021	0.175	0.243	...	0.466
Parameters						
b0	0.2					
b1	0.1					
b2	0.3					
a0	1.1					
a1	-0.7					
a2	0.8					
ts_fact	1					
Outputs						
Out	-0.01	-0.015	0.012	0.073	...	0.257
Exp. Out	-0.01	-0.015	0.012	0.073	...	0.257
Out (DSP)	-335	-505	399	2402	...	8434
Exp. Out (DSP)	-335	-504	401	2403	...	8434

Test settings	
Tolerance Out	±1,5259e-04 (±5 LSB)

Test statistics	
Min CPU cycles	133
Max CPU cycles	133
Avg CPU cycles	133

Test case: Conversion test OK

Conversion test for Filter block Biquad.

Test results						
Time step	1	2	3	4	...	8
Mask parameters						
b0	0	0.1	0.2	0.5	...	10
b1	0	0.1	0.2	0.5	...	10
b2	0	0.1	0.2	0.5	...	10
a0	0.1	0.1	0.1	1	...	1
a1	0	0.1	0.2	0.5	...	10
a2	0	0.1	0.2	0.5	...	10
ts_fact	1	1	1	1	...	1
Controller parameters						
b2	0	16384	16384	16384	...	20480
a1	0	16384	16384	16384	...	20480
a2	0	16384	16384	16384	...	20480
sfra2	15	14	13	15	...	11
sfrb0	15	14	13	15	...	11
sfrb1	15	14	13	15	...	11
sfrb2	15	14	13	15	...	11
sfra1	15	14	13	15	...	11
b0	0	16384	16384	16384	...	20480
b1	0	16384	16384	16384	...	20480
Exp. b2	0	16384	16384	16384	...	20480
Exp. a1	0	16384	16384	16384	...	20480
Exp. a2	0	16384	16384	16384	...	20480
Exp. sfra2	15	14	13	15	...	11
Exp. sfrb0	15	14	13	15	...	11
Exp. sfrb1	15	14	13	15	...	11
Exp. sfrb2	15	14	13	15	...	11
Exp. sfra1	15	14	13	15	...	11
Exp. b0	0	16384	16384	16384	...	20480
Exp. b1	0	16384	16384	16384	...	20480

Test settings	
Tolerance b2	±0,0000e+00
Tolerance a1	±0,0000e+00
Tolerance a2	±0,0000e+00
Tolerance sfra2	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance sfrb2	±0,0000e+00
Tolerance sfra1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Filter block Biquad.

Test results						
Time step	1	2	3	4	...	8
Mask parameters						
b0	0	0.1	0.2	0.5	...	10
b1	0	0.1	0.2	0.5	...	10
b2	0	0.1	0.2	0.5	...	10
a0	0.1	0.1	0.1	1	...	1
a1	0	0.1	0.2	0.5	...	10
a2	0	0.1	0.2	0.5	...	10
ts_fact	1	1	1	1	...	1
Controller parameters						
b2	0	16384	16384	16384	...	20480
a1	0	16384	16384	16384	...	20480
a2	0	16384	16384	16384	...	20480
sfra2	15	14	13	15	...	11
sfrb0	15	14	13	15	...	11
sfrb1	15	14	13	15	...	11
sfrb2	15	14	13	15	...	11
sfra1	15	14	13	15	...	11
b0	0	16384	16384	16384	...	20480
b1	0	16384	16384	16384	...	20480
Exp. b2	0	16384	16384	16384	...	20480
Exp. a1	0	16384	16384	16384	...	20480
Exp. a2	0	16384	16384	16384	...	20480
Exp. sfra2	15	14	13	15	...	11
Exp. sfrb0	15	14	13	15	...	11
Exp. sfrb1	15	14	13	15	...	11
Exp. sfrb2	15	14	13	15	...	11
Exp. sfra1	15	14	13	15	...	11
Exp. b0	0	16384	16384	16384	...	20480
Exp. b1	0	16384	16384	16384	...	20480

Test settings	
Tolerance b2	±0,0000e+00
Tolerance a1	±0,0000e+00
Tolerance a2	±0,0000e+00
Tolerance sfra2	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance sfrb2	±0,0000e+00
Tolerance sfra1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test statistics	
Min CPU cycles	8245
Max CPU cycles	24696
Avg CPU cycles	17166

Verification: Biquad FiP16 CPU PIC32MX170F256

Date of Test	2026-06-25
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for Filter block Biquad.

Test results						
Time step	1	2	3	4	...	73
CPU cycles	90	90	90	90	...	90
Inputs						
In (DSP)	-1842	-679	5729	7954	...	15256
In	-0.056	-0.021	0.175	0.243	...	0.466
Parameters						
b0	0.2					
b1	0.1					
b2	0.3					
a0	1.1					
a1	-0.7					
a2	0.8					
ts_fact	1					
Outputs						
Out	-0.01	-0.015	0.012	0.073	...	0.257
Exp. Out	-0.01	-0.015	0.012	0.073	...	0.257
Out (DSP)	-335	-505	399	2402	...	8434
Exp. Out (DSP)	-335	-504	401	2403	...	8434

Test settings	
Tolerance Out	±1,5259e-04 (±5 LSB)

Test statistics	
Min CPU cycles	90
Max CPU cycles	90
Avg CPU cycles	90

Test case: Conversion test OK

Conversion test for Filter block Biquad.

Test results						
Time step	1	2	3	4	...	8
Mask parameters						
b0	0	0.1	0.2	0.5	...	10
b1	0	0.1	0.2	0.5	...	10
b2	0	0.1	0.2	0.5	...	10
a0	0.1	0.1	0.1	1	...	1
a1	0	0.1	0.2	0.5	...	10
a2	0	0.1	0.2	0.5	...	10
ts_fact	1	1	1	1	...	1
Controller parameters						
b2	0	16384	16384	16384	...	20480
a1	0	16384	16384	16384	...	20480
a2	0	16384	16384	16384	...	20480
sfra2	15	14	13	15	...	11
sfrb0	15	14	13	15	...	11
sfrb1	15	14	13	15	...	11
sfrb2	15	14	13	15	...	11
sfra1	15	14	13	15	...	11
b0	0	16384	16384	16384	...	20480
b1	0	16384	16384	16384	...	20480
Exp. b2	0	16384	16384	16384	...	20480
Exp. a1	0	16384	16384	16384	...	20480
Exp. a2	0	16384	16384	16384	...	20480
Exp. sfra2	15	14	13	15	...	11
Exp. sfrb0	15	14	13	15	...	11
Exp. sfrb1	15	14	13	15	...	11
Exp. sfrb2	15	14	13	15	...	11
Exp. sfra1	15	14	13	15	...	11
Exp. b0	0	16384	16384	16384	...	20480
Exp. b1	0	16384	16384	16384	...	20480

Test settings	
Tolerance b2	±0,0000e+00
Tolerance a1	±0,0000e+00
Tolerance a2	±0,0000e+00
Tolerance sfra2	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance sfrb2	±0,0000e+00
Tolerance sfra1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Filter block Biquad.

Test results						
Time step	1	2	3	4	...	8
Mask parameters						
b0	0	0.1	0.2	0.5	...	10
b1	0	0.1	0.2	0.5	...	10
b2	0	0.1	0.2	0.5	...	10
a0	0.1	0.1	0.1	1	...	1
a1	0	0.1	0.2	0.5	...	10
a2	0	0.1	0.2	0.5	...	10
ts_fact	1	1	1	1	...	1
Controller parameters						
b2	0	16384	16384	16384	...	20480
a1	0	16384	16384	16384	...	20480
a2	0	16384	16384	16384	...	20480
sfra2	15	14	13	15	...	11
sfrb0	15	14	13	15	...	11
sfrb1	15	14	13	15	...	11
sfrb2	15	14	13	15	...	11
sfra1	15	14	13	15	...	11
b0	0	16384	16384	16384	...	20480
b1	0	16384	16384	16384	...	20480
Exp. b2	0	16384	16384	16384	...	20480
Exp. a1	0	16384	16384	16384	...	20480
Exp. a2	0	16384	16384	16384	...	20480
Exp. sfra2	15	14	13	15	...	11
Exp. sfrb0	15	14	13	15	...	11
Exp. sfrb1	15	14	13	15	...	11
Exp. sfrb2	15	14	13	15	...	11
Exp. sfra1	15	14	13	15	...	11
Exp. b0	0	16384	16384	16384	...	20480
Exp. b1	0	16384	16384	16384	...	20480

Test settings	
Tolerance b2	±0,0000e+00
Tolerance a1	±0,0000e+00
Tolerance a2	±0,0000e+00
Tolerance sfra2	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance sfrb2	±0,0000e+00
Tolerance sfra1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test statistics	
Min CPU cycles	3765
Max CPU cycles	10429
Avg CPU cycles	7178

Verification: Biquad FiP16 CPU dsPIC33EP256MC502

Date of Test	2026-06-25
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for Filter block Biquad.

Test results						
Time step	1	2	3	4	...	73
CPU cycles	144	144	144	144	...	144
Inputs						
In (DSP)	-1842	-679	5729	7954	...	15256
In	-0.056	-0.021	0.175	0.243	...	0.466
Parameters						
b0	0.2					
b1	0.1					
b2	0.3					
a0	1.1					
a1	-0.7					
a2	0.8					
ts_fact	1					
Outputs						
Out	-0.01	-0.015	0.012	0.073	...	0.257
Exp. Out	-0.01	-0.015	0.012	0.073	...	0.257
Out (DSP)	-335	-505	399	2402	...	8434
Exp. Out (DSP)	-335	-504	401	2403	...	8434

Test settings	
Tolerance Out	±1,5259e-04 (±5 LSB)

Test statistics	
Min CPU cycles	144
Max CPU cycles	144
Avg CPU cycles	144

Test case: Conversion test OK

Conversion test for Filter block Biquad.

Test results						
Time step	1	2	3	4	...	8
Mask parameters						
b0	0	0.1	0.2	0.5	...	10
b1	0	0.1	0.2	0.5	...	10
b2	0	0.1	0.2	0.5	...	10
a0	0.1	0.1	0.1	1	...	1
a1	0	0.1	0.2	0.5	...	10
a2	0	0.1	0.2	0.5	...	10
ts_fact	1	1	1	1	...	1
Controller parameters						
b2	0	16384	16384	16384	...	20480
a1	0	16384	16384	16384	...	20480
a2	0	16384	16384	16384	...	20480
sfra2	15	14	13	15	...	11
sfrb0	15	14	13	15	...	11
sfrb1	15	14	13	15	...	11
sfrb2	15	14	13	15	...	11
sfra1	15	14	13	15	...	11
b0	0	16384	16384	16384	...	20480
b1	0	16384	16384	16384	...	20480
Exp. b2	0	16384	16384	16384	...	20480
Exp. a1	0	16384	16384	16384	...	20480
Exp. a2	0	16384	16384	16384	...	20480
Exp. sfra2	15	14	13	15	...	11
Exp. sfrb0	15	14	13	15	...	11
Exp. sfrb1	15	14	13	15	...	11
Exp. sfrb2	15	14	13	15	...	11
Exp. sfra1	15	14	13	15	...	11
Exp. b0	0	16384	16384	16384	...	20480
Exp. b1	0	16384	16384	16384	...	20480

Test settings	
Tolerance b2	±0,0000e+00
Tolerance a1	±0,0000e+00
Tolerance a2	±0,0000e+00
Tolerance sfra2	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance sfrb2	±0,0000e+00
Tolerance sfra1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Filter block Biquad.

Test results						
Time step	1	2	3	4	...	8
Mask parameters						
b0	0	0.1	0.2	0.5	...	10
b1	0	0.1	0.2	0.5	...	10
b2	0	0.1	0.2	0.5	...	10
a0	0.1	0.1	0.1	1	...	1
a1	0	0.1	0.2	0.5	...	10
a2	0	0.1	0.2	0.5	...	10
ts_fact	1	1	1	1	...	1
Controller parameters						
b2	0	16384	16384	16384	...	20480
a1	0	16384	16384	16384	...	20480
a2	0	16384	16384	16384	...	20480
sfra2	15	14	13	15	...	11
sfrb0	15	14	13	15	...	11
sfrb1	15	14	13	15	...	11
sfrb2	15	14	13	15	...	11
sfra1	15	14	13	15	...	11
b0	0	16384	16384	16384	...	20480
b1	0	16384	16384	16384	...	20480
Exp. b2	0	16384	16384	16384	...	20480
Exp. a1	0	16384	16384	16384	...	20480
Exp. a2	0	16384	16384	16384	...	20480
Exp. sfra2	15	14	13	15	...	11
Exp. sfrb0	15	14	13	15	...	11
Exp. sfrb1	15	14	13	15	...	11
Exp. sfrb2	15	14	13	15	...	11
Exp. sfra1	15	14	13	15	...	11
Exp. b0	0	16384	16384	16384	...	20480
Exp. b1	0	16384	16384	16384	...	20480

Test settings	
Tolerance b2	±0,0000e+00
Tolerance a1	±0,0000e+00
Tolerance a2	±0,0000e+00
Tolerance sfra2	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance sfrb2	±0,0000e+00
Tolerance sfra1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test statistics	
Min CPU cycles	13829
Max CPU cycles	59790
Avg CPU cycles	37812

Verification: Biquad FiP16 CPU XMC4800-F144K2048

Date of Test	2026-06-25
Target controller	XMC4800-F144K2048

Test case: Inport test

OK

Inport test for Filter block Biquad.

Test results						
Time step	1	2	3	4	...	73
CPU cycles	153	127	127	127	...	127
Inputs						
In (DSP)	-1842	-679	5729	7954	...	15256
In	-0.056	-0.021	0.175	0.243	...	0.466
Parameters						
b0	0.2					
b1	0.1					
b2	0.3					
a0	1.1					
a1	-0.7					
a2	0.8					
ts_fact	1					
Outputs						
Out	-0.01	-0.015	0.012	0.073	...	0.257
Exp. Out	-0.01	-0.015	0.012	0.073	...	0.257
Out (DSP)	-335	-505	399	2402	...	8434
Exp. Out (DSP)	-335	-504	401	2403	...	8434

Test settings	
Tolerance Out	±1,5259e-04 (±5 LSB)

Test statistics	
Min CPU cycles	127
Max CPU cycles	153
Avg CPU cycles	127

Test case: Conversion test

OK

Conversion test for Filter block Biquad.

Test results						
Time step	1	2	3	4	...	8
Mask parameters						
b0	0	0.1	0.2	0.5	...	10
b1	0	0.1	0.2	0.5	...	10
b2	0	0.1	0.2	0.5	...	10
a0	0.1	0.1	0.1	1	...	1
a1	0	0.1	0.2	0.5	...	10
a2	0	0.1	0.2	0.5	...	10
ts_fact	1	1	1	1	...	1
Controller parameters						
b2	0	16384	16384	16384	...	20480
a1	0	16384	16384	16384	...	20480
a2	0	16384	16384	16384	...	20480
sfra2	15	14	13	15	...	11
sfrb0	15	14	13	15	...	11
sfrb1	15	14	13	15	...	11
sfrb2	15	14	13	15	...	11
sfra1	15	14	13	15	...	11
b0	0	16384	16384	16384	...	20480
b1	0	16384	16384	16384	...	20480
Exp. b2	0	16384	16384	16384	...	20480
Exp. a1	0	16384	16384	16384	...	20480
Exp. a2	0	16384	16384	16384	...	20480
Exp. sfra2	15	14	13	15	...	11
Exp. sfrb0	15	14	13	15	...	11
Exp. sfrb1	15	14	13	15	...	11
Exp. sfrb2	15	14	13	15	...	11
Exp. sfra1	15	14	13	15	...	11
Exp. b0	0	16384	16384	16384	...	20480
Exp. b1	0	16384	16384	16384	...	20480

Test settings	
Tolerance b2	±0,0000e+00
Tolerance a1	±0,0000e+00
Tolerance a2	±0,0000e+00
Tolerance sfra2	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance sfrb2	±0,0000e+00
Tolerance sfra1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Filter block Biquad.

Test results						
Time step	1	2	3	4	...	8
Mask parameters						
b0	0	0.1	0.2	0.5	...	10
b1	0	0.1	0.2	0.5	...	10
b2	0	0.1	0.2	0.5	...	10
a0	0.1	0.1	0.1	1	...	1
a1	0	0.1	0.2	0.5	...	10
a2	0	0.1	0.2	0.5	...	10
ts_fact	1	1	1	1	...	1
Controller parameters						
b2	0	16384	16384	16384	...	20480
a1	0	16384	16384	16384	...	20480
a2	0	16384	16384	16384	...	20480
sfra2	15	14	13	15	...	11
sfrb0	15	14	13	15	...	11
sfrb1	15	14	13	15	...	11
sfrb2	15	14	13	15	...	11
sfra1	15	14	13	15	...	11
b0	0	16384	16384	16384	...	20480
b1	0	16384	16384	16384	...	20480
Exp. b2	0	16384	16384	16384	...	20480
Exp. a1	0	16384	16384	16384	...	20480
Exp. a2	0	16384	16384	16384	...	20480
Exp. sfra2	15	14	13	15	...	11
Exp. sfrb0	15	14	13	15	...	11
Exp. sfrb1	15	14	13	15	...	11
Exp. sfrb2	15	14	13	15	...	11
Exp. sfra1	15	14	13	15	...	11
Exp. b0	0	16384	16384	16384	...	20480
Exp. b1	0	16384	16384	16384	...	20480

Test settings	
Tolerance b2	±0,0000e+00
Tolerance a1	±0,0000e+00
Tolerance a2	±0,0000e+00
Tolerance sfra2	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance sfrb2	±0,0000e+00
Tolerance sfra1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test statistics	
Min CPU cycles	2662
Max CPU cycles	6839
Avg CPU cycles	4414

Verification: Biquad FiP16 CPU TMS320F28379D

Date of Test	2026-06-25
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for Filter block Biquad.

Test results						
Time step	1	2	3	4	...	73
CPU cycles	111	111	111	111	...	111
Inputs						
In (DSP)	-1842	-679	5729	7954	...	15256
In	-0.056	-0.021	0.175	0.243	...	0.466
Parameters						
b0	0.2					
b1	0.1					
b2	0.3					
a0	1.1					
a1	-0.7					
a2	0.8					
ts_fact	1					
Outputs						
Out	-0.01	-0.015	0.012	0.073	...	0.257
Exp. Out	-0.01	-0.015	0.012	0.073	...	0.257
Out (DSP)	-335	-505	399	2402	...	8434
Exp. Out (DSP)	-335	-504	401	2403	...	8434

Test settings	
Tolerance Out	±1,5259e-04 (±5 LSB)

Test statistics	
Min CPU cycles	111
Max CPU cycles	111
Avg CPU cycles	111

Test case: Conversion test OK

Conversion test for Filter block Biquad.

Test results						
Time step	1	2	3	4	...	8
Mask parameters						
b0	0	0.1	0.2	0.5	...	10
b1	0	0.1	0.2	0.5	...	10
b2	0	0.1	0.2	0.5	...	10
a0	0.1	0.1	0.1	1	...	1
a1	0	0.1	0.2	0.5	...	10
a2	0	0.1	0.2	0.5	...	10
ts_fact	1	1	1	1	...	1
Controller parameters						
b2	0	16384	16384	16384	...	20480
a1	0	16384	16384	16384	...	20480
a2	0	16384	16384	16384	...	20480
sfra2	15	14	13	15	...	11
sfrb0	15	14	13	15	...	11
sfrb1	15	14	13	15	...	11
sfrb2	15	14	13	15	...	11
sfra1	15	14	13	15	...	11
b0	0	16384	16384	16384	...	20480
b1	0	16384	16384	16384	...	20480
Exp. b2	0	16384	16384	16384	...	20480
Exp. a1	0	16384	16384	16384	...	20480
Exp. a2	0	16384	16384	16384	...	20480
Exp. sfra2	15	14	13	15	...	11
Exp. sfrb0	15	14	13	15	...	11
Exp. sfrb1	15	14	13	15	...	11
Exp. sfrb2	15	14	13	15	...	11
Exp. sfra1	15	14	13	15	...	11
Exp. b0	0	16384	16384	16384	...	20480
Exp. b1	0	16384	16384	16384	...	20480

Test settings	
Tolerance b2	±0,0000e+00
Tolerance a1	±0,0000e+00
Tolerance a2	±0,0000e+00
Tolerance sfra2	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance sfrb2	±0,0000e+00
Tolerance sfra1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Filter block Biquad.

Test results						
Time step	1	2	3	4	...	8
Mask parameters						
b0	0	0.1	0.2	0.5	...	10
b1	0	0.1	0.2	0.5	...	10
b2	0	0.1	0.2	0.5	...	10
a0	0.1	0.1	0.1	1	...	1
a1	0	0.1	0.2	0.5	...	10
a2	0	0.1	0.2	0.5	...	10
ts_fact	1	1	1	1	...	1
Controller parameters						
b2	0	16384	16384	16384	...	20480
a1	0	16384	16384	16384	...	20480
a2	0	16384	16384	16384	...	20480
sfra2	15	14	13	15	...	11
sfrb0	15	14	13	15	...	11
sfrb1	15	14	13	15	...	11
sfrb2	15	14	13	15	...	11
sfra1	15	14	13	15	...	11
b0	0	16384	16384	16384	...	20480
b1	0	16384	16384	16384	...	20480
Exp. b2	0	16384	16384	16384	...	20480
Exp. a1	0	16384	16384	16384	...	20480
Exp. a2	0	16384	16384	16384	...	20480
Exp. sfra2	15	14	13	15	...	11
Exp. sfrb0	15	14	13	15	...	11
Exp. sfrb1	15	14	13	15	...	11
Exp. sfrb2	15	14	13	15	...	11
Exp. sfra1	15	14	13	15	...	11
Exp. b0	0	16384	16384	16384	...	20480
Exp. b1	0	16384	16384	16384	...	20480

Test settings	
Tolerance b2	±0,0000e+00
Tolerance a1	±0,0000e+00
Tolerance a2	±0,0000e+00
Tolerance sfra2	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance sfrb2	±0,0000e+00
Tolerance sfra1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test statistics	
Min CPU cycles	4877
Max CPU cycles	22097
Avg CPU cycles	12191

Verification: Biquad FiP32 CPU TMS320F28335

Date of Test	2026-06-25
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for Filter block Biquad.

Test results				
Time step	1	2	...	73
CPU cycles	266	266	...	266
Inputs				
In (DSP)	-120706110	-44469415	...	999834674
In	-0.056	-0.021	...	0.466
Parameters				
b0	0.2			
b1	0.1			
b2	0.3			
a0	1.1			
a1	-0.7			
a2	0.8			
ts_fact	1			
Outputs				
Out	-0.01	-0.015	...	0.257
Exp. Out	-0.01	-0.015	...	0.257
Out (DSP)	-21946566	-33024628	...	552726178
Exp. Out (DSP)	-21946566	-33024627	...	552726179

Test settings	
Tolerance Out	±2,3283e-09 (±5 LSB)

Test statistics	
Min CPU cycles	266
Max CPU cycles	266
Avg CPU cycles	266

Test case: Conversion test OK

Conversion test for Filter block Biquad.

Test results				
Time step	1	2	...	8
Mask parameters				
b0	0	0.1	...	10
b1	0	0.1	...	10
b2	0	0.1	...	10
a0	0.1	0.1	...	1
a1	0	0.1	...	10
a2	0	0.1	...	10
ts_fact	1	1	...	1
Controller parameters				
b2	0	1073741824	...	1342177280
a1	0	1073741824	...	1342177280
a2	0	1073741824	...	1342177280
sfra2	31	30	...	27
sfrb0	31	30	...	27
sfrb1	31	30	...	27
sfrb2	31	30	...	27
sfra1	31	30	...	27
b0	0	1073741824	...	1342177280
b1	0	1073741824	...	1342177280
Exp. b2	0	1073741824	...	1342177280
Exp. a1	0	1073741824	...	1342177280
Exp. a2	0	1073741824	...	1342177280
Exp. sfra2	31	30	...	27
Exp. sfrb0	31	30	...	27
Exp. sfrb1	31	30	...	27
Exp. sfrb2	31	30	...	27
Exp. sfra1	31	30	...	27
Exp. b0	0	1073741824	...	1342177280
Exp. b1	0	1073741824	...	1342177280

Test settings	
Tolerance b2	±0,0000e+00
Tolerance a1	±0,0000e+00
Tolerance a2	±0,0000e+00
Tolerance sfra2	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance sfrb2	±0,0000e+00
Tolerance sfra1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Filter block Biquad.

Test results				
Time step	1	2	...	8
Mask parameters				
b0	0	0.1	...	10
b1	0	0.1	...	10
b2	0	0.1	...	10
a0	0.1	0.1	...	1
a1	0	0.1	...	10
a2	0	0.1	...	10
ts_fact	1	1	...	1
Controller parameters				
b2	0	1073741824	...	1342177280
a1	0	1073741824	...	1342177280
a2	0	1073741824	...	1342177280
sfra2	31	30	...	27
sfrb0	31	30	...	27
sfrb1	31	30	...	27
sfrb2	31	30	...	27
sfra1	31	30	...	27
b0	0	1073741824	...	1342177280
b1	0	1073741824	...	1342177280
Exp. b2	0	1073741824	...	1342177280
Exp. a1	0	1073741824	...	1342177280
Exp. a2	0	1073741824	...	1342177280
Exp. sfra2	31	30	...	27
Exp. sfrb0	31	30	...	27
Exp. sfrb1	31	30	...	27
Exp. sfrb2	31	30	...	27
Exp. sfra1	31	30	...	27
Exp. b0	0	1073741824	...	1342177280
Exp. b1	0	1073741824	...	1342177280

Test settings	
Tolerance b2	±0,0000e+00
Tolerance a1	±0,0000e+00
Tolerance a2	±0,0000e+00
Tolerance sfra2	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance sfrb2	±0,0000e+00
Tolerance sfra1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test statistics	
Min CPU cycles	7639
Max CPU cycles	31129
Avg CPU cycles	17599

Verification: Biquad FiP32 CPU TM4C123GH6

Date of Test	2026-06-25
Target controller	TM4C123GH6

Test case: Inport test — OK

Inport test for Filter block Biquad.

Test results				
Time step	1	2	...	73
CPU cycles	243	243	...	243
Inputs				
In (DSP)	-120706110	-44469415	...	999834674
In	-0.056	-0.021	...	0.466
Parameters				
b0	0.2			
b1	0.1			
b2	0.3			
a0	1.1			
a1	-0.7			
a2	0.8			
ts_fact	1			
Outputs				
Out	-0.01	-0.015	...	0.257
Exp. Out	-0.01	-0.015	...	0.257
Out (DSP)	-21946566	-33024628	...	552726178
Exp. Out (DSP)	-21946566	-33024627	...	552726179

Test settings	
Tolerance Out	±2,3283e-09 (±5 LSB)

Test statistics	
Min CPU cycles	243
Max CPU cycles	243
Avg CPU cycles	243

Test case: Conversion test — OK

Conversion test for Filter block Biquad.

Test results				
Time step	1	2	...	8
Mask parameters				
b0	0	0.1	...	10
b1	0	0.1	...	10
b2	0	0.1	...	10
a0	0.1	0.1	...	1
a1	0	0.1	...	10
a2	0	0.1	...	10
ts_fact	1	1	...	1
Controller parameters				
b2	0	1073741824	...	1342177280
a1	0	1073741824	...	1342177280
a2	0	1073741824	...	1342177280
sfra2	31	30	...	27
sfrb0	31	30	...	27
sfrb1	31	30	...	27
sfrb2	31	30	...	27
sfra1	31	30	...	27
b0	0	1073741824	...	1342177280
b1	0	1073741824	...	1342177280
Exp. b2	0	1073741824	...	1342177280
Exp. a1	0	1073741824	...	1342177280
Exp. a2	0	1073741824	...	1342177280
Exp. sfra2	31	30	...	27
Exp. sfrb0	31	30	...	27
Exp. sfrb1	31	30	...	27
Exp. sfrb2	31	30	...	27
Exp. sfra1	31	30	...	27
Exp. b0	0	1073741824	...	1342177280
Exp. b1	0	1073741824	...	1342177280

Test settings	
Tolerance b2	±0,0000e+00
Tolerance a1	±0,0000e+00
Tolerance a2	±0,0000e+00
Tolerance sfra2	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance sfrb2	±0,0000e+00
Tolerance sfra1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Filter block Biquad.

Test results				
Time step	1	2	...	8
Mask parameters				
b0	0	0.1	...	10
b1	0	0.1	...	10
b2	0	0.1	...	10
a0	0.1	0.1	...	1
a1	0	0.1	...	10
a2	0	0.1	...	10
ts_fact	1	1	...	1
Controller parameters				
b2	0	1073741824	...	1342177280
a1	0	1073741824	...	1342177280
a2	0	1073741824	...	1342177280
sfra2	31	30	...	27
sfrb0	31	30	...	27
sfrb1	31	30	...	27
sfrb2	31	30	...	27
sfra1	31	30	...	27
b0	0	1073741824	...	1342177280
b1	0	1073741824	...	1342177280
Exp. b2	0	1073741824	...	1342177280
Exp. a1	0	1073741824	...	1342177280
Exp. a2	0	1073741824	...	1342177280
Exp. sfra2	31	30	...	27
Exp. sfrb0	31	30	...	27
Exp. sfrb1	31	30	...	27
Exp. sfrb2	31	30	...	27
Exp. sfra1	31	30	...	27
Exp. b0	0	1073741824	...	1342177280
Exp. b1	0	1073741824	...	1342177280

Test settings	
Tolerance b2	±0,0000e+00
Tolerance a1	±0,0000e+00
Tolerance a2	±0,0000e+00
Tolerance sfra2	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance sfrb2	±0,0000e+00
Tolerance sfra1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test statistics	
Min CPU cycles	3217
Max CPU cycles	12887
Avg CPU cycles	7338

Verification: Biquad FiP32 CPU STM32G474RE

Date of Test	2026-06-25
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for Filter block Biquad.

Test results				
Time step	1	2	...	73
CPU cycles	235	235	...	235
Inputs				
In (DSP)	-120706110	-44469415	...	999834674
In	-0.056	-0.021	...	0.466
Parameters				
b0	0.2			
b1	0.1			
b2	0.3			
a0	1.1			
a1	-0.7			
a2	0.8			
ts_fact	1			
Outputs				
Out	-0.01	-0.015	...	0.257
Exp. Out	-0.01	-0.015	...	0.257
Out (DSP)	-21946566	-33024628	...	552726178
Exp. Out (DSP)	-21946566	-33024627	...	552726179

Test settings	
Tolerance Out	±2,3283e-09 (±5 LSB)

Test statistics	
Min CPU cycles	235
Max CPU cycles	299
Avg CPU cycles	235

Test case: Conversion test OK

Conversion test for Filter block Biquad.

Test results				
Time step	1	2	...	8
Mask parameters				
b0	0	0.1	...	10
b1	0	0.1	...	10
b2	0	0.1	...	10
a0	0.1	0.1	...	1
a1	0	0.1	...	10
a2	0	0.1	...	10
ts_fact	1	1	...	1
Controller parameters				
b2	0	1073741824	...	1342177280
a1	0	1073741824	...	1342177280
a2	0	1073741824	...	1342177280
sfra2	31	30	...	27
sfrb0	31	30	...	27
sfrb1	31	30	...	27
sfrb2	31	30	...	27
sfra1	31	30	...	27
b0	0	1073741824	...	1342177280
b1	0	1073741824	...	1342177280
Exp. b2	0	1073741824	...	1342177280
Exp. a1	0	1073741824	...	1342177280
Exp. a2	0	1073741824	...	1342177280
Exp. sfra2	31	30	...	27
Exp. sfrb0	31	30	...	27
Exp. sfrb1	31	30	...	27
Exp. sfrb2	31	30	...	27
Exp. sfra1	31	30	...	27
Exp. b0	0	1073741824	...	1342177280
Exp. b1	0	1073741824	...	1342177280

Test settings	
Tolerance b2	±0,0000e+00
Tolerance a1	±0,0000e+00
Tolerance a2	±0,0000e+00
Tolerance sfra2	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance sfrb2	±0,0000e+00
Tolerance sfra1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Filter block Biquad.

Test results				
Time step	1	2	...	8
Mask parameters				
b0	0	0.1	...	10
b1	0	0.1	...	10
b2	0	0.1	...	10
a0	0.1	0.1	...	1
a1	0	0.1	...	10
a2	0	0.1	...	10
ts_fact	1	1	...	1
Controller parameters				
b2	0	1073741824	...	1342177280
a1	0	1073741824	...	1342177280
a2	0	1073741824	...	1342177280
sfra2	31	30	...	27
sfrb0	31	30	...	27
sfrb1	31	30	...	27
sfrb2	31	30	...	27
sfra1	31	30	...	27
b0	0	1073741824	...	1342177280
b1	0	1073741824	...	1342177280
Exp. b2	0	1073741824	...	1342177280
Exp. a1	0	1073741824	...	1342177280
Exp. a2	0	1073741824	...	1342177280
Exp. sfra2	31	30	...	27
Exp. sfrb0	31	30	...	27
Exp. sfrb1	31	30	...	27
Exp. sfrb2	31	30	...	27
Exp. sfra1	31	30	...	27
Exp. b0	0	1073741824	...	1342177280
Exp. b1	0	1073741824	...	1342177280

Test settings	
Tolerance b2	±0,0000e+00
Tolerance a1	±0,0000e+00
Tolerance a2	±0,0000e+00
Tolerance sfra2	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance sfrb2	±0,0000e+00
Tolerance sfra1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test statistics	
Min CPU cycles	4225
Max CPU cycles	8478
Avg CPU cycles	6000

Verification: Biquad FiP32 CPU STM32F072RB

Date of Test	2026-06-25
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for Filter block Biquad.

Test results				
Time step	1	2	...	73
CPU cycles	699	637	...	633
Inputs				
In (DSP)	-120706110	-44469415	...	999834674
In	-0.056	-0.021	...	0.466
Parameters				
b0	0.2			
b1	0.1			
b2	0.3			
a0	1.1			
a1	-0.7			
a2	0.8			
ts_fact	1			
Outputs				
Out	-0.01	-0.015	...	0.257
Exp. Out	-0.01	-0.015	...	0.257
Out (DSP)	-21946566	-33024628	...	552726178
Exp. Out (DSP)	-21946566	-33024627	...	552726179

Test settings	
Tolerance Out	±2,3283e-09 (±5 LSB)

Test statistics	
Min CPU cycles	633
Max CPU cycles	699
Avg CPU cycles	636

Test case: Conversion test OK

Conversion test for Filter block Biquad.

Test results				
Time step	1	2	...	8
Mask parameters				
b0	0	0.1	...	10
b1	0	0.1	...	10
b2	0	0.1	...	10
a0	0.1	0.1	...	1
a1	0	0.1	...	10
a2	0	0.1	...	10
ts_fact	1	1	...	1
Controller parameters				
b2	0	1073741824	...	1342177280
a1	0	1073741824	...	1342177280
a2	0	1073741824	...	1342177280
sfra2	31	30	...	27
sfrb0	31	30	...	27
sfrb1	31	30	...	27
sfrb2	31	30	...	27
sfra1	31	30	...	27
b0	0	1073741824	...	1342177280
b1	0	1073741824	...	1342177280
Exp. b2	0	1073741824	...	1342177280
Exp. a1	0	1073741824	...	1342177280
Exp. a2	0	1073741824	...	1342177280
Exp. sfra2	31	30	...	27
Exp. sfrb0	31	30	...	27
Exp. sfrb1	31	30	...	27
Exp. sfrb2	31	30	...	27
Exp. sfra1	31	30	...	27
Exp. b0	0	1073741824	...	1342177280
Exp. b1	0	1073741824	...	1342177280

Test settings	
Tolerance b2	±0,0000e+00
Tolerance a1	±0,0000e+00
Tolerance a2	±0,0000e+00
Tolerance sfra2	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance sfrb2	±0,0000e+00
Tolerance sfra1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Filter block Biquad.

Test results				
Time step	1	2	...	8
Mask parameters				
b0	0	0.1	...	10
b1	0	0.1	...	10
b2	0	0.1	...	10
a0	0.1	0.1	...	1
a1	0	0.1	...	10
a2	0	0.1	...	10
ts_fact	1	1	...	1
Controller parameters				
b2	0	1073741824	...	1342177280
a1	0	1073741824	...	1342177280
a2	0	1073741824	...	1342177280
sfra2	31	30	...	27
sfrb0	31	30	...	27
sfrb1	31	30	...	27
sfrb2	31	30	...	27
sfra1	31	30	...	27
b0	0	1073741824	...	1342177280
b1	0	1073741824	...	1342177280
Exp. b2	0	1073741824	...	1342177280
Exp. a1	0	1073741824	...	1342177280
Exp. a2	0	1073741824	...	1342177280
Exp. sfra2	31	30	...	27
Exp. sfrb0	31	30	...	27
Exp. sfrb1	31	30	...	27
Exp. sfrb2	31	30	...	27
Exp. sfra1	31	30	...	27
Exp. b0	0	1073741824	...	1342177280
Exp. b1	0	1073741824	...	1342177280

Test settings	
Tolerance b2	±0,0000e+00
Tolerance a1	±0,0000e+00
Tolerance a2	±0,0000e+00
Tolerance sfra2	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance sfrb2	±0,0000e+00
Tolerance sfra1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test statistics	
Min CPU cycles	13455
Max CPU cycles	31085
Avg CPU cycles	23389

Verification: Biquad FiP32 CPU PIC32MX170F256

Date of Test	2026-06-25
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for Filter block Biquad.

Test results				
Time step	1	2	...	73
CPU cycles	208	208	...	208
Inputs				
In (DSP)	-120706110	-44469415	...	999834674
In	-0.056	-0.021	...	0.466
Parameters				
b0	0.2			
b1	0.1			
b2	0.3			
a0	1.1			
a1	-0.7			
a2	0.8			
ts_fact	1			
Outputs				
Out	-0.01	-0.015	...	0.257
Exp. Out	-0.01	-0.015	...	0.257
Out (DSP)	-21946566	-33024628	...	552726178
Exp. Out (DSP)	-21946566	-33024627	...	552726179

Test settings	
Tolerance Out	±2,3283e-09 (±5 LSB)

Test statistics	
Min CPU cycles	208
Max CPU cycles	208
Avg CPU cycles	208

Test case: Conversion test OK

Conversion test for Filter block Biquad.

Test results				
Time step	1	2	...	8
Mask parameters				
b0	0	0.1	...	10
b1	0	0.1	...	10
b2	0	0.1	...	10
a0	0.1	0.1	...	1
a1	0	0.1	...	10
a2	0	0.1	...	10
ts_fact	1	1	...	1
Controller parameters				
b2	0	1073741824	...	1342177280
a1	0	1073741824	...	1342177280
a2	0	1073741824	...	1342177280
sfra2	31	30	...	27
sfrb0	31	30	...	27
sfrb1	31	30	...	27
sfrb2	31	30	...	27
sfra1	31	30	...	27
b0	0	1073741824	...	1342177280
b1	0	1073741824	...	1342177280
Exp. b2	0	1073741824	...	1342177280
Exp. a1	0	1073741824	...	1342177280
Exp. a2	0	1073741824	...	1342177280
Exp. sfra2	31	30	...	27
Exp. sfrb0	31	30	...	27
Exp. sfrb1	31	30	...	27
Exp. sfrb2	31	30	...	27
Exp. sfra1	31	30	...	27
Exp. b0	0	1073741824	...	1342177280
Exp. b1	0	1073741824	...	1342177280

Test settings	
Tolerance b2	±0,0000e+00
Tolerance a1	±0,0000e+00
Tolerance a2	±0,0000e+00
Tolerance sfra2	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance sfrb2	±0,0000e+00
Tolerance sfra1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Filter block Biquad.

Test results				
Time step	1	2	...	8
Mask parameters				
b0	0	0.1	...	10
b1	0	0.1	...	10
b2	0	0.1	...	10
a0	0.1	0.1	...	1
a1	0	0.1	...	10
a2	0	0.1	...	10
ts_fact	1	1	...	1
Controller parameters				
b2	0	1073741824	...	1342177280
a1	0	1073741824	...	1342177280
a2	0	1073741824	...	1342177280
sfra2	31	30	...	27
sfrb0	31	30	...	27
sfrb1	31	30	...	27
sfrb2	31	30	...	27
sfra1	31	30	...	27
b0	0	1073741824	...	1342177280
b1	0	1073741824	...	1342177280
Exp. b2	0	1073741824	...	1342177280
Exp. a1	0	1073741824	...	1342177280
Exp. a2	0	1073741824	...	1342177280
Exp. sfra2	31	30	...	27
Exp. sfrb0	31	30	...	27
Exp. sfrb1	31	30	...	27
Exp. sfrb2	31	30	...	27
Exp. sfra1	31	30	...	27
Exp. b0	0	1073741824	...	1342177280
Exp. b1	0	1073741824	...	1342177280

Test settings	
Tolerance b2	±0,0000e+00
Tolerance a1	±0,0000e+00
Tolerance a2	±0,0000e+00
Tolerance sfra2	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance sfrb2	±0,0000e+00
Tolerance sfra1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test statistics	
Min CPU cycles	6035
Max CPU cycles	12729
Avg CPU cycles	9517

Verification: Biquad FiP32 CPU dsPIC33EP256MC502

Date of Test	2026-06-25
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for Filter block Biquad.

Test results				
Time step	1	2	...	73
CPU cycles	2239	2247	...	2232
Inputs				
In (DSP)	-120706110	-44469415	...	999834674
In	-0.056	-0.021	...	0.466
Parameters				
b0	0.2			
b1	0.1			
b2	0.3			
a0	1.1			
a1	-0.7			
a2	0.8			
ts_fact	1			
Outputs				
Out	-0.01	-0.015	...	0.257
Exp. Out	-0.01	-0.015	...	0.257
Out (DSP)	-21946566	-33024628	...	552726178
Exp. Out (DSP)	-21946566	-33024627	...	552726179

Test settings	
Tolerance Out	±2,3283e-09 (±5 LSB)

Test statistics	
Min CPU cycles	2232
Max CPU cycles	2261
Avg CPU cycles	2245

Test case: Conversion test OK

Conversion test for Filter block Biquad.

Test results				
Time step	1	2	...	8
Mask parameters				
b0	0	0.1	...	10
b1	0	0.1	...	10
b2	0	0.1	...	10
a0	0.1	0.1	...	1
a1	0	0.1	...	10
a2	0	0.1	...	10
ts_fact	1	1	...	1
Controller parameters				
b2	0	1073741824	...	1342177280
a1	0	1073741824	...	1342177280
a2	0	1073741824	...	1342177280
sfra2	31	30	...	27
sfrb0	31	30	...	27
sfrb1	31	30	...	27
sfrb2	31	30	...	27
sfra1	31	30	...	27
b0	0	1073741824	...	1342177280
b1	0	1073741824	...	1342177280
Exp. b2	0	1073741824	...	1342177280
Exp. a1	0	1073741824	...	1342177280
Exp. a2	0	1073741824	...	1342177280
Exp. sfra2	31	30	...	27
Exp. sfrb0	31	30	...	27
Exp. sfrb1	31	30	...	27
Exp. sfrb2	31	30	...	27
Exp. sfra1	31	30	...	27
Exp. b0	0	1073741824	...	1342177280
Exp. b1	0	1073741824	...	1342177280

Test settings	
Tolerance b2	±0,0000e+00
Tolerance a1	±0,0000e+00
Tolerance a2	±0,0000e+00
Tolerance sfra2	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance sfrb2	±0,0000e+00
Tolerance sfra1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Filter block Biquad.

Test results				
Time step	1	2	...	8
Mask parameters				
b0	0	0.1	...	10
b1	0	0.1	...	10
b2	0	0.1	...	10
a0	0.1	0.1	...	1
a1	0	0.1	...	10
a2	0	0.1	...	10
ts_fact	1	1	...	1
Controller parameters				
b2	0	1073741824	...	1342177280
a1	0	1073741824	...	1342177280
a2	0	1073741824	...	1342177280
sfra2	31	30	...	27
sfrb0	31	30	...	27
sfrb1	31	30	...	27
sfrb2	31	30	...	27
sfra1	31	30	...	27
b0	0	1073741824	...	1342177280
b1	0	1073741824	...	1342177280
Exp. b2	0	1073741824	...	1342177280
Exp. a1	0	1073741824	...	1342177280
Exp. a2	0	1073741824	...	1342177280
Exp. sfra2	31	30	...	27
Exp. sfrb0	31	30	...	27
Exp. sfrb1	31	30	...	27
Exp. sfrb2	31	30	...	27
Exp. sfra1	31	30	...	27
Exp. b0	0	1073741824	...	1342177280
Exp. b1	0	1073741824	...	1342177280

Test settings	
Tolerance b2	±0,0000e+00
Tolerance a1	±0,0000e+00
Tolerance a2	±0,0000e+00
Tolerance sfra2	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance sfrb2	±0,0000e+00
Tolerance sfra1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test statistics	
Min CPU cycles	15859
Max CPU cycles	60490
Avg CPU cycles	39307

Verification: Biquad FiP32 CPU XMC4800-F144K2048

Date of Test	2026-06-25
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for Filter block Biquad.

Test results				
Time step	1	2	...	73
CPU cycles	265	224	...	224
Inputs				
In (DSP)	-120706110	-44469415	...	999834674
In	-0.056	-0.021	...	0.466
Parameters				
b0	0.2			
b1	0.1			
b2	0.3			
a0	1.1			
a1	-0.7			
a2	0.8			
ts_fact	1			
Outputs				
Out	-0.01	-0.015	...	0.257
Exp. Out	-0.01	-0.015	...	0.257
Out (DSP)	-21946566	-33024628	...	552726178
Exp. Out (DSP)	-21946566	-33024627	...	552726179

Test settings	
Tolerance Out	±2,3283e-09 (±5 LSB)

Test statistics	
Min CPU cycles	224
Max CPU cycles	265
Avg CPU cycles	224

Test case: Conversion test OK

Conversion test for Filter block Biquad.

Test results				
Time step	1	2	...	8
Mask parameters				
b0	0	0.1	...	10
b1	0	0.1	...	10
b2	0	0.1	...	10
a0	0.1	0.1	...	1
a1	0	0.1	...	10
a2	0	0.1	...	10
ts_fact	1	1	...	1
Controller parameters				
b2	0	1073741824	...	1342177280
a1	0	1073741824	...	1342177280
a2	0	1073741824	...	1342177280
sfra2	31	30	...	27
sfrb0	31	30	...	27
sfrb1	31	30	...	27
sfrb2	31	30	...	27
sfra1	31	30	...	27
b0	0	1073741824	...	1342177280
b1	0	1073741824	...	1342177280
Exp. b2	0	1073741824	...	1342177280
Exp. a1	0	1073741824	...	1342177280
Exp. a2	0	1073741824	...	1342177280
Exp. sfra2	31	30	...	27
Exp. sfrb0	31	30	...	27
Exp. sfrb1	31	30	...	27
Exp. sfrb2	31	30	...	27
Exp. sfra1	31	30	...	27
Exp. b0	0	1073741824	...	1342177280
Exp. b1	0	1073741824	...	1342177280

Test settings	
Tolerance b2	±0,0000e+00
Tolerance a1	±0,0000e+00
Tolerance a2	±0,0000e+00
Tolerance sfra2	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance sfrb2	±0,0000e+00
Tolerance sfra1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Filter block Biquad.

Test results				
Time step	1	2	...	8
Mask parameters				
b0	0	0.1	...	10
b1	0	0.1	...	10
b2	0	0.1	...	10
a0	0.1	0.1	...	1
a1	0	0.1	...	10
a2	0	0.1	...	10
ts_fact	1	1	...	1
Controller parameters				
b2	0	1073741824	...	1342177280
a1	0	1073741824	...	1342177280
a2	0	1073741824	...	1342177280
sfra2	31	30	...	27
sfrb0	31	30	...	27
sfrb1	31	30	...	27
sfrb2	31	30	...	27
sfra1	31	30	...	27
b0	0	1073741824	...	1342177280
b1	0	1073741824	...	1342177280
Exp. b2	0	1073741824	...	1342177280
Exp. a1	0	1073741824	...	1342177280
Exp. a2	0	1073741824	...	1342177280
Exp. sfra2	31	30	...	27
Exp. sfrb0	31	30	...	27
Exp. sfrb1	31	30	...	27
Exp. sfrb2	31	30	...	27
Exp. sfra1	31	30	...	27
Exp. b0	0	1073741824	...	1342177280
Exp. b1	0	1073741824	...	1342177280

Test settings	
Tolerance b2	±0,0000e+00
Tolerance a1	±0,0000e+00
Tolerance a2	±0,0000e+00
Tolerance sfra2	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance sfrb2	±0,0000e+00
Tolerance sfra1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test statistics	
Min CPU cycles	3975
Max CPU cycles	8100
Avg CPU cycles	5727

Verification: Biquad FiP32 CPU TMS320F28379D

Date of Test	2026-06-25
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for Filter block Biquad.

Test results				
Time step	1	2	...	73
CPU cycles	247	247	...	247
Inputs				
In (DSP)	-120706110	-44469415	...	999834674
In	-0.056	-0.021	...	0.466
Parameters				
b0	0.2			
b1	0.1			
b2	0.3			
a0	1.1			
a1	-0.7			
a2	0.8			
ts_fact	1			
Outputs				
Out	-0.01	-0.015	...	0.257
Exp. Out	-0.01	-0.015	...	0.257
Out (DSP)	-21946566	-33024628	...	552726178
Exp. Out (DSP)	-21946566	-33024627	...	552726179

Test settings	
Tolerance Out	±2,3283e-09 (±5 LSB)

Test statistics	
Min CPU cycles	247
Max CPU cycles	247
Avg CPU cycles	247

Test case: Conversion test OK

Conversion test for Filter block Biquad.

Test results				
Time step	1	2	...	8
Mask parameters				
b0	0	0.1	...	10
b1	0	0.1	...	10
b2	0	0.1	...	10
a0	0.1	0.1	...	1
a1	0	0.1	...	10
a2	0	0.1	...	10
ts_fact	1	1	...	1
Controller parameters				
b2	0	1073741824	...	1342177280
a1	0	1073741824	...	1342177280
a2	0	1073741824	...	1342177280
sfra2	31	30	...	27
sfrb0	31	30	...	27
sfrb1	31	30	...	27
sfrb2	31	30	...	27
sfra1	31	30	...	27
b0	0	1073741824	...	1342177280
b1	0	1073741824	...	1342177280
Exp. b2	0	1073741824	...	1342177280
Exp. a1	0	1073741824	...	1342177280
Exp. a2	0	1073741824	...	1342177280
Exp. sfra2	31	30	...	27
Exp. sfrb0	31	30	...	27
Exp. sfrb1	31	30	...	27
Exp. sfrb2	31	30	...	27
Exp. sfra1	31	30	...	27
Exp. b0	0	1073741824	...	1342177280
Exp. b1	0	1073741824	...	1342177280

Test settings	
Tolerance b2	±0,0000e+00
Tolerance a1	±0,0000e+00
Tolerance a2	±0,0000e+00
Tolerance sfra2	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance sfrb2	±0,0000e+00
Tolerance sfra1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Filter block Biquad.

Test results				
Time step	1	2	...	8
Mask parameters				
b0	0	0.1	...	10
b1	0	0.1	...	10
b2	0	0.1	...	10
a0	0.1	0.1	...	1
a1	0	0.1	...	10
a2	0	0.1	...	10
ts_fact	1	1	...	1
Controller parameters				
b2	0	1073741824	...	1342177280
a1	0	1073741824	...	1342177280
a2	0	1073741824	...	1342177280
sfra2	31	30	...	27
sfrb0	31	30	...	27
sfrb1	31	30	...	27
sfrb2	31	30	...	27
sfra1	31	30	...	27
b0	0	1073741824	...	1342177280
b1	0	1073741824	...	1342177280
Exp. b2	0	1073741824	...	1342177280
Exp. a1	0	1073741824	...	1342177280
Exp. a2	0	1073741824	...	1342177280
Exp. sfra2	31	30	...	27
Exp. sfrb0	31	30	...	27
Exp. sfrb1	31	30	...	27
Exp. sfrb2	31	30	...	27
Exp. sfra1	31	30	...	27
Exp. b0	0	1073741824	...	1342177280
Exp. b1	0	1073741824	...	1342177280

Test settings	
Tolerance b2	±0,0000e+00
Tolerance a1	±0,0000e+00
Tolerance a2	±0,0000e+00
Tolerance sfra2	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance sfrb2	±0,0000e+00
Tolerance sfra1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test statistics	
Min CPU cycles	5424
Max CPU cycles	22844
Avg CPU cycles	12913

Verification: Biquad Float32 CPU TMS320F28335

Date of Test	2026-06-25
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for Filter block Biquad.

Test results				
Time step	1	2	...	73
CPU cycles	93	93	...	93
Inputs				
In (DSP)	-0.056	-0.021	...	0.466
In	-0.056	-0.021	...	0.466
Parameters				
b0	0.2			
b1	0.1			
b2	0.3			
a0	1.1			
a1	-0.7			
a2	0.8			
ts_fact	1			
Outputs				
Out	-0.01	-0.015	...	0.257
Exp. Out	-0.01	-0.015	...	0.257
Out (DSP)	-0.01	-0.015	...	0.257
Exp. Out (DSP)	-0.01	-0.015	...	0.257

Test settings	
Tolerance Out	±9,3132e-08 (±200 LSB)

Test statistics	
Min CPU cycles	93
Max CPU cycles	93
Avg CPU cycles	93

Test case: Conversion test OK

Conversion test for Filter block Biquad.

Test results				
Time step	1	2	...	8
Mask parameters				
b0	0	0.1	...	10
b1	0	0.1	...	10
b2	0	0.1	...	10
a0	0.1	0.1	...	1
a1	0	0.1	...	10
a2	0	0.1	...	10
ts_fact	1	1	...	1
Controller parameters				
b2	0	1	...	10
a1	0	1	...	10
a2	0	1	...	10
b0	0	1	...	10
b1	0	1	...	10
Exp. b2	0	1	...	10
Exp. a1	0	1	...	10
Exp. a2	0	1	...	10
Exp. b0	0	1	...	10
Exp. b1	0	1	...	10

Test settings	
Tolerance b2	±0,0000e+00
Tolerance a1	±0,0000e+00
Tolerance a2	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Filter block Biquad.

Test results				
Time step	1	2	...	8
Mask parameters				
b0	0	0.1	...	10
b1	0	0.1	...	10
b2	0	0.1	...	10
a0	0.1	0.1	...	1
a1	0	0.1	...	10
a2	0	0.1	...	10
ts_fact	1	1	...	1
Controller parameters				
b2	0	1	...	10
a1	0	1	...	10
a2	0	1	...	10
b0	0	1	...	10
b1	0	1	...	10
Exp. b2	0	1	...	10
Exp. a1	0	1	...	10
Exp. a2	0	1	...	10
Exp. b0	0	1	...	10
Exp. b1	0	1	...	10

Test settings	
Tolerance b2	±0,0000e+00
Tolerance a1	±0,0000e+00
Tolerance a2	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test statistics	
Min CPU cycles	3955
Max CPU cycles	21465
Avg CPU cycles	9005

Verification: Biquad Float32 CPU TM4C123GH6

Date of Test	2026-06-25
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for Filter block Biquad.

Test results				
Time step	1	2	...	73
CPU cycles	61	61	...	61
Inputs				
In (DSP)	-0.056	-0.021	...	0.466
In	-0.056	-0.021	...	0.466
Parameters				
b0	0.2			
b1	0.1			
b2	0.3			
a0	1.1			
a1	-0.7			
a2	0.8			
ts_fact	1			
Outputs				
Out	-0.01	-0.015	...	0.257
Exp. Out	-0.01	-0.015	...	0.257
Out (DSP)	-0.01	-0.015	...	0.257
Exp. Out (DSP)	-0.01	-0.015	...	0.257

Test settings	
Tolerance Out	±9,3132e-08 (±200 LSB)

Test statistics	
Min CPU cycles	61
Max CPU cycles	61
Avg CPU cycles	61

Test case: Conversion test OK

Conversion test for Filter block Biquad.

Test results				
Time step	1	2	...	8
Mask parameters				
b0	0	0.1	...	10
b1	0	0.1	...	10
b2	0	0.1	...	10
a0	0.1	0.1	...	1
a1	0	0.1	...	10
a2	0	0.1	...	10
ts_fact	1	1	...	1
Controller parameters				
b2	0	1	...	10
a1	0	1	...	10
a2	0	1	...	10
b0	0	1	...	10
b1	0	1	...	10
Exp. b2	0	1	...	10
Exp. a1	0	1	...	10
Exp. a2	0	1	...	10
Exp. b0	0	1	...	10
Exp. b1	0	1	...	10

Test settings	
Tolerance b2	±0,0000e+00
Tolerance a1	±0,0000e+00
Tolerance a2	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Filter block Biquad.

Test results				
Time step	1	2	...	8
Mask parameters				
b0	0	0.1	...	10
b1	0	0.1	...	10
b2	0	0.1	...	10
a0	0.1	0.1	...	1
a1	0	0.1	...	10
a2	0	0.1	...	10
ts_fact	1	1	...	1
Controller parameters				
b2	0	1	...	10
a1	0	1	...	10
a2	0	1	...	10
b0	0	1	...	10
b1	0	1	...	10
Exp. b2	0	1	...	10
Exp. a1	0	1	...	10
Exp. a2	0	1	...	10
Exp. b0	0	1	...	10
Exp. b1	0	1	...	10

Test settings	
Tolerance b2	±0,0000e+00
Tolerance a1	±0,0000e+00
Tolerance a2	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test statistics	
Min CPU cycles	1789
Max CPU cycles	9019
Avg CPU cycles	3874

Verification: Biquad Float32 CPU STM32G474RE

Date of Test	2026-06-25
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for Filter block Biquad.

Test results				
Time step	1	2	...	73
CPU cycles	103	103	...	103
Inputs				
In (DSP)	-0.056	-0.021	...	0.466
In	-0.056	-0.021	...	0.466
Parameters				
b0	0.2			
b1	0.1			
b2	0.3			
a0	1.1			
a1	-0.7			
a2	0.8			
ts_fact	1			
Outputs				
Out	-0.01	-0.015	...	0.257
Exp. Out	-0.01	-0.015	...	0.257
Out (DSP)	-0.01	-0.015	...	0.257
Exp. Out (DSP)	-0.01	-0.015	...	0.257

Test settings	
Tolerance Out	±9,3132e-08 (±200 LSB)

Test statistics	
Min CPU cycles	103
Max CPU cycles	103
Avg CPU cycles	103

Test case: Conversion test OK

Conversion test for Filter block Biquad.

Test results				
Time step	1	2	...	8
Mask parameters				
b0	0	0.1	...	10
b1	0	0.1	...	10
b2	0	0.1	...	10
a0	0.1	0.1	...	1
a1	0	0.1	...	10
a2	0	0.1	...	10
ts_fact	1	1	...	1
Controller parameters				
b2	0	1	...	10
a1	0	1	...	10
a2	0	1	...	10
b0	0	1	...	10
b1	0	1	...	10
Exp. b2	0	1	...	10
Exp. a1	0	1	...	10
Exp. a2	0	1	...	10
Exp. b0	0	1	...	10
Exp. b1	0	1	...	10

Test settings	
Tolerance b2	±0,0000e+00
Tolerance a1	±0,0000e+00
Tolerance a2	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Filter block Biquad.

Test results				
Time step	1	2	...	8
Mask parameters				
b0	0	0.1	...	10
b1	0	0.1	...	10
b2	0	0.1	...	10
a0	0.1	0.1	...	1
a1	0	0.1	...	10
a2	0	0.1	...	10
ts_fact	1	1	...	1
Controller parameters				
b2	0	1	...	10
a1	0	1	...	10
a2	0	1	...	10
b0	0	1	...	10
b1	0	1	...	10
Exp. b2	0	1	...	10
Exp. a1	0	1	...	10
Exp. a2	0	1	...	10
Exp. b0	0	1	...	10
Exp. b1	0	1	...	10

Test settings	
Tolerance b2	±0,0000e+00
Tolerance a1	±0,0000e+00
Tolerance a2	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test statistics	
Min CPU cycles	1482
Max CPU cycles	4479
Avg CPU cycles	2246

Verification: Biquad Float32 CPU STM32F072RB

Date of Test	2026-06-25
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for Filter block Biquad.

Test results				
Time step	1	2	...	73
CPU cycles	1092	1300	...	1589
Inputs				
In (DSP)	-0.056	-0.021	...	0.466
In	-0.056	-0.021	...	0.466
Parameters				
b0	0.2			
b1	0.1			
b2	0.3			
a0	1.1			
a1	-0.7			
a2	0.8			
ts_fact	1			
Outputs				
Out	-0.01	-0.015	...	0.257
Exp. Out	-0.01	-0.015	...	0.257
Out (DSP)	-0.01	-0.015	...	0.257
Exp. Out (DSP)	-0.01	-0.015	...	0.257

Test settings	
Tolerance Out	±9,3132e-08 (±200 LSB)

Test statistics	
Min CPU cycles	1092
Max CPU cycles	1635
Avg CPU cycles	1530

Test case: Conversion test OK

Conversion test for Filter block Biquad.

Test results				
Time step	1	2	...	8
Mask parameters				
b0	0	0.1	...	10
b1	0	0.1	...	10
b2	0	0.1	...	10
a0	0.1	0.1	...	1
a1	0	0.1	...	10
a2	0	0.1	...	10
ts_fact	1	1	...	1
Controller parameters				
b2	0	1	...	10
a1	0	1	...	10
a2	0	1	...	10
b0	0	1	...	10
b1	0	1	...	10
Exp. b2	0	1	...	10
Exp. a1	0	1	...	10
Exp. a2	0	1	...	10
Exp. b0	0	1	...	10
Exp. b1	0	1	...	10

Test settings	
Tolerance b2	±0,0000e+00
Tolerance a1	±0,0000e+00
Tolerance a2	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Filter block Biquad.

Test results				
Time step	1	2	...	8
Mask parameters				
b0	0	0.1	...	10
b1	0	0.1	...	10
b2	0	0.1	...	10
a0	0.1	0.1	...	1
a1	0	0.1	...	10
a2	0	0.1	...	10
ts_fact	1	1	...	1
Controller parameters				
b2	0	1	...	10
a1	0	1	...	10
a2	0	1	...	10
b0	0	1	...	10
b1	0	1	...	10
Exp. b2	0	1	...	10
Exp. a1	0	1	...	10
Exp. a2	0	1	...	10
Exp. b0	0	1	...	10
Exp. b1	0	1	...	10

Test settings	
Tolerance b2	±0,0000e+00
Tolerance a1	±0,0000e+00
Tolerance a2	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test statistics	
Min CPU cycles	3401
Max CPU cycles	7281
Avg CPU cycles	5669

Verification: Biquad Float32 CPU PIC32MX170F256

Date of Test	2026-06-25
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for Filter block Biquad.

Test results				
Time step	1	2	...	73
CPU cycles	383	477	...	590
Inputs				
In (DSP)	-0.056	-0.021	...	0.466
In	-0.056	-0.021	...	0.466
Parameters				
b0	0.2			
b1	0.1			
b2	0.3			
a0	1.1			
a1	-0.7			
a2	0.8			
ts_fact	1			
Outputs				
Out	-0.01	-0.015	...	0.257
Exp. Out	-0.01	-0.015	...	0.257
Out (DSP)	-0.01	-0.015	...	0.257
Exp. Out (DSP)	-0.01	-0.015	...	0.257

Test settings	
Tolerance Out	±9,3132e-08 (±200 LSB)

Test statistics	
Min CPU cycles	383
Max CPU cycles	590
Avg CPU cycles	573

Test case: Conversion test OK

Conversion test for Filter block Biquad.

Test results				
Time step	1	2	...	8
Mask parameters				
b0	0	0.1	...	10
b1	0	0.1	...	10
b2	0	0.1	...	10
a0	0.1	0.1	...	1
a1	0	0.1	...	10
a2	0	0.1	...	10
ts_fact	1	1	...	1
Controller parameters				
b2	0	1	...	10
a1	0	1	...	10
a2	0	1	...	10
b0	0	1	...	10
b1	0	1	...	10
Exp. b2	0	1	...	10
Exp. a1	0	1	...	10
Exp. a2	0	1	...	10
Exp. b0	0	1	...	10
Exp. b1	0	1	...	10

Test settings	
Tolerance b2	±0,0000e+00
Tolerance a1	±0,0000e+00
Tolerance a2	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Filter block Biquad.

Test results				
Time step	1	2	...	8
Mask parameters				
b0	0	0.1	...	10
b1	0	0.1	...	10
b2	0	0.1	...	10
a0	0.1	0.1	...	1
a1	0	0.1	...	10
a2	0	0.1	...	10
ts_fact	1	1	...	1
Controller parameters				
b2	0	1	...	10
a1	0	1	...	10
a2	0	1	...	10
b0	0	1	...	10
b1	0	1	...	10
Exp. b2	0	1	...	10
Exp. a1	0	1	...	10
Exp. a2	0	1	...	10
Exp. b0	0	1	...	10
Exp. b1	0	1	...	10

Test settings	
Tolerance b2	±0,0000e+00
Tolerance a1	±0,0000e+00
Tolerance a2	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test statistics	
Min CPU cycles	1279
Max CPU cycles	2494
Avg CPU cycles	2104

Verification: Biquad Float32 CPU dsPIC33EP256MC502

Date of Test	2026-06-25
Target controller	dsPIC33EP256MC502

Test case: Inport test

OK

Inport test for Filter block Biquad.

Test results				
Time step	1	2	...	73
CPU cycles	1200	1341	...	1568
Inputs				
In (DSP)	-0.056	-0.021	...	0.466
In	-0.056	-0.021	...	0.466
Parameters				
b0	0.2			
b1	0.1			
b2	0.3			
a0	1.1			
a1	-0.7			
a2	0.8			
ts_fact	1			
Outputs				
Out	-0.01	-0.015	...	0.257
Exp. Out	-0.01	-0.015	...	0.257
Out (DSP)	-0.01	-0.015	...	0.257
Exp. Out (DSP)	-0.01	-0.015	...	0.257

Test settings	
Tolerance Out	±9,3132e-08 (±200 LSB)

Test statistics	
Min CPU cycles	1200
Max CPU cycles	1687
Avg CPU cycles	1566

Test case: Conversion test

OK

Conversion test for Filter block Biquad.

Test results				
Time step	1	2	...	8
Mask parameters				
b0	0	0.1	...	10
b1	0	0.1	...	10
b2	0	0.1	...	10
a0	0.1	0.1	...	1
a1	0	0.1	...	10
a2	0	0.1	...	10
ts_fact	1	1	...	1
Controller parameters				
b2	0	1	...	10
a1	0	1	...	10
a2	0	1	...	10
b0	0	1	...	10
b1	0	1	...	10
Exp. b2	0	1	...	10
Exp. a1	0	1	...	10
Exp. a2	0	1	...	10
Exp. b0	0	1	...	10
Exp. b1	0	1	...	10

Test settings	
Tolerance b2	±0,0000e+00
Tolerance a1	±0,0000e+00
Tolerance a2	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Filter block Biquad.

Test results				
Time step	1	2	...	8
Mask parameters				
b0	0	0.1	...	10
b1	0	0.1	...	10
b2	0	0.1	...	10
a0	0.1	0.1	...	1
a1	0	0.1	...	10
a2	0	0.1	...	10
ts_fact	1	1	...	1
Controller parameters				
b2	0	1	...	10
a1	0	1	...	10
a2	0	1	...	10
b0	0	1	...	10
b1	0	1	...	10
Exp. b2	0	1	...	10
Exp. a1	0	1	...	10
Exp. a2	0	1	...	10
Exp. b0	0	1	...	10
Exp. b1	0	1	...	10

Test settings	
Tolerance b2	±0,0000e+00
Tolerance a1	±0,0000e+00
Tolerance a2	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test statistics	
Min CPU cycles	3904
Max CPU cycles	11900
Avg CPU cycles	10800

Verification: Biquad Float32 CPU XMC4800-F144K2048

Date of Test	2026-06-25
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for Filter block Biquad.

Test results				
Time step	1	2	...	73
CPU cycles	115	99	...	99
Inputs				
In (DSP)	-0.056	-0.021	...	0.466
In	-0.056	-0.021	...	0.466
Parameters				
b0	0.2			
b1	0.1			
b2	0.3			
a0	1.1			
a1	-0.7			
a2	0.8			
ts_fact	1			
Outputs				
Out	-0.01	-0.015	...	0.257
Exp. Out	-0.01	-0.015	...	0.257
Out (DSP)	-0.01	-0.015	...	0.257
Exp. Out (DSP)	-0.01	-0.015	...	0.257

Test settings	
Tolerance Out	±9,3132e-08 (±200 LSB)

Test statistics	
Min CPU cycles	99
Max CPU cycles	115
Avg CPU cycles	99

Test case: Conversion test OK

Conversion test for Filter block Biquad.

Test results				
Time step	1	2	...	8
Mask parameters				
b0	0	0.1	...	10
b1	0	0.1	...	10
b2	0	0.1	...	10
a0	0.1	0.1	...	1
a1	0	0.1	...	10
a2	0	0.1	...	10
ts_fact	1	1	...	1
Controller parameters				
b2	0	1	...	10
a1	0	1	...	10
a2	0	1	...	10
b0	0	1	...	10
b1	0	1	...	10
Exp. b2	0	1	...	10
Exp. a1	0	1	...	10
Exp. a2	0	1	...	10
Exp. b0	0	1	...	10
Exp. b1	0	1	...	10

Test settings	
Tolerance b2	±0,0000e+00
Tolerance a1	±0,0000e+00
Tolerance a2	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Filter block Biquad.

Test results				
Time step	1	2	...	8
Mask parameters				
b0	0	0.1	...	10
b1	0	0.1	...	10
b2	0	0.1	...	10
a0	0.1	0.1	...	1
a1	0	0.1	...	10
a2	0	0.1	...	10
ts_fact	1	1	...	1
Controller parameters				
b2	0	1	...	10
a1	0	1	...	10
a2	0	1	...	10
b0	0	1	...	10
b1	0	1	...	10
Exp. b2	0	1	...	10
Exp. a1	0	1	...	10
Exp. a2	0	1	...	10
Exp. b0	0	1	...	10
Exp. b1	0	1	...	10

Test settings	
Tolerance b2	±0,0000e+00
Tolerance a1	±0,0000e+00
Tolerance a2	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test statistics	
Min CPU cycles	1407
Max CPU cycles	4356
Avg CPU cycles	2173

Verification: Biquad Float32 CPU TMS320F28379D

Date of Test	2026-06-25
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for Filter block Biquad.

Test results				
Time step	1	2	...	73
CPU cycles	86	86	...	86
Inputs				
In (DSP)	-0.056	-0.021	...	0.466
In	-0.056	-0.021	...	0.466
Parameters				
b0	0.2			
b1	0.1			
b2	0.3			
a0	1.1			
a1	-0.7			
a2	0.8			
ts_fact	1			
Outputs				
Out	-0.01	-0.015	...	0.257
Exp. Out	-0.01	-0.015	...	0.257
Out (DSP)	-0.01	-0.015	...	0.257
Exp. Out (DSP)	-0.01	-0.015	...	0.257

Test settings	
Tolerance Out	±9,3132e-08 (±200 LSB)

Test statistics	
Min CPU cycles	86
Max CPU cycles	86
Avg CPU cycles	86

Test case: Conversion test OK

Conversion test for Filter block Biquad.

Test results				
Time step	1	2	...	8
Mask parameters				
b0	0	0.1	...	10
b1	0	0.1	...	10
b2	0	0.1	...	10
a0	0.1	0.1	...	1
a1	0	0.1	...	10
a2	0	0.1	...	10
ts_fact	1	1	...	1
Controller parameters				
b2	0	1	...	10
a1	0	1	...	10
a2	0	1	...	10
b0	0	1	...	10
b1	0	1	...	10
Exp. b2	0	1	...	10
Exp. a1	0	1	...	10
Exp. a2	0	1	...	10
Exp. b0	0	1	...	10
Exp. b1	0	1	...	10

Test settings	
Tolerance b2	±0,0000e+00
Tolerance a1	±0,0000e+00
Tolerance a2	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

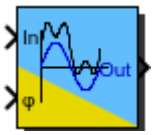
Conversion-on-Target test for Filter block Biquad.

Test results				
Time step	1	2	...	8
Mask parameters				
b0	0	0.1	...	10
b1	0	0.1	...	10
b2	0	0.1	...	10
a0	0.1	0.1	...	1
a1	0	0.1	...	10
a2	0	0.1	...	10
ts_fact	1	1	...	1
Controller parameters				
b2	0	1	...	10
a1	0	1	...	10
a2	0	1	...	10
b0	0	1	...	10
b1	0	1	...	10
Exp. b2	0	1	...	10
Exp. a1	0	1	...	10
Exp. a2	0	1	...	10
Exp. b0	0	1	...	10
Exp. b1	0	1	...	10

Test settings	
Tolerance b2	±0,0000e+00
Tolerance a1	±0,0000e+00
Tolerance a2	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test statistics	
Min CPU cycles	2779
Max CPU cycles	15619
Avg CPU cycles	6508

Block: FundFreq



Calculation of the first harmonic (fundamental frequency) of the input signal.

Inports	
In	Input signal
phi	Angle signal

Outports	
Out	First harmonic

Mask Parameters		
Name	**ID**	**Description**
ts_fact	1	Multiplication factor of base sampling time (in integer format)

Implementations:

FiP16	16 Bit Fixed Point Implementation
FiP32	32 Bit Fixed Point Implementation
Float32	32 Bit Floating Point Implementation
Float64	64 Bit Floating Point Implementation

Implementation: FiP16

16 Bit Fixed Point Implementation

Inports Data Type	
In	int16
phi	int16

Outports Data Type	
Out	int16

Implementation: FiP32

32 Bit Fixed Point Implementation

Inports Data Type	
In	int32
phi	int32

Outports Data Type	
Out	int32

Implementation: Float32

32 Bit Floating Point Implementation

Inports Data Type	
In	float32
phi	float32

Outports Data Type	
Out	float32

Implementation: Float64

64 Bit Floating Point Implementation

Inports Data Type	
In	float64
phi	float64

Outports Data Type	
Out	float64

Verification: FundFreq FiP16 CPU TMS320F28335

Date of Test	2026-06-25
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for Filter block FundFreq.

Test results						
Time step	1	2	3	4	...	111
CPU cycles	201	202	202	202	...	202
Inputs						
In (DSP)	6554	-705	-6595	-10422	...	13812
phi (DSP)	-32768	-30997	-29226	-27454	...	30997
In	0.2	-0.022	-0.201	-0.318	...	0.422
phi	-1	-0.946	-0.892	-0.838	...	0.946
Parameters						
ts_fact	1					
Outputs						
Out	0	0	0	0	...	0.135
Exp. Out	0	0	0	0	...	0.135
Out (DSP)	0	0	0	0	...	4428
Exp. Out (DSP)	0	0	0	0	...	4430

Test settings	
Tolerance Out	±3,0518e-04 (±10 LSB)

Test statistics	
Min CPU cycles	201
Max CPU cycles	372
Avg CPU cycles	205

Verification: FundFreq FiP16 CPU TM4C123GH6

Date of Test	2026-06-25
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for Filter block FundFreq.

Test results						
Time step	1	2	3	4	...	111
CPU cycles	129	129	129	129	...	129
Inputs						
In (DSP)	6554	-705	-6595	-10422	...	13812
phi (DSP)	-32768	-30997	-29226	-27454	...	30997
In	0.2	-0.022	-0.201	-0.318	...	0.422
phi	-1	-0.946	-0.892	-0.838	...	0.946
Parameters						
ts_fact	1					
Outputs						
Out	0	0	0	0	...	0.135
Exp. Out	0	0	0	0	...	0.135
Out (DSP)	0	0	0	0	...	4428
Exp. Out (DSP)	0	0	0	0	...	4430

Test settings	
Tolerance Out	±3,0518e-04 (±10 LSB)

Test statistics	
Min CPU cycles	129
Max CPU cycles	157
Avg CPU cycles	129

Verification: FundFreq FiP16 CPU STM32G474RE

Date of Test	2026-06-25
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for Filter block FundFreq.

Test results						
Time step	1	2	3	4	...	111
CPU cycles	225	230	230	225	...	230
Inputs						
In (DSP)	6554	-705	-6595	-10422	...	13812
phi (DSP)	-32768	-30997	-29226	-27454	...	30997
In	0.2	-0.022	-0.201	-0.318	...	0.422
phi	-1	-0.946	-0.892	-0.838	...	0.946
Parameters						
ts_fact	1					
Outputs						
Out	0	0	0	0	...	0.135
Exp. Out	0	0	0	0	...	0.135
Out (DSP)	0	0	0	0	...	4428
Exp. Out (DSP)	0	0	0	0	...	4430

Test settings	
Tolerance Out	±3,0518e-04 (±10 LSB)

Test statistics	
Min CPU cycles	213
Max CPU cycles	230
Avg CPU cycles	227

Verification: FundFreq FiP16 CPU STM32F072RB

Date of Test	2026-06-25
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for Filter block FundFreq.

Test results						
Time step	1	2	3	4	...	111
CPU cycles	208	208	208	208	...	208
Inputs						
In (DSP)	6554	-705	-6595	-10422	...	13812
phi (DSP)	-32768	-30997	-29226	-27454	...	30997
In	0.2	-0.022	-0.201	-0.318	...	0.422
phi	-1	-0.946	-0.892	-0.838	...	0.946
Parameters						
ts_fact	1					
Outputs						
Out	0	0	0	0	...	0.135
Exp. Out	0	0	0	0	...	0.135
Out (DSP)	0	0	0	0	...	4428
Exp. Out (DSP)	0	0	0	0	...	4430

Test settings	
Tolerance Out	±3,0518e-04 (±10 LSB)

Test statistics	
Min CPU cycles	208
Max CPU cycles	407
Avg CPU cycles	211

Verification: FundFreq FiP16 CPU PIC32MX170F256

Date of Test	2026-06-25
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for Filter block FundFreq.

Test results						
Time step	1	2	3	4	...	111
CPU cycles	124	123	123	123	...	123
Inputs						
In (DSP)	6554	-705	-6595	-10422	...	13812
phi (DSP)	-32768	-30997	-29226	-27454	...	30997
In	0.2	-0.022	-0.201	-0.318	...	0.422
phi	-1	-0.946	-0.892	-0.838	...	0.946
Parameters						
ts_fact	1					
Outputs						
Out	0	0	0	0	...	0.135
Exp. Out	0	0	0	0	...	0.135
Out (DSP)	0	0	0	0	...	4428
Exp. Out (DSP)	0	0	0	0	...	4430

Test settings	
Tolerance Out	±3,0518e-04 (±10 LSB)

Test statistics	
Min CPU cycles	123
Max CPU cycles	173
Avg CPU cycles	123

Verification: FundFreq FiP16 CPU dsPIC33EP256MC502

Date of Test	2026-06-25
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for Filter block FundFreq.

Test results						
Time step	1	2	3	4	...	111
CPU cycles	190	181	181	181	...	181
Inputs						
In (DSP)	6554	-705	-6595	-10422	...	13812
phi (DSP)	-32768	-30997	-29226	-27454	...	30997
In	0.2	-0.022	-0.201	-0.318	...	0.422
phi	-1	-0.946	-0.892	-0.838	...	0.946
Parameters						
ts_fact	1					
Outputs						
Out	0	0	0	0	...	0.135
Exp. Out	0	0	0	0	...	0.135
Out (DSP)	0	0	0	0	...	4428
Exp. Out (DSP)	0	0	0	0	...	4430

Test settings	
Tolerance Out	±3,0518e-04 (±10 LSB)

Test statistics	
Min CPU cycles	181
Max CPU cycles	1314
Avg CPU cycles	201

Verification: FundFreq FiP16 CPU XMC4800-F144K2048

Date of Test	2026-06-25
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for Filter block FundFreq.

Test results						
Time step	1	2	3	4	...	111
CPU cycles	212	179	174	174	...	176
Inputs						
In (DSP)	6554	-705	-6595	-10422	...	13812
phi (DSP)	-32768	-30997	-29226	-27454	...	30997
In	0.2	-0.022	-0.201	-0.318	...	0.422
phi	-1	-0.946	-0.892	-0.838	...	0.946
Parameters						
ts_fact	1					
Outputs						
Out	0	0	0	0	...	0.135
Exp. Out	0	0	0	0	...	0.135
Out (DSP)	0	0	0	0	...	4428
Exp. Out (DSP)	0	0	0	0	...	4430

Test settings	
Tolerance Out	±3,0518e-04 (±10 LSB)

Test statistics	
Min CPU cycles	165
Max CPU cycles	212
Avg CPU cycles	174

Verification: FundFreq FiP16 CPU TMS320F28379D

Date of Test	2026-06-25
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for Filter block FundFreq.

Test results						
Time step	1	2	3	4	...	111
CPU cycles	194	198	195	195	...	198
Inputs						
In (DSP)	6554	-705	-6595	-10422	...	13812
phi (DSP)	-32768	-30997	-29226	-27454	...	30997
In	0.2	-0.022	-0.201	-0.318	...	0.422
phi	-1	-0.946	-0.892	-0.838	...	0.946
Parameters						
ts_fact	1					
Outputs						
Out	0	0	0	0	...	0.135
Exp. Out	0	0	0	0	...	0.135
Out (DSP)	0	0	0	0	...	4428
Exp. Out (DSP)	0	0	0	0	...	4430

Test settings	
Tolerance Out	±3,0518e-04 (±10 LSB)

Test statistics	
Min CPU cycles	190
Max CPU cycles	357
Avg CPU cycles	198

Verification: FundFreq FiP32 CPU TMS320F28335

Date of Test	2026-06-25
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for Filter block FundFreq.

Test results				
Time step	1	2	...	111
CPU cycles	453	451	...	451
Inputs				
In (DSP)	429496730	-46178986	...	905172445
phi (DSP)	-2147483648	-2031403451	...	2031403451
In	0.2	-0.022	...	0.422
phi	-1	-0.946	...	0.946
Parameters				
ts_fact	1			
Outputs				
Out	0	0	...	0.135
Exp. Out	0	0	...	0.135
Out (DSP)	0	0	...	290320398
Exp. Out (DSP)	0	0	...	290341199

Test settings	
Tolerance Out	±2,3283e-04 (±500000 LSB)

Test statistics	
Min CPU cycles	451
Max CPU cycles	897
Avg CPU cycles	459

Verification: FundFreq FiP32 CPU TM4C123GH6

Date of Test	2026-06-25
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for Filter block FundFreq.

Test results				
Time step	1	2	...	111
CPU cycles	175	179	...	179
Inputs				
In (DSP)	429496730	-46178986	...	905172445
phi (DSP)	-2147483648	-2031403451	...	2031403451
In	0.2	-0.022	...	0.422
phi	-1	-0.946	...	0.946
Parameters				
ts_fact	1			
Outputs				
Out	0	0	...	0.135
Exp. Out	0	0	...	0.135
Out (DSP)	0	0	...	290320398
Exp. Out (DSP)	0	0	...	290341199

Test settings	
Tolerance Out	±2,3283e-04 (±500000 LSB)

Test statistics	
Min CPU cycles	175
Max CPU cycles	935
Avg CPU cycles	192

Verification: FundFreq FiP32 CPU STM32G474RE

Date of Test	2026-06-25
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for Filter block FundFreq.

Test results				
Time step	1	2	...	111
CPU cycles	296	301	...	301
Inputs				
In (DSP)	429496730	-46178986	...	905172445
phi (DSP)	-2147483648	-2031403451	...	2031403451
In	0.2	-0.022	...	0.422
phi	-1	-0.946	...	0.946
Parameters				
ts_fact	1			
Outputs				
Out	0	0	...	0.135
Exp. Out	0	0	...	0.135
Out (DSP)	0	0	...	290320398
Exp. Out (DSP)	0	0	...	290341199

Test settings	
Tolerance Out	±2,3283e-04 (±500000 LSB)

Test statistics	
Min CPU cycles	296
Max CPU cycles	602
Avg CPU cycles	306

Verification: FundFreq FiP32 CPU STM32F072RB

Date of Test	2026-06-25
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for Filter block FundFreq.

Test results				
Time step	1	2	...	111
CPU cycles	701	701	...	701
Inputs				
In (DSP)	429496730	-46178986	...	905172445
phi (DSP)	-2147483648	-2031403451	...	2031403451
In	0.2	-0.022	...	0.422
phi	-1	-0.946	...	0.946
Parameters				
ts_fact	1			
Outputs				
Out	0	0	...	0.135
Exp. Out	0	0	...	0.135
Out (DSP)	0	0	...	290320398
Exp. Out (DSP)	0	0	...	290341199

Test settings	
Tolerance Out	±2,3283e-04 (±500000 LSB)

Test statistics	
Min CPU cycles	699
Max CPU cycles	2222
Avg CPU cycles	729

Verification: FundFreq FiP32 CPU PIC32MX170F256

Date of Test	2026-06-25
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for Filter block FundFreq.

Test results				
Time step	1	2	...	111
CPU cycles	237	233	...	235
Inputs				
In (DSP)	429496730	-46178986	...	905172445
phi (DSP)	-2147483648	-2031403451	...	2031403451
In	0.2	-0.022	...	0.422
phi	-1	-0.946	...	0.946
Parameters				
ts_fact	1			
Outputs				
Out	0	0	...	0.135
Exp. Out	0	0	...	0.135
Out (DSP)	0	0	...	290320398
Exp. Out (DSP)	0	0	...	290341199

Test settings	
Tolerance Out	±2,3283e-04 (±500000 LSB)

Test statistics	
Min CPU cycles	233
Max CPU cycles	461
Avg CPU cycles	238

Verification: FundFreq FiP32 CPU dsPIC33EP256MC502

Date of Test	2026-06-25
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for Filter block FundFreq.

Test results				
Time step	1	2	...	111
CPU cycles	964	974	...	952
Inputs				
In (DSP)	429496730	-46178986	...	905172445
phi (DSP)	-2147483648	-2031403451	...	2031403451
In	0.2	-0.022	...	0.422
phi	-1	-0.946	...	0.946
Parameters				
ts_fact	1			
Outputs				
Out	0	0	...	0.135
Exp. Out	0	0	...	0.135
Out (DSP)	0	0	...	290320398
Exp. Out (DSP)	0	0	...	290341199

Test settings	
Tolerance Out	±2,3283e-04 (±500000 LSB)

Test statistics	
Min CPU cycles	930
Max CPU cycles	19683
Avg CPU cycles	1293

Verification: FundFreq FiP32 CPU XMC4800-F144K2048

Date of Test	2026-06-25
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for Filter block FundFreq.

Test results				
Time step	1	2	...	111
CPU cycles	332	266	...	266
Inputs				
In (DSP)	429496730	-46178986	...	905172445
phi (DSP)	-2147483648	-2031403451	...	2031403451
In	0.2	-0.022	...	0.422
phi	-1	-0.946	...	0.946
Parameters				
ts_fact	1			
Outputs				
Out	0	0	...	0.135
Exp. Out	0	0	...	0.135
Out (DSP)	0	0	...	290320398
Exp. Out (DSP)	0	0	...	290341199

Test settings	
Tolerance Out	±2,3283e-04 (±500000 LSB)

Test statistics	
Min CPU cycles	257
Max CPU cycles	701
Avg CPU cycles	273

Verification: FundFreq FiP32 CPU TMS320F28379D

Date of Test	2026-06-25
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for Filter block FundFreq.

Test results				
Time step	1	2	...	111
CPU cycles	426	412	...	412
Inputs				
In (DSP)	429496730	-46178986	...	905172445
phi (DSP)	-2147483648	-2031403451	...	2031403451
In	0.2	-0.022	...	0.422
phi	-1	-0.946	...	0.946
Parameters				
ts_fact	1			
Outputs				
Out	0	0	...	0.135
Exp. Out	0	0	...	0.135
Out (DSP)	0	0	...	290320398
Exp. Out (DSP)	0	0	...	290341199

Test settings	
Tolerance Out	±2,3283e-04 (±500000 LSB)

Test statistics	
Min CPU cycles	412
Max CPU cycles	838
Avg CPU cycles	421

Verification: FundFreq Float32 CPU TMS320F28335

Date of Test	2026-06-25
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for Filter block FundFreq.

Test results				
Time step	1	2	...	111
CPU cycles	475	463	...	451
Inputs				
In (DSP)	1.06	-0.114	...	2.234
phi (DSP)	-3.142	-2.972	...	2.972
In	1.06	-0.114	...	2.234
phi	-3.142	-2.972	...	2.972
Parameters				
ts_fact	1			
Outputs				
Out	0	-0	...	0.717
Exp. Out	0	0	...	0.717
Out (DSP)	0	-0	...	0.717
Exp. Out (DSP)	0	0	...	0.717

Test settings	
Tolerance Out	±1,1642e-06 (±2500 LSB)

Test statistics	
Min CPU cycles	451
Max CPU cycles	993
Avg CPU cycles	466

Verification: FundFreq Float32 CPU TM4C123GH6

Date of Test	2026-06-25
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for Filter block FundFreq.

Test results				
Time step	1	2	...	111
CPU cycles	257	257	...	257
Inputs				
In (DSP)	1.06	-0.114	...	2.234
phi (DSP)	-3.142	-2.972	...	2.972
In	1.06	-0.114	...	2.234
phi	-3.142	-2.972	...	2.972
Parameters				
ts_fact	1			
Outputs				
Out	0	-0	...	0.717
Exp. Out	0	0	...	0.717
Out (DSP)	0	-0	...	0.717
Exp. Out (DSP)	0	0	...	0.717

Test settings	
Tolerance Out	±1,1642e-06 (±2500 LSB)

Test statistics	
Min CPU cycles	257
Max CPU cycles	295
Avg CPU cycles	257

Verification: FundFreq Float32 CPU STM32G474RE

Date of Test	2026-06-25
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for Filter block FundFreq.

Test results				
Time step	1	2	...	111
CPU cycles	976	898	...	880
Inputs				
In (DSP)	1.06	-0.114	...	2.234
phi (DSP)	-3.142	-2.972	...	2.972
In	1.06	-0.114	...	2.234
phi	-3.142	-2.972	...	2.972
Parameters				
ts_fact	1			
Outputs				
Out	0	-0	...	0.717
Exp. Out	0	0	...	0.717
Out (DSP)	0	-0	...	0.717
Exp. Out (DSP)	0	0	...	0.717

Test settings	
Tolerance Out	±1,1642e-06 (±2500 LSB)

Test statistics	
Min CPU cycles	449
Max CPU cycles	988
Avg CPU cycles	716

Verification: FundFreq Float32 CPU STM32F072RB

Date of Test	2026-06-25
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for Filter block FundFreq.

Test results				
Time step	1	2	...	111
CPU cycles	12071	10500	...	10547
Inputs				
In (DSP)	1.06	-0.114	...	2.234
phi (DSP)	-3.142	-2.972	...	2.972
In	1.06	-0.114	...	2.234
phi	-3.142	-2.972	...	2.972
Parameters				
ts_fact	1			
Outputs				
Out	0	-0	...	0.717
Exp. Out	0	0	...	0.717
Out (DSP)	0	-0	...	0.717
Exp. Out (DSP)	0	0	...	0.717

Test settings	
Tolerance Out	±1,1642e-06 (±2500 LSB)

Test statistics	
Min CPU cycles	6544
Max CPU cycles	13543
Avg CPU cycles	8938

Verification: FundFreq Float32 CPU PIC32MX170F256

Date of Test	2026-06-25
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for Filter block FundFreq.

Test results				
Time step	1	2	...	111
CPU cycles	1275	985	...	1044
Inputs				
In (DSP)	1.06	-0.114	...	2.234
phi (DSP)	-3.142	-2.972	...	2.972
In	1.06	-0.114	...	2.234
phi	-3.142	-2.972	...	2.972
Parameters				
ts_fact	1			
Outputs				
Out	0	-0	...	0.717
Exp. Out	0	0	...	0.717
Out (DSP)	0	-0	...	0.717
Exp. Out (DSP)	0	0	...	0.717

Test settings	
Tolerance Out	±1,1642e-06 (±2500 LSB)

Test statistics	
Min CPU cycles	755
Max CPU cycles	1814
Avg CPU cycles	960

Verification: FundFreq Float32 CPU dsPIC33EP256MC502

Date of Test	2026-06-25
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for Filter block FundFreq.

Test results				
Time step	1	2	...	111
CPU cycles	7204	9394	...	9847
Inputs				
In (DSP)	1.06	-0.114	...	2.234
phi (DSP)	-3.142	-2.972	...	2.972
In	1.06	-0.114	...	2.234
phi	-3.142	-2.972	...	2.972
Parameters				
ts_fact	1			
Outputs				
Out	0	-0	...	0.717
Exp. Out	0	0	...	0.717
Out (DSP)	0	-0	...	0.717
Exp. Out (DSP)	0	0	...	0.717

Test settings	
Tolerance Out	±1,1642e-06 (±2500 LSB)

Test statistics	
Min CPU cycles	7204
Max CPU cycles	9847
Avg CPU cycles	8883

Verification: FundFreq Float32 CPU XMC4800-F144K2048

Date of Test	2026-06-25
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for Filter block FundFreq.

Test results				
Time step	1	2	...	111
CPU cycles	1009	669	...	653
Inputs				
In (DSP)	1.06	-0.114	...	2.234
phi (DSP)	-3.142	-2.972	...	2.972
In	1.06	-0.114	...	2.234
phi	-3.142	-2.972	...	2.972
Parameters				
ts_fact	1			
Outputs				
Out	0	-0	...	0.717
Exp. Out	0	0	...	0.717
Out (DSP)	0	-0	...	0.717
Exp. Out (DSP)	0	0	...	0.717

Test settings	
Tolerance Out	±1,1642e-06 (±2500 LSB)

Test statistics	
Min CPU cycles	342
Max CPU cycles	1009
Avg CPU cycles	530

Verification: FundFreq Float32 CPU TMS320F28379D

Date of Test	2026-06-25
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for Filter block FundFreq.

Test results				
Time step	1	2	...	111
CPU cycles	315	312	...	302
Inputs				
In (DSP)	1.06	-0.114	...	2.234
phi (DSP)	-3.142	-2.972	...	2.972
In	1.06	-0.114	...	2.234
phi	-3.142	-2.972	...	2.972
Parameters				
ts_fact	1			
Outputs				
Out	0	-0	...	0.717
Exp. Out	0	0	...	0.717
Out (DSP)	0	-0	...	0.717
Exp. Out (DSP)	0	0	...	0.717

Test settings	
Tolerance Out	±1,1642e-06 (±2500 LSB)

Test statistics	
Min CPU cycles	302
Max CPU cycles	806
Avg CPU cycles	316

Block: HighpassBiQ



Calculates the filter coefficients for a second order highpass and performs filtering on input signal.
Second order transfer function used:
$H(z) = (b0.z^2 + b1.z + b2) / (z^2 + a1.z + a2)$

Inports	
In	Input In(k)

Outports	
Out	Output Out(k)

Mask Parameters		
Name	**ID**	**Description**
characteristic	1	The filter characteristic is one of Butterworth, Chebyshev I, Chebyshev II (also known as inverse Chebyshev) or Bessel
fc	2	Cut-off frequency in Hz
rp	3	The passband ripple is only used and verified with 'Chebyshev I' filters. Must be a positive number
rs	4	The stopband ripple is only used and verified with 'Chebyshev II' filters. Must be a positive number
ts_fact	5	Multiplication factor of base sampling time (in integer format)

Description:

Butterworth

- passband
  - maximal flat
- @cut-off frequency:
  - -3dB attenuation
  - -90 degree phaseshift
- stopband
  - monotonic -40dB decline per decade
  - approx. -37dB decline within fist decade

E.g.: Cut-off frequency is 10Hz. The bodeplot is shown in the figure 5 below.
Chebyshev I

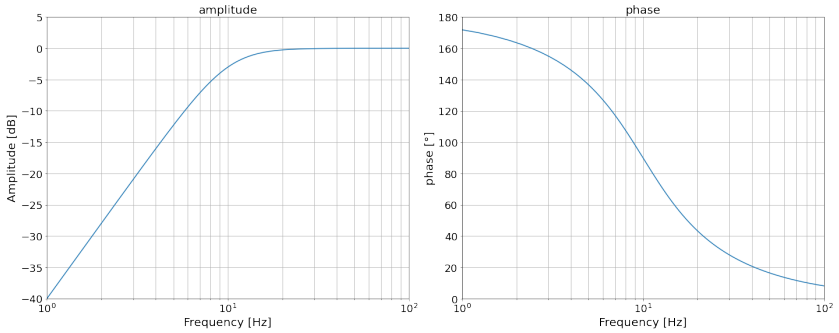


Figure 5: Bodeplot Butterworth highpass.

- passband:
  - N/2=1 ripple in the passband.
  - attenuation from 0 to rp [dB].
- @cut-off frequency: attenuation is bigger than or equal rp [dB].
- stopband:
  - monotonic -40dB decline per decade
- Trade-off:
  - the bigger passband ripple rp is choosen, the steeper is the magnitude cut-off within the first decade in stopband
  - the bigger the passband ripple rp is choosen, the bigger is the overall passband attenuation!

E.g.:
Cut-off frequency is 10Hz.
The maximal ripple in the passband rp must be given in [dB].
To show the mentioned trade-off, two bodelplots are shown. One with a small and one with a bigger rp. The bodeplot is shown in the figures 6 and 7 below.

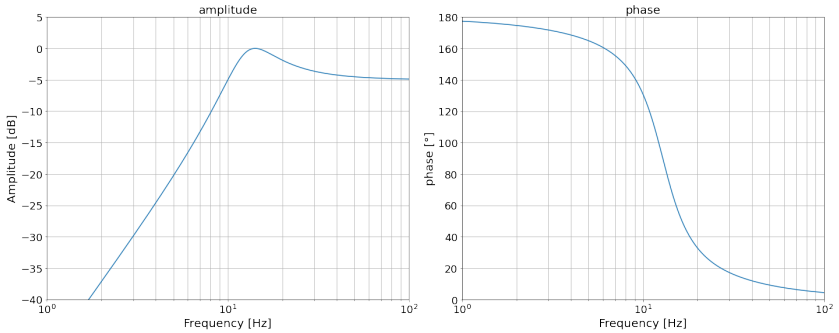


Figure 6: Bodeplot Chebyshev I highpass. $rp = 5$dB

Chebyshev II
Also known as inverse Chebyshev filter.

- passband
  - flat, no ripples

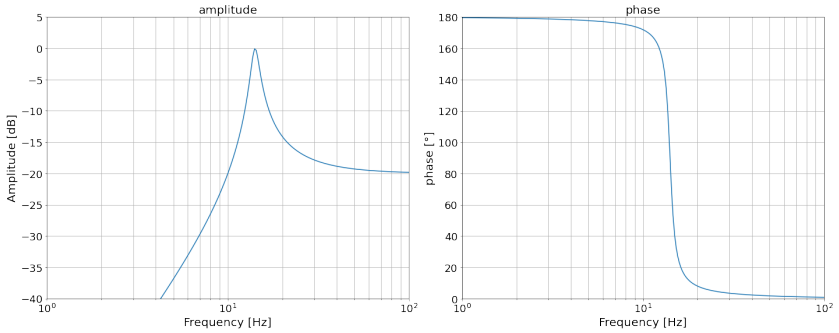


Figure 7: Bodeplot Chebyshev I highpass. $rp = 20$dB

- @cut-off frequency: attenuation is rs [dB].
- stopband
  - N/2=1 ripple in the stopband
  - attenuation is smaller than or equal rs [dB].
- Trade-off:
  - the lower rs is choosen, the sharper is the magnitude cut-off
  - the lower rs is choosen, the lower is the over all stopband attenuation

E.g.:
Cut-off frequency is 10Hz.
The maximal ripple in the stopband rs must be given in [dB].
To show the mentioned trade-off, two bodelplots are shown. One with a small and one with a bigger rs. The bodeplot is shown in the figures 8 and 9 below.

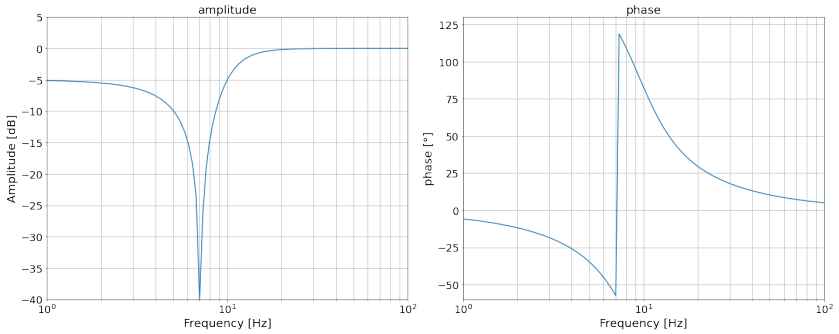


Figure 8: Bodeplot Chebyshev II highpass. $rs = 5$dB

Bessel

- passband
  - constant group-delay in passband.
  - least sharp magnitude roll-off.
- @cut-off frequency:
  - approx. -1.6 dB attenuation
  - approx. -56 degree phaseshift

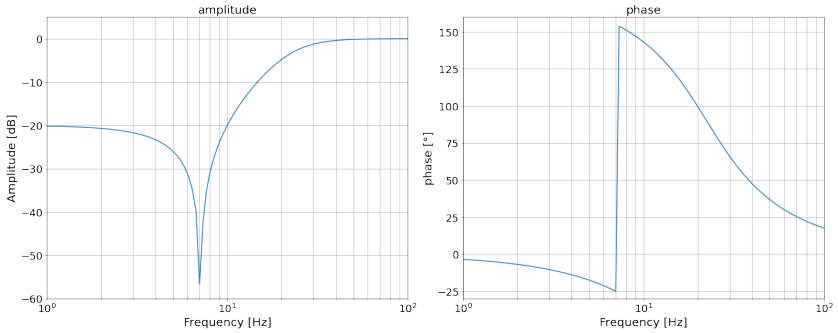


Figure 9: Bodeplot Chebyshev II highpass. $rs = 20$dB

- stopband
  - monotonic -40dB decline per decade
  - approx. -30dB decline within first decade

E.g.:
Cut-off frequency is 10Hz.
The bodeplot is shown in the figure 10 below.

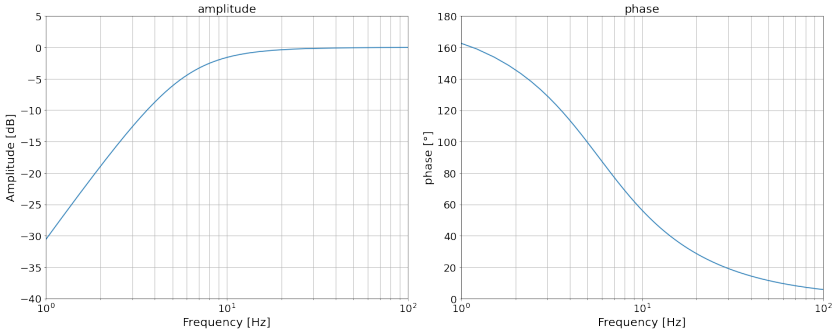


Figure 10: Bodeplot Bessel highpass.

Implementations:

FiP16	16 Bit Fixed Point Implementation
FiP32	32 Bit Fixed Point Implementation
Float32	32 Bit Floating Point Implementation
Float64	64 Bit Floating Point Implementation

Implementation: FiP16

16 Bit Fixed Point Implementation

Inports Data Type	
In	int16

Outports Data Type	
Out	int16

Implementation: FiP32

32 Bit Fixed Point Implementation

Inports Data Type	
In	int32

Outports Data Type	
Out	int32

Implementation: Float32

32 Bit Floating Point Implementation

Inports Data Type	
In	float32

Outports Data Type	
Out	float32

Implementation: Float64

64 Bit Floating Point Implementation

Inports Data Type	
In	float64

Outports Data Type	
Out	float64

Block: IIR



Transfer function:
H(z) = (b0.z^n + b1.z + ...+ bn) / (a0.z^n + a1.z + ... + an)
The maximum filter order is 32.
The order of the denominator has to be greater than or equal to the order of the numerator.

Inports	
In	Input In(k)

Outports	
Out	Output Out(k)

Mask Parameters		
Name	**ID**	**Description**
CoeffB	1	Array with filter coefficients of numerator
CoeffA	2	Array with filter coefficients of denominator
ts_fact	3	Multiplication factor of base sampling time (in integer format)

Implementations:

FiP16 16 Bit Fixed Point Implementation
FiP32 32 Bit Fixed Point Implementation
Float32 32 Bit Floating Point Implementation
Float64 64 Bit Floating Point Implementation

Implementation: FiP16

16 Bit Fixed Point Implementation

Inports Data Type	
In	int16

Outports Data Type	
Out	int16

Implementation: FiP32

32 Bit Fixed Point Implementation

Inports Data Type	
In	int32

Outports Data Type	
Out	int32

Implementation: Float32

32 Bit Floating Point Implementation

Inports Data Type	
In	float32

Outports Data Type	
Out	float32

Implementation: Float64

64 Bit Floating Point Implementation

Inports Data Type	
In	float64

Outports Data Type	
Out	float64

Block: LowpassBiQ



Calculates the filter coefficients for a second order lowpass and performs filtering on input signal.
Second order transfer function used:
$H(z) = (b0.z^2 + b1.z + b2) / (z^2 + a1.z + a2)$

Inports	
In	Input In(k)

Outports	
Out	Output Out(k)

Mask Parameters		
Name	**ID**	**Description**
characteristic	1	The filter characteristic is one of Butterworth, Chebyshev I, Chebyshev II (also known as inverse Chebyshev) or Bessel
fc	2	Cut-off frequency in Hz
rp	3	The passband ripple is only used and verified with 'Chebyshev I' filters. Must be a positive number
rs	4	The stopband ripple is only used and verified with 'Chebyshev II' filters. Must be a positive number
ts_fact	5	Multiplication factor of base sampling time (in integer format)

Description:

Butterworth

- passband
  - maximal flat
- @cut-off frequency:
  - -3dB attenuation
  - -90 degree phaseshift
- stopband
  - monotonic -40dB decline per decade
  - approx. -37dB decline within fist decade

E.g.: Cut-off frequency is 10Hz. The bodeplot is shown in the figure 11 below.
Chebyshev I

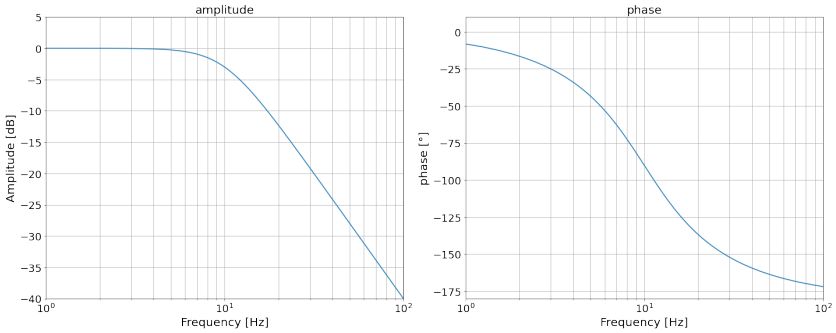


Figure 11: Bodeplot Butterworth lowpass.

- passband:
  - N/2=1 ripple in the passband.
  - attenuation from 0 to rp [dB].
- @cut-off frequency: attenuation is bigger than or equal rp [dB].
- stopband:
  - monotonic -40dB decline per decade
- Trade-off:
  - the bigger passband ripple rp is choosen, the steeper is the magnitude cut-off within the first decade in stopband
  - the bigger the passband ripple rp is choosen, the bigger is the overall passband attenuation!

E.g.:
Cut-off frequency is 10Hz.
The maximal ripple in the passband rp must be given in [dB].
To show the mentioned trade-off, two bodelplots are shown. One with a small and one with a bigger rp. The bodeplot is shown in the figures 12 and 13 below.

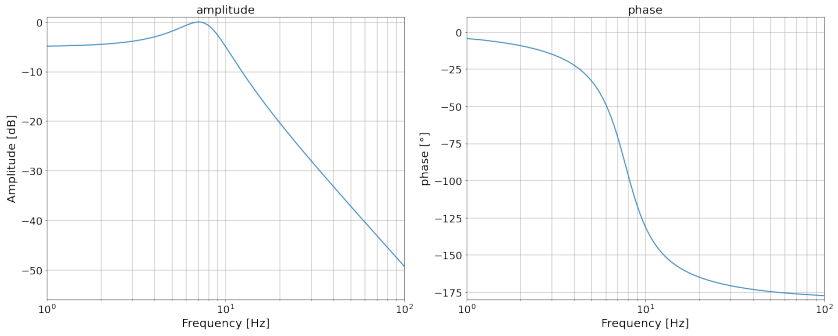


Figure 12: Bodeplot Chebyshev I lowpass. $rp = 5$dB

Chebyshev II
Also known as inverse Chebyshev filter.

- passband
  - flat, no ripples

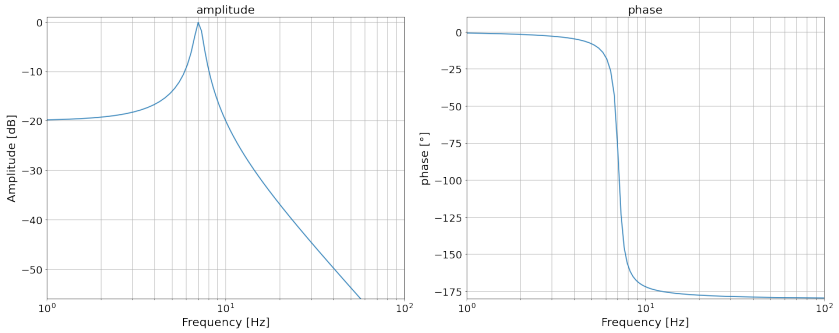


Figure 13: Bodeplot Chebyshev I lowpass. $rp = 20$dB

- @cut-off frequency: attenuation is rs [dB].
- stopband
  - N/2=1 ripple in the stopband
  - attenuation is smaller than or equal rs [dB].
- Trade-off:
  - the lower rs is choosen, the sharper is the magnitude cut-off
  - the lower rs is choosen, the lower is the over all stopband attenuation

E.g.:
Cut-off frequency is 10Hz.
The maximal ripple in the stopband rs must be given in [dB].
To show the mentioned trade-off, two bodelplots are shown. One with a small and one with a bigger rs. The bodeplot is shown in the figures 14 and 15 below.

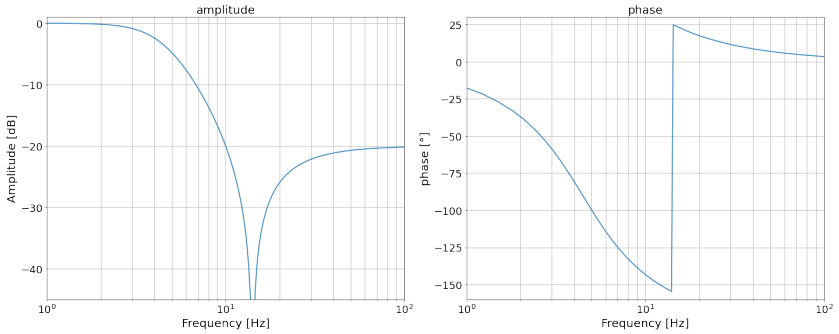


Figure 14: Bodeplot Chebyshev II lowpass. $rs = 20$dB

Bessel

- passband
  - constant group-delay in passband.
  - least sharp magnitude roll-off.
- @cut-off frequency:
  - approx. -1.6 dB attenuation
  - approx. -56 degree phaseshift

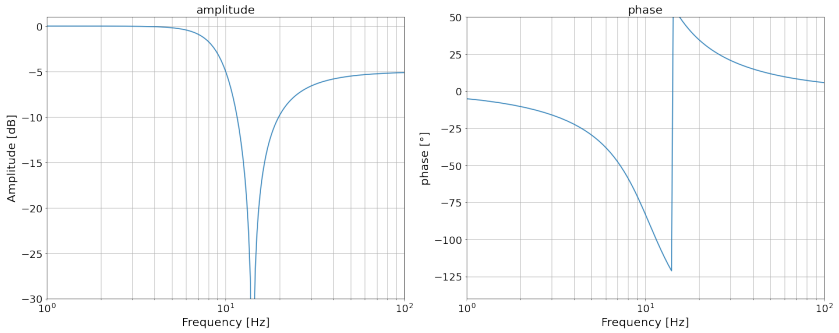


Figure 15: Bodeplot Chebyshev II lowpass. $rs = 5$dB

- stopband
  - monotonic -40dB decline per decade
  - approx. -30dB decline within first decade

E.g.:
Cut-off frequency is 10Hz.
The bodeplot is shown in the figure 16 below.

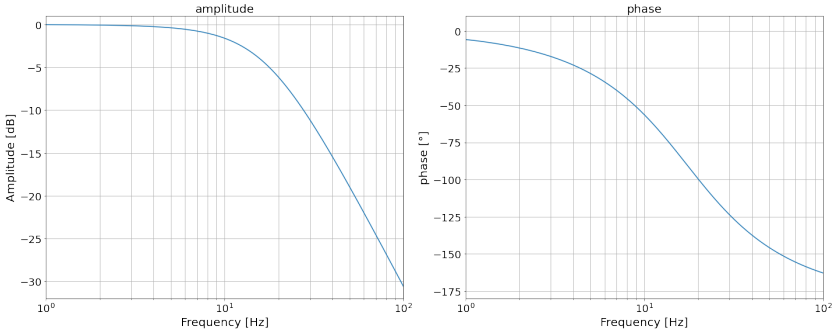


Figure 16: Bodeplot Bessel lowpass.

Implementations:

FiP16	16 Bit Fixed Point Implementation
FiP32	32 Bit Fixed Point Implementation
Float32	32 Bit Floating Point Implementation
Float64	64 Bit Floating Point Implementation

Implementation: FiP16

16 Bit Fixed Point Implementation

Inports Data Type	
In	int16

Outports Data Type	
Out	int16

Implementation: FiP32

32 Bit Fixed Point Implementation

Inports Data Type	
In	int32

Outports Data Type	
Out	int32

Implementation: Float32

32 Bit Floating Point Implementation

Inports Data Type	
In	float32

Outports Data Type	
Out	float32

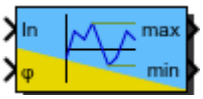
Implementation: Float64

64 Bit Floating Point Implementation

Inports Data Type	
In	float64

Outports Data Type	
Out	float64

Block: MinMaxPeriodic



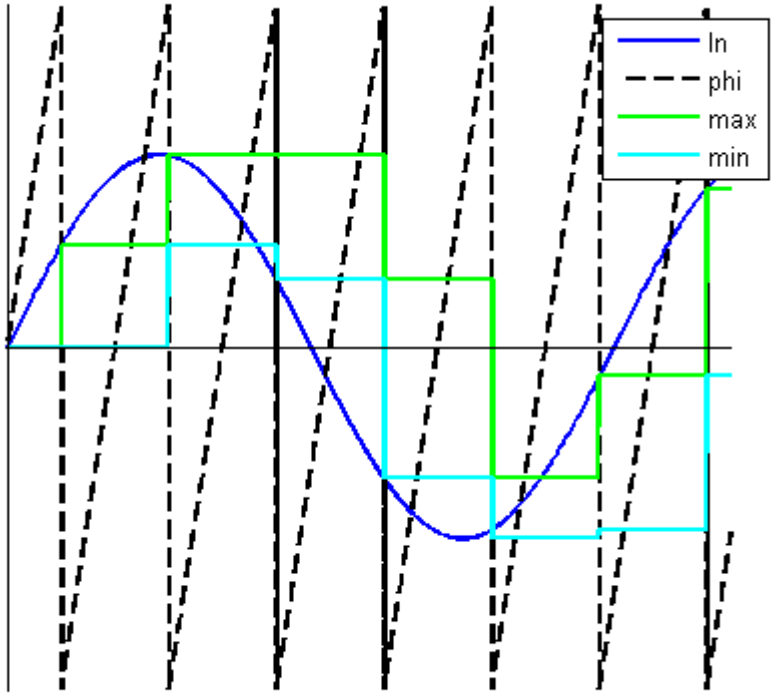
Outputs the minimum and maximum of the input signal over one period of the (angle) signal phi.

Inports	
In	Input signal
phi	Angle signal

Outports	
max	Maximum of input signal
min	Minimum of input signal

Description:

Exemplary signal waveforms:



Implementations:

FiP16	16 Bit Fixed Point Implementation
FiP32	32 Bit Fixed Point Implementation
Float32	32 Bit Floating Point Implementation
Float64	64 Bit Floating Point Implementation

Implementation: FiP16

16 Bit Fixed Point Implementation

Inports Data Type	
In	int16
phi	int16

Outports Data Type	
max	int16
min	int16

Implementation: FiP32

32 Bit Fixed Point Implementation

Inports Data Type	
In	int32
phi	int32

Outports Data Type	
max	int32
min	int32

Implementation: Float32

32 Bit Floating Point Implementation

Inports Data Type	
In	float32
phi	float32

Outports Data Type	
max	float32
min	float32

Implementation: Float64

64 Bit Floating Point Implementation

Inports Data Type	
In	float64
phi	float64

Outports Data Type	
max	float64
min	float64

Verification: MinMaxPeriodic FiP16 CPU TMS320F28335

Date of Test	2026-06-25
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for Filter block MinMaxPeriodic.

Test results						
Time step	1	2	3	4	...	112
CPU cycles	97	97	97	97	...	90
Inputs						
In (DSP)	0	-4552	-8966	-13107	...	0
phi (DSP)	-32768	-30948	-29127	-27307	...	-32768
In	-0	-0.139	-0.274	-0.4	...	0
phi	-1	-0.944	-0.889	-0.833	...	-1
Outputs						
max	0	0	0	0	...	0.9
min	0	0	0	0	...	0.1
Exp. max	0	0	0	0	...	0.9
Exp. min	0	0	0	0	...	0.1
max (DSP)	0	0	0	0	...	29491
min (DSP)	0	0	0	0	...	3277
Exp. max (DSP)	0	0	0	0	...	29491
Exp. min (DSP)	0	0	0	0	...	3277

Test settings	
Tolerance max	±3,0518e-05 (±1 LSB)
Tolerance min	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	90
Max CPU cycles	97
Avg CPU cycles	96

Verification: MinMaxPeriodic FiP16 CPU TM4C123GH6

Date of Test	2026-06-25
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for Filter block MinMaxPeriodic.

Test results						
Time step	1	2	3	4	...	112
CPU cycles	57	53	53	53	...	49
Inputs						
In (DSP)	0	-4552	-8966	-13107	...	0
phi (DSP)	-32768	-30948	-29127	-27307	...	-32768
In	-0	-0.139	-0.274	-0.4	...	0
phi	-1	-0.944	-0.889	-0.833	...	-1
Outputs						
max	0	0	0	0	...	0.9
min	0	0	0	0	...	0.1
Exp. max	0	0	0	0	...	0.9
Exp. min	0	0	0	0	...	0.1
max (DSP)	0	0	0	0	...	29491
min (DSP)	0	0	0	0	...	3277
Exp. max (DSP)	0	0	0	0	...	29491
Exp. min (DSP)	0	0	0	0	...	3277

Test settings	
Tolerance max	±3,0518e-05 (±1 LSB)
Tolerance min	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	49
Max CPU cycles	57
Avg CPU cycles	52

Verification: MinMaxPeriodic FiP16 CPU STM32G474RE

Date of Test	2026-06-25
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for Filter block MinMaxPeriodic.

Test results						
Time step	1	2	3	4	...	112
CPU cycles	91	91	91	91	...	83
Inputs						
In (DSP)	0	-4552	-8966	-13107	...	0
phi (DSP)	-32768	-30948	-29127	-27307	...	-32768
In	-0	-0.139	-0.274	-0.4	...	0
phi	-1	-0.944	-0.889	-0.833	...	-1
Outputs						
max	0	0	0	0	...	0.9
min	0	0	0	0	...	0.1
Exp. max	0	0	0	0	...	0.9
Exp. min	0	0	0	0	...	0.1
max (DSP)	0	0	0	0	...	29491
min (DSP)	0	0	0	0	...	3277
Exp. max (DSP)	0	0	0	0	...	29491
Exp. min (DSP)	0	0	0	0	...	3277

Test settings	
Tolerance max	±3,0518e-05 (±1 LSB)
Tolerance min	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	83
Max CPU cycles	91
Avg CPU cycles	90

Verification: MinMaxPeriodic FiP16 CPU STM32F072RB

Date of Test	2026-06-25
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for Filter block MinMaxPeriodic.

Test results						
Time step	1	2	3	4	...	112
CPU cycles	93	90	90	90	...	80
Inputs						
In (DSP)	0	-4552	-8966	-13107	...	0
phi (DSP)	-32768	-30948	-29127	-27307	...	-32768
In	-0	-0.139	-0.274	-0.4	...	0
phi	-1	-0.944	-0.889	-0.833	...	-1
Outputs						
max	0	0	0	0	...	0.9
min	0	0	0	0	...	0.1
Exp. max	0	0	0	0	...	0.9
Exp. min	0	0	0	0	...	0.1
max (DSP)	0	0	0	0	...	29491
min (DSP)	0	0	0	0	...	3277
Exp. max (DSP)	0	0	0	0	...	29491
Exp. min (DSP)	0	0	0	0	...	3277

Test settings	
Tolerance max	±3,0518e-05 (±1 LSB)
Tolerance min	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	80
Max CPU cycles	155
Avg CPU cycles	91

Verification: MinMaxPeriodic FiP16 CPU PIC32MX170F256

Date of Test	2026-06-25
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for Filter block MinMaxPeriodic.

Test results						
Time step	1	2	3	4	...	112
CPU cycles	60	57	57	57	...	49
Inputs						
In (DSP)	0	-4552	-8966	-13107	...	0
phi (DSP)	-32768	-30948	-29127	-27307	...	-32768
In	-0	-0.139	-0.274	-0.4	...	0
phi	-1	-0.944	-0.889	-0.833	...	-1
Outputs						
max	0	0	0	0	...	0.9
min	0	0	0	0	...	0.1
Exp. max	0	0	0	0	...	0.9
Exp. min	0	0	0	0	...	0.1
max (DSP)	0	0	0	0	...	29491
min (DSP)	0	0	0	0	...	3277
Exp. max (DSP)	0	0	0	0	...	29491
Exp. min (DSP)	0	0	0	0	...	3277

Test settings	
Tolerance max	±3,0518e-05 (±1 LSB)
Tolerance min	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	49
Max CPU cycles	60
Avg CPU cycles	53

Verification: MinMaxPeriodic FiP16 CPU dsPIC33EP256MC502

Date of Test	2026-06-25
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for Filter block MinMaxPeriodic.

Test results						
Time step	1	2	3	4	...	112
CPU cycles	72	66	66	66	...	65
Inputs						
In (DSP)	0	-4552	-8966	-13107	...	0
phi (DSP)	-32768	-30948	-29127	-27307	...	-32768
In	-0	-0.139	-0.274	-0.4	...	0
phi	-1	-0.944	-0.889	-0.833	...	-1
Outputs						
max	0	0	0	0	...	0.9
min	0	0	0	0	...	0.1
Exp. max	0	0	0	0	...	0.9
Exp. min	0	0	0	0	...	0.1
max (DSP)	0	0	0	0	...	29491
min (DSP)	0	0	0	0	...	3277
Exp. max (DSP)	0	0	0	0	...	29491
Exp. min (DSP)	0	0	0	0	...	3277

Test settings	
Tolerance max	±3,0518e-05 (±1 LSB)
Tolerance min	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	64
Max CPU cycles	72
Avg CPU cycles	66

Verification: MinMaxPeriodic FiP16 CPU XMC4800-F144K2048

Date of Test	2026-06-25
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for Filter block MinMaxPeriodic.

Test results						
Time step	1	2	3	4	...	112
CPU cycles	103	88	88	88	...	77
Inputs						
In (DSP)	0	-4552	-8966	-13107	...	0
phi (DSP)	-32768	-30948	-29127	-27307	...	-32768
In	-0	-0.139	-0.274	-0.4	...	0
phi	-1	-0.944	-0.889	-0.833	...	-1
Outputs						
max	0	0	0	0	...	0.9
min	0	0	0	0	...	0.1
Exp. max	0	0	0	0	...	0.9
Exp. min	0	0	0	0	...	0.1
max (DSP)	0	0	0	0	...	29491
min (DSP)	0	0	0	0	...	3277
Exp. max (DSP)	0	0	0	0	...	29491
Exp. min (DSP)	0	0	0	0	...	3277

Test settings	
Tolerance max	±3,0518e-05 (±1 LSB)
Tolerance min	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	77
Max CPU cycles	103
Avg CPU cycles	82

Verification: MinMaxPeriodic FiP16 CPU TMS320F28379D

Date of Test	2026-06-25
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for Filter block MinMaxPeriodic.

Test results						
Time step	1	2	3	4	...	112
CPU cycles	96	97	97	97	...	87
Inputs						
In (DSP)	0	-4552	-8966	-13107	...	0
phi (DSP)	-32768	-30948	-29127	-27307	...	-32768
In	-0	-0.139	-0.274	-0.4	...	0
phi	-1	-0.944	-0.889	-0.833	...	-1
Outputs						
max	0	0	0	0	...	0.9
min	0	0	0	0	...	0.1
Exp. max	0	0	0	0	...	0.9
Exp. min	0	0	0	0	...	0.1
max (DSP)	0	0	0	0	...	29491
min (DSP)	0	0	0	0	...	3277
Exp. max (DSP)	0	0	0	0	...	29491
Exp. min (DSP)	0	0	0	0	...	3277

Test settings	
Tolerance max	±3,0518e-05 (±1 LSB)
Tolerance min	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	87
Max CPU cycles	97
Avg CPU cycles	96

Verification: MinMaxPeriodic FiP32 CPU TMS320F28335

Date of Test	2026-06-25
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for Filter block MinMaxPeriodic.

Test results				
Time step	1	2	...	112
CPU cycles	145	140	...	137
Inputs				
In (DSP)	0	-298325298	...	0
phi (DSP)	-2147483648	-2028179001	...	-2147483648
In	-0	-0.139	...	0
phi	-1	-0.944	...	-1
Outputs				
max	0	0	...	0.9
min	0	0	...	0.1
Exp. max	0	0	...	0.9
Exp. min	0	0	...	0.1
max (DSP)	0	0	...	1932735283
min (DSP)	0	0	...	214748365
Exp. max (DSP)	0	0	...	1932735283
Exp. min (DSP)	0	0	...	214748365

Test settings	
Tolerance max	±4,6566e-10 (±1 LSB)
Tolerance min	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	137
Max CPU cycles	145
Avg CPU cycles	140

Verification: MinMaxPeriodic FiP32 CPU TM4C123GH6

Date of Test	2026-06-25
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for Filter block MinMaxPeriodic.

Test results				
Time step	1	2	...	112
CPU cycles	67	67	...	63
Inputs				
In (DSP)	0	-298325298	...	0
phi (DSP)	-2147483648	-2028179001	...	-2147483648
In	-0	-0.139	...	0
phi	-1	-0.944	...	-1
Outputs				
max	0	0	...	0.9
min	0	0	...	0.1
Exp. max	0	0	...	0.9
Exp. min	0	0	...	0.1
max (DSP)	0	0	...	1932735283
min (DSP)	0	0	...	214748365
Exp. max (DSP)	0	0	...	1932735283
Exp. min (DSP)	0	0	...	214748365

Test settings	
Tolerance max	±4,6566e-10 (±1 LSB)
Tolerance min	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	63
Max CPU cycles	71
Avg CPU cycles	68

Verification: MinMaxPeriodic FiP32 CPU STM32G474RE

Date of Test	2026-06-25
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for Filter block MinMaxPeriodic.

Test results				
Time step	1	2	...	112
CPU cycles	104	104	...	99
Inputs				
In (DSP)	0	-298325298	...	0
phi (DSP)	-2147483648	-2028179001	...	-2147483648
In	-0	-0.139	...	0
phi	-1	-0.944	...	-1
Outputs				
max	0	0	...	0.9
min	0	0	...	0.1
Exp. max	0	0	...	0.9
Exp. min	0	0	...	0.1
max (DSP)	0	0	...	1932735283
min (DSP)	0	0	...	214748365
Exp. max (DSP)	0	0	...	1932735283
Exp. min (DSP)	0	0	...	214748365

Test settings	
Tolerance max	±4,6566e-10 (±1 LSB)
Tolerance min	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	99
Max CPU cycles	104
Avg CPU cycles	103

Verification: MinMaxPeriodic FiP32 CPU STM32F072RB

Date of Test	2026-06-25
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for Filter block MinMaxPeriodic.

Test results				
Time step	1	2	...	112
CPU cycles	109	109	...	113
Inputs				
In (DSP)	0	-298325298	...	0
phi (DSP)	-2147483648	-2028179001	...	-2147483648
In	-0	-0.139	...	0
phi	-1	-0.944	...	-1
Outputs				
max	0	0	...	0.9
min	0	0	...	0.1
Exp. max	0	0	...	0.9
Exp. min	0	0	...	0.1
max (DSP)	0	0	...	1932735283
min (DSP)	0	0	...	214748365
Exp. max (DSP)	0	0	...	1932735283
Exp. min (DSP)	0	0	...	214748365

Test settings	
Tolerance max	±4,6566e-10 (±1 LSB)
Tolerance min	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	109
Max CPU cycles	113
Avg CPU cycles	109

Verification: MinMaxPeriodic FiP32 CPU PIC32MX170F256

Date of Test	2026-06-25
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for Filter block MinMaxPeriodic.

Test results				
Time step	1	2	...	112
CPU cycles	70	64	...	65
Inputs				
In (DSP)	0	-298325298	...	0
phi (DSP)	-2147483648	-2028179001	...	-2147483648
In	-0	-0.139	...	0
phi	-1	-0.944	...	-1
Outputs				
max	0	0	...	0.9
min	0	0	...	0.1
Exp. max	0	0	...	0.9
Exp. min	0	0	...	0.1
max (DSP)	0	0	...	1932735283
min (DSP)	0	0	...	214748365
Exp. max (DSP)	0	0	...	1932735283
Exp. min (DSP)	0	0	...	214748365

Test settings	
Tolerance max	±4,6566e-10 (±1 LSB)
Tolerance min	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	58
Max CPU cycles	70
Avg CPU cycles	60

Verification: MinMaxPeriodic FiP32 CPU dsPIC33EP256MC502

Date of Test	2026-06-25
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for Filter block MinMaxPeriodic.

Test results				
Time step	1	2	...	112
CPU cycles	103	92	...	96
Inputs				
In (DSP)	0	-298325298	...	0
phi (DSP)	-2147483648	-2028179001	...	-2147483648
In	-0	-0.139	...	0
phi	-1	-0.944	...	-1
Outputs				
max	0	0	...	0.9
min	0	0	...	0.1
Exp. max	0	0	...	0.9
Exp. min	0	0	...	0.1
max (DSP)	0	0	...	1932735283
min (DSP)	0	0	...	214748365
Exp. max (DSP)	0	0	...	1932735283
Exp. min (DSP)	0	0	...	214748365

Test settings	
Tolerance max	±4,6566e-10 (±1 LSB)
Tolerance min	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	90
Max CPU cycles	103
Avg CPU cycles	91

Verification: MinMaxPeriodic FiP32 CPU XMC4800-F144K2048

Date of Test	2026-06-25
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for Filter block MinMaxPeriodic.

Test results				
Time step	1	2	...	112
CPU cycles	108	88	...	96
Inputs				
In (DSP)	0	-298325298	...	0
phi (DSP)	-2147483648	-2028179001	...	-2147483648
In	-0	-0.139	...	0
phi	-1	-0.944	...	-1
Outputs				
max	0	0	...	0.9
min	0	0	...	0.1
Exp. max	0	0	...	0.9
Exp. min	0	0	...	0.1
max (DSP)	0	0	...	1932735283
min (DSP)	0	0	...	214748365
Exp. max (DSP)	0	0	...	1932735283
Exp. min (DSP)	0	0	...	214748365

Test settings	
Tolerance max	±4,6566e-10 (±1 LSB)
Tolerance min	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	88
Max CPU cycles	108
Avg CPU cycles	88

Verification: MinMaxPeriodic FiP32 CPU TMS320F28379D

Date of Test	2026-06-25
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for Filter block MinMaxPeriodic.

Test results				
Time step	1	2	...	112
CPU cycles	142	138	...	135
Inputs				
In (DSP)	0	-298325298	...	0
phi (DSP)	-2147483648	-2028179001	...	-2147483648
In	-0	-0.139	...	0
phi	-1	-0.944	...	-1
Outputs				
max	0	0	...	0.9
min	0	0	...	0.1
Exp. max	0	0	...	0.9
Exp. min	0	0	...	0.1
max (DSP)	0	0	...	1932735283
min (DSP)	0	0	...	214748365
Exp. max (DSP)	0	0	...	1932735283
Exp. min (DSP)	0	0	...	214748365

Test settings	
Tolerance max	±4,6566e-10 (±1 LSB)
Tolerance min	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	135
Max CPU cycles	143
Avg CPU cycles	140

Verification: MinMaxPeriodic Float32 CPU TMS320F28335

Date of Test	2026-06-25
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for Filter block MinMaxPeriodic.

Test results				
Time step	1	2	...	112
CPU cycles	81	81	...	82
Inputs				
In (DSP)	-0	-0.139	...	0
phi (DSP)	-3.142	-2.967	...	-3.142
In	-0	-0.139	...	0
phi	-3.142	-2.967	...	-3.142
Outputs				
max	0	0	...	0.9
min	0	0	...	0.1
Exp. max	0	0	...	0.9
Exp. min	0	0	...	0.1
max (DSP)	0	0	...	0.9
min (DSP)	0	0	...	0.1
Exp. max (DSP)	0	0	...	0.9
Exp. min (DSP)	0	0	...	0.1

Test settings	
Tolerance max	±4,6566e-08 (±100 LSB)
Tolerance min	±4,6566e-08 (±100 LSB)

Test statistics	
Min CPU cycles	81
Max CPU cycles	82
Avg CPU cycles	81

Verification: MinMaxPeriodic Float32 CPU TM4C123GH6

Date of Test	2026-06-25
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for Filter block MinMaxPeriodic.

Test results				
Time step	1	2	...	112
CPU cycles	67	61	...	55
Inputs				
In (DSP)	-0	-0.139	...	0
phi (DSP)	-3.142	-2.967	...	-3.142
In	-0	-0.139	...	0
phi	-3.142	-2.967	...	-3.142
Outputs				
max	0	0	...	0.9
min	0	0	...	0.1
Exp. max	0	0	...	0.9
Exp. min	0	0	...	0.1
max (DSP)	0	0	...	0.9
min (DSP)	0	0	...	0.1
Exp. max (DSP)	0	0	...	0.9
Exp. min (DSP)	0	0	...	0.1

Test settings	
Tolerance max	±4,6566e-08 (±100 LSB)
Tolerance min	±4,6566e-08 (±100 LSB)

Test statistics	
Min CPU cycles	55
Max CPU cycles	67
Avg CPU cycles	62

Verification: MinMaxPeriodic Float32 CPU STM32G474RE

Date of Test	2026-06-25
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for Filter block MinMaxPeriodic.

Test results				
Time step	1	2	...	112
CPU cycles	123	123	...	98
Inputs				
In (DSP)	-0	-0.139	...	0
phi (DSP)	-3.142	-2.967	...	-3.142
In	-0	-0.139	...	0
phi	-3.142	-2.967	...	-3.142
Outputs				
max	0	0	...	0.9
min	0	0	...	0.1
Exp. max	0	0	...	0.9
Exp. min	0	0	...	0.1
max (DSP)	0	0	...	0.9
min (DSP)	0	0	...	0.1
Exp. max (DSP)	0	0	...	0.9
Exp. min (DSP)	0	0	...	0.1

Test settings	
Tolerance max	±4,6566e-08 (±100 LSB)
Tolerance min	±4,6566e-08 (±100 LSB)

Test statistics	
Min CPU cycles	98
Max CPU cycles	123
Avg CPU cycles	122

Verification: MinMaxPeriodic Float32 CPU STM32F072RB

Date of Test	2026-06-25
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for Filter block MinMaxPeriodic.

Test results				
Time step	1	2	...	112
CPU cycles	514	591	...	359
Inputs				
In (DSP)	-0	-0.139	...	0
phi (DSP)	-3.142	-2.967	...	-3.142
In	-0	-0.139	...	0
phi	-3.142	-2.967	...	-3.142
Outputs				
max	0	0	...	0.9
min	0	0	...	0.1
Exp. max	0	0	...	0.9
Exp. min	0	0	...	0.1
max (DSP)	0	0	...	0.9
min (DSP)	0	0	...	0.1
Exp. max (DSP)	0	0	...	0.9
Exp. min (DSP)	0	0	...	0.1

Test settings	
Tolerance max	±4,6566e-08 (±100 LSB)
Tolerance min	±4,6566e-08 (±100 LSB)

Test statistics	
Min CPU cycles	359
Max CPU cycles	669
Avg CPU cycles	581

Verification: MinMaxPeriodic Float32 CPU PIC32MX170F256

Date of Test	2026-06-25
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for Filter block MinMaxPeriodic.

Test results				
Time step	1	2	...	112
CPU cycles	252	276	...	216
Inputs				
In (DSP)	-0	-0.139	...	0
phi (DSP)	-3.142	-2.967	...	-3.142
In	-0	-0.139	...	0
phi	-3.142	-2.967	...	-3.142
Outputs				
max	0	0	...	0.9
min	0	0	...	0.1
Exp. max	0	0	...	0.9
Exp. min	0	0	...	0.1
max (DSP)	0	0	...	0.9
min (DSP)	0	0	...	0.1
Exp. max (DSP)	0	0	...	0.9
Exp. min (DSP)	0	0	...	0.1

Test settings	
Tolerance max	±4,6566e-08 (±100 LSB)
Tolerance min	±4,6566e-08 (±100 LSB)

Test statistics	
Min CPU cycles	216
Max CPU cycles	281
Avg CPU cycles	271

Verification: MinMaxPeriodic Float32 CPU dsPIC33EP256MC502

Date of Test	2026-06-25
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for Filter block MinMaxPeriodic.

Test results				
Time step	1	2	...	112
CPU cycles	585	691	...	441
Inputs				
In (DSP)	-0	-0.139	...	0
phi (DSP)	-3.142	-2.967	...	-3.142
In	-0	-0.139	...	0
phi	-3.142	-2.967	...	-3.142
Outputs				
max	0	0	...	0.9
min	0	0	...	0.1
Exp. max	0	0	...	0.9
Exp. min	0	0	...	0.1
max (DSP)	0	0	...	0.9
min (DSP)	0	0	...	0.1
Exp. max (DSP)	0	0	...	0.9
Exp. min (DSP)	0	0	...	0.1

Test settings	
Tolerance max	±4,6566e-08 (±100 LSB)
Tolerance min	±4,6566e-08 (±100 LSB)

Test statistics	
Min CPU cycles	441
Max CPU cycles	703
Avg CPU cycles	666

Verification: MinMaxPeriodic Float32 CPU XMC4800-F144K2048

Date of Test	2026-06-25
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for Filter block MinMaxPeriodic.

Test results				
Time step	1	2	...	112
CPU cycles	119	91	...	90
Inputs				
In (DSP)	-0	-0.139	...	0
phi (DSP)	-3.142	-2.967	...	-3.142
In	-0	-0.139	...	0
phi	-3.142	-2.967	...	-3.142
Outputs				
max	0	0	...	0.9
min	0	0	...	0.1
Exp. max	0	0	...	0.9
Exp. min	0	0	...	0.1
max (DSP)	0	0	...	0.9
min (DSP)	0	0	...	0.1
Exp. max (DSP)	0	0	...	0.9
Exp. min (DSP)	0	0	...	0.1

Test settings	
Tolerance max	±4,6566e-08 (±100 LSB)
Tolerance min	±4,6566e-08 (±100 LSB)

Test statistics	
Min CPU cycles	89
Max CPU cycles	119
Avg CPU cycles	90

Verification: MinMaxPeriodic Float32 CPU TMS320F28379D

Date of Test	2026-06-25
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for Filter block MinMaxPeriodic.

Test results				
Time step	1	2	...	112
CPU cycles	77	77	...	78
Inputs				
In (DSP)	-0	-0.139	...	0
phi (DSP)	-3.142	-2.967	...	-3.142
In	-0	-0.139	...	0
phi	-3.142	-2.967	...	-3.142
Outputs				
max	0	0	...	0.9
min	0	0	...	0.1
Exp. max	0	0	...	0.9
Exp. min	0	0	...	0.1
max (DSP)	0	0	...	0.9
min (DSP)	0	0	...	0.1
Exp. max (DSP)	0	0	...	0.9
Exp. min (DSP)	0	0	...	0.1

Test settings	
Tolerance max	±4,6566e-08 (±100 LSB)
Tolerance min	±4,6566e-08 (±100 LSB)

Test statistics	
Min CPU cycles	77
Max CPU cycles	78
Avg CPU cycles	77

Block: NotchBiQ



Calculates the filter coefficients for a second order notch filter and performs filtering on input signal.
Second order transfer function used:
H(z) = (b0.z^2 + b1.z + b2) / (z^2 + a1.z + a2)

Inports	
In	Input In(k)

Outports	
Out	Output Out(k)

Mask Parameters		
Name	**ID**	**Description**
method	1	Selection between bilinear and matched Z-transform discretization method
fn	2	Notching frequency in Hz
Q	3	Defines a quality factor of the filter
ts_fact	4	Multiplication factor of base sampling time (in integer format)

Description:

Calculation:

$$\mathrm{Out(k)} = \mathrm{In(k)} \cdot \mathrm{H(z)}$$

The transfer function H(z) of the filter is

$$H(z) = \frac{b_0 + b_1 z^{-1} + b_2 z^{-2}}{1 + a_1 z^{-1} + a_2 z^{-2}}$$

with coefficients derived from the transfer function

$$H(s) = \frac{s^2 + \omega_0^2}{s^2 + \frac{\omega_0}{Q} + \omega_0^2}$$

Two methods of discretizing a continuous transfer function are available: bilinear and matching.
Warning: In some cases, the function is very sensitive to the accuracy of the coefficients. Therefore, using a fixed-point implementation can sometimes give inaccurate results.
To illustrate this issue, see step responses in figures 17 and 18 below. Filter settings are $f_n = 50\,\mathrm{Hz}$, $Q = 10$, $f_s = 10\,\mathrm{kHz}$.

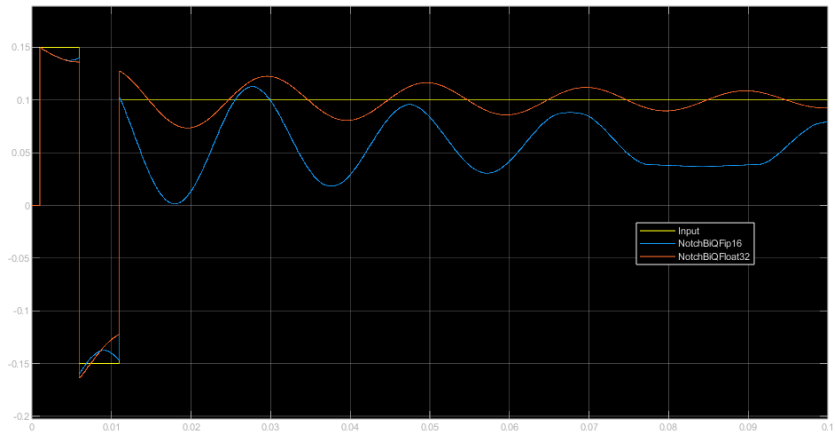


Figure 17: Step response for ts_fact = 1.

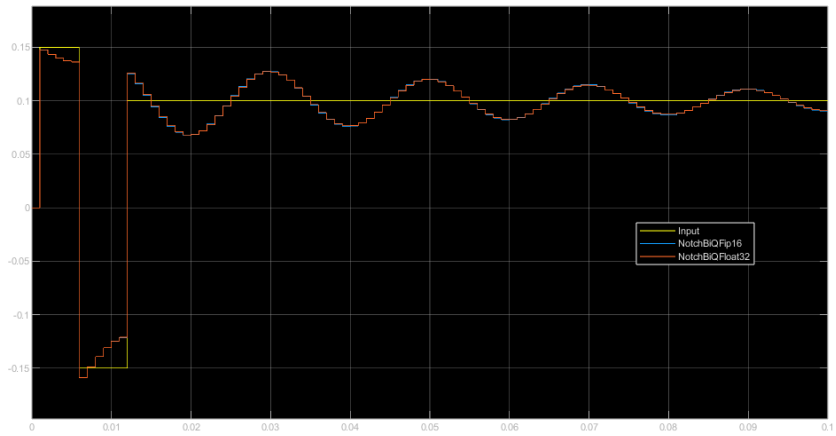


Figure 18: Step response for t_fact = 10.

Implementations:

FiP16	16 Bit Fixed Point Implementation
FiP32	32 Bit Fixed Point Implementation
Float32	32 Bit Floating Point Implementation
Float64	64 Bit Floating Point Implementation

Implementation: FiP16

16 Bit Fixed Point Implementation

Inports Data Type	
In	int16

Outports Data Type	
Out	int16

Implementation: FiP32

32 Bit Fixed Point Implementation

Inports Data Type	
In	int32

Outports Data Type	
Out	int32

Implementation: Float32

32 Bit Floating Point Implementation

Inports Data Type	
In	float32

Outports Data Type	
Out	float32

Implementation: Float64

64 Bit Floating Point Implementation

Inports Data Type	
In	float64

Outports Data Type	
Out	float64

Verification: NotchBiQ FiP16 CPU TM4C123GH6

Date of Test	2026-06-25
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for Filter block NotchBiQ.

Test results						
Time step	1	2	3	4	...	101
CPU cycles	93	93	93	93	...	93
Inputs						
In (DSP)	0	0	0	4915	...	3277
In	0	0	0	0.15	...	0.1
Parameters						
method	bilinear					
fn	50					
Q	25					
ts_fact	1					
Outputs						
Out	0	0	0	0.15	...	0.072
Exp. Out	0	0	0	0.15	...	0.098
Out (DSP)	0	0	0	4911	...	2356
Exp. Out (DSP)	0	0	0	4912	...	3214

Test settings	
Tolerance Out	±2,7466e-02 (±900 LSB)

Test statistics	
Min CPU cycles	93
Max CPU cycles	93
Avg CPU cycles	93

Test case: Conversion test OK

Conversion test for Filter block NotchBiQ.

Test results						
Time step	1	2	3	4	...	10
Mask parameters						
method	bilinear	bilinear	bilinear	bilinear	...	bilinear
fn	10	231.111	452.222	673.333	...	2000
Q	10	20	30	40	...	100
ts_fact	1	1	1	1	...	1
Controller parameters						
b2	32758	32650	32616	32601	...	32613
a1	-32757	-32306	-31308	-29726	...	-20156
a2	32747	32532	32463	32433	...	32458
sfra2	15	15	15	15	...	15
sfrb0	15	15	15	15	...	15
sfrb1	14	14	14	14	...	15
sfrb2	15	15	15	15	...	15
sfra1	14	14	14	14	...	15
b0	32758	32650	32616	32601	...	32613
b1	-32757	-32306	-31308	-29726	...	-20156
Exp. b2	32758	32650	32616	32601	...	32613
Exp. a1	-32757	-32306	-31308	-29726	...	-20156
Exp. a2	32747	32532	32463	32433	...	32458
Exp. sfra2	15	15	15	15	...	15
Exp. sfrb0	15	15	15	15	...	15
Exp. sfrb1	14	14	14	14	...	15
Exp. sfrb2	15	15	15	15	...	15
Exp. sfra1	14	14	14	14	...	15
Exp. b0	32758	32650	32616	32601	...	32613
Exp. b1	-32757	-32306	-31308	-29726	...	-20156

Test settings	
Tolerance b2	±0,0000e+00
Tolerance a1	±0,0000e+00
Tolerance a2	±0,0000e+00
Tolerance sfra2	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance sfrb2	±0,0000e+00
Tolerance sfra1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Filter block NotchBiQ.

Test results						
Time step	1	2	3	4	...	10
Mask parameters						
method	bilinear	bilinear	bilinear	bilinear	...	bilinear
fn	10	231.111	452.222	673.333	...	2000
Q	10	20	30	40	...	100
ts_fact	1	1	1	1	...	1
Controller parameters						
b2	32757	32649	32615	32600	...	32612
a1	-32757	-32306	-31307	-29726	...	-20155
a2	32747	32531	32463	32433	...	32457
sfra2	15	15	15	15	...	15
sfrb0	15	15	15	15	...	15
sfrb1	14	14	14	14	...	15
sfrb2	15	15	15	15	...	15
sfra1	14	14	14	14	...	15
b0	32757	32649	32615	32600	...	32612
b1	-32757	-32306	-31307	-29726	...	-20155
Exp. b2	32758	32650	32616	32601	...	32613
Exp. a1	-32757	-32306	-31308	-29726	...	-20156
Exp. a2	32747	32532	32463	32433	...	32458
Exp. sfra2	15	15	15	15	...	15
Exp. sfrb0	15	15	15	15	...	15
Exp. sfrb1	14	14	14	14	...	15
Exp. sfrb2	15	15	15	15	...	15
Exp. sfra1	14	14	14	14	...	15
Exp. b0	32758	32650	32616	32601	...	32613
Exp. b1	-32757	-32306	-31308	-29726	...	-20156

Test settings	
Tolerance b2	±1,0000e+00
Tolerance a1	±1,0000e+00
Tolerance a2	±1,0000e+00
Tolerance sfra2	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance sfrb2	±0,0000e+00
Tolerance sfra1	±0,0000e+00
Tolerance b0	±1,0000e+00
Tolerance b1	±1,0000e+00

Test statistics	
Min CPU cycles	3267
Max CPU cycles	3843
Avg CPU cycles	3727

Verification: NotchBiQ FiP16 CPU TMS320F28335

Date of Test	2026-06-25
Target controller	TMS320F28335

Test case: Inport test — OK

Inport test for Filter block NotchBiQ.

Test results						
Time step	1	2	3	4	...	101
CPU cycles	116	116	116	116	...	116
Inputs						
In (DSP)	0	0	0	4915	...	3277
In	0	0	0	0.15	...	0.1
Parameters						
method	bilinear					
fn	50					
Q	25					
ts_fact	1					
Outputs						
Out	0	0	0	0.15	...	0.072
Exp. Out	0	0	0	0.15	...	0.098
Out (DSP)	0	0	0	4911	...	2356
Exp. Out (DSP)	0	0	0	4912	...	3214

Test settings	
Tolerance Out	±2,7466e-02 (±900 LSB)

Test statistics	
Min CPU cycles	116
Max CPU cycles	116
Avg CPU cycles	116

Test case: Conversion test — OK

Conversion test for Filter block NotchBiQ.

Test results						
Time step	1	2	3	4	...	10
Mask parameters						
method	bilinear	bilinear	bilinear	bilinear	...	bilinear
fn	10	231.111	452.222	673.333	...	2000
Q	10	20	30	40	...	100
ts_fact	1	1	1	1	...	1
Controller parameters						
b2	32758	32650	32616	32601	...	32613
a1	-32757	-32306	-31308	-29726	...	-20156
a2	32747	32532	32463	32433	...	32458
sfra2	15	15	15	15	...	15
sfrb0	15	15	15	15	...	15
sfrb1	14	14	14	14	...	15
sfrb2	15	15	15	15	...	15
sfra1	14	14	14	14	...	15
b0	32758	32650	32616	32601	...	32613
b1	-32757	-32306	-31308	-29726	...	-20156
Exp. b2	32758	32650	32616	32601	...	32613
Exp. a1	-32757	-32306	-31308	-29726	...	-20156
Exp. a2	32747	32532	32463	32433	...	32458
Exp. sfra2	15	15	15	15	...	15
Exp. sfrb0	15	15	15	15	...	15
Exp. sfrb1	14	14	14	14	...	15
Exp. sfrb2	15	15	15	15	...	15
Exp. sfra1	14	14	14	14	...	15
Exp. b0	32758	32650	32616	32601	...	32613
Exp. b1	-32757	-32306	-31308	-29726	...	-20156

Test settings	
Tolerance b2	±0,0000e+00
Tolerance a1	±0,0000e+00
Tolerance a2	±0,0000e+00
Tolerance sfra2	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance sfrb2	±0,0000e+00
Tolerance sfra1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Filter block NotchBiQ.

Test results						
Time step	1	2	3	4	...	10
Mask parameters						
method	bilinear	bilinear	bilinear	bilinear	...	bilinear
fn	10	231.111	452.222	673.333	...	2000
Q	10	20	30	40	...	100
ts_fact	1	1	1	1	...	1
Controller parameters						
b2	32757	32649	32615	32600	...	32612
a1	-32757	-32306	-31307	-29726	...	-20155
a2	32747	32531	32463	32433	...	32457
sfra2	15	15	15	15	...	15
sfrb0	15	15	15	15	...	15
sfrb1	14	14	14	14	...	15
sfrb2	15	15	15	15	...	15
sfra1	14	14	14	14	...	15
b0	32757	32649	32615	32600	...	32612
b1	-32757	-32306	-31307	-29726	...	-20155
Exp. b2	32758	32650	32616	32601	...	32613
Exp. a1	-32757	-32306	-31308	-29726	...	-20156
Exp. a2	32747	32532	32463	32433	...	32458
Exp. sfra2	15	15	15	15	...	15
Exp. sfrb0	15	15	15	15	...	15
Exp. sfrb1	14	14	14	14	...	15
Exp. sfrb2	15	15	15	15	...	15
Exp. sfra1	14	14	14	14	...	15
Exp. b0	32758	32650	32616	32601	...	32613
Exp. b1	-32757	-32306	-31308	-29726	...	-20156

Test settings	
Tolerance b2	±1,0000e+00
Tolerance a1	±1,0000e+00
Tolerance a2	±1,0000e+00
Tolerance sfra2	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance sfrb2	±0,0000e+00
Tolerance sfra1	±0,0000e+00
Tolerance b0	±1,0000e+00
Tolerance b1	±1,0000e+00

Test statistics	
Min CPU cycles	7494
Max CPU cycles	8524
Avg CPU cycles	8318

Verification: NotchBiQ FiP16 CPU TMS320F28379D

Date of Test	2026-06-25
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for Filter block NotchBiQ.

Test results						
Time step	1	2	3	4	...	101
CPU cycles	113	113	113	113	...	113
Inputs						
In (DSP)	0	0	0	4915	...	3277
In	0	0	0	0.15	...	0.1
Parameters						
method	bilinear					
fn	50					
Q	25					
ts_fact	1					
Outputs						
Out	0	0	0	0.15	...	0.072
Exp. Out	0	0	0	0.15	...	0.098
Out (DSP)	0	0	0	4911	...	2356
Exp. Out (DSP)	0	0	0	4912	...	3214

Test settings	
Tolerance Out	±2,7466e-02 (±900 LSB)

Test statistics	
Min CPU cycles	113
Max CPU cycles	113
Avg CPU cycles	113

Test case: Conversion test OK

Conversion test for Filter block NotchBiQ.

Test results						
Time step	1	2	3	4	...	10
Mask parameters						
method	bilinear	bilinear	bilinear	bilinear	...	bilinear
fn	10	231.111	452.222	673.333	...	2000
Q	10	20	30	40	...	100
ts_fact	1	1	1	1	...	1
Controller parameters						
b2	32758	32650	32616	32601	...	32613
a1	-32757	-32306	-31308	-29726	...	-20156
a2	32747	32532	32463	32433	...	32458
sfra2	15	15	15	15	...	15
sfrb0	15	15	15	15	...	15
sfrb1	14	14	14	14	...	15
sfrb2	15	15	15	15	...	15
sfra1	14	14	14	14	...	15
b0	32758	32650	32616	32601	...	32613
b1	-32757	-32306	-31308	-29726	...	-20156
Exp. b2	32758	32650	32616	32601	...	32613
Exp. a1	-32757	-32306	-31308	-29726	...	-20156
Exp. a2	32747	32532	32463	32433	...	32458
Exp. sfra2	15	15	15	15	...	15
Exp. sfrb0	15	15	15	15	...	15
Exp. sfrb1	14	14	14	14	...	15
Exp. sfrb2	15	15	15	15	...	15
Exp. sfra1	14	14	14	14	...	15
Exp. b0	32758	32650	32616	32601	...	32613
Exp. b1	-32757	-32306	-31308	-29726	...	-20156

Test settings	
Tolerance b2	±0,0000e+00
Tolerance a1	±0,0000e+00
Tolerance a2	±0,0000e+00
Tolerance sfra2	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance sfrb2	±0,0000e+00
Tolerance sfra1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Filter block NotchBiQ.

Test results						
Time step	1	2	3	4	...	10
Mask parameters						
method	bilinear	bilinear	bilinear	bilinear	...	bilinear
fn	10	231.111	452.222	673.333	...	2000
Q	10	20	30	40	...	100
ts_fact	1	1	1	1	...	1
Controller parameters						
b2	32757	32649	32615	32600	...	32612
a1	-32757	-32306	-31307	-29726	...	-20155
a2	32747	32531	32463	32433	...	32457
sfra2	15	15	15	15	...	15
sfrb0	15	15	15	15	...	15
sfrb1	14	14	14	14	...	15
sfrb2	15	15	15	15	...	15
sfra1	14	14	14	14	...	15
b0	32757	32649	32615	32600	...	32612
b1	-32757	-32306	-31307	-29726	...	-20155
Exp. b2	32758	32650	32616	32601	...	32613
Exp. a1	-32757	-32306	-31308	-29726	...	-20156
Exp. a2	32747	32532	32463	32433	...	32458
Exp. sfra2	15	15	15	15	...	15
Exp. sfrb0	15	15	15	15	...	15
Exp. sfrb1	14	14	14	14	...	15
Exp. sfrb2	15	15	15	15	...	15
Exp. sfra1	14	14	14	14	...	15
Exp. b0	32758	32650	32616	32601	...	32613
Exp. b1	-32757	-32306	-31308	-29726	...	-20156

Test settings	
Tolerance b2	±1,0000e+00
Tolerance a1	±1,0000e+00
Tolerance a2	±1,0000e+00
Tolerance sfra2	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance sfrb2	±0,0000e+00
Tolerance sfra1	±0,0000e+00
Tolerance b0	±1,0000e+00
Tolerance b1	±1,0000e+00

Test statistics	
Min CPU cycles	5706
Max CPU cycles	6498
Avg CPU cycles	6339

Verification: NotchBiQ FiP16 CPU dsPIC33EP256MC502

Date of Test	2026-06-25
Target controller	dsPIC33EP256MC502

Test case: Inport test

OK

Inport test for Filter block NotchBiQ.

Test results						
Time step	1	2	3	4	...	101
CPU cycles	144	144	144	144	...	144
Inputs						
In (DSP)	0	0	0	4915	...	3277
In	0	0	0	0.15	...	0.1
Parameters						
method	bilinear					
fn	50					
Q	25					
ts_fact	1					
Outputs						
Out	0	0	0	0.15	...	0.072
Exp. Out	0	0	0	0.15	...	0.098
Out (DSP)	0	0	0	4911	...	2356
Exp. Out (DSP)	0	0	0	4912	...	3214

Test settings	
Tolerance Out	±2,7466e-02 (±900 LSB)

Test statistics	
Min CPU cycles	144
Max CPU cycles	144
Avg CPU cycles	144

Test case: Conversion test

OK

Conversion test for Filter block NotchBiQ.

Test results						
Time step	1	2	3	4	...	10
Mask parameters						
method	bilinear	bilinear	bilinear	bilinear	...	bilinear
fn	10	231.111	452.222	673.333	...	2000
Q	10	20	30	40	...	100
ts_fact	1	1	1	1	...	1
Controller parameters						
b2	32758	32650	32616	32601	...	32613
a1	-32757	-32306	-31308	-29726	...	-20156
a2	32747	32532	32463	32433	...	32458
sfra2	15	15	15	15	...	15
sfrb0	15	15	15	15	...	15
sfrb1	14	14	14	14	...	15
sfrb2	15	15	15	15	...	15
sfra1	14	14	14	14	...	15
b0	32758	32650	32616	32601	...	32613
b1	-32757	-32306	-31308	-29726	...	-20156
Exp. b2	32758	32650	32616	32601	...	32613
Exp. a1	-32757	-32306	-31308	-29726	...	-20156
Exp. a2	32747	32532	32463	32433	...	32458
Exp. sfra2	15	15	15	15	...	15
Exp. sfrb0	15	15	15	15	...	15
Exp. sfrb1	14	14	14	14	...	15
Exp. sfrb2	15	15	15	15	...	15
Exp. sfra1	14	14	14	14	...	15
Exp. b0	32758	32650	32616	32601	...	32613
Exp. b1	-32757	-32306	-31308	-29726	...	-20156

Test settings	
Tolerance b2	±0,0000e+00
Tolerance a1	±0,0000e+00
Tolerance a2	±0,0000e+00
Tolerance sfra2	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance sfrb2	±0,0000e+00
Tolerance sfra1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Filter block NotchBiQ.

Test results						
Time step	1	2	3	4	...	10
Mask parameters						
method	bilinear	bilinear	bilinear	bilinear	...	bilinear
fn	10	231.111	452.222	673.333	...	2000
Q	10	20	30	40	...	100
ts_fact	1	1	1	1	...	1
Controller parameters						
b2	32757	32649	32615	32600	...	32612
a1	-32757	-32306	-31307	-29726	...	-20155
a2	32747	32531	32463	32433	...	32457
sfra2	15	15	15	15	...	15
sfrb0	15	15	15	15	...	15
sfrb1	14	14	14	14	...	15
sfrb2	15	15	15	15	...	15
sfra1	14	14	14	14	...	15
b0	32757	32649	32615	32600	...	32612
b1	-32757	-32306	-31307	-29726	...	-20155
Exp. b2	32758	32650	32616	32601	...	32613
Exp. a1	-32757	-32306	-31308	-29726	...	-20156
Exp. a2	32747	32532	32463	32433	...	32458
Exp. sfra2	15	15	15	15	...	15
Exp. sfrb0	15	15	15	15	...	15
Exp. sfrb1	14	14	14	14	...	15
Exp. sfrb2	15	15	15	15	...	15
Exp. sfra1	14	14	14	14	...	15
Exp. b0	32758	32650	32616	32601	...	32613
Exp. b1	-32757	-32306	-31308	-29726	...	-20156

Test settings	
Tolerance b2	±1,0000e+00
Tolerance a1	±1,0000e+00
Tolerance a2	±1,0000e+00
Tolerance sfra2	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance sfrb2	±0,0000e+00
Tolerance sfra1	±0,0000e+00
Tolerance b0	±1,0000e+00
Tolerance b1	±1,0000e+00

Test statistics	
Min CPU cycles	26082
Max CPU cycles	30598
Avg CPU cycles	29068

Verification: NotchBiQ FiP16 CPU STM32F072RB

Date of Test	2026-06-25
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for Filter block NotchBiQ.

Test results						
Time step	1	2	3	4	...	101
CPU cycles	133	133	133	133	...	133
Inputs						
In (DSP)	0	0	0	4915	...	3277
In	0	0	0	0.15	...	0.1
Parameters						
method	bilinear					
fn	50					
Q	25					
ts_fact	1					
Outputs						
Out	0	0	0	0.15	...	0.072
Exp. Out	0	0	0	0.15	...	0.098
Out (DSP)	0	0	0	4911	...	2356
Exp. Out (DSP)	0	0	0	4912	...	3214

Test settings	
Tolerance Out	±2,7466e-02 (±900 LSB)

Test statistics	
Min CPU cycles	133
Max CPU cycles	133
Avg CPU cycles	133

Test case: Conversion test OK

Conversion test for Filter block NotchBiQ.

Test results						
Time step	1	2	3	4	...	10
Mask parameters						
method	bilinear	bilinear	bilinear	bilinear	...	bilinear
fn	10	231.111	452.222	673.333	...	2000
Q	10	20	30	40	...	100
ts_fact	1	1	1	1	...	1
Controller parameters						
b2	32758	32650	32616	32601	...	32613
a1	-32757	-32306	-31308	-29726	...	-20156
a2	32747	32532	32463	32433	...	32458
sfra2	15	15	15	15	...	15
sfrb0	15	15	15	15	...	15
sfrb1	14	14	14	14	...	15
sfrb2	15	15	15	15	...	15
sfra1	14	14	14	14	...	15
b0	32758	32650	32616	32601	...	32613
b1	-32757	-32306	-31308	-29726	...	-20156
Exp. b2	32758	32650	32616	32601	...	32613
Exp. a1	-32757	-32306	-31308	-29726	...	-20156
Exp. a2	32747	32532	32463	32433	...	32458
Exp. sfra2	15	15	15	15	...	15
Exp. sfrb0	15	15	15	15	...	15
Exp. sfrb1	14	14	14	14	...	15
Exp. sfrb2	15	15	15	15	...	15
Exp. sfra1	14	14	14	14	...	15
Exp. b0	32758	32650	32616	32601	...	32613
Exp. b1	-32757	-32306	-31308	-29726	...	-20156

Test settings	
Tolerance b2	±0,0000e+00
Tolerance a1	±0,0000e+00
Tolerance a2	±0,0000e+00
Tolerance sfra2	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance sfrb2	±0,0000e+00
Tolerance sfra1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Filter block NotchBiQ.

Test results						
Time step	1	2	3	4	...	10
Mask parameters						
method	bilinear	bilinear	bilinear	bilinear	...	bilinear
fn	10	231.111	452.222	673.333	...	2000
Q	10	20	30	40	...	100
ts_fact	1	1	1	1	...	1
Controller parameters						
b2	32757	32649	32615	32600	...	32612
a1	-32757	-32306	-31307	-29726	...	-20155
a2	32747	32531	32463	32433	...	32457
sfra2	15	15	15	15	...	15
sfrb0	15	15	15	15	...	15
sfrb1	14	14	14	14	...	15
sfrb2	15	15	15	15	...	15
sfra1	14	14	14	14	...	15
b0	32757	32649	32615	32600	...	32612
b1	-32757	-32306	-31307	-29726	...	-20155
Exp. b2	32758	32650	32616	32601	...	32613
Exp. a1	-32757	-32306	-31308	-29726	...	-20156
Exp. a2	32747	32532	32463	32433	...	32458
Exp. sfra2	15	15	15	15	...	15
Exp. sfrb0	15	15	15	15	...	15
Exp. sfrb1	14	14	14	14	...	15
Exp. sfrb2	15	15	15	15	...	15
Exp. sfra1	14	14	14	14	...	15
Exp. b0	32758	32650	32616	32601	...	32613
Exp. b1	-32757	-32306	-31308	-29726	...	-20156

Test settings	
Tolerance b2	±1,0000e+00
Tolerance a1	±1,0000e+00
Tolerance a2	±1,0000e+00
Tolerance sfra2	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance sfrb2	±0,0000e+00
Tolerance sfra1	±0,0000e+00
Tolerance b0	±1,0000e+00
Tolerance b1	±1,0000e+00

Test statistics	
Min CPU cycles	20698
Max CPU cycles	22002
Avg CPU cycles	21690

Verification: NotchBiQ FiP16 CPU STM32G474RE

Date of Test	2026-06-25
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for Filter block NotchBiQ.

Test results						
Time step	1	2	3	4	...	101
CPU cycles	147	147	147	147	...	147
Inputs						
In (DSP)	0	0	0	4915	...	3277
In	0	0	0	0.15	...	0.1
Parameters						
method	bilinear					
fn	50					
Q	25					
ts_fact	1					
Outputs						
Out	0	0	0	0.15	...	0.072
Exp. Out	0	0	0	0.15	...	0.098
Out (DSP)	0	0	0	4911	...	2356
Exp. Out (DSP)	0	0	0	4912	...	3214

Test settings	
Tolerance Out	±2,7466e-02 (±900 LSB)

Test statistics	
Min CPU cycles	147
Max CPU cycles	206
Avg CPU cycles	147

Test case: Conversion test OK

Conversion test for Filter block NotchBiQ.

Test results						
Time step	1	2	3	4	...	10
Mask parameters						
method	bilinear	bilinear	bilinear	bilinear	...	bilinear
fn	10	231.111	452.222	673.333	...	2000
Q	10	20	30	40	...	100
ts_fact	1	1	1	1	...	1
Controller parameters						
b2	32758	32650	32616	32601	...	32613
a1	-32757	-32306	-31308	-29726	...	-20156
a2	32747	32532	32463	32433	...	32458
sfra2	15	15	15	15	...	15
sfrb0	15	15	15	15	...	15
sfrb1	14	14	14	14	...	15
sfrb2	15	15	15	15	...	15
sfra1	14	14	14	14	...	15
b0	32758	32650	32616	32601	...	32613
b1	-32757	-32306	-31308	-29726	...	-20156
Exp. b2	32758	32650	32616	32601	...	32613
Exp. a1	-32757	-32306	-31308	-29726	...	-20156
Exp. a2	32747	32532	32463	32433	...	32458
Exp. sfra2	15	15	15	15	...	15
Exp. sfrb0	15	15	15	15	...	15
Exp. sfrb1	14	14	14	14	...	15
Exp. sfrb2	15	15	15	15	...	15
Exp. sfra1	14	14	14	14	...	15
Exp. b0	32758	32650	32616	32601	...	32613
Exp. b1	-32757	-32306	-31308	-29726	...	-20156

Test settings	
Tolerance b2	±0,0000e+00
Tolerance a1	±0,0000e+00
Tolerance a2	±0,0000e+00
Tolerance sfra2	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance sfrb2	±0,0000e+00
Tolerance sfra1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Filter block NotchBiQ.

Test results						
Time step	1	2	3	4	...	10
Mask parameters						
method	bilinear	bilinear	bilinear	bilinear	...	bilinear
fn	10	231.111	452.222	673.333	...	2000
Q	10	20	30	40	...	100
ts_fact	1	1	1	1	...	1
Controller parameters						
b2	32757	32649	32615	32600	...	32612
a1	-32757	-32306	-31307	-29726	...	-20155
a2	32747	32531	32463	32433	...	32457
sfra2	15	15	15	15	...	15
sfrb0	15	15	15	15	...	15
sfrb1	14	14	14	14	...	15
sfrb2	15	15	15	15	...	15
sfra1	14	14	14	14	...	15
b0	32757	32649	32615	32600	...	32612
b1	-32757	-32306	-31307	-29726	...	-20155
Exp. b2	32758	32650	32616	32601	...	32613
Exp. a1	-32757	-32306	-31308	-29726	...	-20156
Exp. a2	32747	32532	32463	32433	...	32458
Exp. sfra2	15	15	15	15	...	15
Exp. sfrb0	15	15	15	15	...	15
Exp. sfrb1	14	14	14	14	...	15
Exp. sfrb2	15	15	15	15	...	15
Exp. sfra1	14	14	14	14	...	15
Exp. b0	32758	32650	32616	32601	...	32613
Exp. b1	-32757	-32306	-31308	-29726	...	-20156

Test settings	
Tolerance b2	±1,0000e+00
Tolerance a1	±1,0000e+00
Tolerance a2	±1,0000e+00
Tolerance sfra2	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance sfrb2	±0,0000e+00
Tolerance sfra1	±0,0000e+00
Tolerance b0	±1,0000e+00
Tolerance b1	±1,0000e+00

Test statistics	
Min CPU cycles	2887
Max CPU cycles	3139
Avg CPU cycles	3088

Verification: NotchBiQ FiP16 CPU XMC4800-F144K2048

Date of Test	2026-06-25
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for Filter block NotchBiQ.

Test results						
Time step	1	2	3	4	...	101
CPU cycles	153	127	127	127	...	127
Inputs						
In (DSP)	0	0	0	4915	...	3277
In	0	0	0	0.15	...	0.1
Parameters						
method	bilinear					
fn	50					
Q	25					
ts_fact	1					
Outputs						
Out	0	0	0	0.15	...	0.072
Exp. Out	0	0	0	0.15	...	0.098
Out (DSP)	0	0	0	4911	...	2356
Exp. Out (DSP)	0	0	0	4912	...	3214

Test settings	
Tolerance Out	±2,7466e-02 (±900 LSB)

Test statistics	
Min CPU cycles	127
Max CPU cycles	153
Avg CPU cycles	127

Test case: Conversion test OK

Conversion test for Filter block NotchBiQ.

Test results						
Time step	1	2	3	4	...	10
Mask parameters						
method	bilinear	bilinear	bilinear	bilinear	...	bilinear
fn	10	231.111	452.222	673.333	...	2000
Q	10	20	30	40	...	100
ts_fact	1	1	1	1	...	1
Controller parameters						
b2	32758	32650	32616	32601	...	32613
a1	-32757	-32306	-31308	-29726	...	-20156
a2	32747	32532	32463	32433	...	32458
sfra2	15	15	15	15	...	15
sfrb0	15	15	15	15	...	15
sfrb1	14	14	14	14	...	15
sfrb2	15	15	15	15	...	15
sfra1	14	14	14	14	...	15
b0	32758	32650	32616	32601	...	32613
b1	-32757	-32306	-31308	-29726	...	-20156
Exp. b2	32758	32650	32616	32601	...	32613
Exp. a1	-32757	-32306	-31308	-29726	...	-20156
Exp. a2	32747	32532	32463	32433	...	32458
Exp. sfra2	15	15	15	15	...	15
Exp. sfrb0	15	15	15	15	...	15
Exp. sfrb1	14	14	14	14	...	15
Exp. sfrb2	15	15	15	15	...	15
Exp. sfra1	14	14	14	14	...	15
Exp. b0	32758	32650	32616	32601	...	32613
Exp. b1	-32757	-32306	-31308	-29726	...	-20156

Test settings	
Tolerance b2	±0,0000e+00
Tolerance a1	±0,0000e+00
Tolerance a2	±0,0000e+00
Tolerance sfra2	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance sfrb2	±0,0000e+00
Tolerance sfra1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Filter block NotchBiQ.

Test results						
Time step	1	2	3	4	...	10
Mask parameters						
method	bilinear	bilinear	bilinear	bilinear	...	bilinear
fn	10	231.111	452.222	673.333	...	2000
Q	10	20	30	40	...	100
ts_fact	1	1	1	1	...	1
Controller parameters						
b2	32757	32649	32615	32600	...	32612
a1	-32757	-32306	-31307	-29726	...	-20155
a2	32747	32531	32463	32433	...	32457
sfra2	15	15	15	15	...	15
sfrb0	15	15	15	15	...	15
sfrb1	14	14	14	14	...	15
sfrb2	15	15	15	15	...	15
sfra1	14	14	14	14	...	15
b0	32757	32649	32615	32600	...	32612
b1	-32757	-32306	-31307	-29726	...	-20155
Exp. b2	32758	32650	32616	32601	...	32613
Exp. a1	-32757	-32306	-31308	-29726	...	-20156
Exp. a2	32747	32532	32463	32433	...	32458
Exp. sfra2	15	15	15	15	...	15
Exp. sfrb0	15	15	15	15	...	15
Exp. sfrb1	14	14	14	14	...	15
Exp. sfrb2	15	15	15	15	...	15
Exp. sfra1	14	14	14	14	...	15
Exp. b0	32758	32650	32616	32601	...	32613
Exp. b1	-32757	-32306	-31308	-29726	...	-20156

Test settings	
Tolerance b2	±1,0000e+00
Tolerance a1	±1,0000e+00
Tolerance a2	±1,0000e+00
Tolerance sfra2	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance sfrb2	±0,0000e+00
Tolerance sfra1	±0,0000e+00
Tolerance b0	±1,0000e+00
Tolerance b1	±1,0000e+00

Test statistics	
Min CPU cycles	2543
Max CPU cycles	3059
Avg CPU cycles	2765

Verification: NotchBiQ FiP16 CPU PIC32MX170F256

Date of Test	2026-06-25
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for Filter block NotchBiQ.

Test results						
Time step	1	2	3	4	...	101
CPU cycles	90	90	90	90	...	90
Inputs						
In (DSP)	0	0	0	4915	...	3277
In	0	0	0	0.15	...	0.1
Parameters						
method	bilinear					
fn	50					
Q	25					
ts_fact	1					
Outputs						
Out	0	0	0	0.15	...	0.072
Exp. Out	0	0	0	0.15	...	0.098
Out (DSP)	0	0	0	4911	...	2356
Exp. Out (DSP)	0	0	0	4912	...	3214

Test settings	
Tolerance Out	±2,7466e-02 (±900 LSB)

Test statistics	
Min CPU cycles	90
Max CPU cycles	90
Avg CPU cycles	90

Test case: Conversion test OK

Conversion test for Filter block NotchBiQ.

Test results						
Time step	1	2	3	4	...	10
Mask parameters						
method	bilinear	bilinear	bilinear	bilinear	...	bilinear
fn	10	231.111	452.222	673.333	...	2000
Q	10	20	30	40	...	100
ts_fact	1	1	1	1	...	1
Controller parameters						
b2	32758	32650	32616	32601	...	32613
a1	-32757	-32306	-31308	-29726	...	-20156
a2	32747	32532	32463	32433	...	32458
sfra2	15	15	15	15	...	15
sfrb0	15	15	15	15	...	15
sfrb1	14	14	14	14	...	15
sfrb2	15	15	15	15	...	15
sfra1	14	14	14	14	...	15
b0	32758	32650	32616	32601	...	32613
b1	-32757	-32306	-31308	-29726	...	-20156
Exp. b2	32758	32650	32616	32601	...	32613
Exp. a1	-32757	-32306	-31308	-29726	...	-20156
Exp. a2	32747	32532	32463	32433	...	32458
Exp. sfra2	15	15	15	15	...	15
Exp. sfrb0	15	15	15	15	...	15
Exp. sfrb1	14	14	14	14	...	15
Exp. sfrb2	15	15	15	15	...	15
Exp. sfra1	14	14	14	14	...	15
Exp. b0	32758	32650	32616	32601	...	32613
Exp. b1	-32757	-32306	-31308	-29726	...	-20156

Test settings	
Tolerance b2	±0,0000e+00
Tolerance a1	±0,0000e+00
Tolerance a2	±0,0000e+00
Tolerance sfra2	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance sfrb2	±0,0000e+00
Tolerance sfra1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Filter block NotchBiQ.

Test results						
Time step	1	2	3	4	...	10
Mask parameters						
method	bilinear	bilinear	bilinear	bilinear	...	bilinear
fn	10	231.111	452.222	673.333	...	2000
Q	10	20	30	40	...	100
ts_fact	1	1	1	1	...	1
Controller parameters						
b2	32757	32649	32615	32600	...	32612
a1	-32757	-32306	-31307	-29726	...	-20155
a2	32747	32531	32463	32433	...	32457
sfra2	15	15	15	15	...	15
sfrb0	15	15	15	15	...	15
sfrb1	14	14	14	14	...	15
sfrb2	15	15	15	15	...	15
sfra1	14	14	14	14	...	15
b0	32757	32649	32615	32600	...	32612
b1	-32757	-32306	-31307	-29726	...	-20155
Exp. b2	32758	32650	32616	32601	...	32613
Exp. a1	-32757	-32306	-31308	-29726	...	-20156
Exp. a2	32747	32532	32463	32433	...	32458
Exp. sfra2	15	15	15	15	...	15
Exp. sfrb0	15	15	15	15	...	15
Exp. sfrb1	14	14	14	14	...	15
Exp. sfrb2	15	15	15	15	...	15
Exp. sfra1	14	14	14	14	...	15
Exp. b0	32758	32650	32616	32601	...	32613
Exp. b1	-32757	-32306	-31308	-29726	...	-20156

Test settings	
Tolerance b2	±1,0000e+00
Tolerance a1	±1,0000e+00
Tolerance a2	±1,0000e+00
Tolerance sfra2	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance sfrb2	±0,0000e+00
Tolerance sfra1	±0,0000e+00
Tolerance b0	±1,0000e+00
Tolerance b1	±1,0000e+00

Test statistics	
Min CPU cycles	6067
Max CPU cycles	6586
Avg CPU cycles	6471

Verification: NotchBiQ FiP32 CPU TM4C123GH6

Date of Test	2026-06-25
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for Filter block NotchBiQ.

Test results				
Time step	1	2	...	101
CPU cycles	243	243	...	243
Inputs				
In (DSP)	0	0	...	214748365
In	0	0	...	0.1
Parameters				
method	bilinear			
fn	50			
Q	25			
ts_fact	1			
Outputs				
Out	0	0	...	0.098
Exp. Out	0	0	...	0.098
Out (DSP)	0	0	...	210653100
Exp. Out (DSP)	0	0	...	210653187

Test settings	
Tolerance Out	±4,6566e-07 (±1000 LSB)

Test statistics	
Min CPU cycles	243
Max CPU cycles	243
Avg CPU cycles	243

Test case: Conversion test OK

Conversion test for Filter block NotchBiQ.

Test results				
Time step	1	2	...	10
Mask parameters				
method	bilinear	bilinear	...	bilinear
fn	10	231.111	...	2000
Q	10	20	...	100
ts_fact	1	1	...	1
Controller parameters				
b2	2146809212	2139743042	...	2137320087
a1	-2146766836	-2117222972	...	-1320936459
a2	2146134777	2132002436	...	2127156526
sfra2	31	31	...	31
sfrb0	31	31	...	31
sfrb1	30	30	...	31
sfrb2	31	31	...	31
sfra1	30	30	...	31
b0	2146809212	2139743042	...	2137320087
b1	-2146766836	-2117222972	...	-1320936459
Exp. b2	2146809212	2139743042	...	2137320087
Exp. a1	-2146766836	-2117222972	...	-1320936459
Exp. a2	2146134777	2132002436	...	2127156526
Exp. sfra2	31	31	...	31
Exp. sfrb0	31	31	...	31
Exp. sfrb1	30	30	...	31
Exp. sfrb2	31	31	...	31
Exp. sfra1	30	30	...	31
Exp. b0	2146809212	2139743042	...	2137320087
Exp. b1	-2146766836	-2117222972	...	-1320936459

Test settings	
Tolerance b2	±0,0000e+00
Tolerance a1	±0,0000e+00
Tolerance a2	±0,0000e+00
Tolerance sfra2	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance sfrb2	±0,0000e+00
Tolerance sfra1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Filter block NotchBiQ.

Test results				
Time step	1	2	...	10
Mask parameters				
method	bilinear	bilinear	...	bilinear
fn	10	231.111	...	2000
Q	10	20	...	100
ts_fact	1	1	...	1
Controller parameters				
b2	2146809088	2139742848	...	2137320064
a1	-2146766848	-2117223040	...	-1320936320
a2	2146134656	2132002304	...	2127156352
sfra2	31	31	...	31
sfrb0	31	31	...	31
sfrb1	30	30	...	31
sfrb2	31	31	...	31
sfra1	30	30	...	31
b0	2146809088	2139742848	...	2137320064
b1	-2146766848	-2117223040	...	-1320936320
Exp. b2	2146809212	2139743042	...	2137320087
Exp. a1	-2146766836	-2117222972	...	-1320936459
Exp. a2	2146134777	2132002436	...	2127156526
Exp. sfra2	31	31	...	31
Exp. sfrb0	31	31	...	31
Exp. sfrb1	30	30	...	31
Exp. sfrb2	31	31	...	31
Exp. sfra1	30	30	...	31
Exp. b0	2146809212	2139743042	...	2137320087
Exp. b1	-2146766836	-2117222972	...	-1320936459

Test settings	
Tolerance b2	±2,0000e+02
Tolerance a1	±5,0000e+02
Tolerance a2	±2,0000e+02
Tolerance sfra2	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance sfrb2	±0,0000e+00
Tolerance sfra1	±0,0000e+00
Tolerance b0	±2,0000e+02
Tolerance b1	±5,0000e+02

Test statistics	
Min CPU cycles	3139
Max CPU cycles	3523
Avg CPU cycles	3446

Verification: NotchBiQ FiP32 CPU TMS320F28335

Date of Test	2026-06-25
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for Filter block NotchBiQ.

Test results				
Time step	1	2	...	101
CPU cycles	266	266	...	266
Inputs				
In (DSP)	0	0	...	214748365
In	0	0	...	0.1
Parameters				
method	bilinear			
fn	50			
Q	25			
ts_fact	1			
Outputs				
Out	0	0	...	0.098
Exp. Out	0	0	...	0.098
Out (DSP)	0	0	...	210653100
Exp. Out (DSP)	0	0	...	210653187

Test settings	
Tolerance Out	±4,6566e-07 (±1000 LSB)

Test statistics	
Min CPU cycles	266
Max CPU cycles	266
Avg CPU cycles	266

Test case: Conversion test OK

Conversion test for Filter block NotchBiQ.

Test results				
Time step	1	2	...	10
Mask parameters				
method	bilinear	bilinear	...	bilinear
fn	10	231.111	...	2000
Q	10	20	...	100
ts_fact	1	1	...	1
Controller parameters				
b2	2146809212	2139743042	...	2137320087
a1	-2146766836	-2117222972	...	-1320936459
a2	2146134777	2132002436	...	2127156526
sfra2	31	31	...	31
sfrb0	31	31	...	31
sfrb1	30	30	...	31
sfrb2	31	31	...	31
sfra1	30	30	...	31
b0	2146809212	2139743042	...	2137320087
b1	-2146766836	-2117222972	...	-1320936459
Exp. b2	2146809212	2139743042	...	2137320087
Exp. a1	-2146766836	-2117222972	...	-1320936459
Exp. a2	2146134777	2132002436	...	2127156526
Exp. sfra2	31	31	...	31
Exp. sfrb0	31	31	...	31
Exp. sfrb1	30	30	...	31
Exp. sfrb2	31	31	...	31
Exp. sfra1	30	30	...	31
Exp. b0	2146809212	2139743042	...	2137320087
Exp. b1	-2146766836	-2117222972	...	-1320936459

Test settings	
Tolerance b2	±0,0000e+00
Tolerance a1	±0,0000e+00
Tolerance a2	±0,0000e+00
Tolerance sfra2	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance sfrb2	±0,0000e+00
Tolerance sfra1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Filter block NotchBiQ.

Test results				
Time step	1	2	...	10
Mask parameters				
method	bilinear	bilinear	...	bilinear
fn	10	231.111	...	2000
Q	10	20	...	100
ts_fact	1	1	...	1
Controller parameters				
b2	2146808960	2139742848	...	2137319936
a1	-2146766848	-2117223040	...	-1320936704
a2	2146134656	2132002304	...	2127156352
sfra2	31	31	...	31
sfrb0	31	31	...	31
sfrb1	30	30	...	31
sfrb2	31	31	...	31
sfra1	30	30	...	31
b0	2146808960	2139742848	...	2137319936
b1	-2146766848	-2117223040	...	-1320936704
Exp. b2	2146809212	2139743042	...	2137320087
Exp. a1	-2146766836	-2117222972	...	-1320936459
Exp. a2	2146134777	2132002436	...	2127156526
Exp. sfra2	31	31	...	31
Exp. sfrb0	31	31	...	31
Exp. sfrb1	30	30	...	31
Exp. sfrb2	31	31	...	31
Exp. sfra1	30	30	...	31
Exp. b0	2146809212	2139743042	...	2137320087
Exp. b1	-2146766836	-2117222972	...	-1320936459

Test settings	
Tolerance b2	±2,5200e+02
Tolerance a1	±5,0000e+02
Tolerance a2	±2,0000e+02
Tolerance sfra2	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance sfrb2	±0,0000e+00
Tolerance sfra1	±0,0000e+00
Tolerance b0	±2,5200e+02
Tolerance b1	±5,0000e+02

Test statistics	
Min CPU cycles	8601
Max CPU cycles	9631
Avg CPU cycles	9425

Verification: NotchBiQ FiP32 CPU TMS320F28379D

Date of Test	2026-06-25
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for Filter block NotchBiQ.

Test results				
Time step	1	2	...	101
CPU cycles	248	248	...	248
Inputs				
In (DSP)	0	0	...	214748365
In	0	0	...	0.1
Parameters				
method	bilinear			
fn	50			
Q	25			
ts_fact	1			
Outputs				
Out	0	0	...	0.098
Exp. Out	0	0	...	0.098
Out (DSP)	0	0	...	210653100
Exp. Out (DSP)	0	0	...	210653187

Test settings	
Tolerance Out	±4,6566e-07 (±1000 LSB)

Test statistics	
Min CPU cycles	248
Max CPU cycles	248
Avg CPU cycles	248

Test case: Conversion test OK

Conversion test for Filter block NotchBiQ.

Test results				
Time step	1	2	...	10
Mask parameters				
method	bilinear	bilinear	...	bilinear
fn	10	231.111	...	2000
Q	10	20	...	100
ts_fact	1	1	...	1
Controller parameters				
b2	2146809212	2139743042	...	2137320087
a1	-2146766836	-2117222972	...	-1320936459
a2	2146134777	2132002436	...	2127156526
sfra2	31	31	...	31
sfrb0	31	31	...	31
sfrb1	30	30	...	31
sfrb2	31	31	...	31
sfra1	30	30	...	31
b0	2146809212	2139743042	...	2137320087
b1	-2146766836	-2117222972	...	-1320936459
Exp. b2	2146809212	2139743042	...	2137320087
Exp. a1	-2146766836	-2117222972	...	-1320936459
Exp. a2	2146134777	2132002436	...	2127156526
Exp. sfra2	31	31	...	31
Exp. sfrb0	31	31	...	31
Exp. sfrb1	30	30	...	31
Exp. sfrb2	31	31	...	31
Exp. sfra1	30	30	...	31
Exp. b0	2146809212	2139743042	...	2137320087
Exp. b1	-2146766836	-2117222972	...	-1320936459

Test settings	
Tolerance b2	±0,0000e+00
Tolerance a1	±0,0000e+00
Tolerance a2	±0,0000e+00
Tolerance sfra2	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance sfrb2	±0,0000e+00
Tolerance sfra1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Filter block NotchBiQ.

Test results				
Time step	1	2	...	10
Mask parameters				
method	bilinear	bilinear	...	bilinear
fn	10	231.111	...	2000
Q	10	20	...	100
ts_fact	1	1	...	1
Controller parameters				
b2	2146808960	2139742848	...	2137319936
a1	-2146766848	-2117223040	...	-1320936704
a2	2146134656	2132002304	...	2127156352
sfra2	31	31	...	31
sfrb0	31	31	...	31
sfrb1	30	30	...	31
sfrb2	31	31	...	31
sfra1	30	30	...	31
b0	2146808960	2139742848	...	2137319936
b1	-2146766848	-2117223040	...	-1320936704
Exp. b2	2146809212	2139743042	...	2137320087
Exp. a1	-2146766836	-2117222972	...	-1320936459
Exp. a2	2146134777	2132002436	...	2127156526
Exp. sfra2	31	31	...	31
Exp. sfrb0	31	31	...	31
Exp. sfrb1	30	30	...	31
Exp. sfrb2	31	31	...	31
Exp. sfra1	30	30	...	31
Exp. b0	2146809212	2139743042	...	2137320087
Exp. b1	-2146766836	-2117222972	...	-1320936459

Test settings	
Tolerance b2	±2,5200e+02
Tolerance a1	±5,0000e+02
Tolerance a2	±2,0000e+02
Tolerance sfra2	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance sfrb2	±0,0000e+00
Tolerance sfra1	±0,0000e+00
Tolerance b0	±2,5200e+02
Tolerance b1	±5,0000e+02

Test statistics	
Min CPU cycles	6452
Max CPU cycles	7244
Avg CPU cycles	7085

Verification: NotchBiQ FiP32 CPU dsPIC33EP256MC502

Date of Test	2026-06-25
Target controller	dsPIC33EP256MC502

Test case: Inport test

OK

Inport test for Filter block NotchBiQ.

Test results				
Time step	1	2	...	101
CPU cycles	2219	2219	...	2219
Inputs				
In (DSP)	0	0	...	214748365
In	0	0	...	0.1
Parameters				
method	bilinear			
fn	50			
Q	25			
ts_fact	1			
Outputs				
Out	0	0	...	0.098
Exp. Out	0	0	...	0.098
Out (DSP)	0	0	...	210653100
Exp. Out (DSP)	0	0	...	210653187

Test settings	
Tolerance Out	±4,6566e-07 (±1000 LSB)

Test statistics	
Min CPU cycles	2219
Max CPU cycles	2242
Avg CPU cycles	2230

Test case: Conversion test

OK

Conversion test for Filter block NotchBiQ.

Test results				
Time step	1	2	...	10
Mask parameters				
method	bilinear	bilinear	...	bilinear
fn	10	231.111	...	2000
Q	10	20	...	100
ts_fact	1	1	...	1
Controller parameters				
b2	2146809212	2139743042	...	2137320087
a1	-2146766836	-2117222972	...	-1320936459
a2	2146134777	2132002436	...	2127156526
sfra2	31	31	...	31
sfrb0	31	31	...	31
sfrb1	30	30	...	31
sfrb2	31	31	...	31
sfra1	30	30	...	31
b0	2146809212	2139743042	...	2137320087
b1	-2146766836	-2117222972	...	-1320936459
Exp. b2	2146809212	2139743042	...	2137320087
Exp. a1	-2146766836	-2117222972	...	-1320936459
Exp. a2	2146134777	2132002436	...	2127156526
Exp. sfra2	31	31	...	31
Exp. sfrb0	31	31	...	31
Exp. sfrb1	30	30	...	31
Exp. sfrb2	31	31	...	31
Exp. sfra1	30	30	...	31
Exp. b0	2146809212	2139743042	...	2137320087
Exp. b1	-2146766836	-2117222972	...	-1320936459

Test settings	
Tolerance b2	±0,0000e+00
Tolerance a1	±0,0000e+00
Tolerance a2	±0,0000e+00
Tolerance sfra2	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance sfrb2	±0,0000e+00
Tolerance sfra1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Filter block NotchBiQ.

Test results				
Time step	1	2	...	10
Mask parameters				
method	bilinear	bilinear	...	bilinear
fn	10	231.111	...	2000
Q	10	20	...	100
ts_fact	1	1	...	1
Controller parameters				
b2	2146809088	2139742848	...	2137320064
a1	-2146766848	-2117223040	...	-1320936320
a2	2146134656	2132002304	...	2127156352
sfra2	31	31	...	31
sfrb0	31	31	...	31
sfrb1	30	30	...	31
sfrb2	31	31	...	31
sfra1	30	30	...	31
b0	2146809088	2139742848	...	2137320064
b1	-2146766848	-2117223040	...	-1320936320
Exp. b2	2146809212	2139743042	...	2137320087
Exp. a1	-2146766836	-2117222972	...	-1320936459
Exp. a2	2146134777	2132002436	...	2127156526
Exp. sfra2	31	31	...	31
Exp. sfrb0	31	31	...	31
Exp. sfrb1	30	30	...	31
Exp. sfrb2	31	31	...	31
Exp. sfra1	30	30	...	31
Exp. b0	2146809212	2139743042	...	2137320087
Exp. b1	-2146766836	-2117222972	...	-1320936459

Test settings	
Tolerance b2	±2,0000e+02
Tolerance a1	±5,0000e+02
Tolerance a2	±2,0000e+02
Tolerance sfra2	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance sfrb2	±0,0000e+00
Tolerance sfra1	±0,0000e+00
Tolerance b0	±2,0000e+02
Tolerance b1	±5,0000e+02

Test statistics	
Min CPU cycles	28126
Max CPU cycles	32508
Avg CPU cycles	31004

Verification: NotchBiQ FiP32 CPU STM32F072RB

Date of Test	2026-06-25
Target controller	STM32F072RB

Test case: Inport test

OK

Inport test for Filter block NotchBiQ.

Test results				
Time step	1	2	...	101
CPU cycles	633	633	...	633
Inputs				
In (DSP)	0	0	...	214748365
In	0	0	...	0.1
Parameters				
method	bilinear			
fn	50			
Q	25			
ts_fact	1			
Outputs				
Out	0	0	...	0.098
Exp. Out	0	0	...	0.098
Out (DSP)	0	0	...	210653100
Exp. Out (DSP)	0	0	...	210653187

Test settings	
Tolerance Out	±4,6566e-07 (±1000 LSB)

Test statistics	
Min CPU cycles	633
Max CPU cycles	699
Avg CPU cycles	637

Test case: Conversion test

OK

Conversion test for Filter block NotchBiQ.

Test results				
Time step	1	2	...	10
Mask parameters				
method	bilinear	bilinear	...	bilinear
fn	10	231.111	...	2000
Q	10	20	...	100
ts_fact	1	1	...	1
Controller parameters				
b2	2146809212	2139743042	...	2137320087
a1	-2146766836	-2117222972	...	-1320936459
a2	2146134777	2132002436	...	2127156526
sfra2	31	31	...	31
sfrb0	31	31	...	31
sfrb1	30	30	...	31
sfrb2	31	31	...	31
sfra1	30	30	...	31
b0	2146809212	2139743042	...	2137320087
b1	-2146766836	-2117222972	...	-1320936459
Exp. b2	2146809212	2139743042	...	2137320087
Exp. a1	-2146766836	-2117222972	...	-1320936459
Exp. a2	2146134777	2132002436	...	2127156526
Exp. sfra2	31	31	...	31
Exp. sfrb0	31	31	...	31
Exp. sfrb1	30	30	...	31
Exp. sfrb2	31	31	...	31
Exp. sfra1	30	30	...	31
Exp. b0	2146809212	2139743042	...	2137320087
Exp. b1	-2146766836	-2117222972	...	-1320936459

Test settings	
Tolerance b2	±0,0000e+00
Tolerance a1	±0,0000e+00
Tolerance a2	±0,0000e+00
Tolerance sfra2	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance sfrb2	±0,0000e+00
Tolerance sfra1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Filter block NotchBiQ.

Test results				
Time step	1	2	...	10
Mask parameters				
method	bilinear	bilinear	...	bilinear
fn	10	231.111	...	2000
Q	10	20	...	100
ts_fact	1	1	...	1
Controller parameters				
b2	2146809088	2139742848	...	2137320064
a1	-2146766848	-2117223040	...	-1320936320
a2	2146134656	2132002304	...	2127156352
sfra2	31	31	...	31
sfrb0	31	31	...	31
sfrb1	30	30	...	31
sfrb2	31	31	...	31
sfra1	30	30	...	31
b0	2146809088	2139742848	...	2137320064
b1	-2146766848	-2117223040	...	-1320936320
Exp. b2	2146809212	2139743042	...	2137320087
Exp. a1	-2146766836	-2117222972	...	-1320936459
Exp. a2	2146134777	2132002436	...	2127156526
Exp. sfra2	31	31	...	31
Exp. sfrb0	31	31	...	31
Exp. sfrb1	30	30	...	31
Exp. sfrb2	31	31	...	31
Exp. sfra1	30	30	...	31
Exp. b0	2146809212	2139743042	...	2137320087
Exp. b1	-2146766836	-2117222972	...	-1320936459

Test settings	
Tolerance b2	±2,0000e+02
Tolerance a1	±5,0000e+02
Tolerance a2	±2,0000e+02
Tolerance sfra2	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance sfrb2	±0,0000e+00
Tolerance sfra1	±0,0000e+00
Tolerance b0	±2,0000e+02
Tolerance b1	±5,0000e+02

Test statistics	
Min CPU cycles	27074
Max CPU cycles	28443
Avg CPU cycles	28116

Verification: NotchBiQ FiP32 CPU STM32G474RE

Date of Test	2026-06-25
Target controller	STM32G474RE

Test case: Inport test

OK

Inport test for Filter block NotchBiQ.

Test results				
Time step	1	2	...	101
CPU cycles	235	235	...	235
Inputs				
In (DSP)	0	0	...	214748365
In	0	0	...	0.1
Parameters				
method	bilinear			
fn	50			
Q	25			
ts_fact	1			
Outputs				
Out	0	0	...	0.098
Exp. Out	0	0	...	0.098
Out (DSP)	0	0	...	210653100
Exp. Out (DSP)	0	0	...	210653187

Test settings	
Tolerance Out	±4,6566e-07 (±1000 LSB)

Test statistics	
Min CPU cycles	235
Max CPU cycles	235
Avg CPU cycles	235

Test case: Conversion test

OK

Conversion test for Filter block NotchBiQ.

Test results				
Time step	1	2	...	10
Mask parameters				
method	bilinear	bilinear	...	bilinear
fn	10	231.111	...	2000
Q	10	20	...	100
ts_fact	1	1	...	1
Controller parameters				
b2	2146809212	2139743042	...	2137320087
a1	-2146766836	-2117222972	...	-1320936459
a2	2146134777	2132002436	...	2127156526
sfra2	31	31	...	31
sfrb0	31	31	...	31
sfrb1	30	30	...	31
sfrb2	31	31	...	31
sfra1	30	30	...	31
b0	2146809212	2139743042	...	2137320087
b1	-2146766836	-2117222972	...	-1320936459
Exp. b2	2146809212	2139743042	...	2137320087
Exp. a1	-2146766836	-2117222972	...	-1320936459
Exp. a2	2146134777	2132002436	...	2127156526
Exp. sfra2	31	31	...	31
Exp. sfrb0	31	31	...	31
Exp. sfrb1	30	30	...	31
Exp. sfrb2	31	31	...	31
Exp. sfra1	30	30	...	31
Exp. b0	2146809212	2139743042	...	2137320087
Exp. b1	-2146766836	-2117222972	...	-1320936459

Test settings	
Tolerance b2	±0,0000e+00
Tolerance a1	±0,0000e+00
Tolerance a2	±0,0000e+00
Tolerance sfra2	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance sfrb2	±0,0000e+00
Tolerance sfra1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Filter block NotchBiQ.

Test results				
Time step	1	2	...	10
Mask parameters				
method	bilinear	bilinear	...	bilinear
fn	10	231.111	...	2000
Q	10	20	...	100
ts_fact	1	1	...	1
Controller parameters				
b2	2146809088	2139742848	...	2137320192
a1	-2146766848	-2117223040	...	-1320936448
a2	2146134656	2132002304	...	2127156608
sfra2	31	31	...	31
sfrb0	31	31	...	31
sfrb1	30	30	...	31
sfrb2	31	31	...	31
sfra1	30	30	...	31
b0	2146809088	2139742848	...	2137320192
b1	-2146766848	-2117223040	...	-1320936448
Exp. b2	2146809212	2139743042	...	2137320087
Exp. a1	-2146766836	-2117222972	...	-1320936459
Exp. a2	2146134777	2132002436	...	2127156526
Exp. sfra2	31	31	...	31
Exp. sfrb0	31	31	...	31
Exp. sfrb1	30	30	...	31
Exp. sfrb2	31	31	...	31
Exp. sfra1	30	30	...	31
Exp. b0	2146809212	2139743042	...	2137320087
Exp. b1	-2146766836	-2117222972	...	-1320936459

Test settings	
Tolerance b2	±2,5200e+02
Tolerance a1	±5,0000e+02
Tolerance a2	±2,0000e+02
Tolerance sfra2	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance sfrb2	±0,0000e+00
Tolerance sfra1	±0,0000e+00
Tolerance b0	±2,5200e+02
Tolerance b1	±5,0000e+02

Test statistics	
Min CPU cycles	4208
Max CPU cycles	4460
Avg CPU cycles	4409

Verification: NotchBiQ FiP32 CPU XMC4800-F144K2048

Date of Test	2026-06-25
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for Filter block NotchBiQ.

Test results				
Time step	1	2	...	101
CPU cycles	282	224	...	224
Inputs				
In (DSP)	0	0	...	214748365
In	0	0	...	0.1
Parameters				
method	bilinear			
fn	50			
Q	25			
ts_fact	1			
Outputs				
Out	0	0	...	0.098
Exp. Out	0	0	...	0.098
Out (DSP)	0	0	...	210653100
Exp. Out (DSP)	0	0	...	210653187

Test settings	
Tolerance Out	±4,6566e-07 (±1000 LSB)

Test statistics	
Min CPU cycles	224
Max CPU cycles	282
Avg CPU cycles	224

Test case: Conversion test OK

Conversion test for Filter block NotchBiQ.

Test results				
Time step	1	2	...	10
Mask parameters				
method	bilinear	bilinear	...	bilinear
fn	10	231.111	...	2000
Q	10	20	...	100
ts_fact	1	1	...	1
Controller parameters				
b2	2146809212	2139743042	...	2137320087
a1	-2146766836	-2117222972	...	-1320936459
a2	2146134777	2132002436	...	2127156526
sfra2	31	31	...	31
sfrb0	31	31	...	31
sfrb1	30	30	...	31
sfrb2	31	31	...	31
sfra1	30	30	...	31
b0	2146809212	2139743042	...	2137320087
b1	-2146766836	-2117222972	...	-1320936459
Exp. b2	2146809212	2139743042	...	2137320087
Exp. a1	-2146766836	-2117222972	...	-1320936459
Exp. a2	2146134777	2132002436	...	2127156526
Exp. sfra2	31	31	...	31
Exp. sfrb0	31	31	...	31
Exp. sfrb1	30	30	...	31
Exp. sfrb2	31	31	...	31
Exp. sfra1	30	30	...	31
Exp. b0	2146809212	2139743042	...	2137320087
Exp. b1	-2146766836	-2117222972	...	-1320936459

Test settings	
Tolerance b2	±0,0000e+00
Tolerance a1	±0,0000e+00
Tolerance a2	±0,0000e+00
Tolerance sfra2	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance sfrb2	±0,0000e+00
Tolerance sfra1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Filter block NotchBiQ.

Test results				
Time step	1	2	...	10
Mask parameters				
method	bilinear	bilinear	...	bilinear
fn	10	231.111	...	2000
Q	10	20	...	100
ts_fact	1	1	...	1
Controller parameters				
b2	2146809088	2139742848	...	2137320192
a1	-2146766848	-2117223040	...	-1320936448
a2	2146134656	2132002304	...	2127156608
sfra2	31	31	...	31
sfrb0	31	31	...	31
sfrb1	30	30	...	31
sfrb2	31	31	...	31
sfra1	30	30	...	31
b0	2146809088	2139742848	...	2137320192
b1	-2146766848	-2117223040	...	-1320936448
Exp. b2	2146809212	2139743042	...	2137320087
Exp. a1	-2146766836	-2117222972	...	-1320936459
Exp. a2	2146134777	2132002436	...	2127156526
Exp. sfra2	31	31	...	31
Exp. sfrb0	31	31	...	31
Exp. sfrb1	30	30	...	31
Exp. sfrb2	31	31	...	31
Exp. sfra1	30	30	...	31
Exp. b0	2146809212	2139743042	...	2137320087
Exp. b1	-2146766836	-2117222972	...	-1320936459

Test settings	
Tolerance b2	±2,5200e+02
Tolerance a1	±5,0000e+02
Tolerance a2	±2,0000e+02
Tolerance sfra2	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance sfrb2	±0,0000e+00
Tolerance sfra1	±0,0000e+00
Tolerance b0	±2,5200e+02
Tolerance b1	±5,0000e+02

Test statistics	
Min CPU cycles	3930
Max CPU cycles	4405
Avg CPU cycles	4148

Verification: NotchBiQ FiP32 CPU PIC32MX170F256

Date of Test	2026-06-25
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for Filter block NotchBiQ.

Test results				
Time step	1	2	...	101
CPU cycles	208	208	...	208
Inputs				
In (DSP)	0	0	...	214748365
In	0	0	...	0.1
Parameters				
method	bilinear			
fn	50			
Q	25			
ts_fact	1			
Outputs				
Out	0	0	...	0.098
Exp. Out	0	0	...	0.098
Out (DSP)	0	0	...	210653100
Exp. Out (DSP)	0	0	...	210653187

Test settings	
Tolerance Out	±4,6566e-07 (±1000 LSB)

Test statistics	
Min CPU cycles	208
Max CPU cycles	208
Avg CPU cycles	208

Test case: Conversion test OK

Conversion test for Filter block NotchBiQ.

Test results				
Time step	1	2	...	10
Mask parameters				
method	bilinear	bilinear	...	bilinear
fn	10	231.111	...	2000
Q	10	20	...	100
ts_fact	1	1	...	1
Controller parameters				
b2	2146809212	2139743042	...	2137320087
a1	-2146766836	-2117222972	...	-1320936459
a2	2146134777	2132002436	...	2127156526
sfra2	31	31	...	31
sfrb0	31	31	...	31
sfrb1	30	30	...	31
sfrb2	31	31	...	31
sfra1	30	30	...	31
b0	2146809212	2139743042	...	2137320087
b1	-2146766836	-2117222972	...	-1320936459
Exp. b2	2146809212	2139743042	...	2137320087
Exp. a1	-2146766836	-2117222972	...	-1320936459
Exp. a2	2146134777	2132002436	...	2127156526
Exp. sfra2	31	31	...	31
Exp. sfrb0	31	31	...	31
Exp. sfrb1	30	30	...	31
Exp. sfrb2	31	31	...	31
Exp. sfra1	30	30	...	31
Exp. b0	2146809212	2139743042	...	2137320087
Exp. b1	-2146766836	-2117222972	...	-1320936459

Test settings	
Tolerance b2	±0,0000e+00
Tolerance a1	±0,0000e+00
Tolerance a2	±0,0000e+00
Tolerance sfra2	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance sfrb2	±0,0000e+00
Tolerance sfra1	±0,0000e+00
Tolerance b0	±0,0000e+00
Tolerance b1	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Filter block NotchBiQ.

Test results				
Time step	1	2	...	10
Mask parameters				
method	bilinear	bilinear	...	bilinear
fn	10	231.111	...	2000
Q	10	20	...	100
ts_fact	1	1	...	1
Controller parameters				
b2	2146809088	2139742848	...	2137320064
a1	-2146766848	-2117223040	...	-1320936704
a2	2146134656	2132002304	...	2127156352
sfra2	31	31	...	31
sfrb0	31	31	...	31
sfrb1	30	30	...	31
sfrb2	31	31	...	31
sfra1	30	30	...	31
b0	2146809088	2139742848	...	2137320064
b1	-2146766848	-2117223040	...	-1320936704
Exp. b2	2146809212	2139743042	...	2137320087
Exp. a1	-2146766836	-2117222972	...	-1320936459
Exp. a2	2146134777	2132002436	...	2127156526
Exp. sfra2	31	31	...	31
Exp. sfrb0	31	31	...	31
Exp. sfrb1	30	30	...	31
Exp. sfrb2	31	31	...	31
Exp. sfra1	30	30	...	31
Exp. b0	2146809212	2139743042	...	2137320087
Exp. b1	-2146766836	-2117222972	...	-1320936459

Test settings	
Tolerance b2	±2,5200e+02
Tolerance a1	±5,0000e+02
Tolerance a2	±2,0000e+02
Tolerance sfra2	±0,0000e+00
Tolerance sfrb0	±0,0000e+00
Tolerance sfrb1	±0,0000e+00
Tolerance sfrb2	±0,0000e+00
Tolerance sfra1	±0,0000e+00
Tolerance b0	±2,5200e+02
Tolerance b1	±5,0000e+02

Test statistics	
Min CPU cycles	8707
Max CPU cycles	9098
Avg CPU cycles	9008

Verification: NotchBiQ Float32 CPU TM4C123GH6

Date of Test	2026-06-25
Target controller	TM4C123GH6

Test case: Inport test — OK

Inport test for Filter block NotchBiQ.

Test results				
Time step	1	2	...	101
CPU cycles	61	61	...	61
Inputs				
In (DSP)	0	0	...	0.1
In	0	0	...	0.1
Parameters				
method	bilinear			
fn	50			
Q	25			
ts_fact	1			
Outputs				
Out	0	0	...	0.098
Exp. Out	0	0	...	0.098
Out (DSP)	0	0	...	0.098
Exp. Out (DSP)	0	0	...	0.098

Test settings	
Tolerance Out	±4,6566e-06 (±10000 LSB)

Test statistics	
Min CPU cycles	61
Max CPU cycles	61
Avg CPU cycles	61

Test case: Conversion test — OK

Conversion test for Filter block NotchBiQ.

Test results				
Time step	1	2	...	10
Mask parameters				
method	bilinear	bilinear	...	bilinear
fn	10	231.111	...	2000
Q	10	20	...	100
ts_fact	1	1	...	1
Controller parameters				
b2	1	0.996	...	0.995
a1	-1.999	-1.972	...	-0.615
a2	0.999	0.993	...	0.991
b0	1	0.996	...	0.995
b1	-1.999	-1.972	...	-0.615
Exp. b2	1	0.996	...	0.995
Exp. a1	-1.999	-1.972	...	-0.615
Exp. a2	0.999	0.993	...	0.991
Exp. b0	1	0.996	...	0.995
Exp. b1	-1.999	-1.972	...	-0.615

Test settings	
Tolerance b2	±8,8818e-16
Tolerance a1	±8,8818e-16
Tolerance a2	±8,8818e-16
Tolerance b0	±8,8818e-16
Tolerance b1	±8,8818e-16

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Filter block NotchBiQ.

Test results				
Time step	1	2	...	10
Mask parameters				
method	bilinear	bilinear	...	bilinear
fn	10	231.111	...	2000
Q	10	20	...	100
ts_fact	1	1	...	1
Controller parameters				
b2	1	0.996	...	0.995
a1	-1.999	-1.972	...	-0.615
a2	0.999	0.993	...	0.991
b0	1	0.996	...	0.995
b1	-1.999	-1.972	...	-0.615
Exp. b2	1	0.996	...	0.995
Exp. a1	-1.999	-1.972	...	-0.615
Exp. a2	0.999	0.993	...	0.991
Exp. b0	1	0.996	...	0.995
Exp. b1	-1.999	-1.972	...	-0.615

Test settings	
Tolerance b2	±1,0000e-07
Tolerance a1	±5,0000e-07
Tolerance a2	±1,0000e-07
Tolerance b0	±1,0000e-07
Tolerance b1	±5,0000e-07

Test statistics	
Min CPU cycles	1235
Max CPU cycles	1235
Avg CPU cycles	1235

Verification: NotchBiQ Float32 CPU TMS320F28335

Date of Test	2026-06-25
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for Filter block NotchBiQ.

Test results				
Time step	1	2	...	101
CPU cycles	93	93	...	93
Inputs				
In (DSP)	0	0	...	0.1
In	0	0	...	0.1
Parameters				
method	bilinear			
fn	50			
Q	25			
ts_fact	1			
Outputs				
Out	0	0	...	0.098
Exp. Out	0	0	...	0.098
Out (DSP)	0	0	...	0.098
Exp. Out (DSP)	0	0	...	0.098

Test settings	
Tolerance Out	±8,3819e-06 (±18000 LSB)

Test statistics	
Min CPU cycles	93
Max CPU cycles	93
Avg CPU cycles	93

Test case: Conversion test OK

Conversion test for Filter block NotchBiQ.

Test results				
Time step	1	2	...	10
Mask parameters				
method	bilinear	bilinear	...	bilinear
fn	10	231.111	...	2000
Q	10	20	...	100
ts_fact	1	1	...	1
Controller parameters				
b2	1	0.996	...	0.995
a1	-1.999	-1.972	...	-0.615
a2	0.999	0.993	...	0.991
b0	1	0.996	...	0.995
b1	-1.999	-1.972	...	-0.615
Exp. b2	1	0.996	...	0.995
Exp. a1	-1.999	-1.972	...	-0.615
Exp. a2	0.999	0.993	...	0.991
Exp. b0	1	0.996	...	0.995
Exp. b1	-1.999	-1.972	...	-0.615

Test settings	
Tolerance b2	±8,8818e-16
Tolerance a1	±8,8818e-16
Tolerance a2	±8,8818e-16
Tolerance b0	±8,8818e-16
Tolerance b1	±8,8818e-16

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Filter block NotchBiQ.

Test results				
Time step	1	2	...	10
Mask parameters				
method	bilinear	bilinear	...	bilinear
fn	10	231.111	...	2000
Q	10	20	...	100
ts_fact	1	1	...	1
Controller parameters				
b2	1	0.996	...	0.995
a1	-1.999	-1.972	...	-0.615
a2	0.999	0.993	...	0.991
b0	1	0.996	...	0.995
b1	-1.999	-1.972	...	-0.615
Exp. b2	1	0.996	...	0.995
Exp. a1	-1.999	-1.972	...	-0.615
Exp. a2	0.999	0.993	...	0.991
Exp. b0	1	0.996	...	0.995
Exp. b1	-1.999	-1.972	...	-0.615

Test settings	
Tolerance b2	±2,0000e-07
Tolerance a1	±5,0000e-07
Tolerance a2	±1,0000e-07
Tolerance b0	±2,0000e-07
Tolerance b1	±5,0000e-07

Test statistics	
Min CPU cycles	4104
Max CPU cycles	4104
Avg CPU cycles	4104

Verification: NotchBiQ Float32 CPU TMS320F28379D

Date of Test	2026-06-25
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for Filter block NotchBiQ.

Test results				
Time step	1	2	...	101
CPU cycles	86	86	...	86
Inputs				
In (DSP)	0	0	...	0.1
In	0	0	...	0.1
Parameters				
method	bilinear			
fn	50			
Q	25			
ts_fact	1			
Outputs				
Out	0	0	...	0.098
Exp. Out	0	0	...	0.098
Out (DSP)	0	0	...	0.098
Exp. Out (DSP)	0	0	...	0.098

Test settings	
Tolerance Out	±8,3819e-06 (±18000 LSB)

Test statistics	
Min CPU cycles	86
Max CPU cycles	86
Avg CPU cycles	86

Test case: Conversion test OK

Conversion test for Filter block NotchBiQ.

Test results				
Time step	1	2	...	10
Mask parameters				
method	bilinear	bilinear	...	bilinear
fn	10	231.111	...	2000
Q	10	20	...	100
ts_fact	1	1	...	1
Controller parameters				
b2	1	0.996	...	0.995
a1	-1.999	-1.972	...	-0.615
a2	0.999	0.993	...	0.991
b0	1	0.996	...	0.995
b1	-1.999	-1.972	...	-0.615
Exp. b2	1	0.996	...	0.995
Exp. a1	-1.999	-1.972	...	-0.615
Exp. a2	0.999	0.993	...	0.991
Exp. b0	1	0.996	...	0.995
Exp. b1	-1.999	-1.972	...	-0.615

Test settings	
Tolerance b2	±8,8818e-16
Tolerance a1	±8,8818e-16
Tolerance a2	±8,8818e-16
Tolerance b0	±8,8818e-16
Tolerance b1	±8,8818e-16

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Filter block NotchBiQ.

Test results				
Time step	1	2	...	10
Mask parameters				
method	bilinear	bilinear	...	bilinear
fn	10	231.111	...	2000
Q	10	20	...	100
ts_fact	1	1	...	1
Controller parameters				
b2	1	0.996	...	0.995
a1	-1.999	-1.972	...	-0.615
a2	0.999	0.993	...	0.991
b0	1	0.996	...	0.995
b1	-1.999	-1.972	...	-0.615
Exp. b2	1	0.996	...	0.995
Exp. a1	-1.999	-1.972	...	-0.615
Exp. a2	0.999	0.993	...	0.991
Exp. b0	1	0.996	...	0.995
Exp. b1	-1.999	-1.972	...	-0.615

Test settings	
Tolerance b2	±2,0000e-07
Tolerance a1	±5,0000e-07
Tolerance a2	±1,0000e-07
Tolerance b0	±2,0000e-07
Tolerance b1	±5,0000e-07

Test statistics	
Min CPU cycles	3207
Max CPU cycles	3207
Avg CPU cycles	3207

Verification: NotchBiQ Float32 CPU dsPIC33EP256MC502

Date of Test	2026-06-25
Target controller	dsPIC33EP256MC502

Test case: Inport test — OK

Inport test for Filter block NotchBiQ.

Test results				
Time step	1	2	...	101
CPU cycles	1324	1324	...	1774
Inputs				
In (DSP)	0	0	...	0.1
In	0	0	...	0.1
Parameters				
method	bilinear			
fn	50			
Q	25			
ts_fact	1			
Outputs				
Out	0	0	...	0.098
Exp. Out	0	0	...	0.098
Out (DSP)	0	0	...	0.098
Exp. Out (DSP)	0	0	...	0.098

Test settings	
Tolerance Out	±4,6566e-06 (±10000 LSB)

Test statistics	
Min CPU cycles	1201
Max CPU cycles	1778
Avg CPU cycles	1736

Test case: Conversion test — OK

Conversion test for Filter block NotchBiQ.

Test results				
Time step	1	2	...	10
Mask parameters				
method	bilinear	bilinear	...	bilinear
fn	10	231.111	...	2000
Q	10	20	...	100
ts_fact	1	1	...	1
Controller parameters				
b2	1	0.996	...	0.995
a1	-1.999	-1.972	...	-0.615
a2	0.999	0.993	...	0.991
b0	1	0.996	...	0.995
b1	-1.999	-1.972	...	-0.615
Exp. b2	1	0.996	...	0.995
Exp. a1	-1.999	-1.972	...	-0.615
Exp. a2	0.999	0.993	...	0.991
Exp. b0	1	0.996	...	0.995
Exp. b1	-1.999	-1.972	...	-0.615

Test settings	
Tolerance b2	±8,8818e-16
Tolerance a1	±8,8818e-16
Tolerance a2	±8,8818e-16
Tolerance b0	±8,8818e-16
Tolerance b1	±8,8818e-16

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Filter block NotchBiQ.

Test results				
Time step	1	2	...	10
Mask parameters				
method	bilinear	bilinear	...	bilinear
fn	10	231.111	...	2000
Q	10	20	...	100
ts_fact	1	1	...	1
Controller parameters				
b2	1	0.996	...	0.995
a1	-1.999	-1.972	...	-0.615
a2	0.999	0.993	...	0.991
b0	1	0.996	...	0.995
b1	-1.999	-1.972	...	-0.615
Exp. b2	1	0.996	...	0.995
Exp. a1	-1.999	-1.972	...	-0.615
Exp. a2	0.999	0.993	...	0.991
Exp. b0	1	0.996	...	0.995
Exp. b1	-1.999	-1.972	...	-0.615

Test settings	
Tolerance b2	±1,0000e-07
Tolerance a1	±5,0000e-07
Tolerance a2	±1,0000e-07
Tolerance b0	±1,0000e-07
Tolerance b1	±5,0000e-07

Test statistics	
Min CPU cycles	12660
Max CPU cycles	13740
Avg CPU cycles	12897

Verification: NotchBiQ Float32 CPU STM32F072RB

Date of Test	2026-06-25
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for Filter block NotchBiQ.

Test results				
Time step	1	2	...	101
CPU cycles	1073	1073	...	1572
Inputs				
In (DSP)	0	0	...	0.1
In	0	0	...	0.1
Parameters				
method	bilinear			
fn	50			
Q	25			
ts_fact	1			
Outputs				
Out	0	0	...	0.098
Exp. Out	0	0	...	0.098
Out (DSP)	0	0	...	0.098
Exp. Out (DSP)	0	0	...	0.098

Test settings	
Tolerance Out	±4,6566e-06 (±10000 LSB)

Test statistics	
Min CPU cycles	1073
Max CPU cycles	1633
Avg CPU cycles	1550

Test case: Conversion test OK

Conversion test for Filter block NotchBiQ.

Test results				
Time step	1	2	...	10
Mask parameters				
method	bilinear	bilinear	...	bilinear
fn	10	231.111	...	2000
Q	10	20	...	100
ts_fact	1	1	...	1
Controller parameters				
b2	1	0.996	...	0.995
a1	-1.999	-1.972	...	-0.615
a2	0.999	0.993	...	0.991
b0	1	0.996	...	0.995
b1	-1.999	-1.972	...	-0.615
Exp. b2	1	0.996	...	0.995
Exp. a1	-1.999	-1.972	...	-0.615
Exp. a2	0.999	0.993	...	0.991
Exp. b0	1	0.996	...	0.995
Exp. b1	-1.999	-1.972	...	-0.615

Test settings	
Tolerance b2	±8,8818e-16
Tolerance a1	±8,8818e-16
Tolerance a2	±8,8818e-16
Tolerance b0	±8,8818e-16
Tolerance b1	±8,8818e-16

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Filter block NotchBiQ.

Test results				
Time step	1	2	...	10
Mask parameters				
method	bilinear	bilinear	...	bilinear
fn	10	231.111	...	2000
Q	10	20	...	100
ts_fact	1	1	...	1
Controller parameters				
b2	1	0.996	...	0.995
a1	-1.999	-1.972	...	-0.615
a2	0.999	0.993	...	0.991
b0	1	0.996	...	0.995
b1	-1.999	-1.972	...	-0.615
Exp. b2	1	0.996	...	0.995
Exp. a1	-1.999	-1.972	...	-0.615
Exp. a2	0.999	0.993	...	0.991
Exp. b0	1	0.996	...	0.995
Exp. b1	-1.999	-1.972	...	-0.615

Test settings	
Tolerance b2	±1,0000e-07
Tolerance a1	±5,0000e-07
Tolerance a2	±1,0000e-07
Tolerance b0	±1,0000e-07
Tolerance b1	±5,0000e-07

Test statistics	
Min CPU cycles	14055
Max CPU cycles	14260
Avg CPU cycles	14190

Verification: NotchBiQ Float32 CPU STM32G474RE

Date of Test	2026-06-25
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for Filter block NotchBiQ.

Test results				
Time step	1	2	...	101
CPU cycles	103	103	...	103
Inputs				
In (DSP)	0	0	...	0.1
In	0	0	...	0.1
Parameters				
method	bilinear			
fn	50			
Q	25			
ts_fact	1			
Outputs				
Out	0	0	...	0.098
Exp. Out	0	0	...	0.098
Out (DSP)	0	0	...	0.098
Exp. Out (DSP)	0	0	...	0.098

Test settings	
Tolerance Out	±8,3819e-06 (±18000 LSB)

Test statistics	
Min CPU cycles	103
Max CPU cycles	103
Avg CPU cycles	103

Test case: Conversion test OK

Conversion test for Filter block NotchBiQ.

Test results				
Time step	1	2	...	10
Mask parameters				
method	bilinear	bilinear	...	bilinear
fn	10	231.111	...	2000
Q	10	20	...	100
ts_fact	1	1	...	1
Controller parameters				
b2	1	0.996	...	0.995
a1	-1.999	-1.972	...	-0.615
a2	0.999	0.993	...	0.991
b0	1	0.996	...	0.995
b1	-1.999	-1.972	...	-0.615
Exp. b2	1	0.996	...	0.995
Exp. a1	-1.999	-1.972	...	-0.615
Exp. a2	0.999	0.993	...	0.991
Exp. b0	1	0.996	...	0.995
Exp. b1	-1.999	-1.972	...	-0.615

Test settings	
Tolerance b2	±8,8818e-16
Tolerance a1	±8,8818e-16
Tolerance a2	±8,8818e-16
Tolerance b0	±8,8818e-16
Tolerance b1	±8,8818e-16

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Filter block NotchBiQ.

Test results				
Time step	1	2	...	10
Mask parameters				
method	bilinear	bilinear	...	bilinear
fn	10	231.111	...	2000
Q	10	20	...	100
ts_fact	1	1	...	1
Controller parameters				
b2	1	0.996	...	0.995
a1	-1.999	-1.972	...	-0.615
a2	0.999	0.993	...	0.991
b0	1	0.996	...	0.995
b1	-1.999	-1.972	...	-0.615
Exp. b2	1	0.996	...	0.995
Exp. a1	-1.999	-1.972	...	-0.615
Exp. a2	0.999	0.993	...	0.991
Exp. b0	1	0.996	...	0.995
Exp. b1	-1.999	-1.972	...	-0.615

Test settings	
Tolerance b2	±2,0000e-07
Tolerance a1	±5,0000e-07
Tolerance a2	±1,0000e-07
Tolerance b0	±2,0000e-07
Tolerance b1	±5,0000e-07

Test statistics	
Min CPU cycles	1430
Max CPU cycles	1430
Avg CPU cycles	1430

Verification: NotchBiQ Float32 CPU XMC4800-F144K2048

Date of Test	2026-06-25
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for Filter block NotchBiQ.

Test results				
Time step	1	2	...	101
CPU cycles	111	99	...	99
Inputs				
In (DSP)	0	0	...	0.1
In	0	0	...	0.1
Parameters				
method	bilinear			
fn	50			
Q	25			
ts_fact	1			
Outputs				
Out	0	0	...	0.098
Exp. Out	0	0	...	0.098
Out (DSP)	0	0	...	0.098
Exp. Out (DSP)	0	0	...	0.098

Test settings	
Tolerance Out	±8,3819e-06 (±18000 LSB)

Test statistics	
Min CPU cycles	99
Max CPU cycles	111
Avg CPU cycles	99

Test case: Conversion test OK

Conversion test for Filter block NotchBiQ.

Test results				
Time step	1	2	...	10
Mask parameters				
method	bilinear	bilinear	...	bilinear
fn	10	231.111	...	2000
Q	10	20	...	100
ts_fact	1	1	...	1
Controller parameters				
b2	1	0.996	...	0.995
a1	-1.999	-1.972	...	-0.615
a2	0.999	0.993	...	0.991
b0	1	0.996	...	0.995
b1	-1.999	-1.972	...	-0.615
Exp. b2	1	0.996	...	0.995
Exp. a1	-1.999	-1.972	...	-0.615
Exp. a2	0.999	0.993	...	0.991
Exp. b0	1	0.996	...	0.995
Exp. b1	-1.999	-1.972	...	-0.615

Test settings	
Tolerance b2	±8,8818e-16
Tolerance a1	±8,8818e-16
Tolerance a2	±8,8818e-16
Tolerance b0	±8,8818e-16
Tolerance b1	±8,8818e-16

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Filter block NotchBiQ.

Test results				
Time step	1	2	...	10
Mask parameters				
method	bilinear	bilinear	...	bilinear
fn	10	231.111	...	2000
Q	10	20	...	100
ts_fact	1	1	...	1
Controller parameters				
b2	1	0.996	...	0.995
a1	-1.999	-1.972	...	-0.615
a2	0.999	0.993	...	0.991
b0	1	0.996	...	0.995
b1	-1.999	-1.972	...	-0.615
Exp. b2	1	0.996	...	0.995
Exp. a1	-1.999	-1.972	...	-0.615
Exp. a2	0.999	0.993	...	0.991
Exp. b0	1	0.996	...	0.995
Exp. b1	-1.999	-1.972	...	-0.615

Test settings	
Tolerance b2	±2,0000e-07
Tolerance a1	±5,0000e-07
Tolerance a2	±1,0000e-07
Tolerance b0	±2,0000e-07
Tolerance b1	±5,0000e-07

Test statistics	
Min CPU cycles	1323
Max CPU cycles	1579
Avg CPU cycles	1348

Verification: NotchBiQ Float32 CPU PIC32MX170F256

Date of Test	2026-06-25
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for Filter block NotchBiQ.

Test results				
Time step	1	2	...	101
CPU cycles	377	377	...	575
Inputs				
In (DSP)	0	0	...	0.1
In	0	0	...	0.1
Parameters				
method	bilinear			
fn	50			
Q	25			
ts_fact	1			
Outputs				
Out	0	0	...	0.098
Exp. Out	0	0	...	0.098
Out (DSP)	0	0	...	0.098
Exp. Out (DSP)	0	0	...	0.098

Test settings	
Tolerance Out	±8,3819e-06 (±18000 LSB)

Test statistics	
Min CPU cycles	377
Max CPU cycles	578
Avg CPU cycles	566

Test case: Conversion test OK

Conversion test for Filter block NotchBiQ.

Test results				
Time step	1	2	...	10
Mask parameters				
method	bilinear	bilinear	...	bilinear
fn	10	231.111	...	2000
Q	10	20	...	100
ts_fact	1	1	...	1
Controller parameters				
b2	1	0.996	...	0.995
a1	-1.999	-1.972	...	-0.615
a2	0.999	0.993	...	0.991
b0	1	0.996	...	0.995
b1	-1.999	-1.972	...	-0.615
Exp. b2	1	0.996	...	0.995
Exp. a1	-1.999	-1.972	...	-0.615
Exp. a2	0.999	0.993	...	0.991
Exp. b0	1	0.996	...	0.995
Exp. b1	-1.999	-1.972	...	-0.615

Test settings	
Tolerance b2	±8,8818e-16
Tolerance a1	±8,8818e-16
Tolerance a2	±8,8818e-16
Tolerance b0	±8,8818e-16
Tolerance b1	±8,8818e-16

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Filter block NotchBiQ.

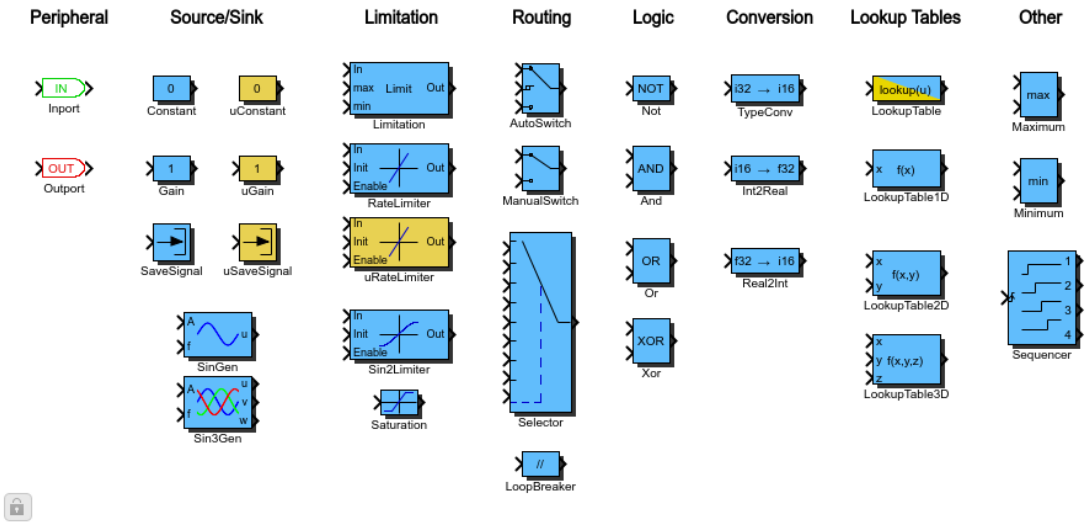
Test results				
Time step	1	2	...	10
Mask parameters				
method	bilinear	bilinear	...	bilinear
fn	10	231.111	...	2000
Q	10	20	...	100
ts_fact	1	1	...	1
Controller parameters				
b2	1	0.996	...	0.995
a1	-1.999	-1.972	...	-0.615
a2	0.999	0.993	...	0.991
b0	1	0.996	...	0.995
b1	-1.999	-1.972	...	-0.615
Exp. b2	1	0.996	...	0.995
Exp. a1	-1.999	-1.972	...	-0.615
Exp. a2	0.999	0.993	...	0.991
Exp. b0	1	0.996	...	0.995
Exp. b1	-1.999	-1.972	...	-0.615

Test settings	
Tolerance b2	±2,0000e-07
Tolerance a1	±5,0000e-07
Tolerance a2	±1,0000e-07
Tolerance b0	±2,0000e-07
Tolerance b1	±5,0000e-07

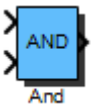
Test statistics	
Min CPU cycles	3093
Max CPU cycles	3166
Avg CPU cycles	3116

5 General

Library with general purpose blocks.



Block: And



Logical AND block.

Inports	
In1	
In2	

Outports	
Out	

Implementations:

Bool Boolean Implementation

Implementation: Bool

Boolean Implementation

Inports Data Type	
In1	bool
In2	bool

Outports Data Type	
Out	bool

Verification: And Bool CPU TMS320F28335

Date of Test 2026-06-19

Target controller TMS320F28335

Test case: Inport test OK

Inport test for General block And.

Test results						
Time step	1	2	3	4	...	25
CPU cycles	64	64	64	64	...	67
Inputs						
In1 (DSP)	0	0	0	0	...	1
In2 (DSP)	0	0	0	0	...	1
In1	0	-1	-0.5	-0.2	...	1
In2	0	0	0	0	...	1
Outputs						
Out	0	0	0	0	...	1
Exp. Out	0	0	0	0	...	1
Out (DSP)	0	0	0	0	...	1
Exp. Out (DSP)	0	0	0	0	...	1

Test settings	
Tolerance Out	±0,0000e+00 (±0 LSB)

Test statistics	
Min CPU cycles	64
Max CPU cycles	67
Avg CPU cycles	64

Verification: And Bool CPU TM4C123GH6

Date of Test 2026-06-19

Target controller TM4C123GH6

Test case: Inport test OK

Inport test for General block And.

Test results						
Time step	1	2	3	4	...	25
CPU cycles	31	31	31	31	...	33
Inputs						
In1 (DSP)	0	0	0	0	...	1
In2 (DSP)	0	0	0	0	...	1
In1	0	-1	-0.5	-0.2	...	1
In2	0	0	0	0	...	1
Outputs						
Out	0	0	0	0	...	1
Exp. Out	0	0	0	0	...	1
Out (DSP)	0	0	0	0	...	1
Exp. Out (DSP)	0	0	0	0	...	1

Test settings	
Tolerance Out	±0,0000e+00 (±0 LSB)

Test statistics	
Min CPU cycles	31
Max CPU cycles	33
Avg CPU cycles	31

Verification: And Bool CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for General block And.

Test results						
Time step	1	2	3	4	...	25
CPU cycles	57	57	57	57	...	57
Inputs						
In1 (DSP)	0	0	0	0	...	1
In2 (DSP)	0	0	0	0	...	1
In1	0	-1	-0.5	-0.2	...	1
In2	0	0	0	0	...	1
Outputs						
Out	0	0	0	0	...	1
Exp. Out	0	0	0	0	...	1
Out (DSP)	0	0	0	0	...	1
Exp. Out (DSP)	0	0	0	0	...	1

Test settings	
Tolerance Out	±0,0000e+00 (±0 LSB)

Test statistics	
Min CPU cycles	57
Max CPU cycles	57
Avg CPU cycles	57

Verification: And Bool CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for General block And.

Test results						
Time step	1	2	3	4	...	25
CPU cycles	50	50	50	50	...	52
Inputs						
In1 (DSP)	0	0	0	0	...	1
In2 (DSP)	0	0	0	0	...	1
In1	0	-1	-0.5	-0.2	...	1
In2	0	0	0	0	...	1
Outputs						
Out	0	0	0	0	...	1
Exp. Out	0	0	0	0	...	1
Out (DSP)	0	0	0	0	...	1
Exp. Out (DSP)	0	0	0	0	...	1

Test settings	
Tolerance Out	±0,0000e+00 (±0 LSB)

Test statistics	
Min CPU cycles	50
Max CPU cycles	52
Avg CPU cycles	50

Verification: And Bool CPU PIC32MX170F256

Date of Test 2026-06-19

Target controller PIC32MX170F256

Test case: Inport test OK

Inport test for General block And.

Test results						
Time step	1	2	3	4	...	25
CPU cycles	30	30	30	30	...	35
Inputs						
In1 (DSP)	0	0	0	0	...	1
In2 (DSP)	0	0	0	0	...	1
In1	0	-1	-0.5	-0.2	...	1
In2	0	0	0	0	...	1
Outputs						
Out	0	0	0	0	...	1
Exp. Out	0	0	0	0	...	1
Out (DSP)	0	0	0	0	...	1
Exp. Out (DSP)	0	0	0	0	...	1

Test settings	
Tolerance Out	±0,0000e+00 (±0 LSB)

Test statistics	
Min CPU cycles	30
Max CPU cycles	35
Avg CPU cycles	30

Verification: And Bool CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for General block And.

Test results						
Time step	1	2	3	4	...	25
CPU cycles	45	45	45	45	...	45
Inputs						
In1 (DSP)	0	0	0	0	...	1
In2 (DSP)	0	0	0	0	...	1
In1	0	-1	-0.5	-0.2	...	1
In2	0	0	0	0	...	1
Outputs						
Out	0	0	0	0	...	1
Exp. Out	0	0	0	0	...	1
Out (DSP)	0	0	0	0	...	1
Exp. Out (DSP)	0	0	0	0	...	1

Test settings	
Tolerance Out	±0,0000e+00 (±0 LSB)

Test statistics	
Min CPU cycles	45
Max CPU cycles	45
Avg CPU cycles	45

Verification: And Bool CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for General block And.

Test results						
Time step	1	2	3	4	...	25
CPU cycles	58	58	58	58	...	60
Inputs						
In1 (DSP)	0	0	0	0	...	1
In2 (DSP)	0	0	0	0	...	1
In1	0	-1	-0.5	-0.2	...	1
In2	0	0	0	0	...	1
Outputs						
Out	0	0	0	0	...	1
Exp. Out	0	0	0	0	...	1
Out (DSP)	0	0	0	0	...	1
Exp. Out (DSP)	0	0	0	0	...	1

Test settings	
Tolerance Out	±0,0000e+00 (±0 LSB)

Test statistics	
Min CPU cycles	58
Max CPU cycles	60
Avg CPU cycles	58

Verification: And Bool CPU TMS320F28379D

Date of Test 2026-06-22

Target controller TMS320F28379D

Test case: Inport test OK

Inport test for General block And.

Test results						
Time step	1	2	3	4	...	25
CPU cycles	47	47	47	47	...	49
Inputs						
In1 (DSP)	0	0	0	0	...	1
In2 (DSP)	0	0	0	0	...	1
In1	0	-1	-0.5	-0.2	...	1
In2	0	0	0	0	...	1
Outputs						
Out	0	0	0	0	...	1
Exp. Out	0	0	0	0	...	1
Out (DSP)	0	0	0	0	...	1
Exp. Out (DSP)	0	0	0	0	...	1

Test settings	
Tolerance Out	±0,0000e+00 (±0 LSB)

Test statistics	
Min CPU cycles	47
Max CPU cycles	49
Avg CPU cycles	47

Block: AutoSwitch



Switch between In1 and In3 dependent on Switch signal:
Switch signal rising: Switch >= Threshold up –> Out = In1
Switch signal falling: Switch < Threshold down –> Out = In3

Inports	
In1	Input #1
Switch	Input #2: Threshold signal
In3	Input #3

Outports	
Out	Either value of input #1 or input #3 dependent on value of input #2

Mask Parameters		
Name	**ID**	**Description**
Thresh_up	1	Threshold level for rising switch signal
Thresh_down	2	Threshold level for falling switch signal

Implementations:

FiP16	16 Bit Fixed Point Implementation
FiP32	32 Bit Fixed Point Implementation
Float32	32 Bit Floating Point Implementation
Float64	64 Bit Floating Point Implementation

Implementation: FiP16

16 Bit Fixed Point Implementation

Inports Data Type	
In1	int16
Switch	int16
In3	int16

Outports Data Type	
Out	int16

Implementation: FiP32

32 Bit Fixed Point Implementation

Inports Data Type	
In1	int32
Switch	int32
In3	int32

Outports Data Type	
Out	int32

Implementation: Float32

32 Bit Floating Point Implementation

Inports Data Type	
In1	float32
Switch	float32
In3	float32

Outports Data Type	
Out	float32

Implementation: Float64

64 Bit Floating Point Implementation

Inports Data Type	
In1	float64
Switch	float64
In3	float64

Outports Data Type	
Out	float64

Verification: AutoSwitch FiP16 CPU TMS320F28335

Date of Test 2026-06-19

Target controller TMS320F28335

Test case: Inport test OK

Inport test for General block AutoSwitch.

Test results						
Time step	1	2	3	4	...	137
CPU cycles	71	71	71	71	...	71
Inputs						
In1 (DSP)	-32768	-32293	-31818	-31343	...	32293
Switch (DSP)	30005	28152	32440	32440	...	14425
In3 (DSP)	32767	32293	31818	31343	...	-32293
In1	-1	-0.986	-0.971	-0.957	...	0.986
Switch	0.916	0.859	0.99	0.99	...	0.44
In3	1	0.986	0.971	0.957	...	-0.986
Parameters						
Thresh_up	0.3					
Thresh_down	-0.1					
Outputs						
Out	-1	-0.986	-0.971	-0.957	...	0.986
Exp. Out	-1	-0.986	-0.971	-0.957	...	0.986
Out (DSP)	-32768	-32293	-31818	-31343	...	32293
Exp. Out (DSP)	-32768	-32293	-31818	-31343	...	32293

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	71
Max CPU cycles	79
Avg CPU cycles	74

Test case: Inport test OK

Inport test for General block AutoSwitch.

Test results						
Time step	1	2	3	4	...	137
CPU cycles	71	71	71	71	...	71
Inputs						
In1 (DSP)	-32768	-32293	-31818	-31343	...	32293
Switch (DSP)	30005	28152	32440	32440	...	14425
In3 (DSP)	32767	32293	31818	31343	...	-32293
In1	-1	-0.986	-0.971	-0.957	...	0.986
Switch	0.916	0.859	0.99	0.99	...	0.44
In3	1	0.986	0.971	0.957	...	-0.986
Parameters						
Thresh_up	0					
Thresh_down	0					
Outputs						
Out	-1	-0.986	-0.971	-0.957	...	0.986
Exp. Out	-1	-0.986	-0.971	-0.957	...	0.986
Out (DSP)	-32768	-32293	-31818	-31343	...	32293
Exp. Out (DSP)	-32768	-32293	-31818	-31343	...	32293

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	71
Max CPU cycles	79
Avg CPU cycles	74

Test case: Conversion test **OK**

Conversion test for General block AutoSwitch.

Test results						
Time step	1	2	3	4	...	11
Mask parameters						
Thresh_up	0	0.1	0.2	0.5	...	-1.1
Thresh_down	0	0.1	0.2	0.5	...	-1.1
Controller parameters						
Thresh_down	0	3277	6554	16384	...	-32767
Thresh_up	0	3277	6554	16384	...	-32767
Exp. Thresh_down	0	3277	6554	16384	...	-32767
Exp. Thresh_up	0	3277	6554	16384	...	-32767

Test settings	
Tolerance Thresh_down	±0,0000e+00
Tolerance Thresh_up	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block AutoSwitch.

Test results						
Time step	1	2	3	4	...	11
Mask parameters						
Thresh_up	0	0.1	0.2	0.5	...	-1.1
Thresh_down	0	0.1	0.2	0.5	...	-1.1
Controller parameters						
Thresh_down	0	3276	6553	16384	...	-32767
Thresh_up	0	3276	6553	16384	...	-32767
Exp. Thresh_down	0	3277	6554	16384	...	-32767
Exp. Thresh_up	0	3277	6554	16384	...	-32767

Test settings	
Tolerance Thresh_down	±1,0000e+00
Tolerance Thresh_up	±1,0000e+00

Test statistics	
Min CPU cycles	1350
Max CPU cycles	1384
Avg CPU cycles	1353

Verification: AutoSwitch FiP16 CPU TM4C123GH6

Date of Test 2026-06-19

Target controller TM4C123GH6

Test case: Inport test OK

Inport test for General block AutoSwitch.

Test results						
Time step	1	2	3	4	...	137
CPU cycles	31	31	31	31	...	31
Inputs						
In1 (DSP)	-32768	-32293	-31818	-31343	...	32293
Switch (DSP)	30005	28152	32440	32440	...	14425
In3 (DSP)	32767	32293	31818	31343	...	-32293
In1	-1	-0.986	-0.971	-0.957	...	0.986
Switch	0.916	0.859	0.99	0.99	...	0.44
In3	1	0.986	0.971	0.957	...	-0.986
Parameters						
Thresh_up	0.3					
Thresh_down	-0.1					
Outputs						
Out	-1	-0.986	-0.971	-0.957	...	0.986
Exp. Out	-1	-0.986	-0.971	-0.957	...	0.986
Out (DSP)	-32768	-32293	-31818	-31343	...	32293
Exp. Out (DSP)	-32768	-32293	-31818	-31343	...	32293

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	31
Max CPU cycles	39
Avg CPU cycles	34

Test case: Inport test OK

Inport test for General block AutoSwitch.

Test results						
Time step	1	2	3	4	...	137
CPU cycles	31	31	31	31	...	31
Inputs						
In1 (DSP)	-32768	-32293	-31818	-31343	...	32293
Switch (DSP)	30005	28152	32440	32440	...	14425
In3 (DSP)	32767	32293	31818	31343	...	-32293
In1	-1	-0.986	-0.971	-0.957	...	0.986
Switch	0.916	0.859	0.99	0.99	...	0.44
In3	1	0.986	0.971	0.957	...	-0.986
Parameters						
Thresh_up	0					
Thresh_down	0					
Outputs						
Out	-1	-0.986	-0.971	-0.957	...	0.986
Exp. Out	-1	-0.986	-0.971	-0.957	...	0.986
Out (DSP)	-32768	-32293	-31818	-31343	...	32293
Exp. Out (DSP)	-32768	-32293	-31818	-31343	...	32293

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	31
Max CPU cycles	39
Avg CPU cycles	34

Test case: Conversion test **OK**

Conversion test for General block AutoSwitch.

Test results						
Time step	1	2	3	4	...	11
Mask parameters						
Thresh_up	0	0.1	0.2	0.5	...	-1.1
Thresh_down	0	0.1	0.2	0.5	...	-1.1
Controller parameters						
Thresh_down	0	3277	6554	16384	...	-32767
Thresh_up	0	3277	6554	16384	...	-32767
Exp. Thresh_down	0	3277	6554	16384	...	-32767
Exp. Thresh_up	0	3277	6554	16384	...	-32767

Test settings	
Tolerance Thresh_down	±0,0000e+00
Tolerance Thresh_up	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block AutoSwitch.

Test results						
Time step	1	2	3	4	...	11
Mask parameters						
Thresh_up	0	0.1	0.2	0.5	...	-1.1
Thresh_down	0	0.1	0.2	0.5	...	-1.1
Controller parameters						
Thresh_down	0	3276	6553	16384	...	-32767
Thresh_up	0	3276	6553	16384	...	-32767
Exp. Thresh_down	0	3277	6554	16384	...	-32767
Exp. Thresh_up	0	3277	6554	16384	...	-32767

Test settings	
Tolerance Thresh_down	±1,0000e+00
Tolerance Thresh_up	±1,0000e+00

Test statistics	
Min CPU cycles	637
Max CPU cycles	649
Avg CPU cycles	644

Verification: AutoSwitch FiP16 CPU STM32G474RE

Date of Test 2026-06-19

Target controller STM32G474RE

Test case: Inport test OK

Inport test for General block AutoSwitch.

Test results						
Time step	1	2	3	4	...	137
CPU cycles	62	62	62	62	...	62
Inputs						
In1 (DSP)	-32768	-32293	-31818	-31343	...	32293
Switch (DSP)	30005	28152	32440	32440	...	14425
In3 (DSP)	32767	32293	31818	31343	...	-32293
In1	-1	-0.986	-0.971	-0.957	...	0.986
Switch	0.916	0.859	0.99	0.99	...	0.44
In3	1	0.986	0.971	0.957	...	-0.986
Parameters						
Thresh_up	0.3					
Thresh_down	-0.1					
Outputs						
Out	-1	-0.986	-0.971	-0.957	...	0.986
Exp. Out	-1	-0.986	-0.971	-0.957	...	0.986
Out (DSP)	-32768	-32293	-31818	-31343	...	32293
Exp. Out (DSP)	-32768	-32293	-31818	-31343	...	32293

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	62
Max CPU cycles	77
Avg CPU cycles	70

Test case: Inport test OK

Inport test for General block AutoSwitch.

Test results						
Time step	1	2	3	4	...	137
CPU cycles	62	62	62	62	...	62
Inputs						
In1 (DSP)	-32768	-32293	-31818	-31343	...	32293
Switch (DSP)	30005	28152	32440	32440	...	14425
In3 (DSP)	32767	32293	31818	31343	...	-32293
In1	-1	-0.986	-0.971	-0.957	...	0.986
Switch	0.916	0.859	0.99	0.99	...	0.44
In3	1	0.986	0.971	0.957	...	-0.986
Parameters						
Thresh_up	0					
Thresh_down	0					
Outputs						
Out	-1	-0.986	-0.971	-0.957	...	0.986
Exp. Out	-1	-0.986	-0.971	-0.957	...	0.986
Out (DSP)	-32768	-32293	-31818	-31343	...	32293
Exp. Out (DSP)	-32768	-32293	-31818	-31343	...	32293

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	62
Max CPU cycles	77
Avg CPU cycles	68

Test case: Conversion test **OK**

Conversion test for General block AutoSwitch.

Test results						
Time step	1	2	3	4	...	11
Mask parameters						
Thresh_up	0	0.1	0.2	0.5	...	-1.1
Thresh_down	0	0.1	0.2	0.5	...	-1.1
Controller parameters						
Thresh_down	0	3277	6554	16384	...	-32767
Thresh_up	0	3277	6554	16384	...	-32767
Exp. Thresh_down	0	3277	6554	16384	...	-32767
Exp. Thresh_up	0	3277	6554	16384	...	-32767

Test settings	
Tolerance Thresh_down	±0,0000e+00
Tolerance Thresh_up	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block AutoSwitch.

Test results						
Time step	1	2	3	4	...	11
Mask parameters						
Thresh_up	0	0.1	0.2	0.5	...	-1.1
Thresh_down	0	0.1	0.2	0.5	...	-1.1
Controller parameters						
Thresh_down	0	3276	6553	16384	...	-32767
Thresh_up	0	3276	6553	16384	...	-32767
Exp. Thresh_down	0	3277	6554	16384	...	-32767
Exp. Thresh_up	0	3277	6554	16384	...	-32767

Test settings	
Tolerance Thresh_down	±1,0000e+00
Tolerance Thresh_up	±1,0000e+00

Test statistics	
Min CPU cycles	800
Max CPU cycles	848
Avg CPU cycles	804

Verification: AutoSwitch FiP16 CPU STM32F072RB

Date of Test 2026-06-19

Target controller STM32F072RB

Test case: Inport test OK

Inport test for General block AutoSwitch.

Test results						
Time step	1	2	3	4	...	137
CPU cycles	59	59	59	59	...	59
Inputs						
In1 (DSP)	-32768	-32293	-31818	-31343	...	32293
Switch (DSP)	30005	28152	32440	32440	...	14425
In3 (DSP)	32767	32293	31818	31343	...	-32293
In1	-1	-0.986	-0.971	-0.957	...	0.986
Switch	0.916	0.859	0.99	0.99	...	0.44
In3	1	0.986	0.971	0.957	...	-0.986
Parameters						
Thresh_up	0.3					
Thresh_down	-0.1					
Outputs						
Out	-1	-0.986	-0.971	-0.957	...	0.986
Exp. Out	-1	-0.986	-0.971	-0.957	...	0.986
Out (DSP)	-32768	-32293	-31818	-31343	...	32293
Exp. Out (DSP)	-32768	-32293	-31818	-31343	...	32293

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	59
Max CPU cycles	73
Avg CPU cycles	66

Test case: Inport test OK

Inport test for General block AutoSwitch.

Test results						
Time step	1	2	3	4	...	137
CPU cycles	59	59	59	59	...	59
Inputs						
In1 (DSP)	-32768	-32293	-31818	-31343	...	32293
Switch (DSP)	30005	28152	32440	32440	...	14425
In3 (DSP)	32767	32293	31818	31343	...	-32293
In1	-1	-0.986	-0.971	-0.957	...	0.986
Switch	0.916	0.859	0.99	0.99	...	0.44
In3	1	0.986	0.971	0.957	...	-0.986
Parameters						
Thresh_up	0					
Thresh_down	0					
Outputs						
Out	-1	-0.986	-0.971	-0.957	...	0.986
Exp. Out	-1	-0.986	-0.971	-0.957	...	0.986
Out (DSP)	-32768	-32293	-31818	-31343	...	32293
Exp. Out (DSP)	-32768	-32293	-31818	-31343	...	32293

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	59
Max CPU cycles	73
Avg CPU cycles	65

Test case: Conversion test **OK**

Conversion test for General block AutoSwitch.

Test results						
Time step	1	2	3	4	...	11
Mask parameters						
Thresh_up	0	0.1	0.2	0.5	...	-1.1
Thresh_down	0	0.1	0.2	0.5	...	-1.1
Controller parameters						
Thresh_down	0	3277	6554	16384	...	-32767
Thresh_up	0	3277	6554	16384	...	-32767
Exp. Thresh_down	0	3277	6554	16384	...	-32767
Exp. Thresh_up	0	3277	6554	16384	...	-32767

Test settings	
Tolerance Thresh_down	±0,0000e+00
Tolerance Thresh_up	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block AutoSwitch.

Test results						
Time step	1	2	3	4	...	11
Mask parameters						
Thresh_up	0	0.1	0.2	0.5	...	-1.1
Thresh_down	0	0.1	0.2	0.5	...	-1.1
Controller parameters						
Thresh_down	0	3276	6553	16384	...	-32767
Thresh_up	0	3276	6553	16384	...	-32767
Exp. Thresh_down	0	3277	6554	16384	...	-32767
Exp. Thresh_up	0	3277	6554	16384	...	-32767

Test settings	
Tolerance Thresh_down	±1,0000e+00
Tolerance Thresh_up	±1,0000e+00

Test statistics	
Min CPU cycles	1429
Max CPU cycles	1657
Avg CPU cycles	1626

Verification: AutoSwitch FiP16 CPU PIC32MX170F256

Date of Test 2026-06-19

Target controller PIC32MX170F256

Test case: Inport test OK

Inport test for General block AutoSwitch.

Test results						
Time step	1	2	3	4	...	137
CPU cycles	39	39	39	39	...	39
Inputs						
In1 (DSP)	-32768	-32293	-31818	-31343	...	32293
Switch (DSP)	30005	28152	32440	32440	...	14425
In3 (DSP)	32767	32293	31818	31343	...	-32293
In1	-1	-0.986	-0.971	-0.957	...	0.986
Switch	0.916	0.859	0.99	0.99	...	0.44
In3	1	0.986	0.971	0.957	...	-0.986
Parameters						
Thresh_up	0.3					
Thresh_down	-0.1					
Outputs						
Out	-1	-0.986	-0.971	-0.957	...	0.986
Exp. Out	-1	-0.986	-0.971	-0.957	...	0.986
Out (DSP)	-32768	-32293	-31818	-31343	...	32293
Exp. Out (DSP)	-32768	-32293	-31818	-31343	...	32293

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	39
Max CPU cycles	43
Avg CPU cycles	41

Test case: Inport test OK

Inport test for General block AutoSwitch.

Test results						
Time step	1	2	3	4	...	137
CPU cycles	39	39	39	39	...	39
Inputs						
In1 (DSP)	-32768	-32293	-31818	-31343	...	32293
Switch (DSP)	30005	28152	32440	32440	...	14425
In3 (DSP)	32767	32293	31818	31343	...	-32293
In1	-1	-0.986	-0.971	-0.957	...	0.986
Switch	0.916	0.859	0.99	0.99	...	0.44
In3	1	0.986	0.971	0.957	...	-0.986
Parameters						
Thresh_up	0					
Thresh_down	0					
Outputs						
Out	-1	-0.986	-0.971	-0.957	...	0.986
Exp. Out	-1	-0.986	-0.971	-0.957	...	0.986
Out (DSP)	-32768	-32293	-31818	-31343	...	32293
Exp. Out (DSP)	-32768	-32293	-31818	-31343	...	32293

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	39
Max CPU cycles	43
Avg CPU cycles	40

Test case: Conversion test **OK**

Conversion test for General block AutoSwitch.

Test results						
Time step	1	2	3	4	...	11
Mask parameters						
Thresh_up	0	0.1	0.2	0.5	...	-1.1
Thresh_down	0	0.1	0.2	0.5	...	-1.1
Controller parameters						
Thresh_down	0	3277	6554	16384	...	-32767
Thresh_up	0	3277	6554	16384	...	-32767
Exp. Thresh_down	0	3277	6554	16384	...	-32767
Exp. Thresh_up	0	3277	6554	16384	...	-32767

Test settings	
Tolerance Thresh_down	±0,0000e+00
Tolerance Thresh_up	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block AutoSwitch.

Test results						
Time step	1	2	3	4	...	11
Mask parameters						
Thresh_up	0	0.1	0.2	0.5	...	-1.1
Thresh_down	0	0.1	0.2	0.5	...	-1.1
Controller parameters						
Thresh_down	0	3276	6553	16384	...	-32767
Thresh_up	0	3276	6553	16384	...	-32767
Exp. Thresh_down	0	3277	6554	16384	...	-32767
Exp. Thresh_up	0	3277	6554	16384	...	-32767

Test settings	
Tolerance Thresh_down	±1,0000e+00
Tolerance Thresh_up	±1,0000e+00

Test statistics	
Min CPU cycles	648
Max CPU cycles	724
Avg CPU cycles	713

Verification: AutoSwitch FiP16 CPU dsPIC33EP256MC502

Date of Test 2026-06-19

Target controller dsPIC33EP256MC502

Test case: Inport test OK

Inport test for General block AutoSwitch.

Test results						
Time step	1	2	3	4	...	137
CPU cycles	50	50	50	50	...	50
Inputs						
In1 (DSP)	-32768	-32293	-31818	-31343	...	32293
Switch (DSP)	30005	28152	32440	32440	...	14425
In3 (DSP)	32767	32293	31818	31343	...	-32293
In1	-1	-0.986	-0.971	-0.957	...	0.986
Switch	0.916	0.859	0.99	0.99	...	0.44
In3	1	0.986	0.971	0.957	...	-0.986
Parameters						
Thresh_up	0.3					
Thresh_down	-0.1					
Outputs						
Out	-1	-0.986	-0.971	-0.957	...	0.986
Exp. Out	-1	-0.986	-0.971	-0.957	...	0.986
Out (DSP)	-32768	-32293	-31818	-31343	...	32293
Exp. Out (DSP)	-32768	-32293	-31818	-31343	...	32293

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	50
Max CPU cycles	53
Avg CPU cycles	50

Test case: Inport test OK

Inport test for General block AutoSwitch.

Test results						
Time step	1	2	3	4	...	137
CPU cycles	50	50	50	50	...	50
Inputs						
In1 (DSP)	-32768	-32293	-31818	-31343	...	32293
Switch (DSP)	30005	28152	32440	32440	...	14425
In3 (DSP)	32767	32293	31818	31343	...	-32293
In1	-1	-0.986	-0.971	-0.957	...	0.986
Switch	0.916	0.859	0.99	0.99	...	0.44
In3	1	0.986	0.971	0.957	...	-0.986
Parameters						
Thresh_up	0					
Thresh_down	0					
Outputs						
Out	-1	-0.986	-0.971	-0.957	...	0.986
Exp. Out	-1	-0.986	-0.971	-0.957	...	0.986
Out (DSP)	-32768	-32293	-31818	-31343	...	32293
Exp. Out (DSP)	-32768	-32293	-31818	-31343	...	32293

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	50
Max CPU cycles	50
Avg CPU cycles	50

Test case: Conversion test **OK**

Conversion test for General block AutoSwitch.

Test results						
Time step	1	2	3	4	...	11
Mask parameters						
Thresh_up	0	0.1	0.2	0.5	...	-1.1
Thresh_down	0	0.1	0.2	0.5	...	-1.1
Controller parameters						
Thresh_down	0	3277	6554	16384	...	-32767
Thresh_up	0	3277	6554	16384	...	-32767
Exp. Thresh_down	0	3277	6554	16384	...	-32767
Exp. Thresh_up	0	3277	6554	16384	...	-32767

Test settings	
Tolerance Thresh_down	±0,0000e+00
Tolerance Thresh_up	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block AutoSwitch.

Test results						
Time step	1	2	3	4	...	11
Mask parameters						
Thresh_up	0	0.1	0.2	0.5	...	-1.1
Thresh_down	0	0.1	0.2	0.5	...	-1.1
Controller parameters						
Thresh_down	0	3276	6553	16384	...	-32767
Thresh_up	0	3276	6553	16384	...	-32767
Exp. Thresh_down	0	3277	6554	16384	...	-32767
Exp. Thresh_up	0	3277	6554	16384	...	-32767

Test settings	
Tolerance Thresh_down	±1,0000e+00
Tolerance Thresh_up	±1,0000e+00

Test statistics	
Min CPU cycles	1623
Max CPU cycles	2545
Avg CPU cycles	2426

Verification: AutoSwitch FiP16 CPU XMC4800-F144K2048

Date of Test 2026-06-19

Target controller XMC4800-F144K2048

Test case: Inport test OK

Inport test for General block AutoSwitch.

Test results						
Time step	1	2	3	4	...	137
CPU cycles	61	61	61	61	...	61
Inputs						
In1 (DSP)	-32768	-32293	-31818	-31343	...	32293
Switch (DSP)	30005	28152	32440	32440	...	14425
In3 (DSP)	32767	32293	31818	31343	...	-32293
In1	-1	-0.986	-0.971	-0.957	...	0.986
Switch	0.916	0.859	0.99	0.99	...	0.44
In3	1	0.986	0.971	0.957	...	-0.986
Parameters						
Thresh_up	0.3					
Thresh_down	-0.1					
Outputs						
Out	-1	-0.986	-0.971	-0.957	...	0.986
Exp. Out	-1	-0.986	-0.971	-0.957	...	0.986
Out (DSP)	-32768	-32293	-31818	-31343	...	32293
Exp. Out (DSP)	-32768	-32293	-31818	-31343	...	32293

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	61
Max CPU cycles	66
Avg CPU cycles	63

Test case: Inport test OK

Inport test for General block AutoSwitch.

Test results						
Time step	1	2	3	4	...	137
CPU cycles	61	61	61	61	...	61
Inputs						
In1 (DSP)	-32768	-32293	-31818	-31343	...	32293
Switch (DSP)	30005	28152	32440	32440	...	14425
In3 (DSP)	32767	32293	31818	31343	...	-32293
In1	-1	-0.986	-0.971	-0.957	...	0.986
Switch	0.916	0.859	0.99	0.99	...	0.44
In3	1	0.986	0.971	0.957	...	-0.986
Parameters						
Thresh_up	0					
Thresh_down	0					
Outputs						
Out	-1	-0.986	-0.971	-0.957	...	0.986
Exp. Out	-1	-0.986	-0.971	-0.957	...	0.986
Out (DSP)	-32768	-32293	-31818	-31343	...	32293
Exp. Out (DSP)	-32768	-32293	-31818	-31343	...	32293

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	61
Max CPU cycles	66
Avg CPU cycles	63

Test case: Conversion test **OK**

Conversion test for General block AutoSwitch.

Test results						
Time step	1	2	3	4	...	11
Mask parameters						
Thresh_up	0	0.1	0.2	0.5	...	-1.1
Thresh_down	0	0.1	0.2	0.5	...	-1.1
Controller parameters						
Thresh_down	0	3277	6554	16384	...	-32767
Thresh_up	0	3277	6554	16384	...	-32767
Exp. Thresh_down	0	3277	6554	16384	...	-32767
Exp. Thresh_up	0	3277	6554	16384	...	-32767

Test settings	
Tolerance Thresh_down	±0,0000e+00
Tolerance Thresh_up	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block AutoSwitch.

Test results						
Time step	1	2	3	4	...	11
Mask parameters						
Thresh_up	0	0.1	0.2	0.5	...	-1.1
Thresh_down	0	0.1	0.2	0.5	...	-1.1
Controller parameters						
Thresh_down	0	3276	6553	16384	...	-32767
Thresh_up	0	3276	6553	16384	...	-32767
Exp. Thresh_down	0	3277	6554	16384	...	-32767
Exp. Thresh_up	0	3277	6554	16384	...	-32767

Test settings	
Tolerance Thresh_down	±1,0000e+00
Tolerance Thresh_up	±1,0000e+00

Test statistics	
Min CPU cycles	613
Max CPU cycles	757
Avg CPU cycles	626

Verification: AutoSwitch FiP16 CPU TMS320F28379D

Date of Test 2026-06-22

Target controller TMS320F28379D

Test case: Inport test OK

Inport test for General block AutoSwitch.

Test results						
Time step	1	2	3	4	...	137
CPU cycles	54	54	54	54	...	54
Inputs						
In1 (DSP)	-32768	-32293	-31818	-31343	...	32293
Switch (DSP)	30005	28152	32440	32440	...	14425
In3 (DSP)	32767	32293	31818	31343	...	-32293
In1	-1	-0.986	-0.971	-0.957	...	0.986
Switch	0.916	0.859	0.99	0.99	...	0.44
In3	1	0.986	0.971	0.957	...	-0.986
Parameters						
Thresh_up	0.3					
Thresh_down	-0.1					
Outputs						
Out	-1	-0.986	-0.971	-0.957	...	0.986
Exp. Out	-1	-0.986	-0.971	-0.957	...	0.986
Out (DSP)	-32768	-32293	-31818	-31343	...	32293
Exp. Out (DSP)	-32768	-32293	-31818	-31343	...	32293

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	54
Max CPU cycles	69
Avg CPU cycles	61

Test case: Inport test OK

Inport test for General block AutoSwitch.

Test results						
Time step	1	2	3	4	...	137
CPU cycles	54	54	54	54	...	54
Inputs						
In1 (DSP)	-32768	-32293	-31818	-31343	...	32293
Switch (DSP)	30005	28152	32440	32440	...	14425
In3 (DSP)	32767	32293	31818	31343	...	-32293
In1	-1	-0.986	-0.971	-0.957	...	0.986
Switch	0.916	0.859	0.99	0.99	...	0.44
In3	1	0.986	0.971	0.957	...	-0.986
Parameters						
Thresh_up	0					
Thresh_down	0					
Outputs						
Out	-1	-0.986	-0.971	-0.957	...	0.986
Exp. Out	-1	-0.986	-0.971	-0.957	...	0.986
Out (DSP)	-32768	-32293	-31818	-31343	...	32293
Exp. Out (DSP)	-32768	-32293	-31818	-31343	...	32293

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	54
Max CPU cycles	69
Avg CPU cycles	60

Test case: Conversion test **OK**

Conversion test for General block AutoSwitch.

Test results						
Time step	1	2	3	4	...	11
Mask parameters						
Thresh_up	0	0.1	0.2	0.5	...	-1.1
Thresh_down	0	0.1	0.2	0.5	...	-1.1
Controller parameters						
Thresh_down	0	3277	6554	16384	...	-32767
Thresh_up	0	3277	6554	16384	...	-32767
Exp. Thresh_down	0	3277	6554	16384	...	-32767
Exp. Thresh_up	0	3277	6554	16384	...	-32767

Test settings	
Tolerance Thresh_down	±0,0000e+00
Tolerance Thresh_up	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block AutoSwitch.

Test results						
Time step	1	2	3	4	...	11
Mask parameters						
Thresh_up	0	0.1	0.2	0.5	...	-1.1
Thresh_down	0	0.1	0.2	0.5	...	-1.1
Controller parameters						
Thresh_down	0	3276	6553	16384	...	-32767
Thresh_up	0	3276	6553	16384	...	-32767
Exp. Thresh_down	0	3277	6554	16384	...	-32767
Exp. Thresh_up	0	3277	6554	16384	...	-32767

Test settings	
Tolerance Thresh_down	±1,0000e+00
Tolerance Thresh_up	±1,0000e+00

Test statistics	
Min CPU cycles	976
Max CPU cycles	984
Avg CPU cycles	978

Verification: AutoSwitch FiP32 CPU TMS320F28335

Date of Test 2026-06-19

Target controller TMS320F28335

Test case: Inport test OK

Inport test for General block AutoSwitch.

Test results				
Time step	1	2	...	137
CPU cycles	70	70	...	70
Inputs				
In1 (DSP)	-2147483648	-2116360697	...	2116360697
Switch (DSP)	1966424482	1844940891	...	945361786
In3 (DSP)	2147483647	2116360697	...	-2116360697
In1	-1	-0.986	...	0.986
Switch	0.916	0.859	...	0.44
In3	1	0.986	...	-0.986
Parameters				
Thresh_up	0.3			
Thresh_down	-0.1			
Outputs				
Out	-1	-0.986	...	0.986
Exp. Out	-1	-0.986	...	0.986
Out (DSP)	-2147483648	-2116360697	...	2116360697
Exp. Out (DSP)	-2147483648	-2116360697	...	2116360697

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	70
Max CPU cycles	79
Avg CPU cycles	74

Test case: Inport test OK

Inport test for General block AutoSwitch.

Test results				
Time step	1	2	...	137
CPU cycles	70	70	...	70
Inputs				
In1 (DSP)	-2147483648	-2116360697	...	2116360697
Switch (DSP)	1966424482	1844940891	...	945361786
In3 (DSP)	2147483647	2116360697	...	-2116360697
In1	-1	-0.986	...	0.986
Switch	0.916	0.859	...	0.44
In3	1	0.986	...	-0.986
Parameters				
Thresh_up	0			
Thresh_down	0			
Outputs				
Out	-1	-0.986	...	0.986
Exp. Out	-1	-0.986	...	0.986
Out (DSP)	-2147483648	-2116360697	...	2116360697
Exp. Out (DSP)	-2147483648	-2116360697	...	2116360697

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	70
Max CPU cycles	79
Avg CPU cycles	74

Test case: Conversion test **OK**

Conversion test for General block AutoSwitch.

Test results				
Time step	1	2	...	11
Mask parameters				
Thresh_up	0	0.1	...	-1.1
Thresh_down	0	0.1	...	-1.1
Controller parameters				
Thresh_down	0	214748365	...	-2147483647
Thresh_up	0	214748365	...	-2147483647
Exp. Thresh_down	0	214748365	...	-2147483647
Exp. Thresh_up	0	214748365	...	-2147483647

Test settings	
Tolerance Thresh_down	±0,0000e+00
Tolerance Thresh_up	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block AutoSwitch.

Test results				
Time step	1	2	...	11
Mask parameters				
Thresh_up	0	0.1	...	-1.1
Thresh_down	0	0.1	...	-1.1
Controller parameters				
Thresh_down	0	214748368	...	-2147483647
Thresh_up	0	214748368	...	-2147483647
Exp. Thresh_down	0	214748365	...	-2147483647
Exp. Thresh_up	0	214748365	...	-2147483647

Test settings	
Tolerance Thresh_down	±6,0000e+00
Tolerance Thresh_up	±6,0000e+00

Test statistics	
Min CPU cycles	1671
Max CPU cycles	1791
Avg CPU cycles	1753

Verification: AutoSwitch FiP32 CPU TM4C123GH6

Date of Test 2026-06-19

Target controller TM4C123GH6

Test case: Inport test OK

Inport test for General block AutoSwitch.

Test results				
Time step	1	2	...	137
CPU cycles	31	31	...	31
Inputs				
In1 (DSP)	-2147483648	-2116360697	...	2116360697
Switch (DSP)	1966424482	1844940891	...	945361786
In3 (DSP)	2147483647	2116360697	...	-2116360697
In1	-1	-0.986	...	0.986
Switch	0.916	0.859	...	0.44
In3	1	0.986	...	-0.986
Parameters				
Thresh_up	0.3			
Thresh_down	-0.1			
Outputs				
Out	-1	-0.986	...	0.986
Exp. Out	-1	-0.986	...	0.986
Out (DSP)	-2147483648	-2116360697	...	2116360697
Exp. Out (DSP)	-2147483648	-2116360697	...	2116360697

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	31
Max CPU cycles	37
Avg CPU cycles	34

Test case: Inport test OK

Inport test for General block AutoSwitch.

Test results				
Time step	1	2	...	137
CPU cycles	31	31	...	31
Inputs				
In1 (DSP)	-2147483648	-2116360697	...	2116360697
Switch (DSP)	1966424482	1844940891	...	945361786
In3 (DSP)	2147483647	2116360697	...	-2116360697
In1	-1	-0.986	...	0.986
Switch	0.916	0.859	...	0.44
In3	1	0.986	...	-0.986
Parameters				
Thresh_up	0			
Thresh_down	0			
Outputs				
Out	-1	-0.986	...	0.986
Exp. Out	-1	-0.986	...	0.986
Out (DSP)	-2147483648	-2116360697	...	2116360697
Exp. Out (DSP)	-2147483648	-2116360697	...	2116360697

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	31
Max CPU cycles	37
Avg CPU cycles	33

Test case: Conversion test **OK**

Conversion test for General block AutoSwitch.

Test results				
Time step	1	2	...	11
Mask parameters				
Thresh_up	0	0.1	...	-1.1
Thresh_down	0	0.1	...	-1.1
Controller parameters				
Thresh_down	0	214748365	...	-2147483647
Thresh_up	0	214748365	...	-2147483647
Exp. Thresh_down	0	214748365	...	-2147483647
Exp. Thresh_up	0	214748365	...	-2147483647

Test settings	
Tolerance Thresh_down	±0,0000e+00
Tolerance Thresh_up	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block AutoSwitch.

Test results				
Time step	1	2	...	11
Mask parameters				
Thresh_up	0	0.1	...	-1.1
Thresh_down	0	0.1	...	-1.1
Controller parameters				
Thresh_down	0	214748368	...	-2147483647
Thresh_up	0	214748368	...	-2147483647
Exp. Thresh_down	0	214748365	...	-2147483647
Exp. Thresh_up	0	214748365	...	-2147483647

Test settings	
Tolerance Thresh_down	±6,0000e+00
Tolerance Thresh_up	±6,0000e+00

Test statistics	
Min CPU cycles	737
Max CPU cycles	793
Avg CPU cycles	783

Verification: AutoSwitch FiP32 CPU STM32G474RE

Date of Test 2026-06-19

Target controller STM32G474RE

Test case: Inport test OK

Inport test for General block AutoSwitch.

Test results				
Time step	1	2	...	137
CPU cycles	62	62	...	62
Inputs				
In1 (DSP)	-2147483648	-2116360697	...	2116360697
Switch (DSP)	1966424482	1844940891	...	945361786
In3 (DSP)	2147483647	2116360697	...	-2116360697
In1	-1	-0.986	...	0.986
Switch	0.916	0.859	...	0.44
In3	1	0.986	...	-0.986
Parameters				
Thresh_up	0.3			
Thresh_down	-0.1			
Outputs				
Out	-1	-0.986	...	0.986
Exp. Out	-1	-0.986	...	0.986
Out (DSP)	-2147483648	-2116360697	...	2116360697
Exp. Out (DSP)	-2147483648	-2116360697	...	2116360697

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	62
Max CPU cycles	72
Avg CPU cycles	67

Test case: Inport test OK

Inport test for General block AutoSwitch.

Test results				
Time step	1	2	...	137
CPU cycles	62	62	...	62
Inputs				
In1 (DSP)	-2147483648	-2116360697	...	2116360697
Switch (DSP)	1966424482	1844940891	...	945361786
In3 (DSP)	2147483647	2116360697	...	-2116360697
In1	-1	-0.986	...	0.986
Switch	0.916	0.859	...	0.44
In3	1	0.986	...	-0.986
Parameters				
Thresh_up	0			
Thresh_down	0			
Outputs				
Out	-1	-0.986	...	0.986
Exp. Out	-1	-0.986	...	0.986
Out (DSP)	-2147483648	-2116360697	...	2116360697
Exp. Out (DSP)	-2147483648	-2116360697	...	2116360697

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	62
Max CPU cycles	72
Avg CPU cycles	66

Test case: Conversion test **OK**

Conversion test for General block AutoSwitch.

Test results				
Time step	1	2	...	11
Mask parameters				
Thresh_up	0	0.1	...	-1.1
Thresh_down	0	0.1	...	-1.1
Controller parameters				
Thresh_down	0	214748365	...	-2147483647
Thresh_up	0	214748365	...	-2147483647
Exp. Thresh_down	0	214748365	...	-2147483647
Exp. Thresh_up	0	214748365	...	-2147483647

Test settings	
Tolerance Thresh_down	±0,0000e+00
Tolerance Thresh_up	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block AutoSwitch.

Test results				
Time step	1	2	...	11
Mask parameters				
Thresh_up	0	0.1	...	-1.1
Thresh_down	0	0.1	...	-1.1
Controller parameters				
Thresh_down	0	214748368	...	-2147483647
Thresh_up	0	214748368	...	-2147483647
Exp. Thresh_down	0	214748365	...	-2147483647
Exp. Thresh_up	0	214748365	...	-2147483647

Test settings	
Tolerance Thresh_down	±6,0000e+00
Tolerance Thresh_up	±6,0000e+00

Test statistics	
Min CPU cycles	1418
Max CPU cycles	1503
Avg CPU cycles	1481

Verification: AutoSwitch FiP32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for General block AutoSwitch.

Test results				
Time step	1	2	...	137
CPU cycles	56	56	...	56
Inputs				
In1 (DSP)	-2147483648	-2116360697	...	2116360697
Switch (DSP)	1966424482	1844940891	...	945361786
In3 (DSP)	2147483647	2116360697	...	-2116360697
In1	-1	-0.986	...	0.986
Switch	0.916	0.859	...	0.44
In3	1	0.986	...	-0.986
Parameters				
Thresh_up	0.3			
Thresh_down	-0.1			
Outputs				
Out	-1	-0.986	...	0.986
Exp. Out	-1	-0.986	...	0.986
Out (DSP)	-2147483648	-2116360697	...	2116360697
Exp. Out (DSP)	-2147483648	-2116360697	...	2116360697

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	56
Max CPU cycles	68
Avg CPU cycles	62

Test case: Inport test OK

Inport test for General block AutoSwitch.

Test results				
Time step	1	2	...	137
CPU cycles	56	56	...	56
Inputs				
In1 (DSP)	-2147483648	-2116360697	...	2116360697
Switch (DSP)	1966424482	1844940891	...	945361786
In3 (DSP)	2147483647	2116360697	...	-2116360697
In1	-1	-0.986	...	0.986
Switch	0.916	0.859	...	0.44
In3	1	0.986	...	-0.986
Parameters				
Thresh_up	0			
Thresh_down	0			
Outputs				
Out	-1	-0.986	...	0.986
Exp. Out	-1	-0.986	...	0.986
Out (DSP)	-2147483648	-2116360697	...	2116360697
Exp. Out (DSP)	-2147483648	-2116360697	...	2116360697

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	56
Max CPU cycles	68
Avg CPU cycles	61

Test case: Conversion test **OK**

Conversion test for General block AutoSwitch.

Test results				
Time step	1	2	...	11
Mask parameters				
Thresh_up	0	0.1	...	-1.1
Thresh_down	0	0.1	...	-1.1
Controller parameters				
Thresh_down	0	214748365	...	-2147483647
Thresh_up	0	214748365	...	-2147483647
Exp. Thresh_down	0	214748365	...	-2147483647
Exp. Thresh_up	0	214748365	...	-2147483647

Test settings	
Tolerance Thresh_down	±0,0000e+00
Tolerance Thresh_up	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block AutoSwitch.

Test results				
Time step	1	2	...	11
Mask parameters				
Thresh_up	0	0.1	...	-1.1
Thresh_down	0	0.1	...	-1.1
Controller parameters				
Thresh_down	0	214748368	...	-2147483647
Thresh_up	0	214748368	...	-2147483647
Exp. Thresh_down	0	214748365	...	-2147483647
Exp. Thresh_up	0	214748365	...	-2147483647

Test settings	
Tolerance Thresh_down	±6,0000e+00
Tolerance Thresh_up	±6,0000e+00

Test statistics	
Min CPU cycles	3451
Max CPU cycles	4689
Avg CPU cycles	4252

Verification: AutoSwitch FiP32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for General block AutoSwitch.

Test results				
Time step	1	2	...	137
CPU cycles	39	39	...	39
Inputs				
In1 (DSP)	-2147483648	-2116360697	...	2116360697
Switch (DSP)	1966424482	1844940891	...	945361786
In3 (DSP)	2147483647	2116360697	...	-2116360697
In1	-1	-0.986	...	0.986
Switch	0.916	0.859	...	0.44
In3	1	0.986	...	-0.986
Parameters				
Thresh_up	0.3			
Thresh_down	-0.1			
Outputs				
Out	-1	-0.986	...	0.986
Exp. Out	-1	-0.986	...	0.986
Out (DSP)	-2147483648	-2116360697	...	2116360697
Exp. Out (DSP)	-2147483648	-2116360697	...	2116360697

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	39
Max CPU cycles	43
Avg CPU cycles	41

Test case: Inport test OK

Inport test for General block AutoSwitch.

Test results				
Time step	1	2	...	137
CPU cycles	39	39	...	39
Inputs				
In1 (DSP)	-2147483648	-2116360697	...	2116360697
Switch (DSP)	1966424482	1844940891	...	945361786
In3 (DSP)	2147483647	2116360697	...	-2116360697
In1	-1	-0.986	...	0.986
Switch	0.916	0.859	...	0.44
In3	1	0.986	...	-0.986
Parameters				
Thresh_up	0			
Thresh_down	0			
Outputs				
Out	-1	-0.986	...	0.986
Exp. Out	-1	-0.986	...	0.986
Out (DSP)	-2147483648	-2116360697	...	2116360697
Exp. Out (DSP)	-2147483648	-2116360697	...	2116360697

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	39
Max CPU cycles	43
Avg CPU cycles	40

Test case: Conversion test **OK**

Conversion test for General block AutoSwitch.

Test results				
Time step	1	2	...	11
Mask parameters				
Thresh_up	0	0.1	...	-1.1
Thresh_down	0	0.1	...	-1.1
Controller parameters				
Thresh_down	0	214748365	...	-2147483647
Thresh_up	0	214748365	...	-2147483647
Exp. Thresh_down	0	214748365	...	-2147483647
Exp. Thresh_up	0	214748365	...	-2147483647

Test settings	
Tolerance Thresh_down	±0,0000e+00
Tolerance Thresh_up	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block AutoSwitch.

Test results				
Time step	1	2	...	11
Mask parameters				
Thresh_up	0	0.1	...	-1.1
Thresh_down	0	0.1	...	-1.1
Controller parameters				
Thresh_down	0	214748368	...	-2147483647
Thresh_up	0	214748368	...	-2147483647
Exp. Thresh_down	0	214748365	...	-2147483647
Exp. Thresh_up	0	214748365	...	-2147483647

Test settings	
Tolerance Thresh_down	±6,0000e+00
Tolerance Thresh_up	±6,0000e+00

Test statistics	
Min CPU cycles	1334
Max CPU cycles	1572
Avg CPU cycles	1536

Verification: AutoSwitch FiP32 CPU dsPIC33EP256MC502

Date of Test 2026-06-19

Target controller dsPIC33EP256MC502

Test case: Inport test OK

Inport test for General block AutoSwitch.

Test results				
Time step	1	2	...	137
CPU cycles	55	55	...	55
Inputs				
In1 (DSP)	-2147483648	-2116360697	...	2116360697
Switch (DSP)	1966424482	1844940891	...	945361786
In3 (DSP)	2147483647	2116360697	...	-2116360697
In1	-1	-0.986	...	0.986
Switch	0.916	0.859	...	0.44
In3	1	0.986	...	-0.986
Parameters				
Thresh_up	0.3			
Thresh_down	-0.1			
Outputs				
Out	-1	-0.986	...	0.986
Exp. Out	-1	-0.986	...	0.986
Out (DSP)	-2147483648	-2116360697	...	2116360697
Exp. Out (DSP)	-2147483648	-2116360697	...	2116360697

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	55
Max CPU cycles	60
Avg CPU cycles	56

Test case: Inport test OK

Inport test for General block AutoSwitch.

Test results				
Time step	1	2	...	137
CPU cycles	55	55	...	55
Inputs				
In1 (DSP)	-2147483648	-2116360697	...	2116360697
Switch (DSP)	1966424482	1844940891	...	945361786
In3 (DSP)	2147483647	2116360697	...	-2116360697
In1	-1	-0.986	...	0.986
Switch	0.916	0.859	...	0.44
In3	1	0.986	...	-0.986
Parameters				
Thresh_up	0			
Thresh_down	0			
Outputs				
Out	-1	-0.986	...	0.986
Exp. Out	-1	-0.986	...	0.986
Out (DSP)	-2147483648	-2116360697	...	2116360697
Exp. Out (DSP)	-2147483648	-2116360697	...	2116360697

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	55
Max CPU cycles	57
Avg CPU cycles	55

Test case: Conversion test **OK**

Conversion test for General block AutoSwitch.

Test results				
Time step	1	2	...	11
Mask parameters				
Thresh_up	0	0.1	...	-1.1
Thresh_down	0	0.1	...	-1.1
Controller parameters				
Thresh_down	0	214748365	...	-2147483647
Thresh_up	0	214748365	...	-2147483647
Exp. Thresh_down	0	214748365	...	-2147483647
Exp. Thresh_up	0	214748365	...	-2147483647

Test settings	
Tolerance Thresh_down	±0,0000e+00
Tolerance Thresh_up	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block AutoSwitch.

Test results				
Time step	1	2	...	11
Mask parameters				
Thresh_up	0	0.1	...	-1.1
Thresh_down	0	0.1	...	-1.1
Controller parameters				
Thresh_down	0	214748368	...	-2147483647
Thresh_up	0	214748368	...	-2147483647
Exp. Thresh_down	0	214748365	...	-2147483647
Exp. Thresh_up	0	214748365	...	-2147483647

Test settings	
Tolerance Thresh_down	±6,0000e+00
Tolerance Thresh_up	±6,0000e+00

Test statistics	
Min CPU cycles	2253
Max CPU cycles	3159
Avg CPU cycles	3045

Verification: AutoSwitch FiP32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for General block AutoSwitch.

Test results				
Time step	1	2	...	137
CPU cycles	61	61	...	61
Inputs				
In1 (DSP)	-2147483648	-2116360697	...	2116360697
Switch (DSP)	1966424482	1844940891	...	945361786
In3 (DSP)	2147483647	2116360697	...	-2116360697
In1	-1	-0.986	...	0.986
Switch	0.916	0.859	...	0.44
In3	1	0.986	...	-0.986
Parameters				
Thresh_up	0.3			
Thresh_down	-0.1			
Outputs				
Out	-1	-0.986	...	0.986
Exp. Out	-1	-0.986	...	0.986
Out (DSP)	-2147483648	-2116360697	...	2116360697
Exp. Out (DSP)	-2147483648	-2116360697	...	2116360697

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	61
Max CPU cycles	66
Avg CPU cycles	63

Test case: Inport test OK

Inport test for General block AutoSwitch.

Test results				
Time step	1	2	...	137
CPU cycles	61	61	...	61
Inputs				
In1 (DSP)	-2147483648	-2116360697	...	2116360697
Switch (DSP)	1966424482	1844940891	...	945361786
In3 (DSP)	2147483647	2116360697	...	-2116360697
In1	-1	-0.986	...	0.986
Switch	0.916	0.859	...	0.44
In3	1	0.986	...	-0.986
Parameters				
Thresh_up	0			
Thresh_down	0			
Outputs				
Out	-1	-0.986	...	0.986
Exp. Out	-1	-0.986	...	0.986
Out (DSP)	-2147483648	-2116360697	...	2116360697
Exp. Out (DSP)	-2147483648	-2116360697	...	2116360697

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	61
Max CPU cycles	66
Avg CPU cycles	63

Test case: Conversion test **OK**

Conversion test for General block AutoSwitch.

Test results				
Time step	1	2	...	11
Mask parameters				
Thresh_up	0	0.1	...	-1.1
Thresh_down	0	0.1	...	-1.1
Controller parameters				
Thresh_down	0	214748365	...	-2147483647
Thresh_up	0	214748365	...	-2147483647
Exp. Thresh_down	0	214748365	...	-2147483647
Exp. Thresh_up	0	214748365	...	-2147483647

Test settings	
Tolerance Thresh_down	±0,0000e+00
Tolerance Thresh_up	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block AutoSwitch.

Test results				
Time step	1	2	...	11
Mask parameters				
Thresh_up	0	0.1	...	-1.1
Thresh_down	0	0.1	...	-1.1
Controller parameters				
Thresh_down	0	214748368	...	-2147483647
Thresh_up	0	214748368	...	-2147483647
Exp. Thresh_down	0	214748365	...	-2147483647
Exp. Thresh_up	0	214748365	...	-2147483647

Test settings	
Tolerance Thresh_down	±6,0000e+00
Tolerance Thresh_up	±6,0000e+00

Test statistics	
Min CPU cycles	1155
Max CPU cycles	1287
Avg CPU cycles	1182

Verification: AutoSwitch FiP32 CPU TMS320F28379D

Date of Test 2026-06-22

Target controller TMS320F28379D

Test case: Inport test OK

Inport test for General block AutoSwitch.

Test results				
Time step	1	2	...	137
CPU cycles	55	55	...	55
Inputs				
In1 (DSP)	-2147483648	-2116360697	...	2116360697
Switch (DSP)	1966424482	1844940891	...	945361786
In3 (DSP)	2147483647	2116360697	...	-2116360697
In1	-1	-0.986	...	0.986
Switch	0.916	0.859	...	0.44
In3	1	0.986	...	-0.986
Parameters				
Thresh_up	0.3			
Thresh_down	-0.1			
Outputs				
Out	-1	-0.986	...	0.986
Exp. Out	-1	-0.986	...	0.986
Out (DSP)	-2147483648	-2116360697	...	2116360697
Exp. Out (DSP)	-2147483648	-2116360697	...	2116360697

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	55
Max CPU cycles	69
Avg CPU cycles	61

Test case: Inport test OK

Inport test for General block AutoSwitch.

Test results				
Time step	1	2	...	137
CPU cycles	55	55	...	55
Inputs				
In1 (DSP)	-2147483648	-2116360697	...	2116360697
Switch (DSP)	1966424482	1844940891	...	945361786
In3 (DSP)	2147483647	2116360697	...	-2116360697
In1	-1	-0.986	...	0.986
Switch	0.916	0.859	...	0.44
In3	1	0.986	...	-0.986
Parameters				
Thresh_up	0			
Thresh_down	0			
Outputs				
Out	-1	-0.986	...	0.986
Exp. Out	-1	-0.986	...	0.986
Out (DSP)	-2147483648	-2116360697	...	2116360697
Exp. Out (DSP)	-2147483648	-2116360697	...	2116360697

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	55
Max CPU cycles	69
Avg CPU cycles	61

Test case: Conversion test **OK**

Conversion test for General block AutoSwitch.

Test results				
Time step	1	2	...	11
Mask parameters				
Thresh_up	0	0.1	...	-1.1
Thresh_down	0	0.1	...	-1.1
Controller parameters				
Thresh_down	0	214748365	...	-2147483647
Thresh_up	0	214748365	...	-2147483647
Exp. Thresh_down	0	214748365	...	-2147483647
Exp. Thresh_up	0	214748365	...	-2147483647

Test settings	
Tolerance Thresh_down	±0,0000e+00
Tolerance Thresh_up	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block AutoSwitch.

Test results				
Time step	1	2	...	11
Mask parameters				
Thresh_up	0	0.1	...	-1.1
Thresh_down	0	0.1	...	-1.1
Controller parameters				
Thresh_down	0	214748368	...	-2147483647
Thresh_up	0	214748368	...	-2147483647
Exp. Thresh_down	0	214748365	...	-2147483647
Exp. Thresh_up	0	214748365	...	-2147483647

Test settings	
Tolerance Thresh_down	±6,0000e+00
Tolerance Thresh_up	±6,0000e+00

Test statistics	
Min CPU cycles	1235
Max CPU cycles	1315
Avg CPU cycles	1288

Verification: AutoSwitch Float32 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for General block AutoSwitch.

Test results				
Time step	1	2	...	137
CPU cycles	73	73	...	73
Inputs				
In1 (DSP)	-1	-0.986	...	0.986
Switch (DSP)	0.916	0.859	...	0.44
In3 (DSP)	1	0.986	...	-0.986
In1	-1	-0.986	...	0.986
Switch	0.916	0.859	...	0.44
In3	1	0.986	...	-0.986
Parameters				
Thresh_up	0.3			
Thresh_down	-0.1			
Outputs				
Out	-1	-0.986	...	0.986
Exp. Out	-1	-0.986	...	0.986
Out (DSP)	-1	-0.986	...	0.986
Exp. Out (DSP)	-1	-0.986	...	0.986

Test settings	
Tolerance Out	±3,0268e-08 (±65 LSB)

Test statistics	
Min CPU cycles	73
Max CPU cycles	83
Avg CPU cycles	78

Test case: Inport test OK

Inport test for General block AutoSwitch.

Test results				
Time step	1	2	...	137
CPU cycles	73	73	...	73
Inputs				
In1 (DSP)	-1	-0.986	...	0.986
Switch (DSP)	0.916	0.859	...	0.44
In3 (DSP)	1	0.986	...	-0.986
In1	-1	-0.986	...	0.986
Switch	0.916	0.859	...	0.44
In3	1	0.986	...	-0.986
Parameters				
Thresh_up	0			
Thresh_down	0			
Outputs				
Out	-1	-0.986	...	0.986
Exp. Out	-1	-0.986	...	0.986
Out (DSP)	-1	-0.986	...	0.986
Exp. Out (DSP)	-1	-0.986	...	0.986

Test settings	
Tolerance Out	±3,0268e-08 (±65 LSB)

Test statistics	
Min CPU cycles	73
Max CPU cycles	83
Avg CPU cycles	77

Test case: Conversion test **OK**

Conversion test for General block AutoSwitch.

Test results				
Time step	1	2	...	11
Mask parameters				
Thresh_up	0	0.1	...	-1.1
Thresh_down	0	0.1	...	-1.1
Controller parameters				
Thresh_down	0	0.1	...	-1.1
Thresh_up	0	0.1	...	-1.1
Exp. Thresh_down	0	0.1	...	-1.1
Exp. Thresh_up	0	0.1	...	-1.1

Test settings	
Tolerance Thresh_down	±0,0000e+00
Tolerance Thresh_up	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block AutoSwitch.

Test results				
Time step	1	2	...	11
Mask parameters				
Thresh_up	0	0.1	...	-1.1
Thresh_down	0	0.1	...	-1.1
Controller parameters				
Thresh_down	0	0.1	...	-1.1
Thresh_up	0	0.1	...	-1.1
Exp. Thresh_down	0	0.1	...	-1.1
Exp. Thresh_up	0	0.1	...	-1.1

Test settings	
Tolerance Thresh_down	±3,0000e-08
Tolerance Thresh_up	±3,0000e-08

Test statistics	
Min CPU cycles	1265
Max CPU cycles	1299
Avg CPU cycles	1268

Verification: AutoSwitch Float32 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for General block AutoSwitch.

Test results				
Time step	1	2	...	137
CPU cycles	35	35	...	35
Inputs				
In1 (DSP)	-1	-0.986	...	0.986
Switch (DSP)	0.916	0.859	...	0.44
In3 (DSP)	1	0.986	...	-0.986
In1	-1	-0.986	...	0.986
Switch	0.916	0.859	...	0.44
In3	1	0.986	...	-0.986
Parameters				
Thresh_up	0.3			
Thresh_down	-0.1			
Outputs				
Out	-1	-0.986	...	0.986
Exp. Out	-1	-0.986	...	0.986
Out (DSP)	-1	-0.986	...	0.986
Exp. Out (DSP)	-1	-0.986	...	0.986

Test settings	
Tolerance Out	±3,0268e-08 (±65 LSB)

Test statistics	
Min CPU cycles	35
Max CPU cycles	43
Avg CPU cycles	39

Test case: Inport test OK

Inport test for General block AutoSwitch.

Test results				
Time step	1	2	...	137
CPU cycles	35	35	...	35
Inputs				
In1 (DSP)	-1	-0.986	...	0.986
Switch (DSP)	0.916	0.859	...	0.44
In3 (DSP)	1	0.986	...	-0.986
In1	-1	-0.986	...	0.986
Switch	0.916	0.859	...	0.44
In3	1	0.986	...	-0.986
Parameters				
Thresh_up	0			
Thresh_down	0			
Outputs				
Out	-1	-0.986	...	0.986
Exp. Out	-1	-0.986	...	0.986
Out (DSP)	-1	-0.986	...	0.986
Exp. Out (DSP)	-1	-0.986	...	0.986

Test settings	
Tolerance Out	±3,0268e-08 (±65 LSB)

Test statistics	
Min CPU cycles	35
Max CPU cycles	43
Avg CPU cycles	38

Test case: Conversion test **OK**

Conversion test for General block AutoSwitch.

Test results				
Time step	1	2	...	11
Mask parameters				
Thresh_up	0	0.1	...	-1.1
Thresh_down	0	0.1	...	-1.1
Controller parameters				
Thresh_down	0	0.1	...	-1.1
Thresh_up	0	0.1	...	-1.1
Exp. Thresh_down	0	0.1	...	-1.1
Exp. Thresh_up	0	0.1	...	-1.1

Test settings	
Tolerance Thresh_down	±0,0000e+00
Tolerance Thresh_up	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block AutoSwitch.

Test results				
Time step	1	2	...	11
Mask parameters				
Thresh_up	0	0.1	...	-1.1
Thresh_down	0	0.1	...	-1.1
Controller parameters				
Thresh_down	0	0.1	...	-1.1
Thresh_up	0	0.1	...	-1.1
Exp. Thresh_down	0	0.1	...	-1.1
Exp. Thresh_up	0	0.1	...	-1.1

Test settings	
Tolerance Thresh_down	±3,0000e-08
Tolerance Thresh_up	±3,0000e-08

Test statistics	
Min CPU cycles	613
Max CPU cycles	613
Avg CPU cycles	613

Verification: AutoSwitch Float32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for General block AutoSwitch.

Test results				
Time step	1	2	...	137
CPU cycles	67	67	...	67
Inputs				
In1 (DSP)	-1	-0.986	...	0.986
Switch (DSP)	0.916	0.859	...	0.44
In3 (DSP)	1	0.986	...	-0.986
In1	-1	-0.986	...	0.986
Switch	0.916	0.859	...	0.44
In3	1	0.986	...	-0.986
Parameters				
Thresh_up	0.3			
Thresh_down	-0.1			
Outputs				
Out	-1	-0.986	...	0.986
Exp. Out	-1	-0.986	...	0.986
Out (DSP)	-1	-0.986	...	0.986
Exp. Out (DSP)	-1	-0.986	...	0.986

Test settings	
Tolerance Out	±3,0268e-08 (±65 LSB)

Test statistics	
Min CPU cycles	67
Max CPU cycles	87
Avg CPU cycles	78

Test case: Inport test OK

Inport test for General block AutoSwitch.

Test results				
Time step	1	2	...	137
CPU cycles	67	67	...	67
Inputs				
In1 (DSP)	-1	-0.986	...	0.986
Switch (DSP)	0.916	0.859	...	0.44
In3 (DSP)	1	0.986	...	-0.986
In1	-1	-0.986	...	0.986
Switch	0.916	0.859	...	0.44
In3	1	0.986	...	-0.986
Parameters				
Thresh_up	0			
Thresh_down	0			
Outputs				
Out	-1	-0.986	...	0.986
Exp. Out	-1	-0.986	...	0.986
Out (DSP)	-1	-0.986	...	0.986
Exp. Out (DSP)	-1	-0.986	...	0.986

Test settings	
Tolerance Out	±3,0268e-08 (±65 LSB)

Test statistics	
Min CPU cycles	67
Max CPU cycles	87
Avg CPU cycles	75

Test case: Conversion test **OK**

Conversion test for General block AutoSwitch.

Test results				
Time step	1	2	...	11
Mask parameters				
Thresh_up	0	0.1	...	-1.1
Thresh_down	0	0.1	...	-1.1
Controller parameters				
Thresh_down	0	0.1	...	-1.1
Thresh_up	0	0.1	...	-1.1
Exp. Thresh_down	0	0.1	...	-1.1
Exp. Thresh_up	0	0.1	...	-1.1

Test settings	
Tolerance Thresh_down	±0,0000e+00
Tolerance Thresh_up	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block AutoSwitch.

Test results				
Time step	1	2	...	11
Mask parameters				
Thresh_up	0	0.1	...	-1.1
Thresh_down	0	0.1	...	-1.1
Controller parameters				
Thresh_down	0	0.1	...	-1.1
Thresh_up	0	0.1	...	-1.1
Exp. Thresh_down	0	0.1	...	-1.1
Exp. Thresh_up	0	0.1	...	-1.1

Test settings	
Tolerance Thresh_down	±3,0000e-08
Tolerance Thresh_up	±3,0000e-08

Test statistics	
Min CPU cycles	718
Max CPU cycles	718
Avg CPU cycles	718

Verification: AutoSwitch Float32 CPU STM32F072RB

Date of Test 2026-06-19

Target controller STM32F072RB

Test case: Inport test OK

Inport test for General block AutoSwitch.

Test results				
Time step	1	2	...	137
CPU cycles	153	153	...	156
Inputs				
In1 (DSP)	-1	-0.986	...	0.986
Switch (DSP)	0.916	0.859	...	0.44
In3 (DSP)	1	0.986	...	-0.986
In1	-1	-0.986	...	0.986
Switch	0.916	0.859	...	0.44
In3	1	0.986	...	-0.986
Parameters				
Thresh_up	0.3			
Thresh_down	-0.1			
Outputs				
Out	-1	-0.986	...	0.986
Exp. Out	-1	-0.986	...	0.986
Out (DSP)	-1	-0.986	...	0.986
Exp. Out (DSP)	-1	-0.986	...	0.986

Test settings	
Tolerance Out	±3,0268e-08 (±65 LSB)

Test statistics	
Min CPU cycles	153
Max CPU cycles	243
Avg CPU cycles	200

Test case: Inport test OK

Inport test for General block AutoSwitch.

Test results				
Time step	1	2	...	137
CPU cycles	141	141	...	141
Inputs				
In1 (DSP)	-1	-0.986	...	0.986
Switch (DSP)	0.916	0.859	...	0.44
In3 (DSP)	1	0.986	...	-0.986
In1	-1	-0.986	...	0.986
Switch	0.916	0.859	...	0.44
In3	1	0.986	...	-0.986
Parameters				
Thresh_up	0			
Thresh_down	0			
Outputs				
Out	-1	-0.986	...	0.986
Exp. Out	-1	-0.986	...	0.986
Out (DSP)	-1	-0.986	...	0.986
Exp. Out (DSP)	-1	-0.986	...	0.986

Test settings	
Tolerance Out	±3,0268e-08 (±65 LSB)

Test statistics	
Min CPU cycles	141
Max CPU cycles	229
Avg CPU cycles	180

Test case: Conversion test **OK**

Conversion test for General block AutoSwitch.

Test results				
Time step	1	2	...	11
Mask parameters				
Thresh_up	0	0.1	...	-1.1
Thresh_down	0	0.1	...	-1.1
Controller parameters				
Thresh_down	0	0.1	...	-1.1
Thresh_up	0	0.1	...	-1.1
Exp. Thresh_down	0	0.1	...	-1.1
Exp. Thresh_up	0	0.1	...	-1.1

Test settings	
Tolerance Thresh_down	±0,0000e+00
Tolerance Thresh_up	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block AutoSwitch.

Test results				
Time step	1	2	...	11
Mask parameters				
Thresh_up	0	0.1	...	-1.1
Thresh_down	0	0.1	...	-1.1
Controller parameters				
Thresh_down	0	0.1	...	-1.1
Thresh_up	0	0.1	...	-1.1
Exp. Thresh_down	0	0.1	...	-1.1
Exp. Thresh_up	0	0.1	...	-1.1

Test settings	
Tolerance Thresh_down	±3,0000e-08
Tolerance Thresh_up	±3,0000e-08

Test statistics	
Min CPU cycles	1150
Max CPU cycles	1232
Avg CPU cycles	1218

Verification: AutoSwitch Float32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for General block AutoSwitch.

Test results				
Time step	1	2	...	137
CPU cycles	87	87	...	87
Inputs				
In1 (DSP)	-1	-0.986	...	0.986
Switch (DSP)	0.916	0.859	...	0.44
In3 (DSP)	1	0.986	...	-0.986
In1	-1	-0.986	...	0.986
Switch	0.916	0.859	...	0.44
In3	1	0.986	...	-0.986
Parameters				
Thresh_up	0.3			
Thresh_down	-0.1			
Outputs				
Out	-1	-0.986	...	0.986
Exp. Out	-1	-0.986	...	0.986
Out (DSP)	-1	-0.986	...	0.986
Exp. Out (DSP)	-1	-0.986	...	0.986

Test settings	
Tolerance Out	±3,0268e-08 (±65 LSB)

Test statistics	
Min CPU cycles	87
Max CPU cycles	123
Avg CPU cycles	106

Test case: Inport test OK

Inport test for General block AutoSwitch.

Test results				
Time step	1	2	...	137
CPU cycles	87	87	...	87
Inputs				
In1 (DSP)	-1	-0.986	...	0.986
Switch (DSP)	0.916	0.859	...	0.44
In3 (DSP)	1	0.986	...	-0.986
In1	-1	-0.986	...	0.986
Switch	0.916	0.859	...	0.44
In3	1	0.986	...	-0.986
Parameters				
Thresh_up	0			
Thresh_down	0			
Outputs				
Out	-1	-0.986	...	0.986
Exp. Out	-1	-0.986	...	0.986
Out (DSP)	-1	-0.986	...	0.986
Exp. Out (DSP)	-1	-0.986	...	0.986

Test settings	
Tolerance Out	±3,0268e-08 (±65 LSB)

Test statistics	
Min CPU cycles	87
Max CPU cycles	120
Avg CPU cycles	101

Test case: Conversion test **OK**

Conversion test for General block AutoSwitch.

Test results				
Time step	1	2	...	11
Mask parameters				
Thresh_up	0	0.1	...	-1.1
Thresh_down	0	0.1	...	-1.1
Controller parameters				
Thresh_down	0	0.1	...	-1.1
Thresh_up	0	0.1	...	-1.1
Exp. Thresh_down	0	0.1	...	-1.1
Exp. Thresh_up	0	0.1	...	-1.1

Test settings	
Tolerance Thresh_down	±0,0000e+00
Tolerance Thresh_up	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block AutoSwitch.

Test results				
Time step	1	2	...	11
Mask parameters				
Thresh_up	0	0.1	...	-1.1
Thresh_down	0	0.1	...	-1.1
Controller parameters				
Thresh_down	0	0.1	...	-1.1
Thresh_up	0	0.1	...	-1.1
Exp. Thresh_down	0	0.1	...	-1.1
Exp. Thresh_up	0	0.1	...	-1.1

Test settings	
Tolerance Thresh_down	±3,0000e-08
Tolerance Thresh_up	±3,0000e-08

Test statistics	
Min CPU cycles	434
Max CPU cycles	468
Avg CPU cycles	462

Verification: AutoSwitch Float32 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for General block AutoSwitch.

Test results				
Time step	1	2	...	137
CPU cycles	160	160	...	160
Inputs				
In1 (DSP)	-1	-0.986	...	0.986
Switch (DSP)	0.916	0.859	...	0.44
In3 (DSP)	1	0.986	...	-0.986
In1	-1	-0.986	...	0.986
Switch	0.916	0.859	...	0.44
In3	1	0.986	...	-0.986
Parameters				
Thresh_up	0.3			
Thresh_down	-0.1			
Outputs				
Out	-1	-0.986	...	0.986
Exp. Out	-1	-0.986	...	0.986
Out (DSP)	-1	-0.986	...	0.986
Exp. Out (DSP)	-1	-0.986	...	0.986

Test settings	
Tolerance Out	±3,0268e-08 (±65 LSB)

Test statistics	
Min CPU cycles	160
Max CPU cycles	256
Avg CPU cycles	213

Test case: Inport test OK

Inport test for General block AutoSwitch.

Test results				
Time step	1	2	...	137
CPU cycles	162	162	...	162
Inputs				
In1 (DSP)	-1	-0.986	...	0.986
Switch (DSP)	0.916	0.859	...	0.44
In3 (DSP)	1	0.986	...	-0.986
In1	-1	-0.986	...	0.986
Switch	0.916	0.859	...	0.44
In3	1	0.986	...	-0.986
Parameters				
Thresh_up	0			
Thresh_down	0			
Outputs				
Out	-1	-0.986	...	0.986
Exp. Out	-1	-0.986	...	0.986
Out (DSP)	-1	-0.986	...	0.986
Exp. Out (DSP)	-1	-0.986	...	0.986

Test settings	
Tolerance Out	±3,0268e-08 (±65 LSB)

Test statistics	
Min CPU cycles	162
Max CPU cycles	255
Avg CPU cycles	203

Test case: Conversion test **OK**

Conversion test for General block AutoSwitch.

Test results				
Time step	1	2	...	11
Mask parameters				
Thresh_up	0	0.1	...	-1.1
Thresh_down	0	0.1	...	-1.1
Controller parameters				
Thresh_down	0	0.1	...	-1.1
Thresh_up	0	0.1	...	-1.1
Exp. Thresh_down	0	0.1	...	-1.1
Exp. Thresh_up	0	0.1	...	-1.1

Test settings	
Tolerance Thresh_down	±0,0000e+00
Tolerance Thresh_up	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block AutoSwitch.

Test results				
Time step	1	2	...	11
Mask parameters				
Thresh_up	0	0.1	...	-1.1
Thresh_down	0	0.1	...	-1.1
Controller parameters				
Thresh_down	0	0.1	...	-1.1
Thresh_up	0	0.1	...	-1.1
Exp. Thresh_down	0	0.1	...	-1.1
Exp. Thresh_up	0	0.1	...	-1.1

Test settings	
Tolerance Thresh_down	±3,0000e-08
Tolerance Thresh_up	±3,0000e-08

Test statistics	
Min CPU cycles	983
Max CPU cycles	1641
Avg CPU cycles	1578

Verification: AutoSwitch Float32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for General block AutoSwitch.

Test results				
Time step	1	2	...	137
CPU cycles	78	62	...	62
Inputs				
In1 (DSP)	-1	-0.986	...	0.986
Switch (DSP)	0.916	0.859	...	0.44
In3 (DSP)	1	0.986	...	-0.986
In1	-1	-0.986	...	0.986
Switch	0.916	0.859	...	0.44
In3	1	0.986	...	-0.986
Parameters				
Thresh_up	0.3			
Thresh_down	-0.1			
Outputs				
Out	-1	-0.986	...	0.986
Exp. Out	-1	-0.986	...	0.986
Out (DSP)	-1	-0.986	...	0.986
Exp. Out (DSP)	-1	-0.986	...	0.986

Test settings	
Tolerance Out	±3,0268e-08 (±65 LSB)

Test statistics	
Min CPU cycles	62
Max CPU cycles	78
Avg CPU cycles	65

Test case: Inport test OK

Inport test for General block AutoSwitch.

Test results				
Time step	1	2	...	137
CPU cycles	78	62	...	62
Inputs				
In1 (DSP)	-1	-0.986	...	0.986
Switch (DSP)	0.916	0.859	...	0.44
In3 (DSP)	1	0.986	...	-0.986
In1	-1	-0.986	...	0.986
Switch	0.916	0.859	...	0.44
In3	1	0.986	...	-0.986
Parameters				
Thresh_up	0			
Thresh_down	0			
Outputs				
Out	-1	-0.986	...	0.986
Exp. Out	-1	-0.986	...	0.986
Out (DSP)	-1	-0.986	...	0.986
Exp. Out (DSP)	-1	-0.986	...	0.986

Test settings	
Tolerance Out	±3,0268e-08 (±65 LSB)

Test statistics	
Min CPU cycles	62
Max CPU cycles	78
Avg CPU cycles	65

Test case: Conversion test **OK**

Conversion test for General block AutoSwitch.

Test results				
Time step	1	2	...	11
Mask parameters				
Thresh_up	0	0.1	...	-1.1
Thresh_down	0	0.1	...	-1.1
Controller parameters				
Thresh_down	0	0.1	...	-1.1
Thresh_up	0	0.1	...	-1.1
Exp. Thresh_down	0	0.1	...	-1.1
Exp. Thresh_up	0	0.1	...	-1.1

Test settings	
Tolerance Thresh_down	±0,0000e+00
Tolerance Thresh_up	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block AutoSwitch.

Test results				
Time step	1	2	...	11
Mask parameters				
Thresh_up	0	0.1	...	-1.1
Thresh_down	0	0.1	...	-1.1
Controller parameters				
Thresh_down	0	0.1	...	-1.1
Thresh_up	0	0.1	...	-1.1
Exp. Thresh_down	0	0.1	...	-1.1
Exp. Thresh_up	0	0.1	...	-1.1

Test settings	
Tolerance Thresh_down	±3,0000e-08
Tolerance Thresh_up	±3,0000e-08

Test statistics	
Min CPU cycles	627
Max CPU cycles	703
Avg CPU cycles	633

Verification: AutoSwitch Float32 CPU TMS320F28379D

Date of Test 2026-06-22

Target controller TMS320F28379D

Test case: Inport test OK

Inport test for General block AutoSwitch.

Test results				
Time step	1	2	...	137
CPU cycles	58	58	...	58
Inputs				
In1 (DSP)	-1	-0.986	...	0.986
Switch (DSP)	0.916	0.859	...	0.44
In3 (DSP)	1	0.986	...	-0.986
In1	-1	-0.986	...	0.986
Switch	0.916	0.859	...	0.44
In3	1	0.986	...	-0.986
Parameters				
Thresh_up	0.3			
Thresh_down	-0.1			
Outputs				
Out	-1	-0.986	...	0.986
Exp. Out	-1	-0.986	...	0.986
Out (DSP)	-1	-0.986	...	0.986
Exp. Out (DSP)	-1	-0.986	...	0.986

Test settings	
Tolerance Out	±3,0268e-08 (±65 LSB)

Test statistics	
Min CPU cycles	58
Max CPU cycles	73
Avg CPU cycles	66

Test case: Inport test OK

Inport test for General block AutoSwitch.

Test results				
Time step	1	2	...	137
CPU cycles	58	58	...	58
Inputs				
In1 (DSP)	-1	-0.986	...	0.986
Switch (DSP)	0.916	0.859	...	0.44
In3 (DSP)	1	0.986	...	-0.986
In1	-1	-0.986	...	0.986
Switch	0.916	0.859	...	0.44
In3	1	0.986	...	-0.986
Parameters				
Thresh_up	0			
Thresh_down	0			
Outputs				
Out	-1	-0.986	...	0.986
Exp. Out	-1	-0.986	...	0.986
Out (DSP)	-1	-0.986	...	0.986
Exp. Out (DSP)	-1	-0.986	...	0.986

Test settings	
Tolerance Out	±3,0268e-08 (±65 LSB)

Test statistics	
Min CPU cycles	58
Max CPU cycles	73
Avg CPU cycles	64

Test case: Conversion test **OK**

Conversion test for General block AutoSwitch.

Test results				
Time step	1	2	...	11
Mask parameters				
Thresh_up	0	0.1	...	-1.1
Thresh_down	0	0.1	...	-1.1
Controller parameters				
Thresh_down	0	0.1	...	-1.1
Thresh_up	0	0.1	...	-1.1
Exp. Thresh_down	0	0.1	...	-1.1
Exp. Thresh_up	0	0.1	...	-1.1

Test settings	
Tolerance Thresh_down	±0,0000e+00
Tolerance Thresh_up	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block AutoSwitch.

Test results				
Time step	1	2	...	11
Mask parameters				
Thresh_up	0	0.1	...	-1.1
Thresh_down	0	0.1	...	-1.1
Controller parameters				
Thresh_down	0	0.1	...	-1.1
Thresh_up	0	0.1	...	-1.1
Exp. Thresh_down	0	0.1	...	-1.1
Exp. Thresh_up	0	0.1	...	-1.1

Test settings	
Tolerance Thresh_down	±3,0000e-08
Tolerance Thresh_up	±3,0000e-08

Test statistics	
Min CPU cycles	942
Max CPU cycles	948
Avg CPU cycles	942

Block: Constant



Constant value.

Outports	
Out	Constant output

Mask Parameters		
Name	**ID**	**Description**
Value	1	Constant factor

Implementations:

Bool	Boolean Implementation
Int8	8 Bit Integer Implementation
Int16	16 Bit Integer Implementation
Int32	32 Bit Integer Implementation
FiP8	8 Bit Fixed Point Implementation
FiP16	16 Bit Fixed Point Implementation
FiP32	32 Bit Fixed Point Implementation
Float32	32 Bit Floating Point Implementation
Float64	64 Bit Floating Point Implementation

Implementation: Bool

Boolean Implementation

Outports Data Type	
Out	bool

Implementation: Int8

8 Bit Integer Implementation

Outports Data Type	
Out	int8

Implementation: Int16

16 Bit Integer Implementation

Outports Data Type	
Out	int16

Implementation: Int32

32 Bit Integer Implementation

Outports Data Type	
Out	int32

Implementation: FiP8

8 Bit Fixed Point Implementation

Outports Data Type	
Out	int8

Implementation: FiP16

16 Bit Fixed Point Implementation

Outports Data Type	
Out	int16

Implementation: FiP32

32 Bit Fixed Point Implementation

Outports Data Type	
Out	int32

Implementation: Float32

32 Bit Floating Point Implementation

Outports Data Type	
Out	float32

Implementation: Float64

64 Bit Floating Point Implementation

Outports Data Type	
Out	float64

Verification: Constant Bool CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Conversion test — OK

Conversion test for General block Constant.

Test results						
Time step	1	2	3	4	...	7
Mask parameters						
Value	1	-1	0	0.5	...	-2.3
Controller parameters						
K	1	1	0	1	...	1
Exp. K	1	1	0	1	...	1

Test settings	
Tolerance K	±0,0000e+00

Test case: Conversion-on-Target test — OK

Conversion-on-Target test for General block Constant.

Test results						
Time step	1	2	3	4	...	7
Mask parameters						
Value	1	-1	0	0.5	...	-2.3
Controller parameters						
K	1	1	0	1	...	1
Exp. K	1	1	0	1	...	1

Test settings	
Tolerance K	±0,0000e+00

Test statistics	
Min CPU cycles	776
Max CPU cycles	813
Avg CPU cycles	807

Verification: Constant Bool CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Conversion test — OK

Conversion test for General block Constant.

Test results						
Time step	1	2	3	4	...	7
Mask parameters						
Value	1	-1	0	0.5	...	-2.3
Controller parameters						
K	1	1	0	1	...	1
Exp. K	1	1	0	1	...	1

Test settings	
Tolerance K	±0,0000e+00

Test case: Conversion-on-Target test — OK

Conversion-on-Target test for General block Constant.

Test results						
Time step	1	2	3	4	...	7
Mask parameters						
Value	1	-1	0	0.5	...	-2.3
Controller parameters						
K	1	1	0	1	...	1
Exp. K	1	1	0	1	...	1

Test settings	
Tolerance K	±0,0000e+00

Test statistics	
Min CPU cycles	373
Max CPU cycles	399
Avg CPU cycles	393

Verification: Constant Bool CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Conversion test — OK

Conversion test for General block Constant.

Test results						
Time step	1	2	3	4	...	7
Mask parameters						
Value	1	-1	0	0.5	...	-2.3
Controller parameters						
K	1	1	0	1	...	1
Exp. K	1	1	0	1	...	1

Test settings	
Tolerance K	±0,0000e+00

Test case: Conversion-on-Target test — OK

Conversion-on-Target test for General block Constant.

Test results						
Time step	1	2	3	4	...	7
Mask parameters						
Value	1	-1	0	0.5	...	-2.3
Controller parameters						
K	1	1	0	1	...	1
Exp. K	1	1	0	1	...	1

Test settings	
Tolerance K	±0,0000e+00

Test statistics	
Min CPU cycles	518
Max CPU cycles	538
Avg CPU cycles	535

Verification: Constant Bool CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Conversion test — OK

Conversion test for General block Constant.

Test results						
Time step	1	2	3	4	...	7
Mask parameters						
Value	1	-1	0	0.5	...	-2.3
Controller parameters						
K	1	1	0	1	...	1
Exp. K	1	1	0	1	...	1

Test settings	
Tolerance K	±0,0000e+00

Test case: Conversion-on-Target test — OK

Conversion-on-Target test for General block Constant.

Test results						
Time step	1	2	3	4	...	7
Mask parameters						
Value	1	-1	0	0.5	...	-2.3
Controller parameters						
K	1	1	0	1	...	1
Exp. K	1	1	0	1	...	1

Test settings	
Tolerance K	±0,0000e+00

Test statistics	
Min CPU cycles	593
Max CPU cycles	606
Avg CPU cycles	594

Verification: Constant Bool CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Conversion test OK

Conversion test for General block Constant.

Test results						
Time step	1	2	3	4	...	7
Mask parameters						
Value	1	-1	0	0.5	...	-2.3
Controller parameters						
K	1	1	0	1	...	1
Exp. K	1	1	0	1	...	1

Test settings	
Tolerance K	±0,0000e+00

Test case: Conversion-on-Target test OK

Conversion-on-Target test for General block Constant.

Test results						
Time step	1	2	3	4	...	7
Mask parameters						
Value	1	-1	0	0.5	...	-2.3
Controller parameters						
K	1	1	0	1	...	1
Exp. K	1	1	0	1	...	1

Test settings	
Tolerance K	±0,0000e+00

Test statistics	
Min CPU cycles	243
Max CPU cycles	276
Avg CPU cycles	265

Verification: Constant Bool CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Conversion test — OK

Conversion test for General block Constant.

Test results						
Time step	1	2	3	4	...	7
Mask parameters						
Value	1	-1	0	0.5	...	-2.3
Controller parameters						
K	1	1	0	1	...	1
Exp. K	1	1	0	1	...	1

Test settings	
Tolerance K	±0,0000e+00

Test case: Conversion-on-Target test — OK

Conversion-on-Target test for General block Constant.

Test results						
Time step	1	2	3	4	...	7
Mask parameters						
Value	1	-1	0	0.5	...	-2.3
Controller parameters						
K	1	1	0	1	...	1
Exp. K	1	1	0	1	...	1

Test settings	
Tolerance K	±0,0000e+00

Test statistics	
Min CPU cycles	521
Max CPU cycles	552
Avg CPU cycles	528

Verification: Constant Bool CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Conversion test — OK

Conversion test for General block Constant.

Test results						
Time step	1	2	3	4	...	7
Mask parameters						
Value	1	-1	0	0.5	...	-2.3
Controller parameters						
K	1	1	0	1	...	1
Exp. K	1	1	0	1	...	1

Test settings	
Tolerance K	±0,0000e+00

Test case: Conversion-on-Target test — OK

Conversion-on-Target test for General block Constant.

Test results						
Time step	1	2	3	4	...	7
Mask parameters						
Value	1	-1	0	0.5	...	-2.3
Controller parameters						
K	1	1	0	1	...	1
Exp. K	1	1	0	1	...	1

Test settings	
Tolerance K	±0,0000e+00

Test statistics	
Min CPU cycles	439
Max CPU cycles	497
Avg CPU cycles	453

Verification: Constant Bool CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Conversion test — OK

Conversion test for General block Constant.

Test results						
Time step	1	2	3	4	...	7
Mask parameters						
Value	1	-1	0	0.5	...	-2.3
Controller parameters						
K	1	1	0	1	...	1
Exp. K	1	1	0	1	...	1

Test settings	
Tolerance K	±0,0000e+00

Test case: Conversion-on-Target test — OK

Conversion-on-Target test for General block Constant.

Test results						
Time step	1	2	3	4	...	7
Mask parameters						
Value	1	-1	0	0.5	...	-2.3
Controller parameters						
K	1	1	0	1	...	1
Exp. K	1	1	0	1	...	1

Test settings	
Tolerance K	±0,0000e+00

Test statistics	
Min CPU cycles	616
Max CPU cycles	645
Avg CPU cycles	640

Verification: Constant Int16 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Conversion test — OK

Conversion test for General block Constant.

Test results						
Time step	1	2	3	4	...	17
Mask parameters						
Value	33000	32768	32767	32766	...	-33000
Controller parameters						
K	32767	32767	32767	32766	...	-32767
Exp. K	32767	32767	32767	32766	...	-32767

Test settings	
Tolerance K	±0,0000e+00

Test case: Conversion-on-Target test — OK

Conversion-on-Target test for General block Constant.

Test results						
Time step	1	2	3	4	...	17
Mask parameters						
Value	33000	32768	32767	32766	...	-33000
Controller parameters						
K	32767	32767	32767	32766	...	-32767
Exp. K	32767	32767	32767	32766	...	-32767

Test settings	
Tolerance K	±0,0000e+00

Test statistics	
Min CPU cycles	1191
Max CPU cycles	1436
Avg CPU cycles	1406

Verification: Constant Int16 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Conversion test OK

Conversion test for General block Constant.

Test results						
Time step	1	2	3	4	...	17
Mask parameters						
Value	33000	32768	32767	32766	...	-33000
Controller parameters						
K	32767	32767	32767	32766	...	-32767
Exp. K	32767	32767	32767	32766	...	-32767

Test settings	
Tolerance K	±0,0000e+00

Test case: Conversion-on-Target test OK

Conversion-on-Target test for General block Constant.

Test results						
Time step	1	2	3	4	...	17
Mask parameters						
Value	33000	32768	32767	32766	...	-33000
Controller parameters						
K	32767	32767	32767	32766	...	-32767
Exp. K	32767	32767	32767	32766	...	-32767

Test settings	
Tolerance K	±0,0000e+00

Test statistics	
Min CPU cycles	653
Max CPU cycles	889
Avg CPU cycles	842

Verification: Constant Int16 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Conversion test OK

Conversion test for General block Constant.

Test results						
Time step	1	2	3	4	...	17
Mask parameters						
Value	33000	32768	32767	32766	...	-33000
Controller parameters						
K	32767	32767	32767	32766	...	-32767
Exp. K	32767	32767	32767	32766	...	-32767

Test settings	
Tolerance K	±0,0000e+00

Test case: Conversion-on-Target test OK

Conversion-on-Target test for General block Constant.

Test results						
Time step	1	2	3	4	...	17
Mask parameters						
Value	33000	32768	32767	32766	...	-33000
Controller parameters						
K	32767	32767	32767	32766	...	-32767
Exp. K	32767	32767	32767	32766	...	-32767

Test settings	
Tolerance K	±0,0000e+00

Test statistics	
Min CPU cycles	841
Max CPU cycles	1086
Avg CPU cycles	1038

Verification: Constant Int16 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Conversion test — OK

Conversion test for General block Constant.

Test results						
Time step	1	2	3	4	...	17
Mask parameters						
Value	33000	32768	32767	32766	...	-33000
Controller parameters						
K	32767	32767	32767	32766	...	-32767
Exp. K	32767	32767	32767	32766	...	-32767

Test settings	
Tolerance K	±0,0000e+00

Test case: Conversion-on-Target test — OK

Conversion-on-Target test for General block Constant.

Test results						
Time step	1	2	3	4	...	17
Mask parameters						
Value	33000	32768	32767	32766	...	-33000
Controller parameters						
K	32767	32767	32767	32766	...	-32767
Exp. K	32767	32767	32767	32766	...	-32767

Test settings	
Tolerance K	±0,0000e+00

Test statistics	
Min CPU cycles	923
Max CPU cycles	1246
Avg CPU cycles	1199

Verification: Constant Int16 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Conversion test — OK

Conversion test for General block Constant.

Test results						
Time step	1	2	3	4	...	17
Mask parameters						
Value	33000	32768	32767	32766	...	-33000
Controller parameters						
K	32767	32767	32767	32766	...	-32767
Exp. K	32767	32767	32767	32766	...	-32767

Test settings	
Tolerance K	±0,0000e+00

Test case: Conversion-on-Target test — OK

Conversion-on-Target test for General block Constant.

Test results						
Time step	1	2	3	4	...	17
Mask parameters						
Value	33000	32768	32767	32766	...	-33000
Controller parameters						
K	32767	32767	32767	32766	...	-32767
Exp. K	32767	32767	32767	32766	...	-32767

Test settings	
Tolerance K	±0,0000e+00

Test statistics	
Min CPU cycles	399
Max CPU cycles	473
Avg CPU cycles	465

Verification: Constant Int16 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Conversion test — OK

Conversion test for General block Constant.

Test results						
Time step	1	2	3	4	...	17
Mask parameters						
Value	33000	32768	32767	32766	...	-33000
Controller parameters						
K	32767	32767	32767	32766	...	-32767
Exp. K	32767	32767	32767	32766	...	-32767

Test settings	
Tolerance K	±0,0000e+00

Test case: Conversion-on-Target test — OK

Conversion-on-Target test for General block Constant.

Test results						
Time step	1	2	3	4	...	17
Mask parameters						
Value	33000	32768	32767	32766	...	-33000
Controller parameters						
K	32767	32767	32767	32766	...	-32767
Exp. K	32767	32767	32767	32766	...	-32767

Test settings	
Tolerance K	±0,0000e+00

Test statistics	
Min CPU cycles	1300
Max CPU cycles	1729
Avg CPU cycles	1607

Verification: Constant Int16 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Conversion test — OK

Conversion test for General block Constant.

Test results						
Time step	1	2	3	4	...	17
Mask parameters						
Value	33000	32768	32767	32766	...	-33000
Controller parameters						
K	32767	32767	32767	32766	...	-32767
Exp. K	32767	32767	32767	32766	...	-32767

Test settings	
Tolerance K	±0,0000e+00

Test case: Conversion-on-Target test — OK

Conversion-on-Target test for General block Constant.

Test results						
Time step	1	2	3	4	...	17
Mask parameters						
Value	33000	32768	32767	32766	...	-33000
Controller parameters						
K	32767	32767	32767	32766	...	-32767
Exp. K	32767	32767	32767	32766	...	-32767

Test settings	
Tolerance K	±0,0000e+00

Test statistics	
Min CPU cycles	688
Max CPU cycles	1026
Avg CPU cycles	863

Verification: Constant Int16 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Conversion test OK

Conversion test for General block Constant.

Test results						
Time step	1	2	3	4	...	17
Mask parameters						
Value	33000	32768	32767	32766	...	-33000
Controller parameters						
K	32767	32767	32767	32766	...	-32767
Exp. K	32767	32767	32767	32766	...	-32767

Test settings	
Tolerance K	±0,0000e+00

Test case: Conversion-on-Target test OK

Conversion-on-Target test for General block Constant.

Test results						
Time step	1	2	3	4	...	17
Mask parameters						
Value	33000	32768	32767	32766	...	-33000
Controller parameters						
K	32767	32767	32767	32766	...	-32767
Exp. K	32767	32767	32767	32766	...	-32767

Test settings	
Tolerance K	±0,0000e+00

Test statistics	
Min CPU cycles	1091
Max CPU cycles	1473
Avg CPU cycles	1406

Verification: Constant Int32 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Conversion test — OK

Conversion test for General block Constant.

Test results				
Time step	1	2	...	17
Mask parameters				
Value	3300000000	2147483648	...	-3300000000
Controller parameters				
K	2147483647	2147483647	...	-2147483647
Exp. K	2147483647	2147483647	...	-2147483647

Test settings	
Tolerance K	±0,0000e+00

Test case: Conversion-on-Target test — OK

Conversion-on-Target test for General block Constant.

Test results				
Time step	1	2	...	17
Mask parameters				
Value	3300000000	2147483648	...	-3300000000
Controller parameters				
K	2147483647	2147483647	...	-2147483647
Exp. K	2147483647	2147483647	...	-2147483647

Test settings	
Tolerance K	±3,0000e+00

Test statistics	
Min CPU cycles	1210
Max CPU cycles	1456
Avg CPU cycles	1385

Verification: Constant Int32 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Conversion test — OK

Conversion test for General block Constant.

Test results				
Time step	1	2	...	17
Mask parameters				
Value	3300000000	2147483648	...	-3300000000
Controller parameters				
K	2147483647	2147483647	...	-2147483647
Exp. K	2147483647	2147483647	...	-2147483647

Test settings	
Tolerance K	±0,0000e+00

Test case: Conversion-on-Target test — OK

Conversion-on-Target test for General block Constant.

Test results				
Time step	1	2	...	17
Mask parameters				
Value	3300000000	2147483648	...	-3300000000
Controller parameters				
K	2147483647	2147483647	...	-2147483647
Exp. K	2147483647	2147483647	...	-2147483647

Test settings	
Tolerance K	±3,0000e+00

Test statistics	
Min CPU cycles	677
Max CPU cycles	893
Avg CPU cycles	859

Verification: Constant Int32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Conversion test — OK

Conversion test for General block Constant.

Test results				
Time step	1	2	...	17
Mask parameters				
Value	3300000000	2147483648	...	-3300000000
Controller parameters				
K	2147483647	2147483647	...	-2147483647
Exp. K	2147483647	2147483647	...	-2147483647

Test settings	
Tolerance K	±0,0000e+00

Test case: Conversion-on-Target test — OK

Conversion-on-Target test for General block Constant.

Test results				
Time step	1	2	...	17
Mask parameters				
Value	3300000000	2147483648	...	-3300000000
Controller parameters				
K	2147483647	2147483647	...	-2147483647
Exp. K	2147483647	2147483647	...	-2147483647

Test settings	
Tolerance K	±3,0000e+00

Test statistics	
Min CPU cycles	855
Max CPU cycles	1100
Avg CPU cycles	1059

Verification: Constant Int32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Conversion test OK

Conversion test for General block Constant.

Test results				
Time step	1	2	...	17
Mask parameters				
Value	3300000000	2147483648	...	-3300000000
Controller parameters				
K	2147483647	2147483647	...	-2147483647
Exp. K	2147483647	2147483647	...	-2147483647

Test settings	
Tolerance K	±0,0000e+00

Test case: Conversion-on-Target test OK

Conversion-on-Target test for General block Constant.

Test results				
Time step	1	2	...	17
Mask parameters				
Value	3300000000	2147483648	...	-3300000000
Controller parameters				
K	2147483647	2147483647	...	-2147483647
Exp. K	2147483647	2147483647	...	-2147483647

Test settings	
Tolerance K	±3,0000e+00

Test statistics	
Min CPU cycles	953
Max CPU cycles	1314
Avg CPU cycles	1231

Verification: Constant Int32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Conversion test — OK

Conversion test for General block Constant.

Test results				
Time step	1	2	...	17
Mask parameters				
Value	3300000000	2147483648	...	-3300000000
Controller parameters				
K	2147483647	2147483647	...	-2147483647
Exp. K	2147483647	2147483647	...	-2147483647

Test settings	
Tolerance K	±0,0000e+00

Test case: Conversion-on-Target test — OK

Conversion-on-Target test for General block Constant.

Test results				
Time step	1	2	...	17
Mask parameters				
Value	3300000000	2147483648	...	-3300000000
Controller parameters				
K	2147483647	2147483647	...	-2147483647
Exp. K	2147483647	2147483647	...	-2147483647

Test settings	
Tolerance K	±3,0000e+00

Test statistics	
Min CPU cycles	395
Max CPU cycles	475
Avg CPU cycles	461

Verification: Constant Int32 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Conversion test

OK

Conversion test for General block Constant.

Test results				
Time step	1	2	...	17
Mask parameters				
Value	3300000000	2147483648	...	-3300000000
Controller parameters				
K	2147483647	2147483647	...	-2147483647
Exp. K	2147483647	2147483647	...	-2147483647

Test settings	
Tolerance K	±0,0000e+00

Test case: Conversion-on-Target test

OK

Conversion-on-Target test for General block Constant.

Test results				
Time step	1	2	...	17
Mask parameters				
Value	3300000000	2147483648	...	-3300000000
Controller parameters				
K	2147483647	2147483647	...	-2147483647
Exp. K	2147483647	2147483647	...	-2147483647

Test settings	
Tolerance K	±3,0000e+00

Test statistics	
Min CPU cycles	1321
Max CPU cycles	1731
Avg CPU cycles	1611

Verification: Constant Int32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Conversion test

OK

Conversion test for General block Constant.

Test results				
Time step	1	2	...	17
Mask parameters				
Value	3300000000	2147483648	...	-3300000000
Controller parameters				
K	2147483647	2147483647	...	-2147483647
Exp. K	2147483647	2147483647	...	-2147483647

Test settings	
Tolerance K	±0,0000e+00

Test case: Conversion-on-Target test

OK

Conversion-on-Target test for General block Constant.

Test results				
Time step	1	2	...	17
Mask parameters				
Value	3300000000	2147483648	...	-3300000000
Controller parameters				
K	2147483647	2147483647	...	-2147483647
Exp. K	2147483647	2147483647	...	-2147483647

Test settings	
Tolerance K	±3,0000e+00

Test statistics	
Min CPU cycles	678
Max CPU cycles	960
Avg CPU cycles	844

Verification: Constant Int32 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Conversion test OK

Conversion test for General block Constant.

Test results				
Time step	1	2	...	17
Mask parameters				
Value	3300000000	2147483648	...	-3300000000
Controller parameters				
K	2147483647	2147483647	...	-2147483647
Exp. K	2147483647	2147483647	...	-2147483647

Test settings	
Tolerance K	±0,0000e+00

Test case: Conversion-on-Target test OK

Conversion-on-Target test for General block Constant.

Test results				
Time step	1	2	...	17
Mask parameters				
Value	3300000000	2147483648	...	-3300000000
Controller parameters				
K	2147483647	2147483647	...	-2147483647
Exp. K	2147483647	2147483647	...	-2147483647

Test settings	
Tolerance K	±3,0000e+00

Test statistics	
Min CPU cycles	1116
Max CPU cycles	1485
Avg CPU cycles	1438

Verification: Constant FiP16 CPU TMS320F28335

Date of Test 2026-06-19

Target controller TMS320F28335

Test case: Conversion test OK

Conversion test for General block Constant.

Test results						
Time step	1	2	3	4	...	7
Mask parameters						
Value	1	-1	0	0.5	...	-2.3
Controller parameters						
K	32767	-32767	0	16384	...	-32767
Exp. K	32767	-32767	0	16384	...	-32767

Test settings	
Tolerance K	±0,0000e+00

Test case: Conversion-on-Target test OK

Conversion-on-Target test for General block Constant.

Test results						
Time step	1	2	3	4	...	7
Mask parameters						
Value	1	-1	0	0.5	...	-2.3
Controller parameters						
K	32767	-32767	0	16384	...	-32767
Exp. K	32767	-32767	0	16384	...	-32767

Test settings	
Tolerance K	±0,0000e+00

Test statistics	
Min CPU cycles	854
Max CPU cycles	871
Avg CPU cycles	856

Verification: Constant FiP16 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Conversion test OK

Conversion test for General block Constant.

Test results						
Time step	1	2	3	4	...	7
Mask parameters						
Value	1	-1	0	0.5	...	-2.3
Controller parameters						
K	32767	-32767	0	16384	...	-32767
Exp. K	32767	-32767	0	16384	...	-32767

Test settings	
Tolerance K	±0,0000e+00

Test case: Conversion-on-Target test OK

Conversion-on-Target test for General block Constant.

Test results						
Time step	1	2	3	4	...	7
Mask parameters						
Value	1	-1	0	0.5	...	-2.3
Controller parameters						
K	32767	-32767	0	16384	...	-32767
Exp. K	32767	-32767	0	16384	...	-32767

Test settings	
Tolerance K	±0,0000e+00

Test statistics	
Min CPU cycles	401
Max CPU cycles	407
Avg CPU cycles	404

Verification: Constant FiP16 CPU STM32G474RE

Date of Test 2026-06-19

Target controller STM32G474RE

Test case: Conversion test OK

Conversion test for General block Constant.

Test results						
Time step	1	2	3	4	...	7
Mask parameters						
Value	1	-1	0	0.5	...	-2.3
Controller parameters						
K	32767	-32767	0	16384	...	-32767
Exp. K	32767	-32767	0	16384	...	-32767

Test settings	
Tolerance K	±0,0000e+00

Test case: Conversion-on-Target test OK

Conversion-on-Target test for General block Constant.

Test results						
Time step	1	2	3	4	...	7
Mask parameters						
Value	1	-1	0	0.5	...	-2.3
Controller parameters						
K	32767	-32767	0	16384	...	-32767
Exp. K	32767	-32767	0	16384	...	-32767

Test settings	
Tolerance K	±0,0000e+00

Test statistics	
Min CPU cycles	532
Max CPU cycles	532
Avg CPU cycles	532

Verification: Constant FiP16 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Conversion test — OK

Conversion test for General block Constant.

Test results						
Time step	1	2	3	4	...	7
Mask parameters						
Value	1	-1	0	0.5	...	-2.3
Controller parameters						
K	32767	-32767	0	16384	...	-32767
Exp. K	32767	-32767	0	16384	...	-32767

Test settings	
Tolerance K	±0,0000e+00

Test case: Conversion-on-Target test — OK

Conversion-on-Target test for General block Constant.

Test results						
Time step	1	2	3	4	...	7
Mask parameters						
Value	1	-1	0	0.5	...	-2.3
Controller parameters						
K	32767	-32767	0	16384	...	-32767
Exp. K	32767	-32767	0	16384	...	-32767

Test settings	
Tolerance K	±0,0000e+00

Test statistics	
Min CPU cycles	810
Max CPU cycles	912
Avg CPU cycles	890

Verification: Constant FiP16 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Conversion test OK

Conversion test for General block Constant.

Test results						
Time step	1	2	3	4	...	7
Mask parameters						
Value	1	-1	0	0.5	...	-2.3
Controller parameters						
K	32767	-32767	0	16384	...	-32767
Exp. K	32767	-32767	0	16384	...	-32767

Test settings	
Tolerance K	±0,0000e+00

Test case: Conversion-on-Target test OK

Conversion-on-Target test for General block Constant.

Test results						
Time step	1	2	3	4	...	7
Mask parameters						
Value	1	-1	0	0.5	...	-2.3
Controller parameters						
K	32767	-32767	0	16384	...	-32767
Exp. K	32767	-32767	0	16384	...	-32767

Test settings	
Tolerance K	±0,0000e+00

Test statistics	
Min CPU cycles	384
Max CPU cycles	405
Avg CPU cycles	401

Verification: Constant FiP16 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Conversion test — OK

Conversion test for General block Constant.

Test results						
Time step	1	2	3	4	...	7
Mask parameters						
Value	1	-1	0	0.5	...	-2.3
Controller parameters						
K	32767	-32767	0	16384	...	-32767
Exp. K	32767	-32767	0	16384	...	-32767

Test settings	
Tolerance K	±0,0000e+00

Test case: Conversion-on-Target test — OK

Conversion-on-Target test for General block Constant.

Test results						
Time step	1	2	3	4	...	7
Mask parameters						
Value	1	-1	0	0.5	...	-2.3
Controller parameters						
K	32767	-32767	0	16384	...	-32767
Exp. K	32767	-32767	0	16384	...	-32767

Test settings	
Tolerance K	±0,0000e+00

Test statistics	
Min CPU cycles	839
Max CPU cycles	1291
Avg CPU cycles	1219

Verification: Constant FiP16 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Conversion test — OK

Conversion test for General block Constant.

Test results						
Time step	1	2	3	4	...	7
Mask parameters						
Value	1	-1	0	0.5	...	-2.3
Controller parameters						
K	32767	-32767	0	16384	...	-32767
Exp. K	32767	-32767	0	16384	...	-32767

Test settings	
Tolerance K	±0,0000e+00

Test case: Conversion-on-Target test — OK

Conversion-on-Target test for General block Constant.

Test results						
Time step	1	2	3	4	...	7
Mask parameters						
Value	1	-1	0	0.5	...	-2.3
Controller parameters						
K	32767	-32767	0	16384	...	-32767
Exp. K	32767	-32767	0	16384	...	-32767

Test settings	
Tolerance K	±0,0000e+00

Test statistics	
Min CPU cycles	385
Max CPU cycles	470
Avg CPU cycles	399

Verification: Constant FiP16 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Conversion test — OK

Conversion test for General block Constant.

Test results						
Time step	1	2	3	4	...	7
Mask parameters						
Value	1	-1	0	0.5	...	-2.3
Controller parameters						
K	32767	-32767	0	16384	...	-32767
Exp. K	32767	-32767	0	16384	...	-32767

Test settings	
Tolerance K	±0,0000e+00

Test case: Conversion-on-Target test — OK

Conversion-on-Target test for General block Constant.

Test results						
Time step	1	2	3	4	...	7
Mask parameters						
Value	1	-1	0	0.5	...	-2.3
Controller parameters						
K	32767	-32767	0	16384	...	-32767
Exp. K	32767	-32767	0	16384	...	-32767

Test settings	
Tolerance K	±0,0000e+00

Test statistics	
Min CPU cycles	661
Max CPU cycles	665
Avg CPU cycles	662

Verification: Constant FiP32 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Conversion test — OK

Conversion test for General block Constant.

Test results				
Time step	1	2	...	7
Mask parameters				
Value	1	-1	...	-2.3
Controller parameters				
K	2147483647	-2147483647	...	-2147483647
Exp. K	2147483647	-2147483647	...	-2147483647

Test settings	
Tolerance K	±0,0000e+00

Test case: Conversion-on-Target test — OK

Conversion-on-Target test for General block Constant.

Test results				
Time step	1	2	...	7
Mask parameters				
Value	1	-1	...	-2.3
Controller parameters				
K	2147483647	-2147483647	...	-2147483647
Exp. K	2147483647	-2147483647	...	-2147483647

Test settings	
Tolerance K	±0,0000e+00

Test statistics	
Min CPU cycles	1018
Max CPU cycles	1085
Avg CPU cycles	1055

Verification: Constant FiP32 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Conversion test — OK

Conversion test for General block Constant.

Test results				
Time step	1	2	...	7
Mask parameters				
Value	1	-1	...	-2.3
Controller parameters				
K	2147483647	-2147483647	...	-2147483647
Exp. K	2147483647	-2147483647	...	-2147483647

Test settings	
Tolerance K	±0,0000e+00

Test case: Conversion-on-Target test — OK

Conversion-on-Target test for General block Constant.

Test results				
Time step	1	2	...	7
Mask parameters				
Value	1	-1	...	-2.3
Controller parameters				
K	2147483647	-2147483647	...	-2147483647
Exp. K	2147483647	-2147483647	...	-2147483647

Test settings	
Tolerance K	±0,0000e+00

Test statistics	
Min CPU cycles	457
Max CPU cycles	485
Avg CPU cycles	477

Verification: Constant FiP32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Conversion test OK

Conversion test for General block Constant.

Test results				
Time step	1	2	...	7
Mask parameters				
Value	1	-1	...	-2.3
Controller parameters				
K	2147483647	-2147483647	...	-2147483647
Exp. K	2147483647	-2147483647	...	-2147483647

Test settings	
Tolerance K	±0,0000e+00

Test case: Conversion-on-Target test OK

Conversion-on-Target test for General block Constant.

Test results				
Time step	1	2	...	7
Mask parameters				
Value	1	-1	...	-2.3
Controller parameters				
K	2147483647	-2147483647	...	-2147483647
Exp. K	2147483647	-2147483647	...	-2147483647

Test settings	
Tolerance K	±0,0000e+00

Test statistics	
Min CPU cycles	924
Max CPU cycles	1169
Avg CPU cycles	1021

Verification: Constant FiP32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Conversion test — OK

Conversion test for General block Constant.

Test results				
Time step	1	2	...	7
Mask parameters				
Value	1	-1	...	-2.3
Controller parameters				
K	2147483647	-2147483647	...	-2147483647
Exp. K	2147483647	-2147483647	...	-2147483647

Test settings	
Tolerance K	±0,0000e+00

Test case: Conversion-on-Target test — OK

Conversion-on-Target test for General block Constant.

Test results				
Time step	1	2	...	7
Mask parameters				
Value	1	-1	...	-2.3
Controller parameters				
K	2147483647	-2147483647	...	-2147483647
Exp. K	2147483647	-2147483647	...	-2147483647

Test settings	
Tolerance K	±0,0000e+00

Test statistics	
Min CPU cycles	1819
Max CPU cycles	2575
Avg CPU cycles	2263

Verification: Constant FiP32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Conversion test — OK

Conversion test for General block Constant.

Test results				
Time step	1	2	...	7
Mask parameters				
Value	1	-1	...	-2.3
Controller parameters				
K	2147483647	-2147483647	...	-2147483647
Exp. K	2147483647	-2147483647	...	-2147483647

Test settings	
Tolerance K	±0,0000e+00

Test case: Conversion-on-Target test — OK

Conversion-on-Target test for General block Constant.

Test results				
Time step	1	2	...	7
Mask parameters				
Value	1	-1	...	-2.3
Controller parameters				
K	2147483647	-2147483647	...	-2147483647
Exp. K	2147483647	-2147483647	...	-2147483647

Test settings	
Tolerance K	±0,0000e+00

Test statistics	
Min CPU cycles	729
Max CPU cycles	922
Avg CPU cycles	837

Verification: Constant FiP32 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Conversion test — OK

Conversion test for General block Constant.

Test results				
Time step	1	2	...	7
Mask parameters				
Value	1	-1	...	-2.3
Controller parameters				
K	2147483647	-2147483647	...	-2147483647
Exp. K	2147483647	-2147483647	...	-2147483647

Test settings	
Tolerance K	±0,0000e+00

Test case: Conversion-on-Target test — OK

Conversion-on-Target test for General block Constant.

Test results				
Time step	1	2	...	7
Mask parameters				
Value	1	-1	...	-2.3
Controller parameters				
K	2147483647	-2147483647	...	-2147483647
Exp. K	2147483647	-2147483647	...	-2147483647

Test settings	
Tolerance K	±0,0000e+00

Test statistics	
Min CPU cycles	1155
Max CPU cycles	1629
Avg CPU cycles	1552

Verification: Constant FiP32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Conversion test — OK

Conversion test for General block Constant.

Test results				
Time step	1	2	...	7
Mask parameters				
Value	1	-1	...	-2.3
Controller parameters				
K	2147483647	-2147483647	...	-2147483647
Exp. K	2147483647	-2147483647	...	-2147483647

Test settings	
Tolerance K	±0,0000e+00

Test case: Conversion-on-Target test — OK

Conversion-on-Target test for General block Constant.

Test results				
Time step	1	2	...	7
Mask parameters				
Value	1	-1	...	-2.3
Controller parameters				
K	2147483647	-2147483647	...	-2147483647
Exp. K	2147483647	-2147483647	...	-2147483647

Test settings	
Tolerance K	±0,0000e+00

Test statistics	
Min CPU cycles	670
Max CPU cycles	806
Avg CPU cycles	729

Verification: Constant FiP32 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Conversion test — OK

Conversion test for General block Constant.

Test results				
Time step	1	2	...	7
Mask parameters				
Value	1	-1	...	-2.3
Controller parameters				
K	2147483647	-2147483647	...	-2147483647
Exp. K	2147483647	-2147483647	...	-2147483647

Test settings	
Tolerance K	±0,0000e+00

Test case: Conversion-on-Target test — OK

Conversion-on-Target test for General block Constant.

Test results				
Time step	1	2	...	7
Mask parameters				
Value	1	-1	...	-2.3
Controller parameters				
K	2147483647	-2147483647	...	-2147483647
Exp. K	2147483647	-2147483647	...	-2147483647

Test settings	
Tolerance K	±0,0000e+00

Test statistics	
Min CPU cycles	800
Max CPU cycles	846
Avg CPU cycles	823

Verification: Constant Float32 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Conversion test OK

Conversion test for General block Constant.

Test results				
Time step	1	2	...	7
Mask parameters				
Value	1	-1	...	-2.3
Controller parameters				
K	1	-1	...	-2.3
Exp. K	1	-1	...	-2.3

Test settings	
Tolerance K	±0,0000e+00

Test case: Conversion-on-Target test OK

Conversion-on-Target test for General block Constant.

Test results				
Time step	1	2	...	7
Mask parameters				
Value	1	-1	...	-2.3
Controller parameters				
K	1	-1	...	-2.3
Exp. K	1	-1	...	-2.3

Test settings	
Tolerance K	±5,0000e-08

Test statistics	
Min CPU cycles	819
Max CPU cycles	836
Avg CPU cycles	821

Verification: Constant Float32 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Conversion test — OK

Conversion test for General block Constant.

Test results				
Time step	1	2	...	7
Mask parameters				
Value	1	-1	...	-2.3
Controller parameters				
K	1	-1	...	-2.3
Exp. K	1	-1	...	-2.3

Test settings	
Tolerance K	±0,0000e+00

Test case: Conversion-on-Target test — OK

Conversion-on-Target test for General block Constant.

Test results				
Time step	1	2	...	7
Mask parameters				
Value	1	-1	...	-2.3
Controller parameters				
K	1	-1	...	-2.3
Exp. K	1	-1	...	-2.3

Test settings	
Tolerance K	±5,0000e-08

Test statistics	
Min CPU cycles	401
Max CPU cycles	401
Avg CPU cycles	401

Verification: Constant Float32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Conversion test OK

Conversion test for General block Constant.

Test results				
Time step	1	2	...	7
Mask parameters				
Value	1	-1	...	-2.3
Controller parameters				
K	1	-1	...	-2.3
Exp. K	1	-1	...	-2.3

Test settings	
Tolerance K	±0,0000e+00

Test case: Conversion-on-Target test OK

Conversion-on-Target test for General block Constant.

Test results				
Time step	1	2	...	7
Mask parameters				
Value	1	-1	...	-2.3
Controller parameters				
K	1	-1	...	-2.3
Exp. K	1	-1	...	-2.3

Test settings	
Tolerance K	±5,0000e-08

Test statistics	
Min CPU cycles	471
Max CPU cycles	471
Avg CPU cycles	471

Verification: Constant Float32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Conversion test — OK

Conversion test for General block Constant.

Test results				
Time step	1	2	...	7
Mask parameters				
Value	1	-1	...	-2.3
Controller parameters				
K	1	-1	...	-2.3
Exp. K	1	-1	...	-2.3

Test settings	
Tolerance K	±0,0000e+00

Test case: Conversion-on-Target test — OK

Conversion-on-Target test for General block Constant.

Test results				
Time step	1	2	...	7
Mask parameters				
Value	1	-1	...	-2.3
Controller parameters				
K	1	-1	...	-2.3
Exp. K	1	-1	...	-2.3

Test settings	
Tolerance K	±5,0000e-08

Test statistics	
Min CPU cycles	673
Max CPU cycles	752
Avg CPU cycles	701

Verification: Constant Float32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Conversion test — OK

Conversion test for General block Constant.

Test results				
Time step	1	2	...	7
Mask parameters				
Value	1	-1	...	-2.3
Controller parameters				
K	1	-1	...	-2.3
Exp. K	1	-1	...	-2.3

Test settings	
Tolerance K	±0,0000e+00

Test case: Conversion-on-Target test — OK

Conversion-on-Target test for General block Constant.

Test results				
Time step	1	2	...	7
Mask parameters				
Value	1	-1	...	-2.3
Controller parameters				
K	1	-1	...	-2.3
Exp. K	1	-1	...	-2.3

Test settings	
Tolerance K	±5,0000e-08

Test statistics	
Min CPU cycles	279
Max CPU cycles	280
Avg CPU cycles	279

Verification: Constant Float32 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Conversion test — OK

Conversion test for General block Constant.

Test results				
Time step	1	2	...	7
Mask parameters				
Value	1	-1	...	-2.3
Controller parameters				
K	1	-1	...	-2.3
Exp. K	1	-1	...	-2.3

Test settings	
Tolerance K	±0,0000e+00

Test case: Conversion-on-Target test — OK

Conversion-on-Target test for General block Constant.

Test results				
Time step	1	2	...	7
Mask parameters				
Value	1	-1	...	-2.3
Controller parameters				
K	1	-1	...	-2.3
Exp. K	1	-1	...	-2.3

Test settings	
Tolerance K	±5,0000e-08

Test statistics	
Min CPU cycles	527
Max CPU cycles	868
Avg CPU cycles	819

Verification: Constant Float32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Conversion test OK

Conversion test for General block Constant.

Test results				
Time step	1	2	...	7
Mask parameters				
Value	1	-1	...	-2.3
Controller parameters				
K	1	-1	...	-2.3
Exp. K	1	-1	...	-2.3

Test settings	
Tolerance K	±0,0000e+00

Test case: Conversion-on-Target test OK

Conversion-on-Target test for General block Constant.

Test results				
Time step	1	2	...	7
Mask parameters				
Value	1	-1	...	-2.3
Controller parameters				
K	1	-1	...	-2.3
Exp. K	1	-1	...	-2.3

Test settings	
Tolerance K	±5,0000e-08

Test statistics	
Min CPU cycles	397
Max CPU cycles	444
Avg CPU cycles	405

Verification: Constant Float32 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Conversion test — OK

Conversion test for General block Constant.

Test results				
Time step	1	2	...	7
Mask parameters				
Value	1	-1	...	-2.3
Controller parameters				
K	1	-1	...	-2.3
Exp. K	1	-1	...	-2.3

Test settings	
Tolerance K	±0,0000e+00

Test case: Conversion-on-Target test — OK

Conversion-on-Target test for General block Constant.

Test results				
Time step	1	2	...	7
Mask parameters				
Value	1	-1	...	-2.3
Controller parameters				
K	1	-1	...	-2.3
Exp. K	1	-1	...	-2.3

Test settings	
Tolerance K	±5,0000e-08

Test statistics	
Min CPU cycles	649
Max CPU cycles	652
Avg CPU cycles	649

Block: Gain



Amplification of input by gain factor.

Inports	
In	Input

Outports	
Out	Amplified input

Mask Parameters		
Name	**ID**	**Description**
Gain	1	Gain factor in floating point format

Implementations:

FiP8 8 Bit Fixed Point Implementation
FiP16 16 Bit Fixed Point Implementation
FiP32 32 Bit Fixed Point Implementation
Float32 32 Bit Floating Point Implementation
Float64 64 Bit Floating Point Implementation

Implementation: FiP8

8 Bit Fixed Point Implementation

Inports Data Type	
In	int8

Outports Data Type	
Out	int8

Implementation: FiP16

16 Bit Fixed Point Implementation

Inports Data Type	
In	int16

Outports Data Type	
Out	int16

Implementation: FiP32

32 Bit Fixed Point Implementation

Inports Data Type	
In	int32

Outports Data Type	
Out	int32

Implementation: Float32

32 Bit Floating Point Implementation

Inports Data Type	
In	float32

Outports Data Type	
Out	float32

Implementation: Float64

64 Bit Floating Point Implementation

Inports Data Type	
In	float64

Outports Data Type	
Out	float64

Verification: Gain FiP16 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for General block Gain.

Test results						
Time step	1	2	3	4	...	9
CPU cycles	76	76	76	76	...	72
Inputs						
In (DSP)	-32768	-16384	-6554	-3277	...	32767
In	-1	-0.5	-0.2	-0.1	...	1
Parameters						
Gain	2.2					
Outputs						
Out	-1	-1	-0.44	-0.22	...	1
Exp. Out	-1	-1	-0.44	-0.22	...	1
Out (DSP)	-32767	-32767	-14419	-7210	...	32767
Exp. Out (DSP)	-32768	-32768	-14418	-7209	...	32767

Test settings	
Tolerance Out	±6,1035e-05 (±2 LSB)

Test statistics	
Min CPU cycles	72
Max CPU cycles	76
Avg CPU cycles	75

Test case: Parameter test OK

Parameter test for General block Gain.

Test results						
Time step	1	2	3	4	...	21
CPU cycles	76	76	76	76	...	72
Inputs						
In (DSP)	3277					
In	0.1					
Parameters						
Gain	-100	-50	-20	-10	...	100
Outputs						
Out	-1	-1	-1	-1	...	1
Exp. Out	-1	-1	-1	-1	...	1
Out (DSP)	-32767	-32767	-32767	-32767	...	32767
Exp. Out (DSP)	-32768	-32768	-32768	-32768	...	32767

Test settings	
Tolerance Out	±6,1035e-05 (±2 LSB)

Test statistics	
Min CPU cycles	72
Max CPU cycles	76
Avg CPU cycles	75

Test case: Conversion test **OK**

Conversion test for General block Gain.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Gain	-10	-9.444	-8.889	-8.333	...	10
Controller parameters						
V	-20480	-19342	-18204	-17067	...	20480
sfr	11	11	11	11	...	11
Exp. V	-20480	-19342	-18204	-17067	...	20480
Exp. sfr	11	11	11	11	...	11

Test settings	
Tolerance V	±0,0000e+00
Tolerance sfr	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block Gain.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Gain	-10	-9.444	-8.889	-8.333	...	10
Controller parameters						
V	-20480	-19342	-18204	-17066	...	20480
sfr	11	11	11	11	...	11
Exp. V	-20480	-19342	-18204	-17067	...	20480
Exp. sfr	11	11	11	11	...	11

Test settings	
Tolerance V	±1,0000e+00
Tolerance sfr	±0,0000e+00

Test statistics	
Min CPU cycles	1494
Max CPU cycles	3602
Avg CPU cycles	2854

Verification: Gain FiP16 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for General block Gain.

Test results						
Time step	1	2	3	4	...	9
CPU cycles	41	41	39	39	...	33
Inputs						
In (DSP)	-32768	-16384	-6554	-3277	...	32767
In	-1	-0.5	-0.2	-0.1	...	1
Parameters						
Gain	2.2					
Outputs						
Out	-1	-1	-0.44	-0.22	...	1
Exp. Out	-1	-1	-0.44	-0.22	...	1
Out (DSP)	-32767	-32767	-14419	-7210	...	32767
Exp. Out (DSP)	-32768	-32768	-14418	-7209	...	32767

Test settings	
Tolerance Out	±6,1035e-05 (±2 LSB)

Test statistics	
Min CPU cycles	33
Max CPU cycles	41
Avg CPU cycles	38

Test case: Parameter test OK

Parameter test for General block Gain.

Test results						
Time step	1	2	3	4	...	21
CPU cycles	41	41	41	41	...	33
Inputs						
In (DSP)	3277					
In	0.1					
Parameters						
Gain	-100	-50	-20	-10	...	100
Outputs						
Out	-1	-1	-1	-1	...	1
Exp. Out	-1	-1	-1	-1	...	1
Out (DSP)	-32767	-32767	-32767	-32767	...	32767
Exp. Out (DSP)	-32768	-32768	-32768	-32768	...	32767

Test settings	
Tolerance Out	±6,1035e-05 (±2 LSB)

Test statistics	
Min CPU cycles	33
Max CPU cycles	41
Avg CPU cycles	38

Test case: Conversion test **OK**

Conversion test for General block Gain.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Gain	-10	-9.444	-8.889	-8.333	...	10
Controller parameters						
V	-20480	-19342	-18204	-17067	...	20480
sfr	11	11	11	11	...	11
Exp. V	-20480	-19342	-18204	-17067	...	20480
Exp. sfr	11	11	11	11	...	11

Test settings	
Tolerance V	±0,0000e+00
Tolerance sfr	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block Gain.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Gain	-10	-9.444	-8.889	-8.333	...	10
Controller parameters						
V	-20480	-19342	-18204	-17066	...	20480
sfr	11	11	11	11	...	11
Exp. V	-20480	-19342	-18204	-17067	...	20480
Exp. sfr	11	11	11	11	...	11

Test settings	
Tolerance V	±1,0000e+00
Tolerance sfr	±0,0000e+00

Test statistics	
Min CPU cycles	771
Max CPU cycles	2031
Avg CPU cycles	1585

Verification: Gain FiP16 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for General block Gain.

Test results						
Time step	1	2	3	4	...	9
CPU cycles	77	77	77	77	...	77
Inputs						
In (DSP)	-32768	-16384	-6554	-3277	...	32767
In	-1	-0.5	-0.2	-0.1	...	1
Parameters						
Gain	2.2					
Outputs						
Out	-1	-1	-0.44	-0.22	...	1
Exp. Out	-1	-1	-0.44	-0.22	...	1
Out (DSP)	-32767	-32767	-14419	-7210	...	32767
Exp. Out (DSP)	-32768	-32768	-14418	-7209	...	32767

Test settings	
Tolerance Out	±6,1035e-05 (±2 LSB)

Test statistics	
Min CPU cycles	77
Max CPU cycles	77
Avg CPU cycles	77

Test case: Parameter test OK

Parameter test for General block Gain.

Test results						
Time step	1	2	3	4	...	21
CPU cycles	77	77	77	77	...	77
Inputs						
In (DSP)	3277					
In	0.1					
Parameters						
Gain	-100	-50	-20	-10	...	100
Outputs						
Out	-1	-1	-1	-1	...	1
Exp. Out	-1	-1	-1	-1	...	1
Out (DSP)	-32767	-32767	-32767	-32767	...	32767
Exp. Out (DSP)	-32768	-32768	-32768	-32768	...	32767

Test settings	
Tolerance Out	±6,1035e-05 (±2 LSB)

Test statistics	
Min CPU cycles	77
Max CPU cycles	77
Avg CPU cycles	77

Test case: Conversion test **OK**

Conversion test for General block Gain.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Gain	-10	-9.444	-8.889	-8.333	...	10
Controller parameters						
V	-20480	-19342	-18204	-17067	...	20480
sfr	11	11	11	11	...	11
Exp. V	-20480	-19342	-18204	-17067	...	20480
Exp. sfr	11	11	11	11	...	11

Test settings	
Tolerance V	±0,0000e+00
Tolerance sfr	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block Gain.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Gain	-10	-9.444	-8.889	-8.333	...	10
Controller parameters						
V	-20480	-19342	-18204	-17066	...	20480
sfr	11	11	11	11	...	11
Exp. V	-20480	-19342	-18204	-17067	...	20480
Exp. sfr	11	11	11	11	...	11

Test settings	
Tolerance V	±1,0000e+00
Tolerance sfr	±0,0000e+00

Test statistics	
Min CPU cycles	948
Max CPU cycles	1471
Avg CPU cycles	1288

Verification: Gain FiP16 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for General block Gain.

Test results						
Time step	1	2	3	4	...	9
CPU cycles	66	66	67	67	...	68
Inputs						
In (DSP)	-32768	-16384	-6554	-3277	...	32767
In	-1	-0.5	-0.2	-0.1	...	1
Parameters						
Gain	2.2					
Outputs						
Out	-1	-1	-0.44	-0.22	...	1
Exp. Out	-1	-1	-0.44	-0.22	...	1
Out (DSP)	-32767	-32767	-14419	-7210	...	32767
Exp. Out (DSP)	-32768	-32768	-14418	-7209	...	32767

Test settings	
Tolerance Out	±6,1035e-05 (±2 LSB)

Test statistics	
Min CPU cycles	66
Max CPU cycles	68
Avg CPU cycles	67

Test case: Parameter test OK

Parameter test for General block Gain.

Test results						
Time step	1	2	3	4	...	21
CPU cycles	66	66	66	66	...	68
Inputs						
In (DSP)	3277					
In	0.1					
Parameters						
Gain	-100	-50	-20	-10	...	100
Outputs						
Out	-1	-1	-1	-1	...	1
Exp. Out	-1	-1	-1	-1	...	1
Out (DSP)	-32767	-32767	-32767	-32767	...	32767
Exp. Out (DSP)	-32768	-32768	-32768	-32768	...	32767

Test settings	
Tolerance Out	±6,1035e-05 (±2 LSB)

Test statistics	
Min CPU cycles	66
Max CPU cycles	68
Avg CPU cycles	67

Test case: Conversion test **OK**

Conversion test for General block Gain.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Gain	-10	-9.444	-8.889	-8.333	...	10
Controller parameters						
V	-20480	-19342	-18204	-17067	...	20480
sfr	11	11	11	11	...	11
Exp. V	-20480	-19342	-18204	-17067	...	20480
Exp. sfr	11	11	11	11	...	11

Test settings	
Tolerance V	±0,0000e+00
Tolerance sfr	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block Gain.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Gain	-10	-9.444	-8.889	-8.333	...	10
Controller parameters						
V	-20480	-19342	-18204	-17066	...	20480
sfr	11	11	11	11	...	11
Exp. V	-20480	-19342	-18204	-17067	...	20480
Exp. sfr	11	11	11	11	...	11

Test settings	
Tolerance V	±1,0000e+00
Tolerance sfr	±0,0000e+00

Test statistics	
Min CPU cycles	1708
Max CPU cycles	4701
Avg CPU cycles	3713

Verification: Gain FiP16 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for General block Gain.

Test results						
Time step	1	2	3	4	...	9
CPU cycles	42	42	42	42	...	42
Inputs						
In (DSP)	-32768	-16384	-6554	-3277	...	32767
In	-1	-0.5	-0.2	-0.1	...	1
Parameters						
Gain	2.2					
Outputs						
Out	-1	-1	-0.44	-0.22	...	1
Exp. Out	-1	-1	-0.44	-0.22	...	1
Out (DSP)	-32767	-32767	-14419	-7210	...	32767
Exp. Out (DSP)	-32768	-32768	-14418	-7209	...	32767

Test settings	
Tolerance Out	±6,1035e-05 (±2 LSB)

Test statistics	
Min CPU cycles	42
Max CPU cycles	42
Avg CPU cycles	42

Test case: Parameter test OK

Parameter test for General block Gain.

Test results						
Time step	1	2	3	4	...	21
CPU cycles	42	42	42	42	...	42
Inputs						
In (DSP)	3277					
In	0.1					
Parameters						
Gain	-100	-50	-20	-10	...	100
Outputs						
Out	-1	-1	-1	-1	...	1
Exp. Out	-1	-1	-1	-1	...	1
Out (DSP)	-32767	-32767	-32767	-32767	...	32767
Exp. Out (DSP)	-32768	-32768	-32768	-32768	...	32767

Test settings	
Tolerance Out	±6,1035e-05 (±2 LSB)

Test statistics	
Min CPU cycles	42
Max CPU cycles	42
Avg CPU cycles	42

Test case: Conversion test **OK**

Conversion test for General block Gain.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Gain	-10	-9.444	-8.889	-8.333	...	10
Controller parameters						
V	-20480	-19342	-18204	-17067	...	20480
sfr	11	11	11	11	...	11
Exp. V	-20480	-19342	-18204	-17067	...	20480
Exp. sfr	11	11	11	11	...	11

Test settings	
Tolerance V	±0,0000e+00
Tolerance sfr	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block Gain.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Gain	-10	-9.444	-8.889	-8.333	...	10
Controller parameters						
V	-20480	-19342	-18204	-17066	...	20480
sfr	11	11	11	11	...	11
Exp. V	-20480	-19342	-18204	-17067	...	20480
Exp. sfr	11	11	11	11	...	11

Test settings	
Tolerance V	±1,0000e+00
Tolerance sfr	±0,0000e+00

Test statistics	
Min CPU cycles	815
Max CPU cycles	1984
Avg CPU cycles	1588

Verification: Gain FiP16 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for General block Gain.

Test results						
Time step	1	2	3	4	...	9
CPU cycles	68	68	69	69	...	68
Inputs						
In (DSP)	-32768	-16384	-6554	-3277	...	32767
In	-1	-0.5	-0.2	-0.1	...	1
Parameters						
Gain	2.2					
Outputs						
Out	-1	-1	-0.44	-0.22	...	1
Exp. Out	-1	-1	-0.44	-0.22	...	1
Out (DSP)	-32767	-32767	-14419	-7210	...	32767
Exp. Out (DSP)	-32768	-32768	-14418	-7209	...	32767

Test settings	
Tolerance Out	±6,1035e-05 (±2 LSB)

Test statistics	
Min CPU cycles	68
Max CPU cycles	69
Avg CPU cycles	68

Test case: Parameter test OK

Parameter test for General block Gain.

Test results						
Time step	1	2	3	4	...	21
CPU cycles	68	68	68	68	...	68
Inputs						
In (DSP)	3277					
In	0.1					
Parameters						
Gain	-100	-50	-20	-10	...	100
Outputs						
Out	-1	-1	-1	-1	...	1
Exp. Out	-1	-1	-1	-1	...	1
Out (DSP)	-32767	-32767	-32767	-32767	...	32767
Exp. Out (DSP)	-32768	-32768	-32768	-32768	...	32767

Test settings	
Tolerance Out	±6,1035e-05 (±2 LSB)

Test statistics	
Min CPU cycles	68
Max CPU cycles	69
Avg CPU cycles	68

Test case: Conversion test **OK**

Conversion test for General block Gain.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Gain	-10	-9.444	-8.889	-8.333	...	10
Controller parameters						
V	-20480	-19342	-18204	-17067	...	20480
sfr	11	11	11	11	...	11
Exp. V	-20480	-19342	-18204	-17067	...	20480
Exp. sfr	11	11	11	11	...	11

Test settings	
Tolerance V	±0,0000e+00
Tolerance sfr	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block Gain.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Gain	-10	-9.444	-8.889	-8.333	...	10
Controller parameters						
V	-20480	-19342	-18204	-17066	...	20480
sfr	11	11	11	11	...	11
Exp. V	-20480	-19342	-18204	-17067	...	20480
Exp. sfr	11	11	11	11	...	11

Test settings	
Tolerance V	±1,0000e+00
Tolerance sfr	±0,0000e+00

Test statistics	
Min CPU cycles	2593
Max CPU cycles	10879
Avg CPU cycles	8317

Verification: Gain FiP16 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for General block Gain.

Test results						
Time step	1	2	3	4	...	9
CPU cycles	86	77	77	77	...	77
Inputs						
In (DSP)	-32768	-16384	-6554	-3277	...	32767
In	-1	-0.5	-0.2	-0.1	...	1
Parameters						
Gain	2.2					
Outputs						
Out	-1	-1	-0.44	-0.22	...	1
Exp. Out	-1	-1	-0.44	-0.22	...	1
Out (DSP)	-32767	-32767	-14419	-7210	...	32767
Exp. Out (DSP)	-32768	-32768	-14418	-7209	...	32767

Test settings	
Tolerance Out	±6,1035e-05 (±2 LSB)

Test statistics	
Min CPU cycles	77
Max CPU cycles	86
Avg CPU cycles	78

Test case: Parameter test OK

Parameter test for General block Gain.

Test results						
Time step	1	2	3	4	...	21
CPU cycles	77	77	77	77	...	77
Inputs						
In (DSP)	3277					
In	0.1					
Parameters						
Gain	-100	-50	-20	-10	...	100
Outputs						
Out	-1	-1	-1	-1	...	1
Exp. Out	-1	-1	-1	-1	...	1
Out (DSP)	-32767	-32767	-32767	-32767	...	32767
Exp. Out (DSP)	-32768	-32768	-32768	-32768	...	32767

Test settings	
Tolerance Out	±6,1035e-05 (±2 LSB)

Test statistics	
Min CPU cycles	77
Max CPU cycles	77
Avg CPU cycles	77

Test case: Conversion test **OK**

Conversion test for General block Gain.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Gain	-10	-9.444	-8.889	-8.333	...	10
Controller parameters						
V	-20480	-19342	-18204	-17067	...	20480
sfr	11	11	11	11	...	11
Exp. V	-20480	-19342	-18204	-17067	...	20480
Exp. sfr	11	11	11	11	...	11

Test settings	
Tolerance V	±0,0000e+00
Tolerance sfr	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block Gain.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Gain	-10	-9.444	-8.889	-8.333	...	10
Controller parameters						
V	-20480	-19342	-18204	-17066	...	20480
sfr	11	11	11	11	...	11
Exp. V	-20480	-19342	-18204	-17067	...	20480
Exp. sfr	11	11	11	11	...	11

Test settings	
Tolerance V	±1,0000e+00
Tolerance sfr	±0,0000e+00

Test statistics	
Min CPU cycles	633
Max CPU cycles	1281
Avg CPU cycles	948

Verification: Gain FiP16 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for General block Gain.

Test results						
Time step	1	2	3	4	...	9
CPU cycles	60	60	60	60	...	59
Inputs						
In (DSP)	-32768	-16384	-6554	-3277	...	32767
In	-1	-0.5	-0.2	-0.1	...	1
Parameters						
Gain	2.2					
Outputs						
Out	-1	-1	-0.44	-0.22	...	1
Exp. Out	-1	-1	-0.44	-0.22	...	1
Out (DSP)	-32767	-32767	-14419	-7210	...	32767
Exp. Out (DSP)	-32768	-32768	-14418	-7209	...	32767

Test settings	
Tolerance Out	±6,1035e-05 (±2 LSB)

Test statistics	
Min CPU cycles	59
Max CPU cycles	60
Avg CPU cycles	59

Test case: Parameter test OK

Parameter test for General block Gain.

Test results						
Time step	1	2	3	4	...	21
CPU cycles	60	60	60	60	...	59
Inputs						
In (DSP)	3277					
In	0.1					
Parameters						
Gain	-100	-50	-20	-10	...	100
Outputs						
Out	-1	-1	-1	-1	...	1
Exp. Out	-1	-1	-1	-1	...	1
Out (DSP)	-32767	-32767	-32767	-32767	...	32767
Exp. Out (DSP)	-32768	-32768	-32768	-32768	...	32767

Test settings	
Tolerance Out	±6,1035e-05 (±2 LSB)

Test statistics	
Min CPU cycles	59
Max CPU cycles	60
Avg CPU cycles	59

Test case: Conversion test **OK**

Conversion test for General block Gain.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Gain	-10	-9.444	-8.889	-8.333	...	10
Controller parameters						
V	-20480	-19342	-18204	-17067	...	20480
sfr	11	11	11	11	...	11
Exp. V	-20480	-19342	-18204	-17067	...	20480
Exp. sfr	11	11	11	11	...	11

Test settings	
Tolerance V	±0,0000e+00
Tolerance sfr	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block Gain.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Gain	-10	-9.444	-8.889	-8.333	...	10
Controller parameters						
V	-20480	-19342	-18204	-17066	...	20480
sfr	11	11	11	11	...	11
Exp. V	-20480	-19342	-18204	-17067	...	20480
Exp. sfr	11	11	11	11	...	11

Test settings	
Tolerance V	±1,0000e+00
Tolerance sfr	±0,0000e+00

Test statistics	
Min CPU cycles	1113
Max CPU cycles	2817
Avg CPU cycles	2222

Verification: Gain FiP32 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for General block Gain.

Test results				
Time step	1	2	...	9
CPU cycles	179	172	...	124
Inputs				
In (DSP)	-2147483648	-1073741824	...	2147483647
In	-1	-0.5	...	1
Parameters				
Gain	2.2			
Outputs				
Out	-1	-1	...	1
Exp. Out	-1	-1	...	1
Out (DSP)	-2147483647	-2147483647	...	2147483647
Exp. Out (DSP)	-2147483648	-2147483648	...	2147483647

Test settings	
Tolerance Out	±9,3132e-10 (±2 LSB)

Test statistics	
Min CPU cycles	117
Max CPU cycles	179
Avg CPU cycles	158

Test case: Parameter test OK

Parameter test for General block Gain.

Test results				
Time step	1	2	...	21
CPU cycles	179	179	...	124
Inputs				
In (DSP)	214748365			
In	0.1			
Parameters				
Gain	-100	-50	...	100
Outputs				
Out	-1	-1	...	1
Exp. Out	-1	-1	...	1
Out (DSP)	-2147483647	-2147483647	...	2147483647
Exp. Out (DSP)	-2147483648	-2147483648	...	2147483647

Test settings	
Tolerance Out	±9,3132e-10 (±2 LSB)

Test statistics	
Min CPU cycles	117
Max CPU cycles	179
Avg CPU cycles	159

Test case: Conversion test **OK**

Conversion test for General block Gain.

Test results				
Time step	1	2	...	37
Mask parameters				
Gain	-10	-9.444	...	10
Controller parameters				
V	-1342177280	-1267611876	...	1342177280
sfr	27	27	...	27
Exp. V	-1342177280	-1267611876	...	1342177280
Exp. sfr	27	27	...	27

Test settings	
Tolerance V	±0,0000e+00
Tolerance sfr	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block Gain.

Test results				
Time step	1	2	...	37
Mask parameters				
Gain	-10	-9.444	...	10
Controller parameters				
V	-1342177280	-1267611904	...	1342177280
sfr	27	27	...	27
Exp. V	-1342177280	-1267611876	...	1342177280
Exp. sfr	27	27	...	27

Test settings	
Tolerance V	±7,0000e+01
Tolerance sfr	±0,0000e+00

Test statistics	
Min CPU cycles	1646
Max CPU cycles	3803
Avg CPU cycles	3050

Verification: Gain FiP32 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for General block Gain.

Test results				
Time step	1	2	...	9
CPU cycles	85	85	...	75
Inputs				
In (DSP)	-2147483648	-1073741824	...	2147483647
In	-1	-0.5	...	1
Parameters				
Gain	2.2			
Outputs				
Out	-1	-1	...	1
Exp. Out	-1	-1	...	1
Out (DSP)	-2147483647	-2147483647	...	2147483647
Exp. Out (DSP)	-2147483648	-2147483648	...	2147483647

Test settings	
Tolerance Out	±9,3132e-10 (±2 LSB)

Test statistics	
Min CPU cycles	75
Max CPU cycles	85
Avg CPU cycles	80

Test case: Parameter test OK

Parameter test for General block Gain.

Test results				
Time step	1	2	...	21
CPU cycles	85	85	...	75
Inputs				
In (DSP)	214748365			
In	0.1			
Parameters				
Gain	-100	-50	...	100
Outputs				
Out	-1	-1	...	1
Exp. Out	-1	-1	...	1
Out (DSP)	-2147483647	-2147483647	...	2147483647
Exp. Out (DSP)	-2147483648	-2147483648	...	2147483647

Test settings	
Tolerance Out	±9,3132e-10 (±2 LSB)

Test statistics	
Min CPU cycles	75
Max CPU cycles	85
Avg CPU cycles	80

Test case: Conversion test **OK**

Conversion test for General block Gain.

Test results				
Time step	1	2	...	37
Mask parameters				
Gain	-10	-9.444	...	10
Controller parameters				
V	-1342177280	-1267611876	...	1342177280
sfr	27	27	...	27
Exp. V	-1342177280	-1267611876	...	1342177280
Exp. sfr	27	27	...	27

Test settings	
Tolerance V	±0,0000e+00
Tolerance sfr	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block Gain.

Test results				
Time step	1	2	...	37
Mask parameters				
Gain	-10	-9.444	...	10
Controller parameters				
V	-1342177280	-1267611904	...	1342177280
sfr	27	27	...	27
Exp. V	-1342177280	-1267611876	...	1342177280
Exp. sfr	27	27	...	27

Test settings	
Tolerance V	±7,0000e+01
Tolerance sfr	±0,0000e+00

Test statistics	
Min CPU cycles	725
Max CPU cycles	1629
Avg CPU cycles	1322

Verification: Gain FiP32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for General block Gain.

Test results				
Time step	1	2	...	9
CPU cycles	107	107	...	107
Inputs				
In (DSP)	-2147483648	-1073741824	...	2147483647
In	-1	-0.5	...	1
Parameters				
Gain	2.2			
Outputs				
Out	-1	-1	...	1
Exp. Out	-1	-1	...	1
Out (DSP)	-2147483647	-2147483647	...	2147483647
Exp. Out (DSP)	-2147483648	-2147483648	...	2147483647

Test settings	
Tolerance Out	±9,3132e-10 (±2 LSB)

Test statistics	
Min CPU cycles	107
Max CPU cycles	107
Avg CPU cycles	107

Test case: Parameter test OK

Parameter test for General block Gain.

Test results				
Time step	1	2	...	21
CPU cycles	107	107	...	107
Inputs				
In (DSP)	214748365			
In	0.1			
Parameters				
Gain	-100	-50	...	100
Outputs				
Out	-1	-1	...	1
Exp. Out	-1	-1	...	1
Out (DSP)	-2147483647	-2147483647	...	2147483647
Exp. Out (DSP)	-2147483648	-2147483648	...	2147483647

Test settings	
Tolerance Out	±9,3132e-10 (±2 LSB)

Test statistics	
Min CPU cycles	107
Max CPU cycles	107
Avg CPU cycles	107

Test case: Conversion test **OK**

Conversion test for General block Gain.

Test results				
Time step	1	2	...	37
Mask parameters				
Gain	-10	-9.444	...	10
Controller parameters				
V	-1342177280	-1267611876	...	1342177280
sfr	27	27	...	27
Exp. V	-1342177280	-1267611876	...	1342177280
Exp. sfr	27	27	...	27

Test settings	
Tolerance V	±0,0000e+00
Tolerance sfr	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block Gain.

Test results				
Time step	1	2	...	37
Mask parameters				
Gain	-10	-9.444	...	10
Controller parameters				
V	-1342177280	-1267611904	...	1342177280
sfr	27	27	...	27
Exp. V	-1342177280	-1267611876	...	1342177280
Exp. sfr	27	27	...	27

Test settings	
Tolerance V	±7,0000e+01
Tolerance sfr	±0,0000e+00

Test statistics	
Min CPU cycles	1300
Max CPU cycles	1868
Avg CPU cycles	1676

Verification: Gain FiP32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for General block Gain.

Test results				
Time step	1	2	...	9
CPU cycles	162	168	...	156
Inputs				
In (DSP)	-2147483648	-1073741824	...	2147483647
In	-1	-0.5	...	1
Parameters				
Gain	2.2			
Outputs				
Out	-1	-1	...	1
Exp. Out	-1	-1	...	1
Out (DSP)	-2147483647	-2147483647	...	2147483647
Exp. Out (DSP)	-2147483648	-2147483648	...	2147483647

Test settings	
Tolerance Out	±9,3132e-10 (±2 LSB)

Test statistics	
Min CPU cycles	156
Max CPU cycles	170
Avg CPU cycles	164

Test case: Parameter test OK

Parameter test for General block Gain.

Test results				
Time step	1	2	...	21
CPU cycles	162	162	...	156
Inputs				
In (DSP)	214748365			
In	0.1			
Parameters				
Gain	-100	-50	...	100
Outputs				
Out	-1	-1	...	1
Exp. Out	-1	-1	...	1
Out (DSP)	-2147483647	-2147483647	...	2147483647
Exp. Out (DSP)	-2147483648	-2147483648	...	2147483647

Test settings	
Tolerance Out	±9,3132e-10 (±2 LSB)

Test statistics	
Min CPU cycles	156
Max CPU cycles	170
Avg CPU cycles	163

Test case: Conversion test **OK**

Conversion test for General block Gain.

Test results				
Time step	1	2	...	37
Mask parameters				
Gain	-10	-9.444	...	10
Controller parameters				
V	-1342177280	-1267611876	...	1342177280
sfr	27	27	...	27
Exp. V	-1342177280	-1267611876	...	1342177280
Exp. sfr	27	27	...	27

Test settings	
Tolerance V	±0,0000e+00
Tolerance sfr	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block Gain.

Test results				
Time step	1	2	...	37
Mask parameters				
Gain	-10	-9.444	...	10
Controller parameters				
V	-1342177280	-1267611904	...	1342177280
sfr	27	27	...	27
Exp. V	-1342177280	-1267611876	...	1342177280
Exp. sfr	27	27	...	27

Test settings	
Tolerance V	±7,0000e+01
Tolerance sfr	±0,0000e+00

Test statistics	
Min CPU cycles	2741
Max CPU cycles	5965
Avg CPU cycles	4976

Verification: Gain FiP32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for General block Gain.

Test results				
Time step	1	2	...	9
CPU cycles	54	60	...	54
Inputs				
In (DSP)	-2147483648	-1073741824	...	2147483647
In	-1	-0.5	...	1
Parameters				
Gain	2.2			
Outputs				
Out	-1	-1	...	1
Exp. Out	-1	-1	...	1
Out (DSP)	-2147483647	-2147483647	...	2147483647
Exp. Out (DSP)	-2147483648	-2147483648	...	2147483647

Test settings	
Tolerance Out	±9,3132e-10 (±2 LSB)

Test statistics	
Min CPU cycles	54
Max CPU cycles	60
Avg CPU cycles	57

Test case: Parameter test OK

Parameter test for General block Gain.

Test results				
Time step	1	2	...	21
CPU cycles	54	54	...	54
Inputs				
In (DSP)	214748365			
In	0.1			
Parameters				
Gain	-100	-50	...	100
Outputs				
Out	-1	-1	...	1
Exp. Out	-1	-1	...	1
Out (DSP)	-2147483647	-2147483647	...	2147483647
Exp. Out (DSP)	-2147483648	-2147483648	...	2147483647

Test settings	
Tolerance Out	±9,3132e-10 (±2 LSB)

Test statistics	
Min CPU cycles	54
Max CPU cycles	60
Avg CPU cycles	56

Test case: Conversion test **OK**

Conversion test for General block Gain.

Test results				
Time step	1	2	...	37
Mask parameters				
Gain	-10	-9.444	...	10
Controller parameters				
V	-1342177280	-1267611876	...	1342177280
sfr	27	27	...	27
Exp. V	-1342177280	-1267611876	...	1342177280
Exp. sfr	27	27	...	27

Test settings	
Tolerance V	±0,0000e+00
Tolerance sfr	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block Gain.

Test results				
Time step	1	2	...	37
Mask parameters				
Gain	-10	-9.444	...	10
Controller parameters				
V	-1342177280	-1267611904	...	1342177280
sfr	27	27	...	27
Exp. V	-1342177280	-1267611876	...	1342177280
Exp. sfr	27	27	...	27

Test settings	
Tolerance V	±7,0000e+01
Tolerance sfr	±0,0000e+00

Test statistics	
Min CPU cycles	1271
Max CPU cycles	2454
Avg CPU cycles	2057

Verification: Gain FiP32 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for General block Gain.

Test results				
Time step	1	2	...	9
CPU cycles	474	474	...	467
Inputs				
In (DSP)	-2147483648	-1073741824	...	2147483647
In	-1	-0.5	...	1
Parameters				
Gain	2.2			
Outputs				
Out	-1	-1	...	1
Exp. Out	-1	-1	...	1
Out (DSP)	-2147483647	-2147483647	...	2147483647
Exp. Out (DSP)	-2147483648	-2147483648	...	2147483647

Test settings	
Tolerance Out	±9,3132e-10 (±2 LSB)

Test statistics	
Min CPU cycles	466
Max CPU cycles	474
Avg CPU cycles	469

Test case: Parameter test OK

Parameter test for General block Gain.

Test results				
Time step	1	2	...	21
CPU cycles	424	434	...	417
Inputs				
In (DSP)	214748365			
In	0.1			
Parameters				
Gain	-100	-50	...	100
Outputs				
Out	-1	-1	...	1
Exp. Out	-1	-1	...	1
Out (DSP)	-2147483647	-2147483647	...	2147483647
Exp. Out (DSP)	-2147483648	-2147483648	...	2147483647

Test settings	
Tolerance Out	±9,3132e-10 (±2 LSB)

Test statistics	
Min CPU cycles	417
Max CPU cycles	493
Avg CPU cycles	463

Test case: Conversion test **OK**

Conversion test for General block Gain.

Test results				
Time step	1	2	...	37
Mask parameters				
Gain	-10	-9.444	...	10
Controller parameters				
V	-1342177280	-1267611876	...	1342177280
sfr	27	27	...	27
Exp. V	-1342177280	-1267611876	...	1342177280
Exp. sfr	27	27	...	27

Test settings	
Tolerance V	±0,0000e+00
Tolerance sfr	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block Gain.

Test results				
Time step	1	2	...	37
Mask parameters				
Gain	-10	-9.444	...	10
Controller parameters				
V	-1342177280	-1267611904	...	1342177280
sfr	27	27	...	27
Exp. V	-1342177280	-1267611876	...	1342177280
Exp. sfr	27	27	...	27

Test settings	
Tolerance V	±7,0000e+01
Tolerance sfr	±0,0000e+00

Test statistics	
Min CPU cycles	2999
Max CPU cycles	11019
Avg CPU cycles	8556

Verification: Gain FiP32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for General block Gain.

Test results				
Time step	1	2	...	9
CPU cycles	122	100	...	100
Inputs				
In (DSP)	-2147483648	-1073741824	...	2147483647
In	-1	-0.5	...	1
Parameters				
Gain	2.2			
Outputs				
Out	-1	-1	...	1
Exp. Out	-1	-1	...	1
Out (DSP)	-2147483647	-2147483647	...	2147483647
Exp. Out (DSP)	-2147483648	-2147483648	...	2147483647

Test settings	
Tolerance Out	±9,3132e-10 (±2 LSB)

Test statistics	
Min CPU cycles	100
Max CPU cycles	122
Avg CPU cycles	102

Test case: Parameter test OK

Parameter test for General block Gain.

Test results				
Time step	1	2	...	21
CPU cycles	100	100	...	100
Inputs				
In (DSP)	214748365			
In	0.1			
Parameters				
Gain	-100	-50	...	100
Outputs				
Out	-1	-1	...	1
Exp. Out	-1	-1	...	1
Out (DSP)	-2147483647	-2147483647	...	2147483647
Exp. Out (DSP)	-2147483648	-2147483648	...	2147483647

Test settings	
Tolerance Out	±9,3132e-10 (±2 LSB)

Test statistics	
Min CPU cycles	100
Max CPU cycles	100
Avg CPU cycles	100

Test case: Conversion test **OK**

Conversion test for General block Gain.

Test results				
Time step	1	2	...	37
Mask parameters				
Gain	-10	-9.444	...	10
Controller parameters				
V	-1342177280	-1267611876	...	1342177280
sfr	27	27	...	27
Exp. V	-1342177280	-1267611876	...	1342177280
Exp. sfr	27	27	...	27

Test settings	
Tolerance V	±0,0000e+00
Tolerance sfr	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block Gain.

Test results				
Time step	1	2	...	37
Mask parameters				
Gain	-10	-9.444	...	10
Controller parameters				
V	-1342177280	-1267611904	...	1342177280
sfr	27	27	...	27
Exp. V	-1342177280	-1267611876	...	1342177280
Exp. sfr	27	27	...	27

Test settings	
Tolerance V	±7,0000e+01
Tolerance sfr	±0,0000e+00

Test statistics	
Min CPU cycles	941
Max CPU cycles	1559
Avg CPU cycles	1263

Verification: Gain FiP32 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for General block Gain.

Test results				
Time step	1	2	...	9
CPU cycles	150	144	...	103
Inputs				
In (DSP)	-2147483648	-1073741824	...	2147483647
In	-1	-0.5	...	1
Parameters				
Gain	2.2			
Outputs				
Out	-1	-1	...	1
Exp. Out	-1	-1	...	1
Out (DSP)	-2147483647	-2147483647	...	2147483647
Exp. Out (DSP)	-2147483648	-2147483648	...	2147483647

Test settings	
Tolerance Out	±9,3132e-10 (±2 LSB)

Test statistics	
Min CPU cycles	97
Max CPU cycles	150
Avg CPU cycles	130

Test case: Parameter test OK

Parameter test for General block Gain.

Test results				
Time step	1	2	...	21
CPU cycles	150	150	...	103
Inputs				
In (DSP)	214748365			
In	0.1			
Parameters				
Gain	-100	-50	...	100
Outputs				
Out	-1	-1	...	1
Exp. Out	-1	-1	...	1
Out (DSP)	-2147483647	-2147483647	...	2147483647
Exp. Out (DSP)	-2147483648	-2147483648	...	2147483647

Test settings	
Tolerance Out	±9,3132e-10 (±2 LSB)

Test statistics	
Min CPU cycles	97
Max CPU cycles	150
Avg CPU cycles	131

Test case: Conversion test **OK**

Conversion test for General block Gain.

Test results				
Time step	1	2	...	37
Mask parameters				
Gain	-10	-9.444	...	10
Controller parameters				
V	-1342177280	-1267611876	...	1342177280
sfr	27	27	...	27
Exp. V	-1342177280	-1267611876	...	1342177280
Exp. sfr	27	27	...	27

Test settings	
Tolerance V	±0,0000e+00
Tolerance sfr	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block Gain.

Test results				
Time step	1	2	...	37
Mask parameters				
Gain	-10	-9.444	...	10
Controller parameters				
V	-1342177280	-1267611904	...	1342177280
sfr	27	27	...	27
Exp. V	-1342177280	-1267611876	...	1342177280
Exp. sfr	27	27	...	27

Test settings	
Tolerance V	±7,0000e+01
Tolerance sfr	±0,0000e+00

Test statistics	
Min CPU cycles	1227
Max CPU cycles	2971
Avg CPU cycles	2371

Verification: Gain Float32 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test

OK

Inport test for General block Gain.

Test results				
Time step	1	2	...	9
CPU cycles	58	58	...	58
Inputs				
In (DSP)	-1	-0.5	...	1
In	-1	-0.5	...	1
Parameters				
Gain	2.2			
Outputs				
Out	-2.2	-1.1	...	2.2
Exp. Out	-2.2	-1.1	...	2.2
Out (DSP)	-2.2	-1.1	...	2.2
Exp. Out (DSP)	-2.2	-1.1	...	2.2

Test settings	
Tolerance Out	±5,5879e-08 (±120 LSB)

Test statistics	
Min CPU cycles	58
Max CPU cycles	58
Avg CPU cycles	58

Test case: Parameter test

OK

Parameter test for General block Gain.

Test results				
Time step	1	2	...	21
CPU cycles	58	58	...	58
Inputs				
In (DSP)	0.1			
In	0.1			
Parameters				
Gain	-100	-50	...	100
Outputs				
Out	-10	-5	...	10
Exp. Out	-10	-5	...	10
Out (DSP)	-10	-5	...	10
Exp. Out (DSP)	-10	-5	...	10

Test settings	
Tolerance Out	±9,3132e-09 (±20 LSB)

Test statistics	
Min CPU cycles	58
Max CPU cycles	58
Avg CPU cycles	58

Test case: Conversion test **OK**

Conversion test for General block Gain.

Test results				
Time step	1	2	...	37
Mask parameters				
Gain	-10	-9.444	...	10
Controller parameters				
V	-10	-9.444	...	10
Exp. V	-10	-9.444	...	10

Test settings	
Tolerance V	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block Gain.

Test results				
Time step	1	2	...	37
Mask parameters				
Gain	-10	-9.444	...	10
Controller parameters				
V	-10	-9.444	...	10
Exp. V	-10	-9.444	...	10

Test settings	
Tolerance V	±1,0000e-06

Test statistics	
Min CPU cycles	821
Max CPU cycles	838
Avg CPU cycles	821

Verification: Gain Float32 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for General block Gain.

Test results				
Time step	1	2	...	9
CPU cycles	27	27	...	27
Inputs				
In (DSP)	-1	-0.5	...	1
In	-1	-0.5	...	1
Parameters				
Gain	2.2			
Outputs				
Out	-2.2	-1.1	...	2.2
Exp. Out	-2.2	-1.1	...	2.2
Out (DSP)	-2.2	-1.1	...	2.2
Exp. Out (DSP)	-2.2	-1.1	...	2.2

Test settings	
Tolerance Out	±5,5879e-08 (±120 LSB)

Test statistics	
Min CPU cycles	27
Max CPU cycles	27
Avg CPU cycles	27

Test case: Parameter test OK

Parameter test for General block Gain.

Test results				
Time step	1	2	...	21
CPU cycles	27	27	...	27
Inputs				
In (DSP)	0.1			
In	0.1			
Parameters				
Gain	-100	-50	...	100
Outputs				
Out	-10	-5	...	10
Exp. Out	-10	-5	...	10
Out (DSP)	-10	-5	...	10
Exp. Out (DSP)	-10	-5	...	10

Test settings	
Tolerance Out	±9,3132e-09 (±20 LSB)

Test statistics	
Min CPU cycles	27
Max CPU cycles	27
Avg CPU cycles	27

Test case: Conversion test **OK**

Conversion test for General block Gain.

Test results				
Time step	1	2	...	37
Mask parameters				
Gain	-10	-9.444	...	10
Controller parameters				
V	-10	-9.444	...	10
Exp. V	-10	-9.444	...	10

Test settings	
Tolerance V	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block Gain.

Test results				
Time step	1	2	...	37
Mask parameters				
Gain	-10	-9.444	...	10
Controller parameters				
V	-10	-9.444	...	10
Exp. V	-10	-9.444	...	10

Test settings	
Tolerance V	±1,0000e-06

Test statistics	
Min CPU cycles	397
Max CPU cycles	397
Avg CPU cycles	397

Verification: Gain Float32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for General block Gain.

Test results				
Time step	1	2	...	9
CPU cycles	62	62	...	62
Inputs				
In (DSP)	-1	-0.5	...	1
In	-1	-0.5	...	1
Parameters				
Gain	2.2			
Outputs				
Out	-2.2	-1.1	...	2.2
Exp. Out	-2.2	-1.1	...	2.2
Out (DSP)	-2.2	-1.1	...	2.2
Exp. Out (DSP)	-2.2	-1.1	...	2.2

Test settings	
Tolerance Out	±5,5879e-08 (±120 LSB)

Test statistics	
Min CPU cycles	62
Max CPU cycles	62
Avg CPU cycles	62

Test case: Parameter test OK

Parameter test for General block Gain.

Test results				
Time step	1	2	...	21
CPU cycles	62	62	...	62
Inputs				
In (DSP)	0.1			
In	0.1			
Parameters				
Gain	-100	-50	...	100
Outputs				
Out	-10	-5	...	10
Exp. Out	-10	-5	...	10
Out (DSP)	-10	-5	...	10
Exp. Out (DSP)	-10	-5	...	10

Test settings	
Tolerance Out	±9,3132e-09 (±20 LSB)

Test statistics	
Min CPU cycles	62
Max CPU cycles	62
Avg CPU cycles	62

Test case: Conversion test **OK**

Conversion test for General block Gain.

Test results				
Time step	1	2	...	37
Mask parameters				
Gain	-10	-9.444	...	10
Controller parameters				
V	-10	-9.444	...	10
Exp. V	-10	-9.444	...	10

Test settings	
Tolerance V	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block Gain.

Test results				
Time step	1	2	...	37
Mask parameters				
Gain	-10	-9.444	...	10
Controller parameters				
V	-10	-9.444	...	10
Exp. V	-10	-9.444	...	10

Test settings	
Tolerance V	±1,0000e-06

Test statistics	
Min CPU cycles	467
Max CPU cycles	467
Avg CPU cycles	467

Verification: Gain Float32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for General block Gain.

Test results				
Time step	1	2	...	9
CPU cycles	228	228	...	228
Inputs				
In (DSP)	-1	-0.5	...	1
In	-1	-0.5	...	1
Parameters				
Gain	2.2			
Outputs				
Out	-2.2	-1.1	...	2.2
Exp. Out	-2.2	-1.1	...	2.2
Out (DSP)	-2.2	-1.1	...	2.2
Exp. Out (DSP)	-2.2	-1.1	...	2.2

Test settings	
Tolerance Out	±5,5879e-08 (±120 LSB)

Test statistics	
Min CPU cycles	170
Max CPU cycles	229
Avg CPU cycles	222

Test case: Parameter test OK

Parameter test for General block Gain.

Test results				
Time step	1	2	...	21
CPU cycles	225	225	...	225
Inputs				
In (DSP)	0.1			
In	0.1			
Parameters				
Gain	-100	-50	...	100
Outputs				
Out	-10	-5	...	10
Exp. Out	-10	-5	...	10
Out (DSP)	-10	-5	...	10
Exp. Out (DSP)	-10	-5	...	10

Test settings	
Tolerance Out	±9,3132e-09 (±20 LSB)

Test statistics	
Min CPU cycles	174
Max CPU cycles	228
Avg CPU cycles	223

Test case: Conversion test **OK**

Conversion test for General block Gain.

Test results				
Time step	1	2	...	37
Mask parameters				
Gain	-10	-9.444	...	10
Controller parameters				
V	-10	-9.444	...	10
Exp. V	-10	-9.444	...	10

Test settings	
Tolerance V	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block Gain.

Test results				
Time step	1	2	...	37
Mask parameters				
Gain	-10	-9.444	...	10
Controller parameters				
V	-10	-9.444	...	10
Exp. V	-10	-9.444	...	10

Test settings	
Tolerance V	±1,0000e-06

Test statistics	
Min CPU cycles	667
Max CPU cycles	696
Avg CPU cycles	694

Verification: Gain Float32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for General block Gain.

Test results				
Time step	1	2	...	9
CPU cycles	89	89	...	89
Inputs				
In (DSP)	-1	-0.5	...	1
In	-1	-0.5	...	1
Parameters				
Gain	2.2			
Outputs				
Out	-2.2	-1.1	...	2.2
Exp. Out	-2.2	-1.1	...	2.2
Out (DSP)	-2.2	-1.1	...	2.2
Exp. Out (DSP)	-2.2	-1.1	...	2.2

Test settings	
Tolerance Out	±5,5879e-08 (±120 LSB)

Test statistics	
Min CPU cycles	71
Max CPU cycles	90
Avg CPU cycles	87

Test case: Parameter test OK

Parameter test for General block Gain.

Test results				
Time step	1	2	...	21
CPU cycles	87	87	...	87
Inputs				
In (DSP)	0.1			
In	0.1			
Parameters				
Gain	-100	-50	...	100
Outputs				
Out	-10	-5	...	10
Exp. Out	-10	-5	...	10
Out (DSP)	-10	-5	...	10
Exp. Out (DSP)	-10	-5	...	10

Test settings	
Tolerance Out	±9,3132e-09 (±20 LSB)

Test statistics	
Min CPU cycles	70
Max CPU cycles	89
Avg CPU cycles	86

Test case: Conversion test **OK**

Conversion test for General block Gain.

Test results				
Time step	1	2	...	37
Mask parameters				
Gain	-10	-9.444	...	10
Controller parameters				
V	-10	-9.444	...	10
Exp. V	-10	-9.444	...	10

Test settings	
Tolerance V	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block Gain.

Test results				
Time step	1	2	...	37
Mask parameters				
Gain	-10	-9.444	...	10
Controller parameters				
V	-10	-9.444	...	10
Exp. V	-10	-9.444	...	10

Test settings	
Tolerance V	±1,0000e-06

Test statistics	
Min CPU cycles	277
Max CPU cycles	278
Avg CPU cycles	277

Verification: Gain Float32 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for General block Gain.

Test results				
Time step	1	2	...	9
CPU cycles	195	195	...	195
Inputs				
In (DSP)	-1	-0.5	...	1
In	-1	-0.5	...	1
Parameters				
Gain	2.2			
Outputs				
Out	-2.2	-1.1	...	2.2
Exp. Out	-2.2	-1.1	...	2.2
Out (DSP)	-2.2	-1.1	...	2.2
Exp. Out (DSP)	-2.2	-1.1	...	2.2

Test settings	
Tolerance Out	±5,5879e-08 (±120 LSB)

Test statistics	
Min CPU cycles	149
Max CPU cycles	197
Avg CPU cycles	190

Test case: Parameter test OK

Parameter test for General block Gain.

Test results				
Time step	1	2	...	21
CPU cycles	192	192	...	192
Inputs				
In (DSP)	0.1			
In	0.1			
Parameters				
Gain	-100	-50	...	100
Outputs				
Out	-10	-5	...	10
Exp. Out	-10	-5	...	10
Out (DSP)	-10	-5	...	10
Exp. Out (DSP)	-10	-5	...	10

Test settings	
Tolerance Out	±9,3132e-09 (±20 LSB)

Test statistics	
Min CPU cycles	149
Max CPU cycles	196
Avg CPU cycles	191

Test case: Conversion test **OK**

Conversion test for General block Gain.

Test results				
Time step	1	2	...	37
Mask parameters				
Gain	-10	-9.444	...	10
Controller parameters				
V	-10	-9.444	...	10
Exp. V	-10	-9.444	...	10

Test settings	
Tolerance V	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block Gain.

Test results				
Time step	1	2	...	37
Mask parameters				
Gain	-10	-9.444	...	10
Controller parameters				
V	-10	-9.444	...	10
Exp. V	-10	-9.444	...	10

Test settings	
Tolerance V	±1,0000e-06

Test statistics	
Min CPU cycles	523
Max CPU cycles	868
Avg CPU cycles	856

Verification: Gain Float32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for General block Gain.

Test results				
Time step	1	2	...	9
CPU cycles	68	56	...	56
Inputs				
In (DSP)	-1	-0.5	...	1
In	-1	-0.5	...	1
Parameters				
Gain	2.2			
Outputs				
Out	-2.2	-1.1	...	2.2
Exp. Out	-2.2	-1.1	...	2.2
Out (DSP)	-2.2	-1.1	...	2.2
Exp. Out (DSP)	-2.2	-1.1	...	2.2

Test settings	
Tolerance Out	±5,5879e-08 (±120 LSB)

Test statistics	
Min CPU cycles	56
Max CPU cycles	68
Avg CPU cycles	57

Test case: Parameter test OK

Parameter test for General block Gain.

Test results				
Time step	1	2	...	21
CPU cycles	56	56	...	56
Inputs				
In (DSP)	0.1			
In	0.1			
Parameters				
Gain	-100	-50	...	100
Outputs				
Out	-10	-5	...	10
Exp. Out	-10	-5	...	10
Out (DSP)	-10	-5	...	10
Exp. Out (DSP)	-10	-5	...	10

Test settings	
Tolerance Out	±9,3132e-09 (±20 LSB)

Test statistics	
Min CPU cycles	56
Max CPU cycles	56
Avg CPU cycles	56

Test case: Conversion test **OK**

Conversion test for General block Gain.

Test results				
Time step	1	2	...	37
Mask parameters				
Gain	-10	-9.444	...	10
Controller parameters				
V	-10	-9.444	...	10
Exp. V	-10	-9.444	...	10

Test settings	
Tolerance V	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block Gain.

Test results				
Time step	1	2	...	37
Mask parameters				
Gain	-10	-9.444	...	10
Controller parameters				
V	-10	-9.444	...	10
Exp. V	-10	-9.444	...	10

Test settings	
Tolerance V	±1,0000e-06

Test statistics	
Min CPU cycles	385
Max CPU cycles	437
Avg CPU cycles	386

Verification: Gain Float32 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for General block Gain.

Test results				
Time step	1	2	...	9
CPU cycles	44	44	...	44
Inputs				
In (DSP)	-1	-0.5	...	1
In	-1	-0.5	...	1
Parameters				
Gain	2.2			
Outputs				
Out	-2.2	-1.1	...	2.2
Exp. Out	-2.2	-1.1	...	2.2
Out (DSP)	-2.2	-1.1	...	2.2
Exp. Out (DSP)	-2.2	-1.1	...	2.2

Test settings	
Tolerance Out	±5,5879e-08 (±120 LSB)

Test statistics	
Min CPU cycles	44
Max CPU cycles	44
Avg CPU cycles	44

Test case: Parameter test OK

Parameter test for General block Gain.

Test results				
Time step	1	2	...	21
CPU cycles	44	44	...	44
Inputs				
In (DSP)	0.1			
In	0.1			
Parameters				
Gain	-100	-50	...	100
Outputs				
Out	-10	-5	...	10
Exp. Out	-10	-5	...	10
Out (DSP)	-10	-5	...	10
Exp. Out (DSP)	-10	-5	...	10

Test settings	
Tolerance Out	±9,3132e-09 (±20 LSB)

Test statistics	
Min CPU cycles	44
Max CPU cycles	44
Avg CPU cycles	44

Test case: Conversion test **OK**

Conversion test for General block Gain.

Test results				
Time step	1	2	...	37
Mask parameters				
Gain	-10	-9.444	...	10
Controller parameters				
V	-10	-9.444	...	10
Exp. V	-10	-9.444	...	10

Test settings	
Tolerance V	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block Gain.

Test results				
Time step	1	2	...	37
Mask parameters				
Gain	-10	-9.444	...	10
Controller parameters				
V	-10	-9.444	...	10
Exp. V	-10	-9.444	...	10

Test settings	
Tolerance V	±1,0000e-06

Test statistics	
Min CPU cycles	637
Max CPU cycles	640
Avg CPU cycles	637

Block: Inport

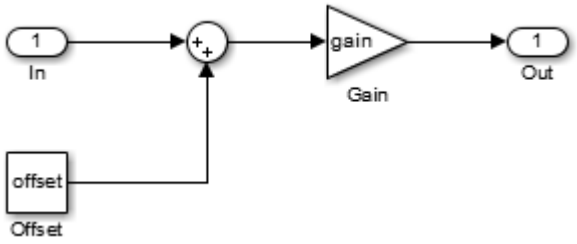


Inports	
IN	Signal from frame program

Mask Parameters	
ts_fact	Multiplication factor of base sampling time (in integer format)
Gain	Gain value used in simulation
Offset	Offset value used in simulation

Description:

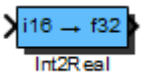
Serves as interface to the frame program. The input of this block is intended for simulation purposes and can be left unconnected if not used. Also the parameters *Gain* and *Offset* are only used during simulation. The schematic for simulation can be seen in the figure below.
Note: Currently, *Gain* and *Offset* parameters are only available in Matlab/Simulink.



Data Types:

bool	Boolean
int8	8 Bit Fixed Point
int16	16 Bit Fixed Point
int32	32 Bit Fixed Point
float32	32 Bit Floating Point
float64	64 Bit Floating Point

Block: Int2Real



Conversion block from integer (fixed point) datatypes to real (floating point) datatypes.
Out = In * Scale

Inports	
In	Integer input

Outports	
Out	Real output

Mask Parameters		
Name	**ID**	**Description**
Scale	1	Scaling factor from integer to real

Implementations:

FiP8_Float32	8 Bit Fixed Point to 32 Bit Floating Point Implementation
FiP16_Float32	16 Bit Fixed Point to 32 Bit Floating Point Implementation
FiP32_Float32	32 Bit Fixed Point to 32 Bit Floating Point Implementation
FiP8_Float64	8 Bit Fixed Point to 64 Bit Floating Point Implementation
FiP16_Float64	16 Bit Fixed Point to 64 Bit Floating Point Implementation
FiP32_Float64	32 Bit Fixed Point to 64 Bit Floating Point Implementation
Bool_Float32	Boolean to 32 Bit Floating Point Implementation
Bool_Float64	Boolean to 64 Bit Floating Point Implementation

Implementation: FiP8_Float32

8 Bit Fixed Point to 32 Bit Floating Point Implementation

Inports Data Type	
In	int8

Outports Data Type	
Out	float32

Implementation: FiP16_Float32

16 Bit Fixed Point to 32 Bit Floating Point Implementation

Inports Data Type	
In	int16

Outports Data Type	
Out	float32

Implementation: FiP32_Float32

32 Bit Fixed Point to 32 Bit Floating Point Implementation

Inports Data Type	
In	int32

Outports Data Type	
Out	float32

Implementation: FiP8_Float64

8 Bit Fixed Point to 64 Bit Floating Point Implementation

Inports Data Type	
In	int8

Outports Data Type	
Out	float64

Implementation: FiP16_Float64

16 Bit Fixed Point to 64 Bit Floating Point Implementation

Inports Data Type	
In	int16

Outports Data Type	
Out	float64

Implementation: FiP32_Float64

32 Bit Fixed Point to 64 Bit Floating Point Implementation

Inports Data Type	
In	int32

Outports Data Type	
Out	float64

Implementation: Bool_Float32

Boolean to 32 Bit Floating Point Implementation

Inports Data Type	
In	bool

Outports Data Type	
Out	float32

Implementation: Bool_Float64

Boolean to 64 Bit Floating Point Implementation

Inports Data Type	
In	bool

Outports Data Type	
Out	float64

Verification: Int2Real FiP16_Float32 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for General block Int2Real.

Test results				
Time step	1	2	...	113
CPU cycles	59	59	...	59
Inputs				
In (DSP)	-32768	-32183	...	32767
In	-1	-0.982	...	1
Parameters				
Scale	7.3			
Outputs				
Out	-7.3	-7.17	...	7.3
Exp. Out	-7.3	-7.17	...	7.3
Out (DSP)	-7.3	-7.17	...	7.3
Exp. Out (DSP)	-7.3	-7.17	...	7.3

Test settings	
Tolerance Out	±3,0518e-04 (±655360 LSB)

Test statistics	
Min CPU cycles	59
Max CPU cycles	59
Avg CPU cycles	59

Test case: Parameter test OK

Parameter test for General block Int2Real.

Test results				
Time step	1	2	...	15
CPU cycles	59	59	...	59
Inputs				
In (DSP)	3277			
In	0.1			
Parameters				
Scale	-10	-5	...	10
Outputs				
Out	-1	-0.5	...	1
Exp. Out	-1	-0.5	...	1
Out (DSP)	-1	-0.5	...	1
Exp. Out (DSP)	-1	-0.5	...	1

Test settings	
Tolerance Out	±6,1035e-05 (±131072 LSB)

Test statistics	
Min CPU cycles	59
Max CPU cycles	59
Avg CPU cycles	59

Test case: Conversion test **OK**

Conversion test for General block Int2Real.

Test results				
Time step	1	2	...	15
Mask parameters				
Scale	-10	-5	...	10
Controller parameters				
scale	-0	-0	...	0
Exp. scale	-0	-0	...	0

Test settings	
Tolerance scale	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block Int2Real.

Test results				
Time step	1	2	...	15
Mask parameters				
Scale	-10	-5	...	10
Controller parameters				
scale	-0	-0	...	0
Exp. scale	-0	-0	...	0

Test settings	
Tolerance scale	±3,0000e-09

Test statistics	
Min CPU cycles	948
Max CPU cycles	1082
Avg CPU cycles	1073

Verification: Int2Real FiP16_Float32 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test — OK

Inport test for General block Int2Real.

Test results				
Time step	1	2	...	113
CPU cycles	29	29	...	29
Inputs				
In (DSP)	-32768	-32183	...	32767
In	-1	-0.982	...	1
Parameters				
Scale	7.3			
Outputs				
Out	-7.3	-7.17	...	7.3
Exp. Out	-7.3	-7.17	...	7.3
Out (DSP)	-7.3	-7.17	...	7.3
Exp. Out (DSP)	-7.3	-7.17	...	7.3

Test settings	
Tolerance Out	±3,0518e-04 (±655360 LSB)

Test statistics	
Min CPU cycles	29
Max CPU cycles	29
Avg CPU cycles	29

Test case: Parameter test — OK

Parameter test for General block Int2Real.

Test results				
Time step	1	2	...	15
CPU cycles	29	29	...	29
Inputs				
In (DSP)	3277			
In	0.1			
Parameters				
Scale	-10	-5	...	10
Outputs				
Out	-1	-0.5	...	1
Exp. Out	-1	-0.5	...	1
Out (DSP)	-1	-0.5	...	1
Exp. Out (DSP)	-1	-0.5	...	1

Test settings	
Tolerance Out	±6,1035e-05 (±131072 LSB)

Test statistics	
Min CPU cycles	29
Max CPU cycles	29
Avg CPU cycles	29

Test case: Conversion test **OK**

Conversion test for General block Int2Real.

Test results				
Time step	1	2	...	15
Mask parameters				
Scale	-10	-5	...	10
Controller parameters				
scale	-0	-0	...	0
Exp. scale	-0	-0	...	0

Test settings	
Tolerance scale	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block Int2Real.

Test results				
Time step	1	2	...	15
Mask parameters				
Scale	-10	-5	...	10
Controller parameters				
scale	-0	-0	...	0
Exp. scale	-0	-0	...	0

Test settings	
Tolerance scale	±3,0000e-09

Test statistics	
Min CPU cycles	467
Max CPU cycles	515
Avg CPU cycles	511

Verification: Int2Real FiP16_Float32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for General block Int2Real.

Test results				
Time step	1	2	...	113
CPU cycles	67	67	...	67
Inputs				
In (DSP)	-32768	-32183	...	32767
In	-1	-0.982	...	1
Parameters				
Scale	7.3			
Outputs				
Out	-7.3	-7.17	...	7.3
Exp. Out	-7.3	-7.17	...	7.3
Out (DSP)	-7.3	-7.17	...	7.3
Exp. Out (DSP)	-7.3	-7.17	...	7.3

Test settings	
Tolerance Out	±3,0518e-04 (±655360 LSB)

Test statistics	
Min CPU cycles	67
Max CPU cycles	67
Avg CPU cycles	67

Test case: Parameter test OK

Parameter test for General block Int2Real.

Test results				
Time step	1	2	...	15
CPU cycles	67	67	...	67
Inputs				
In (DSP)	3277			
In	0.1			
Parameters				
Scale	-10	-5	...	10
Outputs				
Out	-1	-0.5	...	1
Exp. Out	-1	-0.5	...	1
Out (DSP)	-1	-0.5	...	1
Exp. Out (DSP)	-1	-0.5	...	1

Test settings	
Tolerance Out	±6,1035e-05 (±131072 LSB)

Test statistics	
Min CPU cycles	67
Max CPU cycles	67
Avg CPU cycles	67

Test case: Conversion test OK

Conversion test for General block Int2Real.

Test results				
Time step	1	2	...	15
Mask parameters				
Scale	-10	-5	...	10
Controller parameters				
scale	-0	-0	...	0
Exp. scale	-0	-0	...	0

Test settings	
Tolerance scale	±0,0000e+00

Test case: Conversion-on-Target test OK

Conversion-on-Target test for General block Int2Real.

Test results				
Time step	1	2	...	15
Mask parameters				
Scale	-10	-5	...	10
Controller parameters				
scale	-0	-0	...	0
Exp. scale	-0	-0	...	0

Test settings	
Tolerance scale	±3,0000e-09

Test statistics	
Min CPU cycles	538
Max CPU cycles	558
Avg CPU cycles	556

Verification: Int2Real FiP16_Float32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for General block Int2Real.

Test results				
Time step	1	2	...	113
CPU cycles	310	307	...	307
Inputs				
In (DSP)	-32768	-32183	...	32767
In	-1	-0.982	...	1
Parameters				
Scale	7.3			
Outputs				
Out	-7.3	-7.17	...	7.3
Exp. Out	-7.3	-7.17	...	7.3
Out (DSP)	-7.3	-7.17	...	7.3
Exp. Out (DSP)	-7.3	-7.17	...	7.3

Test settings	
Tolerance Out	±3,0518e-04 (±655360 LSB)

Test statistics	
Min CPU cycles	207
Max CPU cycles	311
Avg CPU cycles	306

Test case: Parameter test OK

Parameter test for General block Int2Real.

Test results				
Time step	1	2	...	15
CPU cycles	307	307	...	307
Inputs				
In (DSP)	3277			
In	0.1			
Parameters				
Scale	-10	-5	...	10
Outputs				
Out	-1	-0.5	...	1
Exp. Out	-1	-0.5	...	1
Out (DSP)	-1	-0.5	...	1
Exp. Out (DSP)	-1	-0.5	...	1

Test settings	
Tolerance Out	±6,1035e-05 (±131072 LSB)

Test statistics	
Min CPU cycles	256
Max CPU cycles	310
Avg CPU cycles	304

Test case: Conversion test OK

Conversion test for General block Int2Real.

Test results				
Time step	1	2	...	15
Mask parameters				
Scale	-10	-5	...	10
Controller parameters				
scale	-0	-0	...	0
Exp. scale	-0	-0	...	0

Test settings	
Tolerance scale	±0,0000e+00

Test case: Conversion-on-Target test OK

Conversion-on-Target test for General block Int2Real.

Test results				
Time step	1	2	...	15
Mask parameters				
Scale	-10	-5	...	10
Controller parameters				
scale	-0	-0	...	0
Exp. scale	-0	-0	...	0

Test settings	
Tolerance scale	±3,0000e-09

Test statistics	
Min CPU cycles	829
Max CPU cycles	1075
Avg CPU cycles	1052

Verification: Int2Real FiP16_Float32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for General block Int2Real.

Test results				
Time step	1	2	...	113
CPU cycles	115	114	...	113
Inputs				
In (DSP)	-32768	-32183	...	32767
In	-1	-0.982	...	1
Parameters				
Scale	7.3			
Outputs				
Out	-7.3	-7.17	...	7.3
Exp. Out	-7.3	-7.17	...	7.3
Out (DSP)	-7.3	-7.17	...	7.3
Exp. Out (DSP)	-7.3	-7.17	...	7.3

Test settings	
Tolerance Out	±3,0518e-04 (±655360 LSB)

Test statistics	
Min CPU cycles	80
Max CPU cycles	116
Avg CPU cycles	113

Test case: Parameter test OK

Parameter test for General block Int2Real.

Test results				
Time step	1	2	...	15
CPU cycles	112	112	...	112
Inputs				
In (DSP)	3277			
In	0.1			
Parameters				
Scale	-10	-5	...	10
Outputs				
Out	-1	-0.5	...	1
Exp. Out	-1	-0.5	...	1
Out (DSP)	-1	-0.5	...	1
Exp. Out (DSP)	-1	-0.5	...	1

Test settings	
Tolerance Out	±6,1035e-05 (±131072 LSB)

Test statistics	
Min CPU cycles	95
Max CPU cycles	114
Avg CPU cycles	111

Test case: Conversion test **OK**

Conversion test for General block Int2Real.

Test results				
Time step	1	2	...	15
Mask parameters				
Scale	-10	-5	...	10
Controller parameters				
scale	-0	-0	...	0
Exp. scale	-0	-0	...	0

Test settings	
Tolerance scale	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block Int2Real.

Test results				
Time step	1	2	...	15
Mask parameters				
Scale	-10	-5	...	10
Controller parameters				
scale	-0	-0	...	0
Exp. scale	-0	-0	...	0

Test settings	
Tolerance scale	±3,0000e-09

Test statistics	
Min CPU cycles	323
Max CPU cycles	375
Avg CPU cycles	370

Verification: Int2Real FiP16_Float32 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for General block Int2Real.

Test results				
Time step	1	2	...	113
CPU cycles	383	394	...	389
Inputs				
In (DSP)	-32768	-32183	...	32767
In	-1	-0.982	...	1
Parameters				
Scale	7.3			
Outputs				
Out	-7.3	-7.17	...	7.3
Exp. Out	-7.3	-7.17	...	7.3
Out (DSP)	-7.3	-7.17	...	7.3
Exp. Out (DSP)	-7.3	-7.17	...	7.3

Test settings	
Tolerance Out	±3,0518e-04 (±655360 LSB)

Test statistics	
Min CPU cycles	201
Max CPU cycles	440
Avg CPU cycles	396

Test case: Parameter test OK

Parameter test for General block Int2Real.

Test results				
Time step	1	2	...	15
CPU cycles	417	417	...	417
Inputs				
In (DSP)	3277			
In	0.1			
Parameters				
Scale	-10	-5	...	10
Outputs				
Out	-1	-0.5	...	1
Exp. Out	-1	-0.5	...	1
Out (DSP)	-1	-0.5	...	1
Exp. Out (DSP)	-1	-0.5	...	1

Test settings	
Tolerance Out	±6,1035e-05 (±131072 LSB)

Test statistics	
Min CPU cycles	372
Max CPU cycles	419
Avg CPU cycles	414

Test case: Conversion test **OK**

Conversion test for General block Int2Real.

Test results				
Time step	1	2	...	15
Mask parameters				
Scale	-10	-5	...	10
Controller parameters				
scale	-0	-0	...	0
Exp. scale	-0	-0	...	0

Test settings	
Tolerance scale	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block Int2Real.

Test results				
Time step	1	2	...	15
Mask parameters				
Scale	-10	-5	...	10
Controller parameters				
scale	-0	-0	...	0
Exp. scale	-0	-0	...	0

Test settings	
Tolerance scale	±3,0000e-09

Test statistics	
Min CPU cycles	675
Max CPU cycles	1285
Avg CPU cycles	1241

Verification: Int2Real FiP16_Float32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for General block Int2Real.

Test results				
Time step	1	2	...	113
CPU cycles	59	59	...	59
Inputs				
In (DSP)	-32768	-32183	...	32767
In	-1	-0.982	...	1
Parameters				
Scale	7.3			
Outputs				
Out	-7.3	-7.17	...	7.3
Exp. Out	-7.3	-7.17	...	7.3
Out (DSP)	-7.3	-7.17	...	7.3
Exp. Out (DSP)	-7.3	-7.17	...	7.3

Test settings	
Tolerance Out	±3,0518e-04 (±655360 LSB)

Test statistics	
Min CPU cycles	59
Max CPU cycles	59
Avg CPU cycles	59

Test case: Parameter test OK

Parameter test for General block Int2Real.

Test results				
Time step	1	2	...	15
CPU cycles	59	59	...	59
Inputs				
In (DSP)	3277			
In	0.1			
Parameters				
Scale	-10	-5	...	10
Outputs				
Out	-1	-0.5	...	1
Exp. Out	-1	-0.5	...	1
Out (DSP)	-1	-0.5	...	1
Exp. Out (DSP)	-1	-0.5	...	1

Test settings	
Tolerance Out	±6,1035e-05 (±131072 LSB)

Test statistics	
Min CPU cycles	59
Max CPU cycles	59
Avg CPU cycles	59

Test case: Conversion test **OK**

Conversion test for General block Int2Real.

Test results				
Time step	1	2	...	15
Mask parameters				
Scale	-10	-5	...	10
Controller parameters				
scale	-0	-0	...	0
Exp. scale	-0	-0	...	0

Test settings	
Tolerance scale	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block Int2Real.

Test results				
Time step	1	2	...	15
Mask parameters				
Scale	-10	-5	...	10
Controller parameters				
scale	-0	-0	...	0
Exp. scale	-0	-0	...	0

Test settings	
Tolerance scale	±3,0000e-09

Test statistics	
Min CPU cycles	450
Max CPU cycles	514
Avg CPU cycles	467

Verification: Int2Real FiP16_Float32 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for General block Int2Real.

Test results				
Time step	1	2	...	113
CPU cycles	40	40	...	40
Inputs				
In (DSP)	-32768	-32183	...	32767
In	-1	-0.982	...	1
Parameters				
Scale	7.3			
Outputs				
Out	-7.3	-7.17	...	7.3
Exp. Out	-7.3	-7.17	...	7.3
Out (DSP)	-7.3	-7.17	...	7.3
Exp. Out (DSP)	-7.3	-7.17	...	7.3

Test settings	
Tolerance Out	±3,0518e-04 (±655360 LSB)

Test statistics	
Min CPU cycles	40
Max CPU cycles	40
Avg CPU cycles	40

Test case: Parameter test OK

Parameter test for General block Int2Real.

Test results				
Time step	1	2	...	15
CPU cycles	40	40	...	40
Inputs				
In (DSP)	3277			
In	0.1			
Parameters				
Scale	-10	-5	...	10
Outputs				
Out	-1	-0.5	...	1
Exp. Out	-1	-0.5	...	1
Out (DSP)	-1	-0.5	...	1
Exp. Out (DSP)	-1	-0.5	...	1

Test settings	
Tolerance Out	±6,1035e-05 (±131072 LSB)

Test statistics	
Min CPU cycles	40
Max CPU cycles	40
Avg CPU cycles	40

Test case: Conversion test OK

Conversion test for General block Int2Real.

Test results				
Time step	1	2	...	15
Mask parameters				
Scale	-10	-5	...	10
Controller parameters				
scale	-0	-0	...	0
Exp. scale	-0	-0	...	0

Test settings	
Tolerance scale	±0,0000e+00

Test case: Conversion-on-Target test OK

Conversion-on-Target test for General block Int2Real.

Test results				
Time step	1	2	...	15
Mask parameters				
Scale	-10	-5	...	10
Controller parameters				
scale	-0	-0	...	0
Exp. scale	-0	-0	...	0

Test settings	
Tolerance scale	±3,0000e-09

Test statistics	
Min CPU cycles	719
Max CPU cycles	811
Avg CPU cycles	804

Verification: Int2Real FiP32_Float32 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for General block Int2Real.

Test results				
Time step	1	2	...	113
CPU cycles	59	59	...	59
Inputs				
In (DSP)	-2147483648	-2109135726	...	2147483647
In	-1	-0.982	...	1
Parameters				
Scale	7.3			
Outputs				
Out	-7.3	-7.17	...	7.3
Exp. Out	-7.3	-7.17	...	7.3
Out (DSP)	-7.3	-7.17	...	7.3
Exp. Out (DSP)	-7.3	-7.17	...	7.3

Test settings	
Tolerance Out	±6,5193e-07 (±1400 LSB)

Test statistics	
Min CPU cycles	59
Max CPU cycles	59
Avg CPU cycles	59

Test case: Parameter test OK

Parameter test for General block Int2Real.

Test results				
Time step	1	2	...	15
CPU cycles	59	59	...	59
Inputs				
In (DSP)	214748365			
In	0.1			
Parameters				
Scale	-10	-5	...	10
Outputs				
Out	-1	-0.5	...	1
Exp. Out	-1	-0.5	...	1
Out (DSP)	-1	-0.5	...	1
Exp. Out (DSP)	-1	-0.5	...	1

Test settings	
Tolerance Out	±6,9849e-08 (±150 LSB)

Test statistics	
Min CPU cycles	59
Max CPU cycles	59
Avg CPU cycles	59

Test case: Conversion test **OK**

Conversion test for General block Int2Real.

Test results				
Time step	1	2	...	15
Mask parameters				
Scale	-10	-5	...	10
Controller parameters				
scale	-0	-0	...	0
Exp. scale	-0	-0	...	0

Test settings	
Tolerance scale	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block Int2Real.

Test results				
Time step	1	2	...	15
Mask parameters				
Scale	-10	-5	...	10
Controller parameters				
scale	-0	-0	...	0
Exp. scale	-0	-0	...	0

Test settings	
Tolerance scale	±3,0000e-09

Test statistics	
Min CPU cycles	959
Max CPU cycles	1093
Avg CPU cycles	1084

Verification: Int2Real FiP32_Float32 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for General block Int2Real.

Test results				
Time step	1	2	...	113
CPU cycles	29	29	...	29
Inputs				
In (DSP)	-2147483648	-2109135726	...	2147483647
In	-1	-0.982	...	1
Parameters				
Scale	7.3			
Outputs				
Out	-7.3	-7.17	...	7.3
Exp. Out	-7.3	-7.17	...	7.3
Out (DSP)	-7.3	-7.17	...	7.3
Exp. Out (DSP)	-7.3	-7.17	...	7.3

Test settings	
Tolerance Out	±6,5193e-07 (±1400 LSB)

Test statistics	
Min CPU cycles	29
Max CPU cycles	29
Avg CPU cycles	29

Test case: Parameter test OK

Parameter test for General block Int2Real.

Test results				
Time step	1	2	...	15
CPU cycles	29	29	...	29
Inputs				
In (DSP)	214748365			
In	0.1			
Parameters				
Scale	-10	-5	...	10
Outputs				
Out	-1	-0.5	...	1
Exp. Out	-1	-0.5	...	1
Out (DSP)	-1	-0.5	...	1
Exp. Out (DSP)	-1	-0.5	...	1

Test settings	
Tolerance Out	±6,9849e-08 (±150 LSB)

Test statistics	
Min CPU cycles	29
Max CPU cycles	29
Avg CPU cycles	29

Test case: Conversion test **OK**

Conversion test for General block Int2Real.

Test results				
Time step	1	2	...	15
Mask parameters				
Scale	-10	-5	...	10
Controller parameters				
scale	-0	-0	...	0
Exp. scale	-0	-0	...	0

Test settings	
Tolerance scale	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block Int2Real.

Test results				
Time step	1	2	...	15
Mask parameters				
Scale	-10	-5	...	10
Controller parameters				
scale	-0	-0	...	0
Exp. scale	-0	-0	...	0

Test settings	
Tolerance scale	±3,0000e-09

Test statistics	
Min CPU cycles	467
Max CPU cycles	515
Avg CPU cycles	511

Verification: Int2Real FiP32_Float32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for General block Int2Real.

Test results				
Time step	1	2	...	113
CPU cycles	62	62	...	62
Inputs				
In (DSP)	-2147483648	-2109135726	...	2147483647
In	-1	-0.982	...	1
Parameters				
Scale	7.3			
Outputs				
Out	-7.3	-7.17	...	7.3
Exp. Out	-7.3	-7.17	...	7.3
Out (DSP)	-7.3	-7.17	...	7.3
Exp. Out (DSP)	-7.3	-7.17	...	7.3

Test settings	
Tolerance Out	±6,5193e-07 (±1400 LSB)

Test statistics	
Min CPU cycles	62
Max CPU cycles	62
Avg CPU cycles	62

Test case: Parameter test OK

Parameter test for General block Int2Real.

Test results				
Time step	1	2	...	15
CPU cycles	62	62	...	62
Inputs				
In (DSP)	214748365			
In	0.1			
Parameters				
Scale	-10	-5	...	10
Outputs				
Out	-1	-0.5	...	1
Exp. Out	-1	-0.5	...	1
Out (DSP)	-1	-0.5	...	1
Exp. Out (DSP)	-1	-0.5	...	1

Test settings	
Tolerance Out	±6,9849e-08 (±150 LSB)

Test statistics	
Min CPU cycles	62
Max CPU cycles	62
Avg CPU cycles	62

Test case: Conversion test **OK**

Conversion test for General block Int2Real.

Test results				
Time step	1	2	...	15
Mask parameters				
Scale	-10	-5	...	10
Controller parameters				
scale	-0	-0	...	0
Exp. scale	-0	-0	...	0

Test settings	
Tolerance scale	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block Int2Real.

Test results				
Time step	1	2	...	15
Mask parameters				
Scale	-10	-5	...	10
Controller parameters				
scale	-0	-0	...	0
Exp. scale	-0	-0	...	0

Test settings	
Tolerance scale	±3,0000e-09

Test statistics	
Min CPU cycles	545
Max CPU cycles	565
Avg CPU cycles	563

Verification: Int2Real FiP32_Float32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for General block Int2Real.

Test results				
Time step	1	2	...	113
CPU cycles	337	340	...	343
Inputs				
In (DSP)	-2147483648	-2109135726	...	2147483647
In	-1	-0.982	...	1
Parameters				
Scale	7.3			
Outputs				
Out	-7.3	-7.17	...	7.3
Exp. Out	-7.3	-7.17	...	7.3
Out (DSP)	-7.3	-7.17	...	7.3
Exp. Out (DSP)	-7.3	-7.17	...	7.3

Test settings	
Tolerance Out	±6,5193e-07 (±1400 LSB)

Test statistics	
Min CPU cycles	206
Max CPU cycles	399
Avg CPU cycles	338

Test case: Parameter test OK

Parameter test for General block Int2Real.

Test results				
Time step	1	2	...	15
CPU cycles	341	341	...	341
Inputs				
In (DSP)	214748365			
In	0.1			
Parameters				
Scale	-10	-5	...	10
Outputs				
Out	-1	-0.5	...	1
Exp. Out	-1	-0.5	...	1
Out (DSP)	-1	-0.5	...	1
Exp. Out (DSP)	-1	-0.5	...	1

Test settings	
Tolerance Out	±6,9849e-08 (±150 LSB)

Test statistics	
Min CPU cycles	290
Max CPU cycles	344
Avg CPU cycles	338

Test case: Conversion test **OK**

Conversion test for General block Int2Real.

Test results				
Time step	1	2	...	15
Mask parameters				
Scale	-10	-5	...	10
Controller parameters				
scale	-0	-0	...	0
Exp. scale	-0	-0	...	0

Test settings	
Tolerance scale	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block Int2Real.

Test results				
Time step	1	2	...	15
Mask parameters				
Scale	-10	-5	...	10
Controller parameters				
scale	-0	-0	...	0
Exp. scale	-0	-0	...	0

Test settings	
Tolerance scale	±3,0000e-09

Test statistics	
Min CPU cycles	829
Max CPU cycles	1125
Avg CPU cycles	1056

Verification: Int2Real FiP32_Float32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for General block Int2Real.

Test results				
Time step	1	2	...	113
CPU cycles	115	114	...	114
Inputs				
In (DSP)	-2147483648	-2109135726	...	2147483647
In	-1	-0.982	...	1
Parameters				
Scale	7.3			
Outputs				
Out	-7.3	-7.17	...	7.3
Exp. Out	-7.3	-7.17	...	7.3
Out (DSP)	-7.3	-7.17	...	7.3
Exp. Out (DSP)	-7.3	-7.17	...	7.3

Test settings	
Tolerance Out	±6,5193e-07 (±1400 LSB)

Test statistics	
Min CPU cycles	80
Max CPU cycles	116
Avg CPU cycles	113

Test case: Parameter test OK

Parameter test for General block Int2Real.

Test results				
Time step	1	2	...	15
CPU cycles	112	112	...	112
Inputs				
In (DSP)	214748365			
In	0.1			
Parameters				
Scale	-10	-5	...	10
Outputs				
Out	-1	-0.5	...	1
Exp. Out	-1	-0.5	...	1
Out (DSP)	-1	-0.5	...	1
Exp. Out (DSP)	-1	-0.5	...	1

Test settings	
Tolerance Out	±6,9849e-08 (±150 LSB)

Test statistics	
Min CPU cycles	95
Max CPU cycles	114
Avg CPU cycles	111

Test case: Conversion test **OK**

Conversion test for General block Int2Real.

Test results				
Time step	1	2	...	15
Mask parameters				
Scale	-10	-5	...	10
Controller parameters				
scale	-0	-0	...	0
Exp. scale	-0	-0	...	0

Test settings	
Tolerance scale	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block Int2Real.

Test results				
Time step	1	2	...	15
Mask parameters				
Scale	-10	-5	...	10
Controller parameters				
scale	-0	-0	...	0
Exp. scale	-0	-0	...	0

Test settings	
Tolerance scale	±3,0000e-09

Test statistics	
Min CPU cycles	323
Max CPU cycles	375
Avg CPU cycles	370

Verification: Int2Real FiP32_Float32 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test

OK

Inport test for General block Int2Real.

Test results				
Time step	1	2	...	113
CPU cycles	397	386	...	386
Inputs				
In (DSP)	-2147483648	-2109135726	...	2147483647
In	-1	-0.982	...	1
Parameters				
Scale	7.3			
Outputs				
Out	-7.3	-7.17	...	7.3
Exp. Out	-7.3	-7.17	...	7.3
Out (DSP)	-7.3	-7.17	...	7.3
Exp. Out (DSP)	-7.3	-7.17	...	7.3

Test settings	
Tolerance Out	±6,5193e-07 (±1400 LSB)

Test statistics	
Min CPU cycles	201
Max CPU cycles	397
Avg CPU cycles	371

Test case: Parameter test

OK

Parameter test for General block Int2Real.

Test results				
Time step	1	2	...	15
CPU cycles	345	345	...	345
Inputs				
In (DSP)	214748365			
In	0.1			
Parameters				
Scale	-10	-5	...	10
Outputs				
Out	-1	-0.5	...	1
Exp. Out	-1	-0.5	...	1
Out (DSP)	-1	-0.5	...	1
Exp. Out (DSP)	-1	-0.5	...	1

Test settings	
Tolerance Out	±6,9849e-08 (±150 LSB)

Test statistics	
Min CPU cycles	302
Max CPU cycles	349
Avg CPU cycles	344

Test case: Conversion test **OK**

Conversion test for General block Int2Real.

Test results				
Time step	1	2	...	15
Mask parameters				
Scale	-10	-5	...	10
Controller parameters				
scale	-0	-0	...	0
Exp. scale	-0	-0	...	0

Test settings	
Tolerance scale	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block Int2Real.

Test results				
Time step	1	2	...	15
Mask parameters				
Scale	-10	-5	...	10
Controller parameters				
scale	-0	-0	...	0
Exp. scale	-0	-0	...	0

Test settings	
Tolerance scale	±3,0000e-09

Test statistics	
Min CPU cycles	675
Max CPU cycles	1285
Avg CPU cycles	1241

Verification: Int2Real FiP32_Float32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for General block Int2Real.

Test results				
Time step	1	2	...	113
CPU cycles	58	58	...	58
Inputs				
In (DSP)	-2147483648	-2109135726	...	2147483647
In	-1	-0.982	...	1
Parameters				
Scale	7.3			
Outputs				
Out	-7.3	-7.17	...	7.3
Exp. Out	-7.3	-7.17	...	7.3
Out (DSP)	-7.3	-7.17	...	7.3
Exp. Out (DSP)	-7.3	-7.17	...	7.3

Test settings	
Tolerance Out	±6,5193e-07 (±1400 LSB)

Test statistics	
Min CPU cycles	58
Max CPU cycles	58
Avg CPU cycles	58

Test case: Parameter test OK

Parameter test for General block Int2Real.

Test results				
Time step	1	2	...	15
CPU cycles	58	58	...	58
Inputs				
In (DSP)	214748365			
In	0.1			
Parameters				
Scale	-10	-5	...	10
Outputs				
Out	-1	-0.5	...	1
Exp. Out	-1	-0.5	...	1
Out (DSP)	-1	-0.5	...	1
Exp. Out (DSP)	-1	-0.5	...	1

Test settings	
Tolerance Out	±6,9849e-08 (±150 LSB)

Test statistics	
Min CPU cycles	58
Max CPU cycles	58
Avg CPU cycles	58

Test case: Conversion test **OK**

Conversion test for General block Int2Real.

Test results				
Time step	1	2	...	15
Mask parameters				
Scale	-10	-5	...	10
Controller parameters				
scale	-0	-0	...	0
Exp. scale	-0	-0	...	0

Test settings	
Tolerance scale	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block Int2Real.

Test results				
Time step	1	2	...	15
Mask parameters				
Scale	-10	-5	...	10
Controller parameters				
scale	-0	-0	...	0
Exp. scale	-0	-0	...	0

Test settings	
Tolerance scale	±3,0000e-09

Test statistics	
Min CPU cycles	433
Max CPU cycles	496
Avg CPU cycles	438

Verification: Int2Real FiP32_Float32 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for General block Int2Real.

Test results				
Time step	1	2	...	113
CPU cycles	45	45	...	45
Inputs				
In (DSP)	-2147483648	-2109135726	...	2147483647
In	-1	-0.982	...	1
Parameters				
Scale	7.3			
Outputs				
Out	-7.3	-7.17	...	7.3
Exp. Out	-7.3	-7.17	...	7.3
Out (DSP)	-7.3	-7.17	...	7.3
Exp. Out (DSP)	-7.3	-7.17	...	7.3

Test settings	
Tolerance Out	±6,5193e-07 (±1400 LSB)

Test statistics	
Min CPU cycles	45
Max CPU cycles	45
Avg CPU cycles	45

Test case: Parameter test OK

Parameter test for General block Int2Real.

Test results				
Time step	1	2	...	15
CPU cycles	45	45	...	45
Inputs				
In (DSP)	214748365			
In	0.1			
Parameters				
Scale	-10	-5	...	10
Outputs				
Out	-1	-0.5	...	1
Exp. Out	-1	-0.5	...	1
Out (DSP)	-1	-0.5	...	1
Exp. Out (DSP)	-1	-0.5	...	1

Test settings	
Tolerance Out	±6,9849e-08 (±150 LSB)

Test statistics	
Min CPU cycles	45
Max CPU cycles	45
Avg CPU cycles	45

Test case: Conversion test **OK**

Conversion test for General block Int2Real.

Test results				
Time step	1	2	...	15
Mask parameters				
Scale	-10	-5	...	10
Controller parameters				
scale	-0	-0	...	0
Exp. scale	-0	-0	...	0

Test settings	
Tolerance scale	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block Int2Real.

Test results				
Time step	1	2	...	15
Mask parameters				
Scale	-10	-5	...	10
Controller parameters				
scale	-0	-0	...	0
Exp. scale	-0	-0	...	0

Test settings	
Tolerance scale	±3,0000e-09

Test statistics	
Min CPU cycles	726
Max CPU cycles	818
Avg CPU cycles	811

Verification: Int2Real Bool_Float32 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for General block Int2Real.

Test results				
Time step	1	2	...	5
CPU cycles	59	59	...	59
Inputs				
In (DSP)	0	0	...	1
In	-3.1	-0.31	...	3.3
Parameters				
Scale	10			
Outputs				
Out	0	0	...	10
Exp. Out	0	0	...	10
Out (DSP)	0	0	...	10
Exp. Out (DSP)	0	0	...	10

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	59
Max CPU cycles	59
Avg CPU cycles	59

Test case: Parameter test OK

Parameter test for General block Int2Real.

Test results				
Time step	1	2	...	15
CPU cycles	59	59	...	59
Inputs				
In (DSP)	1			
In	1.1			
Parameters				
Scale	-10	-5	...	10
Outputs				
Out	-10	-5	...	10
Exp. Out	-10	-5	...	10
Out (DSP)	-10	-5	...	10
Exp. Out (DSP)	-10	-5	...	10

Test settings	
Tolerance Out	±4,6566e-09 (±10 LSB)

Test statistics	
Min CPU cycles	59
Max CPU cycles	59
Avg CPU cycles	59

Test case: Conversion test **OK**

Conversion test for General block Int2Real.

Test results				
Time step	1	2	...	15
Mask parameters				
Scale	-10	-5	...	10
Controller parameters				
scale	-10	-5	...	10
Exp. scale	-10	-5	...	10

Test settings	
Tolerance scale	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block Int2Real.

Test results				
Time step	1	2	...	15
Mask parameters				
Scale	-10	-5	...	10
Controller parameters				
scale	-10	-5	...	10
Exp. scale	-10	-5	...	10

Test settings	
Tolerance scale	±3,0000e-09

Test statistics	
Min CPU cycles	827
Max CPU cycles	844
Avg CPU cycles	828

Verification: Int2Real Bool_Float32 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for General block Int2Real.

Test results				
Time step	1	2	...	5
CPU cycles	29	29	...	29
Inputs				
In (DSP)	0	0	...	1
In	-3.1	-0.31	...	3.3
Parameters				
Scale	10			
Outputs				
Out	0	0	...	10
Exp. Out	0	0	...	10
Out (DSP)	0	0	...	10
Exp. Out (DSP)	0	0	...	10

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	29
Max CPU cycles	29
Avg CPU cycles	29

Test case: Parameter test OK

Parameter test for General block Int2Real.

Test results				
Time step	1	2	...	15
CPU cycles	29	29	...	29
Inputs				
In (DSP)	1			
In	1.1			
Parameters				
Scale	-10	-5	...	10
Outputs				
Out	-10	-5	...	10
Exp. Out	-10	-5	...	10
Out (DSP)	-10	-5	...	10
Exp. Out (DSP)	-10	-5	...	10

Test settings	
Tolerance Out	±4,6566e-09 (±10 LSB)

Test statistics	
Min CPU cycles	29
Max CPU cycles	29
Avg CPU cycles	29

Test case: Conversion test **OK**

Conversion test for General block Int2Real.

Test results				
Time step	1	2	...	15
Mask parameters				
Scale	-10	-5	...	10
Controller parameters				
scale	-10	-5	...	10
Exp. scale	-10	-5	...	10

Test settings	
Tolerance scale	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block Int2Real.

Test results				
Time step	1	2	...	15
Mask parameters				
Scale	-10	-5	...	10
Controller parameters				
scale	-10	-5	...	10
Exp. scale	-10	-5	...	10

Test settings	
Tolerance scale	±3,0000e-09

Test statistics	
Min CPU cycles	397
Max CPU cycles	397
Avg CPU cycles	397

Verification: Int2Real Bool_Float32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for General block Int2Real.

Test results				
Time step	1	2	...	5
CPU cycles	62	62	...	62
Inputs				
In (DSP)	0	0	...	1
In	-3.1	-0.31	...	3.3
Parameters				
Scale	10			
Outputs				
Out	0	0	...	10
Exp. Out	0	0	...	10
Out (DSP)	0	0	...	10
Exp. Out (DSP)	0	0	...	10

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	62
Max CPU cycles	62
Avg CPU cycles	62

Test case: Parameter test OK

Parameter test for General block Int2Real.

Test results				
Time step	1	2	...	15
CPU cycles	62	62	...	62
Inputs				
In (DSP)	1			
In	1.1			
Parameters				
Scale	-10	-5	...	10
Outputs				
Out	-10	-5	...	10
Exp. Out	-10	-5	...	10
Out (DSP)	-10	-5	...	10
Exp. Out (DSP)	-10	-5	...	10

Test settings	
Tolerance Out	±4,6566e-09 (±10 LSB)

Test statistics	
Min CPU cycles	62
Max CPU cycles	62
Avg CPU cycles	62

Test case: Conversion test **OK**

Conversion test for General block Int2Real.

Test results				
Time step	1	2	...	15
Mask parameters				
Scale	-10	-5	...	10
Controller parameters				
scale	-10	-5	...	10
Exp. scale	-10	-5	...	10

Test settings	
Tolerance scale	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block Int2Real.

Test results				
Time step	1	2	...	15
Mask parameters				
Scale	-10	-5	...	10
Controller parameters				
scale	-10	-5	...	10
Exp. scale	-10	-5	...	10

Test settings	
Tolerance scale	±3,0000e-09

Test statistics	
Min CPU cycles	467
Max CPU cycles	519
Avg CPU cycles	470

Verification: Int2Real Bool_Float32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for General block Int2Real.

Test results				
Time step	1	2	...	5
CPU cycles	198	198	...	298
Inputs				
In (DSP)	0	0	...	1
In	-3.1	-0.31	...	3.3
Parameters				
Scale	10			
Outputs				
Out	0	0	...	10
Exp. Out	0	0	...	10
Out (DSP)	0	0	...	10
Exp. Out (DSP)	0	0	...	10

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	198
Max CPU cycles	298
Avg CPU cycles	218

Test case: Parameter test OK

Parameter test for General block Int2Real.

Test results				
Time step	1	2	...	15
CPU cycles	298	298	...	298
Inputs				
In (DSP)	1			
In	1.1			
Parameters				
Scale	-10	-5	...	10
Outputs				
Out	-10	-5	...	10
Exp. Out	-10	-5	...	10
Out (DSP)	-10	-5	...	10
Exp. Out (DSP)	-10	-5	...	10

Test settings	
Tolerance Out	±4,6566e-09 (±10 LSB)

Test statistics	
Min CPU cycles	244
Max CPU cycles	357
Avg CPU cycles	298

Test case: Conversion test **OK**

Conversion test for General block Int2Real.

Test results				
Time step	1	2	...	15
Mask parameters				
Scale	-10	-5	...	10
Controller parameters				
scale	-10	-5	...	10
Exp. scale	-10	-5	...	10

Test settings	
Tolerance scale	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block Int2Real.

Test results				
Time step	1	2	...	15
Mask parameters				
Scale	-10	-5	...	10
Controller parameters				
scale	-10	-5	...	10
Exp. scale	-10	-5	...	10

Test settings	
Tolerance scale	±3,0000e-09

Test statistics	
Min CPU cycles	667
Max CPU cycles	747
Avg CPU cycles	692

Verification: Int2Real Bool_Float32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for General block Int2Real.

Test results				
Time step	1	2	...	5
CPU cycles	92	92	...	126
Inputs				
In (DSP)	0	0	...	1
In	-3.1	-0.31	...	3.3
Parameters				
Scale	10			
Outputs				
Out	0	0	...	10
Exp. Out	0	0	...	10
Out (DSP)	0	0	...	10
Exp. Out (DSP)	0	0	...	10

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	92
Max CPU cycles	126
Avg CPU cycles	98

Test case: Parameter test OK

Parameter test for General block Int2Real.

Test results				
Time step	1	2	...	15
CPU cycles	126	126	...	126
Inputs				
In (DSP)	1			
In	1.1			
Parameters				
Scale	-10	-5	...	10
Outputs				
Out	-10	-5	...	10
Exp. Out	-10	-5	...	10
Out (DSP)	-10	-5	...	10
Exp. Out (DSP)	-10	-5	...	10

Test settings	
Tolerance Out	±4,6566e-09 (±10 LSB)

Test statistics	
Min CPU cycles	107
Max CPU cycles	126
Avg CPU cycles	124

Test case: Conversion test **OK**

Conversion test for General block Int2Real.

Test results				
Time step	1	2	...	15
Mask parameters				
Scale	-10	-5	...	10
Controller parameters				
scale	-10	-5	...	10
Exp. scale	-10	-5	...	10

Test settings	
Tolerance scale	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block Int2Real.

Test results				
Time step	1	2	...	15
Mask parameters				
Scale	-10	-5	...	10
Controller parameters				
scale	-10	-5	...	10
Exp. scale	-10	-5	...	10

Test settings	
Tolerance scale	±3,0000e-09

Test statistics	
Min CPU cycles	277
Max CPU cycles	278
Avg CPU cycles	277

Verification: Int2Real Bool_Float32 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for General block Int2Real.

Test results				
Time step	1	2	...	5
CPU cycles	180	180	...	507
Inputs				
In (DSP)	0	0	...	1
In	-3.1	-0.31	...	3.3
Parameters				
Scale	10			
Outputs				
Out	0	0	...	10
Exp. Out	0	0	...	10
Out (DSP)	0	0	...	10
Exp. Out (DSP)	0	0	...	10

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	180
Max CPU cycles	507
Avg CPU cycles	245

Test case: Parameter test OK

Parameter test for General block Int2Real.

Test results				
Time step	1	2	...	15
CPU cycles	507	507	...	507
Inputs				
In (DSP)	1			
In	1.1			
Parameters				
Scale	-10	-5	...	10
Outputs				
Out	-10	-5	...	10
Exp. Out	-10	-5	...	10
Out (DSP)	-10	-5	...	10
Exp. Out (DSP)	-10	-5	...	10

Test settings	
Tolerance Out	±4,6566e-09 (±10 LSB)

Test statistics	
Min CPU cycles	461
Max CPU cycles	507
Avg CPU cycles	503

Test case: Conversion test **OK**

Conversion test for General block Int2Real.

Test results				
Time step	1	2	...	15
Mask parameters				
Scale	-10	-5	...	10
Controller parameters				
scale	-10	-5	...	10
Exp. scale	-10	-5	...	10

Test settings	
Tolerance scale	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block Int2Real.

Test results				
Time step	1	2	...	15
Mask parameters				
Scale	-10	-5	...	10
Controller parameters				
scale	-10	-5	...	10
Exp. scale	-10	-5	...	10

Test settings	
Tolerance scale	±3,0000e-09

Test statistics	
Min CPU cycles	523
Max CPU cycles	868
Avg CPU cycles	842

Verification: Int2Real Bool_Float32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for General block Int2Real.

Test results				
Time step	1	2	...	5
CPU cycles	76	59	...	59
Inputs				
In (DSP)	0	0	...	1
In	-3.1	-0.31	...	3.3
Parameters				
Scale	10			
Outputs				
Out	0	0	...	10
Exp. Out	0	0	...	10
Out (DSP)	0	0	...	10
Exp. Out (DSP)	0	0	...	10

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	59
Max CPU cycles	76
Avg CPU cycles	62

Test case: Parameter test OK

Parameter test for General block Int2Real.

Test results				
Time step	1	2	...	15
CPU cycles	76	76	...	76
Inputs				
In (DSP)	1			
In	1.1			
Parameters				
Scale	-10	-5	...	10
Outputs				
Out	-10	-5	...	10
Exp. Out	-10	-5	...	10
Out (DSP)	-10	-5	...	10
Exp. Out (DSP)	-10	-5	...	10

Test settings	
Tolerance Out	±4,6566e-09 (±10 LSB)

Test statistics	
Min CPU cycles	76
Max CPU cycles	76
Avg CPU cycles	76

Test case: Conversion test **OK**

Conversion test for General block Int2Real.

Test results				
Time step	1	2	...	15
Mask parameters				
Scale	-10	-5	...	10
Controller parameters				
scale	-10	-5	...	10
Exp. scale	-10	-5	...	10

Test settings	
Tolerance scale	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block Int2Real.

Test results				
Time step	1	2	...	15
Mask parameters				
Scale	-10	-5	...	10
Controller parameters				
scale	-10	-5	...	10
Exp. scale	-10	-5	...	10

Test settings	
Tolerance scale	±3,0000e-09

Test statistics	
Min CPU cycles	417
Max CPU cycles	442
Avg CPU cycles	419

Verification: Int2Real Bool_Float32 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for General block Int2Real.

Test results				
Time step	1	2	...	5
CPU cycles	40	40	...	40
Inputs				
In (DSP)	0	0	...	1
In	-3.1	-0.31	...	3.3
Parameters				
Scale	10			
Outputs				
Out	0	0	...	10
Exp. Out	0	0	...	10
Out (DSP)	0	0	...	10
Exp. Out (DSP)	0	0	...	10

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	40
Max CPU cycles	40
Avg CPU cycles	40

Test case: Parameter test OK

Parameter test for General block Int2Real.

Test results				
Time step	1	2	...	15
CPU cycles	40	40	...	40
Inputs				
In (DSP)	1			
In	1.1			
Parameters				
Scale	-10	-5	...	10
Outputs				
Out	-10	-5	...	10
Exp. Out	-10	-5	...	10
Out (DSP)	-10	-5	...	10
Exp. Out (DSP)	-10	-5	...	10

Test settings	
Tolerance Out	±4,6566e-09 (±10 LSB)

Test statistics	
Min CPU cycles	40
Max CPU cycles	40
Avg CPU cycles	40

Test case: Conversion test **OK**

Conversion test for General block Int2Real.

Test results				
Time step	1	2	...	15
Mask parameters				
Scale	-10	-5	...	10
Controller parameters				
scale	-10	-5	...	10
Exp. scale	-10	-5	...	10

Test settings	
Tolerance scale	±0,0000e+00

Test case: Conversion-on-Target test **OK**

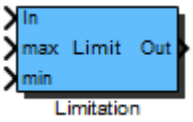
Conversion-on-Target test for General block Int2Real.

Test results				
Time step	1	2	...	15
Mask parameters				
Scale	-10	-5	...	10
Controller parameters				
scale	-10	-5	...	10
Exp. scale	-10	-5	...	10

Test settings	
Tolerance scale	±3,0000e-09

Test statistics	
Min CPU cycles	637
Max CPU cycles	640
Avg CPU cycles	637

Block: Limitation



Limits the input signal to min and max_sci.
Caution: For correct computation the upper limit max has to be greater than the lower limit min!

Inports	
In	Input signal
max	Upper limit
min	Lower limit

Outports	
Out	Limited input signal

Description:

Calculation:

$$\mathrm{Out} = \begin{cases} \max & \mathrm{In} > \max \\ \mathrm{In} & \\ \min & \mathrm{In} < \min \end{cases}$$

Implementations:

FiP16 16 Bit Fixed Point Implementation
FiP32 32 Bit Fixed Point Implementation
Float32 32 Bit Floating Point Implementation
Float64 64 Bit Floating Point Implementation

Implementation: FiP16

16 Bit Fixed Point Implementation

Inports Data Type	
In	int16
max	int16
min	int16

Outports Data Type	
Out	int16

Implementation: FiP32

32 Bit Fixed Point Implementation

Inports Data Type	
In	int32
max	int32
min	int32

Outports Data Type	
Out	int32

Implementation: Float32

32 Bit Floating Point Implementation

Inports Data Type	
In	float32
max	float32
min	float32

Outports Data Type	
Out	float32

Implementation: Float64

64 Bit Floating Point Implementation

Inports Data Type	
In	float64
max	float64
min	float64

Outports Data Type	
Out	float64

Verification: Limitation FiP16 CPU TMS320F28335

Date of Test 2026-06-19

Target controller TMS320F28335

Test case: Inport test OK

Inport test for General block Limitation.

Test results						
Time step	1	2	3	4	...	159
CPU cycles	72	72	72	72	...	72
Inputs						
In (DSP)	-32768	-31508	-30247	-28987	...	19661
max (DSP)	9830	9830	9830	9830	...	32767
min (DSP)	-13107	-13107	-13107	-13107	...	-32768
In	-1	-0.962	-0.923	-0.885	...	0.6
max	0.3	0.3	0.3	0.3	...	1
min	-0.4	-0.4	-0.4	-0.4	...	-1
Outputs						
Out	-0.4	-0.4	-0.4	-0.4	...	0.6
Exp. Out	-0.4	-0.4	-0.4	-0.4	...	0.6
Out (DSP)	-13107	-13107	-13107	-13107	...	19661
Exp. Out (DSP)	-13107	-13107	-13107	-13107	...	19661

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	67
Max CPU cycles	72
Avg CPU cycles	69

Verification: Limitation FiP16 CPU TM4C123GH6

Date of Test 2026-06-19

Target controller TM4C123GH6

Test case: Inport test OK

Inport test for General block Limitation.

Test results						
Time step	1	2	3	4	...	159
CPU cycles	35	35	35	35	...	35
Inputs						
In (DSP)	-32768	-31508	-30247	-28987	...	19661
max (DSP)	9830	9830	9830	9830	...	32767
min (DSP)	-13107	-13107	-13107	-13107	...	-32768
In	-1	-0.962	-0.923	-0.885	...	0.6
max	0.3	0.3	0.3	0.3	...	1
min	-0.4	-0.4	-0.4	-0.4	...	-1
Outputs						
Out	-0.4	-0.4	-0.4	-0.4	...	0.6
Exp. Out	-0.4	-0.4	-0.4	-0.4	...	0.6
Out (DSP)	-13107	-13107	-13107	-13107	...	19661
Exp. Out (DSP)	-13107	-13107	-13107	-13107	...	19661

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	31
Max CPU cycles	35
Avg CPU cycles	32

Verification: Limitation FiP16 CPU STM32G474RE

Date of Test 2026-06-19

Target controller STM32G474RE

Test case: Inport test OK

Inport test for General block Limitation.

Test results						
Time step	1	2	3	4	...	159
CPU cycles	68	68	68	68	...	68
Inputs						
In (DSP)	-32768	-31508	-30247	-28987	...	19661
max (DSP)	9830	9830	9830	9830	...	32767
min (DSP)	-13107	-13107	-13107	-13107	...	-32768
In	-1	-0.962	-0.923	-0.885	...	0.6
max	0.3	0.3	0.3	0.3	...	1
min	-0.4	-0.4	-0.4	-0.4	...	-1
Outputs						
Out	-0.4	-0.4	-0.4	-0.4	...	0.6
Exp. Out	-0.4	-0.4	-0.4	-0.4	...	0.6
Out (DSP)	-13107	-13107	-13107	-13107	...	19661
Exp. Out (DSP)	-13107	-13107	-13107	-13107	...	19661

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	68
Max CPU cycles	72
Avg CPU cycles	70

Verification: Limitation FiP16 CPU STM32F072RB

Date of Test 2026-06-19

Target controller STM32F072RB

Test case: Inport test OK

Inport test for General block Limitation.

Test results						
Time step	1	2	3	4	...	159
CPU cycles	63	63	63	63	...	63
Inputs						
In (DSP)	-32768	-31508	-30247	-28987	...	19661
max (DSP)	9830	9830	9830	9830	...	32767
min (DSP)	-13107	-13107	-13107	-13107	...	-32768
In	-1	-0.962	-0.923	-0.885	...	0.6
max	0.3	0.3	0.3	0.3	...	1
min	-0.4	-0.4	-0.4	-0.4	...	-1
Outputs						
Out	-0.4	-0.4	-0.4	-0.4	...	0.6
Exp. Out	-0.4	-0.4	-0.4	-0.4	...	0.6
Out (DSP)	-13107	-13107	-13107	-13107	...	19661
Exp. Out (DSP)	-13107	-13107	-13107	-13107	...	19661

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	59
Max CPU cycles	122
Avg CPU cycles	60

Verification: Limitation FiP16 CPU PIC32MX170F256

Date of Test 2026-06-19

Target controller PIC32MX170F256

Test case: Inport test OK

Inport test for General block Limitation.

Test results						
Time step	1	2	3	4	...	159
CPU cycles	46	46	46	46	...	45
Inputs						
In (DSP)	-32768	-31508	-30247	-28987	...	19661
max (DSP)	9830	9830	9830	9830	...	32767
min (DSP)	-13107	-13107	-13107	-13107	...	-32768
In	-1	-0.962	-0.923	-0.885	...	0.6
max	0.3	0.3	0.3	0.3	...	1
min	-0.4	-0.4	-0.4	-0.4	...	-1
Outputs						
Out	-0.4	-0.4	-0.4	-0.4	...	0.6
Exp. Out	-0.4	-0.4	-0.4	-0.4	...	0.6
Out (DSP)	-13107	-13107	-13107	-13107	...	19661
Exp. Out (DSP)	-13107	-13107	-13107	-13107	...	19661

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	37
Max CPU cycles	46
Avg CPU cycles	40

Verification: Limitation FiP16 CPU dsPIC33EP256MC502

Date of Test 2026-06-19

Target controller dsPIC33EP256MC502

Test case: Inport test OK

Inport test for General block Limitation.

Test results						
Time step	1	2	3	4	...	159
CPU cycles	52	52	52	52	...	54
Inputs						
In (DSP)	-32768	-31508	-30247	-28987	...	19661
max (DSP)	9830	9830	9830	9830	...	32767
min (DSP)	-13107	-13107	-13107	-13107	...	-32768
In	-1	-0.962	-0.923	-0.885	...	0.6
max	0.3	0.3	0.3	0.3	...	1
min	-0.4	-0.4	-0.4	-0.4	...	-1
Outputs						
Out	-0.4	-0.4	-0.4	-0.4	...	0.6
Exp. Out	-0.4	-0.4	-0.4	-0.4	...	0.6
Out (DSP)	-13107	-13107	-13107	-13107	...	19661
Exp. Out (DSP)	-13107	-13107	-13107	-13107	...	19661

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	50
Max CPU cycles	54
Avg CPU cycles	51

Verification: Limitation FiP16 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for General block Limitation.

Test results						
Time step	1	2	3	4	...	159
CPU cycles	80	69	69	69	...	69
Inputs						
In (DSP)	-32768	-31508	-30247	-28987	...	19661
max (DSP)	9830	9830	9830	9830	...	32767
min (DSP)	-13107	-13107	-13107	-13107	...	-32768
In	-1	-0.962	-0.923	-0.885	...	0.6
max	0.3	0.3	0.3	0.3	...	1
min	-0.4	-0.4	-0.4	-0.4	...	-1
Outputs						
Out	-0.4	-0.4	-0.4	-0.4	...	0.6
Exp. Out	-0.4	-0.4	-0.4	-0.4	...	0.6
Out (DSP)	-13107	-13107	-13107	-13107	...	19661
Exp. Out (DSP)	-13107	-13107	-13107	-13107	...	19661

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	61
Max CPU cycles	80
Avg CPU cycles	64

Verification: Limitation FiP16 CPU TMS320F28379D

Date of Test 2026-06-22

Target controller TMS320F28379D

Test case: Inport test OK

Inport test for General block Limitation.

Test results						
Time step	1	2	3	4	...	159
CPU cycles	52	52	52	52	...	52
Inputs						
In (DSP)	-32768	-31508	-30247	-28987	...	19661
max (DSP)	9830	9830	9830	9830	...	32767
min (DSP)	-13107	-13107	-13107	-13107	...	-32768
In	-1	-0.962	-0.923	-0.885	...	0.6
max	0.3	0.3	0.3	0.3	...	1
min	-0.4	-0.4	-0.4	-0.4	...	-1
Outputs						
Out	-0.4	-0.4	-0.4	-0.4	...	0.6
Exp. Out	-0.4	-0.4	-0.4	-0.4	...	0.6
Out (DSP)	-13107	-13107	-13107	-13107	...	19661
Exp. Out (DSP)	-13107	-13107	-13107	-13107	...	19661

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	52
Max CPU cycles	56
Avg CPU cycles	54

Verification: Limitation FiP32 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for General block Limitation.

Test results				
Time step	1	2	...	159
CPU cycles	76	76	...	76
Inputs				
In (DSP)	-2147483648	-2064888123	...	1288490189
max (DSP)	644245094	644245094	...	2147483647
min (DSP)	-858993459	-858993459	...	-2147483648
In	-1	-0.962	...	0.6
max	0.3	0.3	...	1
min	-0.4	-0.4	...	-1
Outputs				
Out	-0.4	-0.4	...	0.6
Exp. Out	-0.4	-0.4	...	0.6
Out (DSP)	-858993459	-858993459	...	1288490189
Exp. Out (DSP)	-858993459	-858993459	...	1288490189

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	70
Max CPU cycles	76
Avg CPU cycles	72

Verification: Limitation FiP32 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for General block Limitation.

Test results				
Time step	1	2	...	159
CPU cycles	35	35	...	37
Inputs				
In (DSP)	-2147483648	-2064888123	...	1288490189
max (DSP)	644245094	644245094	...	2147483647
min (DSP)	-858993459	-858993459	...	-2147483648
In	-1	-0.962	...	0.6
max	0.3	0.3	...	1
min	-0.4	-0.4	...	-1
Outputs				
Out	-0.4	-0.4	...	0.6
Exp. Out	-0.4	-0.4	...	0.6
Out (DSP)	-858993459	-858993459	...	1288490189
Exp. Out (DSP)	-858993459	-858993459	...	1288490189

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	31
Max CPU cycles	37
Avg CPU cycles	33

Verification: Limitation FiP32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for General block Limitation.

Test results				
Time step	1	2	...	159
CPU cycles	67	67	...	67
Inputs				
In (DSP)	-2147483648	-2064888123	...	1288490189
max (DSP)	644245094	644245094	...	2147483647
min (DSP)	-858993459	-858993459	...	-2147483648
In	-1	-0.962	...	0.6
max	0.3	0.3	...	1
min	-0.4	-0.4	...	-1
Outputs				
Out	-0.4	-0.4	...	0.6
Exp. Out	-0.4	-0.4	...	0.6
Out (DSP)	-858993459	-858993459	...	1288490189
Exp. Out (DSP)	-858993459	-858993459	...	1288490189

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	67
Max CPU cycles	118
Avg CPU cycles	67

Verification: Limitation FiP32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for General block Limitation.

Test results				
Time step	1	2	...	159
CPU cycles	60	60	...	60
Inputs				
In (DSP)	-2147483648	-2064888123	...	1288490189
max (DSP)	644245094	644245094	...	2147483647
min (DSP)	-858993459	-858993459	...	-2147483648
In	-1	-0.962	...	0.6
max	0.3	0.3	...	1
min	-0.4	-0.4	...	-1
Outputs				
Out	-0.4	-0.4	...	0.6
Exp. Out	-0.4	-0.4	...	0.6
Out (DSP)	-858993459	-858993459	...	1288490189
Exp. Out (DSP)	-858993459	-858993459	...	1288490189

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	57
Max CPU cycles	60
Avg CPU cycles	58

Verification: Limitation FiP32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for General block Limitation.

Test results				
Time step	1	2	...	159
CPU cycles	46	46	...	45
Inputs				
In (DSP)	-2147483648	-2064888123	...	1288490189
max (DSP)	644245094	644245094	...	2147483647
min (DSP)	-858993459	-858993459	...	-2147483648
In	-1	-0.962	...	0.6
max	0.3	0.3	...	1
min	-0.4	-0.4	...	-1
Outputs				
Out	-0.4	-0.4	...	0.6
Exp. Out	-0.4	-0.4	...	0.6
Out (DSP)	-858993459	-858993459	...	1288490189
Exp. Out (DSP)	-858993459	-858993459	...	1288490189

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	37
Max CPU cycles	46
Avg CPU cycles	40

Verification: Limitation FiP32 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for General block Limitation.

Test results				
Time step	1	2	...	159
CPU cycles	59	59	...	60
Inputs				
In (DSP)	-2147483648	-2064888123	...	1288490189
max (DSP)	644245094	644245094	...	2147483647
min (DSP)	-858993459	-858993459	...	-2147483648
In	-1	-0.962	...	0.6
max	0.3	0.3	...	1
min	-0.4	-0.4	...	-1
Outputs				
Out	-0.4	-0.4	...	0.6
Exp. Out	-0.4	-0.4	...	0.6
Out (DSP)	-858993459	-858993459	...	1288490189
Exp. Out (DSP)	-858993459	-858993459	...	1288490189

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	55
Max CPU cycles	60
Avg CPU cycles	56

Verification: Limitation FiP32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for General block Limitation.

Test results				
Time step	1	2	...	159
CPU cycles	66	66	...	66
Inputs				
In (DSP)	-2147483648	-2064888123	...	1288490189
max (DSP)	644245094	644245094	...	2147483647
min (DSP)	-858993459	-858993459	...	-2147483648
In	-1	-0.962	...	0.6
max	0.3	0.3	...	1
min	-0.4	-0.4	...	-1
Outputs				
Out	-0.4	-0.4	...	0.6
Exp. Out	-0.4	-0.4	...	0.6
Out (DSP)	-858993459	-858993459	...	1288490189
Exp. Out (DSP)	-858993459	-858993459	...	1288490189

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	59
Max CPU cycles	66
Avg CPU cycles	61

Verification: Limitation FiP32 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for General block Limitation.

Test results				
Time step	1	2	...	159
CPU cycles	59	59	...	63
Inputs				
In (DSP)	-2147483648	-2064888123	...	1288490189
max (DSP)	644245094	644245094	...	2147483647
min (DSP)	-858993459	-858993459	...	-2147483648
In	-1	-0.962	...	0.6
max	0.3	0.3	...	1
min	-0.4	-0.4	...	-1
Outputs				
Out	-0.4	-0.4	...	0.6
Exp. Out	-0.4	-0.4	...	0.6
Out (DSP)	-858993459	-858993459	...	1288490189
Exp. Out (DSP)	-858993459	-858993459	...	1288490189

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	58
Max CPU cycles	63
Avg CPU cycles	59

Verification: Limitation Float32 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for General block Limitation.

Test results				
Time step	1	2	...	159
CPU cycles	75	75	...	75
Inputs				
In (DSP)	-1	-0.962	...	0.6
max (DSP)	0.3	0.3	...	1
min (DSP)	-0.4	-0.4	...	-1
In	-1	-0.962	...	0.6
max	0.3	0.3	...	1
min	-0.4	-0.4	...	-1
Outputs				
Out	-0.4	-0.4	...	0.6
Exp. Out	-0.4	-0.4	...	0.6
Out (DSP)	-0.4	-0.4	...	0.6
Exp. Out (DSP)	-0.4	-0.4	...	0.6

Test settings	
Tolerance Out	±2,7940e-08 (±60 LSB)

Test statistics	
Min CPU cycles	70
Max CPU cycles	75
Avg CPU cycles	72

Verification: Limitation Float32 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for General block Limitation.

Test results				
Time step	1	2	...	159
CPU cycles	41	41	...	41
Inputs				
In (DSP)	-1	-0.962	...	0.6
max (DSP)	0.3	0.3	...	1
min (DSP)	-0.4	-0.4	...	-1
In	-1	-0.962	...	0.6
max	0.3	0.3	...	1
min	-0.4	-0.4	...	-1
Outputs				
Out	-0.4	-0.4	...	0.6
Exp. Out	-0.4	-0.4	...	0.6
Out (DSP)	-0.4	-0.4	...	0.6
Exp. Out (DSP)	-0.4	-0.4	...	0.6

Test settings	
Tolerance Out	±2,7940e-08 (±60 LSB)

Test statistics	
Min CPU cycles	35
Max CPU cycles	41
Avg CPU cycles	37

Verification: Limitation Float32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for General block Limitation.

Test results				
Time step	1	2	...	159
CPU cycles	77	77	...	77
Inputs				
In (DSP)	-1	-0.962	...	0.6
max (DSP)	0.3	0.3	...	1
min (DSP)	-0.4	-0.4	...	-1
In	-1	-0.962	...	0.6
max	0.3	0.3	...	1
min	-0.4	-0.4	...	-1
Outputs				
Out	-0.4	-0.4	...	0.6
Exp. Out	-0.4	-0.4	...	0.6
Out (DSP)	-0.4	-0.4	...	0.6
Exp. Out (DSP)	-0.4	-0.4	...	0.6

Test settings	
Tolerance Out	±2,7940e-08 (±60 LSB)

Test statistics	
Min CPU cycles	77
Max CPU cycles	77
Avg CPU cycles	77

Verification: Limitation Float32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for General block Limitation.

Test results				
Time step	1	2	...	159
CPU cycles	232	232	...	234
Inputs				
In (DSP)	-1	-0.962	...	0.6
max (DSP)	0.3	0.3	...	1
min (DSP)	-0.4	-0.4	...	-1
In	-1	-0.962	...	0.6
max	0.3	0.3	...	1
min	-0.4	-0.4	...	-1
Outputs				
Out	-0.4	-0.4	...	0.6
Exp. Out	-0.4	-0.4	...	0.6
Out (DSP)	-0.4	-0.4	...	0.6
Exp. Out (DSP)	-0.4	-0.4	...	0.6

Test settings	
Tolerance Out	±2,7940e-08 (±60 LSB)

Test statistics	
Min CPU cycles	143
Max CPU cycles	309
Avg CPU cycles	185

Verification: Limitation Float32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for General block Limitation.

Test results				
Time step	1	2	...	159
CPU cycles	126	126	...	125
Inputs				
In (DSP)	-1	-0.962	...	0.6
max (DSP)	0.3	0.3	...	1
min (DSP)	-0.4	-0.4	...	-1
In	-1	-0.962	...	0.6
max	0.3	0.3	...	1
min	-0.4	-0.4	...	-1
Outputs				
Out	-0.4	-0.4	...	0.6
Exp. Out	-0.4	-0.4	...	0.6
Out (DSP)	-0.4	-0.4	...	0.6
Exp. Out (DSP)	-0.4	-0.4	...	0.6

Test settings	
Tolerance Out	±2,7940e-08 (±60 LSB)

Test statistics	
Min CPU cycles	89
Max CPU cycles	128
Avg CPU cycles	104

Verification: Limitation Float32 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for General block Limitation.

Test results				
Time step	1	2	...	159
CPU cycles	265	265	...	264
Inputs				
In (DSP)	-1	-0.962	...	0.6
max (DSP)	0.3	0.3	...	1
min (DSP)	-0.4	-0.4	...	-1
In	-1	-0.962	...	0.6
max	0.3	0.3	...	1
min	-0.4	-0.4	...	-1
Outputs				
Out	-0.4	-0.4	...	0.6
Exp. Out	-0.4	-0.4	...	0.6
Out (DSP)	-0.4	-0.4	...	0.6
Exp. Out (DSP)	-0.4	-0.4	...	0.6

Test settings	
Tolerance Out	±2,7940e-08 (±60 LSB)

Test statistics	
Min CPU cycles	162
Max CPU cycles	269
Avg CPU cycles	204

Verification: Limitation Float32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for General block Limitation.

Test results				
Time step	1	2	...	159
CPU cycles	81	70	...	70
Inputs				
In (DSP)	-1	-0.962	...	0.6
max (DSP)	0.3	0.3	...	1
min (DSP)	-0.4	-0.4	...	-1
In	-1	-0.962	...	0.6
max	0.3	0.3	...	1
min	-0.4	-0.4	...	-1
Outputs				
Out	-0.4	-0.4	...	0.6
Exp. Out	-0.4	-0.4	...	0.6
Out (DSP)	-0.4	-0.4	...	0.6
Exp. Out (DSP)	-0.4	-0.4	...	0.6

Test settings	
Tolerance Out	±2,7940e-08 (±60 LSB)

Test statistics	
Min CPU cycles	63
Max CPU cycles	81
Avg CPU cycles	65

Verification: Limitation Float32 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

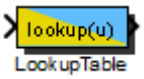
Inport test for General block Limitation.

Test results				
Time step	1	2	...	159
CPU cycles	61	61	...	61
Inputs				
In (DSP)	-1	-0.962	...	0.6
max (DSP)	0.3	0.3	...	1
min (DSP)	-0.4	-0.4	...	-1
In	-1	-0.962	...	0.6
max	0.3	0.3	...	1
min	-0.4	-0.4	...	-1
Outputs				
Out	-0.4	-0.4	...	0.6
Exp. Out	-0.4	-0.4	...	0.6
Out (DSP)	-0.4	-0.4	...	0.6
Exp. Out (DSP)	-0.4	-0.4	...	0.6

Test settings	
Tolerance Out	±2,7940e-08 (±60 LSB)

Test statistics	
Min CPU cycles	54
Max CPU cycles	61
Avg CPU cycles	56

Block: LookupTable



Look-up Table with 256+1 values.
Note: 257th value is used for preventing index overflow during interpolation.
-> for periodic signals the 257th value should be set equal to 1st value
-> for non-periodic signals the 257th value should be set equal to 256th value

Inports	
In	Table index

Outports	
Out	Table output

Mask Parameters		
Name	**ID**	**Description**
Lookup	1	Look-up Table

Implementations:

- **FiP8** 8 Bit Fixed Point Implementation
- **FiP16** 16 Bit Fixed Point Implementation
- **FiP32** 32 Bit Fixed Point Implementation

Implementation: FiP8

8 Bit Fixed Point Implementation

Inports Data Type	
In	int8

Outports Data Type	
Out	int8

Implementation: FiP16

16 Bit Fixed Point Implementation

Inports Data Type	
In	int16

Outports Data Type	
Out	int16

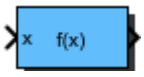
Implementation: FiP32

32 Bit Fixed Point Implementation

Inports Data Type	
In	int32

Outports Data Type	
Out	int32

Block: LookupTable1D



One dimensional look-up table with selectable number of data points.
Table data must be an array of size DimX. If one of the RAM implementations is used, DimX must not exceed 257.
If input is out of specified range, output will be cut off (no extrapolation).

Inports	
x	Table index in x direction

Outports	
Out	Table output

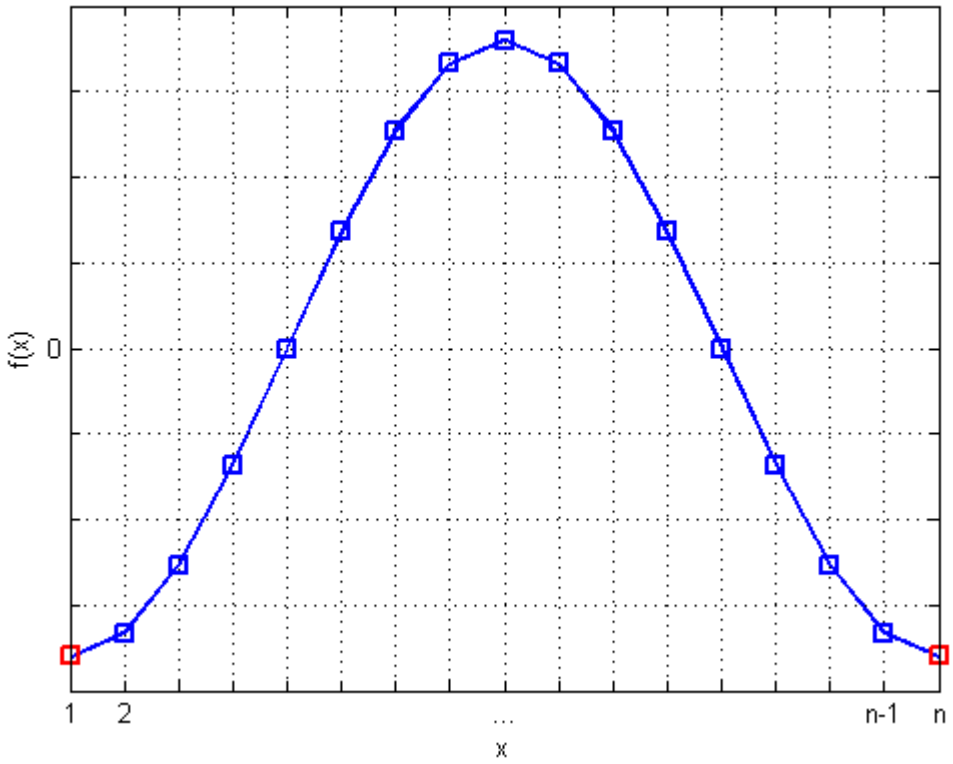
Mask Parameters		
Name	**ID**	**Description**
TableData	1	Look-up table data
DimX	2	Number of data points in x-direction
x_min	3	Minimum input value of x-dimension for look-up table
x_max	4	Maximum input value of x-dimension for look-up table

Description:

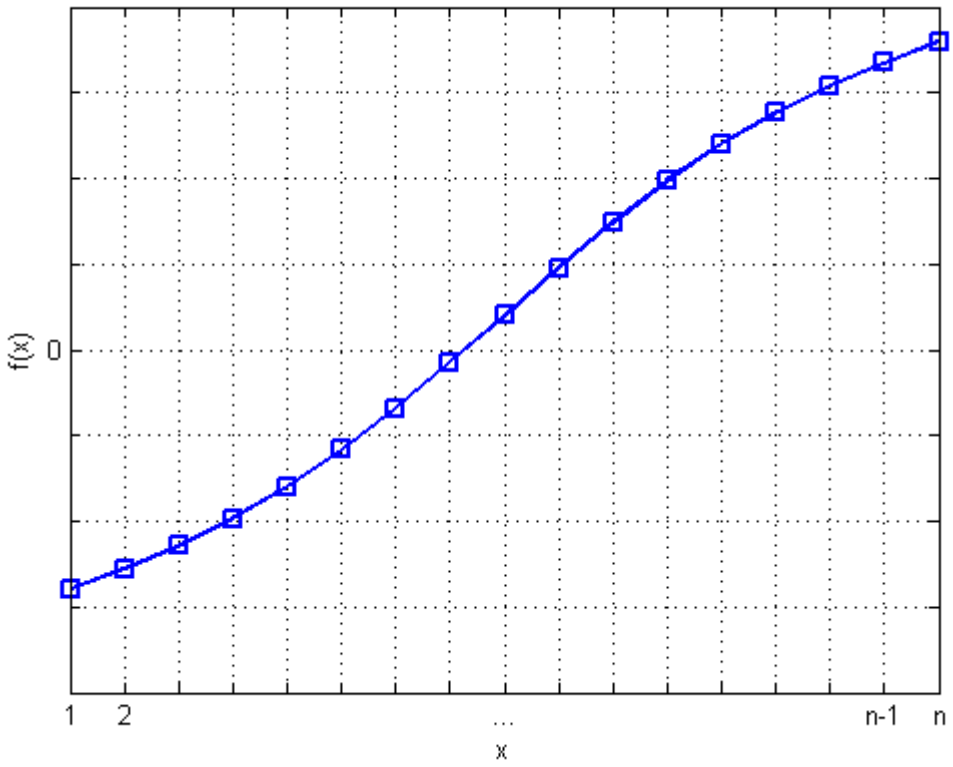
The table of the LookupTable1D block must contain DimX data points and they have to be arranged as

$$\mathrm{TableData} = [f(x_1),\ \ f(x_2),\ \ldots f(x_{n-1}),\ f(x_n)]$$

with n as the selected DimX value.
For periodic signals, the last entry must be identical to the first entry, see the example in the following figure.



For non-periodic signals there is no restriction regarding the last data point, see the example in the figure below.



Implementations:

FiP16	64 Bit Floating Point Implementation with look-up table located in RAM
FiP32	32 Bit Fixed Point Implementation with look-up table located in Flash memory
Float32	32 Bit Floating Point Implementation with look-up table located in Flash memory
Float64	64 Bit Floating Point Implementation with look-up table located in Flash memory
FiP16_RAM	16 Bit Fixed Point Implementation with look-up table located in RAM
FiP32_RAM	32 Bit Fixed Point Implementation with look-up table located in RAM
Float32_RAM	32 Bit Floating Point Implementation with look-up table located in RAM
Float64_RAM	64 Bit Floating Point Implementation with look-up table located in RAM

Implementation: FiP16

64 Bit Floating Point Implementation with look-up table located in RAM

Inports Data Type	
x	int16

Outports Data Type	
Out	int16

Implementation: FiP32

32 Bit Fixed Point Implementation with look-up table located in Flash memory

Inports Data Type	
x	int32

Outports Data Type	
Out	int32

Implementation: Float32

32 Bit Floating Point Implementation with look-up table located in Flash memory

Inports Data Type	
x	float32

Outports Data Type	
Out	float32

Implementation: Float64

64 Bit Floating Point Implementation with look-up table located in Flash memory

Inports Data Type	
x	float64

Outports Data Type	
Out	float64

Implementation: FiP16_RAM

16 Bit Fixed Point Implementation with look-up table located in RAM

Inports Data Type	
x	int16

Outports Data Type	
Out	int16

Implementation: FiP32_RAM

32 Bit Fixed Point Implementation with look-up table located in RAM

Inports Data Type	
x	int32

Outports Data Type	
Out	int32

Implementation: Float32_RAM

32 Bit Floating Point Implementation with look-up table located in RAM

Inports Data Type	
x	float32

Outports Data Type	
Out	float32

Implementation: Float64_RAM

64 Bit Floating Point Implementation with look-up table located in RAM

Inports Data Type	
x	float64

Outports Data Type	
Out	float64

Verification: LookupTable1D FiP16 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for General block LookupTable1D.

Test results						
Time step	1	2	3	4	...	67
CPU cycles	105	105	105	105	...	116
Inputs						
x (DSP)	-32768	-31775	-30782	-29789	...	32767
x	-1	-0.97	-0.939	-0.909	...	1
Parameters						
TableData	[1x257]					
DimX	257					
x_min	-0.8					
x_max	0.7					
Outputs						
Out	0.8	0.8	0.8	0.8	...	-0.7
Exp. Out	0.8	0.8	0.8	0.8	...	-0.7
Out (DSP)	26213	26213	26213	26213	...	-22938
Exp. Out (DSP)	26214	26214	26214	26214	...	-22938

Test settings	
Tolerance Out	±6,1035e-05 (±2 LSB)

Test statistics	
Min CPU cycles	105
Max CPU cycles	123
Avg CPU cycles	120

Test case: Conversion test OK

Conversion test for General block LookupTable1D.

Test results			
Time step	1	2	3
Mask parameters			
TableData	[1x17]	[1x33]	[1x65]
DimX	17	33	65
x_min	-0.5	-0.5	-0.5
x_max	0.7	0.7	0.7
Controller parameters			
gainX	27307	27307	27307
offsetX	3277	3277	3277
maskX	4095	2047	1023
Table	[1x17]	[1x33]	[1x65]
minX	-16384	-16384	-16384
maxX	22938	22938	22938
sfrX	12	11	10
gainXsfr	14	14	14
idxOffsetX	8	16	32
Exp. gainX	27307	27307	27307
Exp. offsetX	3277	3277	3277
Exp. maskX	4095	2047	1023
Exp. Table	[1x17]	[1x33]	[1x65]
Exp. minX	-16384	-16384	-16384
Exp. maxX	22938	22938	22938
Exp. sfrX	12	11	10
Exp. gainXsfr	14	14	14
Exp. idxOffsetX	8	16	32

Test settings	
Tolerance gainX	±0,0000e+00
Tolerance offsetX	±0,0000e+00
Tolerance maskX	±0,0000e+00
Tolerance Table	±0,0000e+00
Tolerance minX	±0,0000e+00
Tolerance maxX	±0,0000e+00
Tolerance sfrX	±0,0000e+00
Tolerance gainXsfr	±0,0000e+00
Tolerance idxOffsetX	±0,0000e+00

Verification: LookupTable1D FiP16 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for General block LookupTable1D.

Test results						
Time step	1	2	3	4	...	67
CPU cycles	63	63	63	63	...	69
Inputs						
x (DSP)	-32768	-31775	-30782	-29789	...	32767
x	-1	-0.97	-0.939	-0.909	...	1
Parameters						
TableData	[1x257]					
DimX	257					
x_min	-0.8					
x_max	0.7					
Outputs						
Out	0.8	0.8	0.8	0.8	...	-0.7
Exp. Out	0.8	0.8	0.8	0.8	...	-0.7
Out (DSP)	26213	26213	26213	26213	...	-22938
Exp. Out (DSP)	26214	26214	26214	26214	...	-22938

Test settings	
Tolerance Out	±6,1035e-05 (±2 LSB)

Test statistics	
Min CPU cycles	63
Max CPU cycles	79
Avg CPU cycles	75

Test case: Conversion test OK

Conversion test for General block LookupTable1D.

Test results			
Time step	1	2	3
Mask parameters			
TableData	[1x17]	[1x33]	[1x65]
DimX	17	33	65
x_min	-0.5	-0.5	-0.5
x_max	0.7	0.7	0.7
Controller parameters			
gainX	27307	27307	27307
offsetX	3277	3277	3277
maskX	4095	2047	1023
Table	[1x17]	[1x33]	[1x65]
minX	-16384	-16384	-16384
maxX	22938	22938	22938
sfrX	12	11	10
gainXsfr	14	14	14
idxOffsetX	8	16	32
Exp. gainX	27307	27307	27307
Exp. offsetX	3277	3277	3277
Exp. maskX	4095	2047	1023
Exp. Table	[1x17]	[1x33]	[1x65]
Exp. minX	-16384	-16384	-16384
Exp. maxX	22938	22938	22938
Exp. sfrX	12	11	10
Exp. gainXsfr	14	14	14
Exp. idxOffsetX	8	16	32

Test settings	
Tolerance gainX	±0,0000e+00
Tolerance offsetX	±0,0000e+00
Tolerance maskX	±0,0000e+00
Tolerance Table	±0,0000e+00
Tolerance minX	±0,0000e+00
Tolerance maxX	±0,0000e+00
Tolerance sfrX	±0,0000e+00
Tolerance gainXsfr	±0,0000e+00
Tolerance idxOffsetX	±0,0000e+00

Verification: LookupTable1D FiP16 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for General block LookupTable1D.

Test results						
Time step	1	2	3	4	...	67
CPU cycles	118	118	118	118	...	118
Inputs						
x (DSP)	-32768	-31775	-30782	-29789	...	32767
x	-1	-0.97	-0.939	-0.909	...	1
Parameters						
TableData	[1x257]					
DimX	257					
x_min	-0.8					
x_max	0.7					
Outputs						
Out	0.8	0.8	0.8	0.8	...	-0.7
Exp. Out	0.8	0.8	0.8	0.8	...	-0.7
Out (DSP)	26213	26213	26213	26213	...	-22938
Exp. Out (DSP)	26214	26214	26214	26214	...	-22938

Test settings	
Tolerance Out	±6,1035e-05 (±2 LSB)

Test statistics	
Min CPU cycles	118
Max CPU cycles	146
Avg CPU cycles	136

Test case: Conversion test OK

Conversion test for General block LookupTable1D.

Test results			
Time step	1	2	3
Mask parameters			
TableData	[1x17]	[1x33]	[1x65]
DimX	17	33	65
x_min	-0.5	-0.5	-0.5
x_max	0.7	0.7	0.7
Controller parameters			
gainX	27307	27307	27307
offsetX	3277	3277	3277
maskX	4095	2047	1023
Table	[1x17]	[1x33]	[1x65]
minX	-16384	-16384	-16384
maxX	22938	22938	22938
sfrX	12	11	10
gainXsfr	14	14	14
idxOffsetX	8	16	32
Exp. gainX	27307	27307	27307
Exp. offsetX	3277	3277	3277
Exp. maskX	4095	2047	1023
Exp. Table	[1x17]	[1x33]	[1x65]
Exp. minX	-16384	-16384	-16384
Exp. maxX	22938	22938	22938
Exp. sfrX	12	11	10
Exp. gainXsfr	14	14	14
Exp. idxOffsetX	8	16	32

Test settings	
Tolerance gainX	±0,0000e+00
Tolerance offsetX	±0,0000e+00
Tolerance maskX	±0,0000e+00
Tolerance Table	±0,0000e+00
Tolerance minX	±0,0000e+00
Tolerance maxX	±0,0000e+00
Tolerance sfrX	±0,0000e+00
Tolerance gainXsfr	±0,0000e+00
Tolerance idxOffsetX	±0,0000e+00

Verification: LookupTable1D FiP16 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for General block LookupTable1D.

Test results						
Time step	1	2	3	4	...	67
CPU cycles	98	98	98	98	...	101
Inputs						
x (DSP)	-32768	-31775	-30782	-29789	...	32767
x	-1	-0.97	-0.939	-0.909	...	1
Parameters						
TableData	[1x257]					
DimX	257					
x_min	-0.8					
x_max	0.7					
Outputs						
Out	0.8	0.8	0.8	0.8	...	-0.7
Exp. Out	0.8	0.8	0.8	0.8	...	-0.7
Out (DSP)	26213	26213	26213	26213	...	-22938
Exp. Out (DSP)	26214	26214	26214	26214	...	-22938

Test settings	
Tolerance Out	±6,1035e-05 (±2 LSB)

Test statistics	
Min CPU cycles	98
Max CPU cycles	175
Avg CPU cycles	112

Test case: Conversion test OK

Conversion test for General block LookupTable1D.

Test results			
Time step	1	2	3
Mask parameters			
TableData	[1x17]	[1x33]	[1x65]
DimX	17	33	65
x_min	-0.5	-0.5	-0.5
x_max	0.7	0.7	0.7
Controller parameters			
gainX	27307	27307	27307
offsetX	3277	3277	3277
maskX	4095	2047	1023
Table	[1x17]	[1x33]	[1x65]
minX	-16384	-16384	-16384
maxX	22938	22938	22938
sfrX	12	11	10
gainXsfr	14	14	14
idxOffsetX	8	16	32
Exp. gainX	27307	27307	27307
Exp. offsetX	3277	3277	3277
Exp. maskX	4095	2047	1023
Exp. Table	[1x17]	[1x33]	[1x65]
Exp. minX	-16384	-16384	-16384
Exp. maxX	22938	22938	22938
Exp. sfrX	12	11	10
Exp. gainXsfr	14	14	14
Exp. idxOffsetX	8	16	32

Test settings	
Tolerance gainX	±0,0000e+00
Tolerance offsetX	±0,0000e+00
Tolerance maskX	±0,0000e+00
Tolerance Table	±0,0000e+00
Tolerance minX	±0,0000e+00
Tolerance maxX	±0,0000e+00
Tolerance sfrX	±0,0000e+00
Tolerance gainXsfr	±0,0000e+00
Tolerance idxOffsetX	±0,0000e+00

Verification: LookupTable1D FiP16 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for General block LookupTable1D.

Test results						
Time step	1	2	3	4	...	67
CPU cycles	57	57	57	57	...	65
Inputs						
x (DSP)	-32768	-31775	-30782	-29789	...	32767
x	-1	-0.97	-0.939	-0.909	...	1
Parameters						
TableData	[1x257]					
DimX	257					
x_min	-0.8					
x_max	0.7					
Outputs						
Out	0.8	0.8	0.8	0.8	...	-0.7
Exp. Out	0.8	0.8	0.8	0.8	...	-0.7
Out (DSP)	26213	26213	26213	26213	...	-22938
Exp. Out (DSP)	26214	26214	26214	26214	...	-22938

Test settings	
Tolerance Out	±6,1035e-05 (±2 LSB)

Test statistics	
Min CPU cycles	57
Max CPU cycles	75
Avg CPU cycles	71

Test case: Conversion test OK

Conversion test for General block LookupTable1D.

Test results			
Time step	1	2	3
Mask parameters			
TableData	[1x17]	[1x33]	[1x65]
DimX	17	33	65
x_min	-0.5	-0.5	-0.5
x_max	0.7	0.7	0.7
Controller parameters			
gainX	27307	27307	27307
offsetX	3277	3277	3277
maskX	4095	2047	1023
Table	[1x17]	[1x33]	[1x65]
minX	-16384	-16384	-16384
maxX	22938	22938	22938
sfrX	12	11	10
gainXsfr	14	14	14
idxOffsetX	8	16	32
Exp. gainX	27307	27307	27307
Exp. offsetX	3277	3277	3277
Exp. maskX	4095	2047	1023
Exp. Table	[1x17]	[1x33]	[1x65]
Exp. minX	-16384	-16384	-16384
Exp. maxX	22938	22938	22938
Exp. sfrX	12	11	10
Exp. gainXsfr	14	14	14
Exp. idxOffsetX	8	16	32

Test settings	
Tolerance gainX	±0,0000e+00
Tolerance offsetX	±0,0000e+00
Tolerance maskX	±0,0000e+00
Tolerance Table	±0,0000e+00
Tolerance minX	±0,0000e+00
Tolerance maxX	±0,0000e+00
Tolerance sfrX	±0,0000e+00
Tolerance gainXsfr	±0,0000e+00
Tolerance idxOffsetX	±0,0000e+00

Verification: LookupTable1D FiP16 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for General block LookupTable1D.

Test results						
Time step	1	2	3	4	...	67
CPU cycles	99	99	99	99	...	102
Inputs						
x (DSP)	-32768	-31775	-30782	-29789	...	32767
x	-1	-0.97	-0.939	-0.909	...	1
Parameters						
TableData	[1x257]					
DimX	257					
x_min	-0.8					
x_max	0.7					
Outputs						
Out	0.8	0.8	0.8	0.8	...	-0.7
Exp. Out	0.8	0.8	0.8	0.8	...	-0.7
Out (DSP)	26213	26213	26213	26213	...	-22938
Exp. Out (DSP)	26214	26214	26214	26214	...	-22938

Test settings	
Tolerance Out	±6,1035e-05 (±2 LSB)

Test statistics	
Min CPU cycles	99
Max CPU cycles	122
Avg CPU cycles	116

Test case: Conversion test OK

Conversion test for General block LookupTable1D.

Test results			
Time step	1	2	3
Mask parameters			
TableData	[1x17]	[1x33]	[1x65]
DimX	17	33	65
x_min	-0.5	-0.5	-0.5
x_max	0.7	0.7	0.7
Controller parameters			
gainX	27307	27307	27307
offsetX	3277	3277	3277
maskX	4095	2047	1023
Table	[1x17]	[1x33]	[1x65]
minX	-16384	-16384	-16384
maxX	22938	22938	22938
sfrX	12	11	10
gainXsfr	14	14	14
idxOffsetX	8	16	32
Exp. gainX	27307	27307	27307
Exp. offsetX	3277	3277	3277
Exp. maskX	4095	2047	1023
Exp. Table	[1x17]	[1x33]	[1x65]
Exp. minX	-16384	-16384	-16384
Exp. maxX	22938	22938	22938
Exp. sfrX	12	11	10
Exp. gainXsfr	14	14	14
Exp. idxOffsetX	8	16	32

Test settings	
Tolerance gainX	±0,0000e+00
Tolerance offsetX	±0,0000e+00
Tolerance maskX	±0,0000e+00
Tolerance Table	±0,0000e+00
Tolerance minX	±0,0000e+00
Tolerance maxX	±0,0000e+00
Tolerance sfrX	±0,0000e+00
Tolerance gainXsfr	±0,0000e+00
Tolerance idxOffsetX	±0,0000e+00

Verification: LookupTable1D FiP16 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for General block LookupTable1D.

Test results						
Time step	1	2	3	4	...	67
CPU cycles	126	109	109	109	...	108
Inputs						
x (DSP)	-32768	-31775	-30782	-29789	...	32767
x	-1	-0.97	-0.939	-0.909	...	1
Parameters						
TableData	[1x257]					
DimX	257					
x_min	-0.8					
x_max	0.7					
Outputs						
Out	0.8	0.8	0.8	0.8	...	-0.7
Exp. Out	0.8	0.8	0.8	0.8	...	-0.7
Out (DSP)	26213	26213	26213	26213	...	-22938
Exp. Out (DSP)	26214	26214	26214	26214	...	-22938

Test settings	
Tolerance Out	±6,1035e-05 (±2 LSB)

Test statistics	
Min CPU cycles	108
Max CPU cycles	126
Avg CPU cycles	110

Test case: Conversion test OK

Conversion test for General block LookupTable1D.

Test results			
Time step	1	2	3
Mask parameters			
TableData	[1x17]	[1x33]	[1x65]
DimX	17	33	65
x_min	-0.5	-0.5	-0.5
x_max	0.7	0.7	0.7
Controller parameters			
gainX	27307	27307	27307
offsetX	3277	3277	3277
maskX	4095	2047	1023
Table	[1x17]	[1x33]	[1x65]
minX	-16384	-16384	-16384
maxX	22938	22938	22938
sfrX	12	11	10
gainXsfr	14	14	14
idxOffsetX	8	16	32
Exp. gainX	27307	27307	27307
Exp. offsetX	3277	3277	3277
Exp. maskX	4095	2047	1023
Exp. Table	[1x17]	[1x33]	[1x65]
Exp. minX	-16384	-16384	-16384
Exp. maxX	22938	22938	22938
Exp. sfrX	12	11	10
Exp. gainXsfr	14	14	14
Exp. idxOffsetX	8	16	32

Test settings	
Tolerance gainX	±0,0000e+00
Tolerance offsetX	±0,0000e+00
Tolerance maskX	±0,0000e+00
Tolerance Table	±0,0000e+00
Tolerance minX	±0,0000e+00
Tolerance maxX	±0,0000e+00
Tolerance sfrX	±0,0000e+00
Tolerance gainXsfr	±0,0000e+00
Tolerance idxOffsetX	±0,0000e+00

Verification: LookupTable1D FiP16 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for General block LookupTable1D.

Test results						
Time step	1	2	3	4	...	67
CPU cycles	84	84	84	84	...	101
Inputs						
x (DSP)	-32768	-31775	-30782	-29789	...	32767
x	-1	-0.97	-0.939	-0.909	...	1
Parameters						
TableData	[1x257]					
DimX	257					
x_min	-0.8					
x_max	0.7					
Outputs						
Out	0.8	0.8	0.8	0.8	...	-0.7
Exp. Out	0.8	0.8	0.8	0.8	...	-0.7
Out (DSP)	26213	26213	26213	26213	...	-22938
Exp. Out (DSP)	26214	26214	26214	26214	...	-22938

Test settings	
Tolerance Out	±6,1035e-05 (±2 LSB)

Test statistics	
Min CPU cycles	84
Max CPU cycles	105
Avg CPU cycles	100

Test case: Conversion test OK

Conversion test for General block LookupTable1D.

Test results			
Time step	1	2	3
Mask parameters			
TableData	[1x17]	[1x33]	[1x65]
DimX	17	33	65
x_min	-0.5	-0.5	-0.5
x_max	0.7	0.7	0.7
Controller parameters			
gainX	27307	27307	27307
offsetX	3277	3277	3277
maskX	4095	2047	1023
Table	[1x17]	[1x33]	[1x65]
minX	-16384	-16384	-16384
maxX	22938	22938	22938
sfrX	12	11	10
gainXsfr	14	14	14
idxOffsetX	8	16	32
Exp. gainX	27307	27307	27307
Exp. offsetX	3277	3277	3277
Exp. maskX	4095	2047	1023
Exp. Table	[1x17]	[1x33]	[1x65]
Exp. minX	-16384	-16384	-16384
Exp. maxX	22938	22938	22938
Exp. sfrX	12	11	10
Exp. gainXsfr	14	14	14
Exp. idxOffsetX	8	16	32

Test settings	
Tolerance gainX	±0,0000e+00
Tolerance offsetX	±0,0000e+00
Tolerance maskX	±0,0000e+00
Tolerance Table	±0,0000e+00
Tolerance minX	±0,0000e+00
Tolerance maxX	±0,0000e+00
Tolerance sfrX	±0,0000e+00
Tolerance gainXsfr	±0,0000e+00
Tolerance idxOffsetX	±0,0000e+00

Verification: LookupTable1D FiP32 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for General block LookupTable1D.

Test results				
Time step	1	2	...	67
CPU cycles	150	150	...	164
Inputs				
x (DSP)	-2147483648	-2082408386	...	2147483647
x	-1	-0.97	...	1
Parameters				
TableData	[1x257]			
DimX	257			
x_min	-0.8			
x_max	0.7			
Outputs				
Out	0.8	0.8	...	-0.7
Exp. Out	0.8	0.8	...	-0.7
Out (DSP)	1717986917	1717986917	...	-1503238554
Exp. Out (DSP)	1717986918	1717986918	...	-1503238554

Test settings	
Tolerance Out	±9,3132e-10 (±2 LSB)

Test statistics	
Min CPU cycles	150
Max CPU cycles	178
Avg CPU cycles	172

Test case: Conversion test OK

Conversion test for General block LookupTable1D.

Test results			
Time step	1	2	3
Mask parameters			
TableData	[1x17]	[1x33]	[1x65]
DimX	17	33	65
x_min	-0.5	-0.5	-0.5
x_max	0.7	0.7	0.7
Controller parameters			
gainX	1789569707	1789569707	1789569707
offsetX	214748365	214748365	214748365
maskX	268435455	134217727	67108863
Table	[1x17]	[1x33]	[1x65]
minX	-1073741824	-1073741824	-1073741824
maxX	1503238554	1503238554	1503238554
sfrX	28	27	26
gainXsfr	30	30	30
idxOffsetX	8	16	32
Exp. gainX	1789569707	1789569707	1789569707
Exp. offsetX	214748365	214748365	214748365
Exp. maskX	268435455	134217727	67108863
Exp. Table	[1x17]	[1x33]	[1x65]
Exp. minX	-1073741824	-1073741824	-1073741824
Exp. maxX	1503238554	1503238554	1503238554
Exp. sfrX	28	27	26
Exp. gainXsfr	30	30	30
Exp. idxOffsetX	8	16	32

Test settings	
Tolerance gainX	±0,0000e+00
Tolerance offsetX	±0,0000e+00
Tolerance maskX	±0,0000e+00
Tolerance Table	±0,0000e+00
Tolerance minX	±0,0000e+00
Tolerance maxX	±0,0000e+00
Tolerance sfrX	±0,0000e+00
Tolerance gainXsfr	±0,0000e+00
Tolerance idxOffsetX	±0,0000e+00

Verification: LookupTable1D FiP32 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for General block LookupTable1D.

Test results				
Time step	1	2	...	67
CPU cycles	147	147	...	155
Inputs				
x (DSP)	-2147483648	-2082408386	...	2147483647
x	-1	-0.97	...	1
Parameters				
TableData	[1x257]			
DimX	257			
x_min	-0.8			
x_max	0.7			
Outputs				
Out	0.8	0.8	...	-0.7
Exp. Out	0.8	0.8	...	-0.7
Out (DSP)	1717986917	1717986917	...	-1503238554
Exp. Out (DSP)	1717986918	1717986918	...	-1503238554

Test settings	
Tolerance Out	±9,3132e-10 (±2 LSB)

Test statistics	
Min CPU cycles	147
Max CPU cycles	209
Avg CPU cycles	194

Test case: Conversion test OK

Conversion test for General block LookupTable1D.

Test results			
Time step	1	2	3
Mask parameters			
TableData	[1x17]	[1x33]	[1x65]
DimX	17	33	65
x_min	-0.5	-0.5	-0.5
x_max	0.7	0.7	0.7
Controller parameters			
gainX	1789569707	1789569707	1789569707
offsetX	214748365	214748365	214748365
maskX	268435455	134217727	67108863
Table	[1x17]	[1x33]	[1x65]
minX	-1073741824	-1073741824	-1073741824
maxX	1503238554	1503238554	1503238554
sfrX	28	27	26
gainXsfr	30	30	30
idxOffsetX	8	16	32
Exp. gainX	1789569707	1789569707	1789569707
Exp. offsetX	214748365	214748365	214748365
Exp. maskX	268435455	134217727	67108863
Exp. Table	[1x17]	[1x33]	[1x65]
Exp. minX	-1073741824	-1073741824	-1073741824
Exp. maxX	1503238554	1503238554	1503238554
Exp. sfrX	28	27	26
Exp. gainXsfr	30	30	30
Exp. idxOffsetX	8	16	32

Test settings	
Tolerance gainX	±0,0000e+00
Tolerance offsetX	±0,0000e+00
Tolerance maskX	±0,0000e+00
Tolerance Table	±0,0000e+00
Tolerance minX	±0,0000e+00
Tolerance maxX	±0,0000e+00
Tolerance sfrX	±0,0000e+00
Tolerance gainXsfr	±0,0000e+00
Tolerance idxOffsetX	±0,0000e+00

Verification: LookupTable1D FiP32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for General block LookupTable1D.

Test results				
Time step	1	2	...	67
CPU cycles	160	160	...	153
Inputs				
x (DSP)	-2147483648	-2082408386	...	2147483647
x	-1	-0.97	...	1
Parameters				
TableData	[1x257]			
DimX	257			
x_min	-0.8			
x_max	0.7			
Outputs				
Out	0.8	0.8	...	-0.7
Exp. Out	0.8	0.8	...	-0.7
Out (DSP)	1717986917	1717986917	...	-1503238554
Exp. Out (DSP)	1717986918	1717986918	...	-1503238554

Test settings	
Tolerance Out	±9,3132e-10 (±2 LSB)

Test statistics	
Min CPU cycles	153
Max CPU cycles	205
Avg CPU cycles	190

Test case: Conversion test OK

Conversion test for General block LookupTable1D.

Test results			
Time step	1	2	3
Mask parameters			
TableData	[1x17]	[1x33]	[1x65]
DimX	17	33	65
x_min	-0.5	-0.5	-0.5
x_max	0.7	0.7	0.7
Controller parameters			
gainX	1789569707	1789569707	1789569707
offsetX	214748365	214748365	214748365
maskX	268435455	134217727	67108863
Table	[1x17]	[1x33]	[1x65]
minX	-1073741824	-1073741824	-1073741824
maxX	1503238554	1503238554	1503238554
sfrX	28	27	26
gainXsfr	30	30	30
idxOffsetX	8	16	32
Exp. gainX	1789569707	1789569707	1789569707
Exp. offsetX	214748365	214748365	214748365
Exp. maskX	268435455	134217727	67108863
Exp. Table	[1x17]	[1x33]	[1x65]
Exp. minX	-1073741824	-1073741824	-1073741824
Exp. maxX	1503238554	1503238554	1503238554
Exp. sfrX	28	27	26
Exp. gainXsfr	30	30	30
Exp. idxOffsetX	8	16	32

Test settings	
Tolerance gainX	±0,0000e+00
Tolerance offsetX	±0,0000e+00
Tolerance maskX	±0,0000e+00
Tolerance Table	±0,0000e+00
Tolerance minX	±0,0000e+00
Tolerance maxX	±0,0000e+00
Tolerance sfrX	±0,0000e+00
Tolerance gainXsfr	±0,0000e+00
Tolerance idxOffsetX	±0,0000e+00

Verification: LookupTable1D FiP32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for General block LookupTable1D.

Test results				
Time step	1	2	...	67
CPU cycles	221	221	...	219
Inputs				
x (DSP)	-2147483648	-2082408386	...	2147483647
x	-1	-0.97	...	1
Parameters				
TableData	[1x257]			
DimX	257			
x_min	-0.8			
x_max	0.7			
Outputs				
Out	0.8	0.8	...	-0.7
Exp. Out	0.8	0.8	...	-0.7
Out (DSP)	1717986917	1717986917	...	-1503238554
Exp. Out (DSP)	1717986918	1717986918	...	-1503238554

Test settings	
Tolerance Out	±9,3132e-10 (±2 LSB)

Test statistics	
Min CPU cycles	219
Max CPU cycles	322
Avg CPU cycles	296

Test case: Conversion test OK

Conversion test for General block LookupTable1D.

Test results			
Time step	1	2	3
Mask parameters			
TableData	[1x17]	[1x33]	[1x65]
DimX	17	33	65
x_min	-0.5	-0.5	-0.5
x_max	0.7	0.7	0.7
Controller parameters			
gainX	1789569707	1789569707	1789569707
offsetX	214748365	214748365	214748365
maskX	268435455	134217727	67108863
Table	[1x17]	[1x33]	[1x65]
minX	-1073741824	-1073741824	-1073741824
maxX	1503238554	1503238554	1503238554
sfrX	28	27	26
gainXsfr	30	30	30
idxOffsetX	8	16	32
Exp. gainX	1789569707	1789569707	1789569707
Exp. offsetX	214748365	214748365	214748365
Exp. maskX	268435455	134217727	67108863
Exp. Table	[1x17]	[1x33]	[1x65]
Exp. minX	-1073741824	-1073741824	-1073741824
Exp. maxX	1503238554	1503238554	1503238554
Exp. sfrX	28	27	26
Exp. gainXsfr	30	30	30
Exp. idxOffsetX	8	16	32

Test settings	
Tolerance gainX	±0,0000e+00
Tolerance offsetX	±0,0000e+00
Tolerance maskX	±0,0000e+00
Tolerance Table	±0,0000e+00
Tolerance minX	±0,0000e+00
Tolerance maxX	±0,0000e+00
Tolerance sfrX	±0,0000e+00
Tolerance gainXsfr	±0,0000e+00
Tolerance idxOffsetX	±0,0000e+00

Verification: LookupTable1D FiP32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for General block LookupTable1D.

Test results				
Time step	1	2	...	67
CPU cycles	82	82	...	92
Inputs				
x (DSP)	-2147483648	-2082408386	...	2147483647
x	-1	-0.97	...	1
Parameters				
TableData	[1x257]			
DimX	257			
x_min	-0.8			
x_max	0.7			
Outputs				
Out	0.8	0.8	...	-0.7
Exp. Out	0.8	0.8	...	-0.7
Out (DSP)	1717986917	1717986917	...	-1503238554
Exp. Out (DSP)	1717986918	1717986918	...	-1503238554

Test settings	
Tolerance Out	±9,3132e-10 (±2 LSB)

Test statistics	
Min CPU cycles	82
Max CPU cycles	122
Avg CPU cycles	113

Test case: Conversion test OK

Conversion test for General block LookupTable1D.

Test results			
Time step	1	2	3
Mask parameters			
TableData	[1x17]	[1x33]	[1x65]
DimX	17	33	65
x_min	-0.5	-0.5	-0.5
x_max	0.7	0.7	0.7
Controller parameters			
gainX	1789569707	1789569707	1789569707
offsetX	214748365	214748365	214748365
maskX	268435455	134217727	67108863
Table	[1x17]	[1x33]	[1x65]
minX	-1073741824	-1073741824	-1073741824
maxX	1503238554	1503238554	1503238554
sfrX	28	27	26
gainXsfr	30	30	30
idxOffsetX	8	16	32
Exp. gainX	1789569707	1789569707	1789569707
Exp. offsetX	214748365	214748365	214748365
Exp. maskX	268435455	134217727	67108863
Exp. Table	[1x17]	[1x33]	[1x65]
Exp. minX	-1073741824	-1073741824	-1073741824
Exp. maxX	1503238554	1503238554	1503238554
Exp. sfrX	28	27	26
Exp. gainXsfr	30	30	30
Exp. idxOffsetX	8	16	32

Test settings	
Tolerance gainX	±0,0000e+00
Tolerance offsetX	±0,0000e+00
Tolerance maskX	±0,0000e+00
Tolerance Table	±0,0000e+00
Tolerance minX	±0,0000e+00
Tolerance maxX	±0,0000e+00
Tolerance sfrX	±0,0000e+00
Tolerance gainXsfr	±0,0000e+00
Tolerance idxOffsetX	±0,0000e+00

Verification: LookupTable1D FiP32 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for General block LookupTable1D.

Test results				
Time step	1	2	...	67
CPU cycles	737	737	...	741
Inputs				
x (DSP)	-2147483648	-2082408386	...	2147483647
x	-1	-0.97	...	1
Parameters				
TableData	[1x257]			
DimX	257			
x_min	-0.8			
x_max	0.7			
Outputs				
Out	0.8	0.8	...	-0.7
Exp. Out	0.8	0.8	...	-0.7
Out (DSP)	1717986917	1717986917	...	-1503238554
Exp. Out (DSP)	1717986918	1717986918	...	-1503238554

Test settings	
Tolerance Out	±9,3132e-10 (±2 LSB)

Test statistics	
Min CPU cycles	737
Max CPU cycles	1155
Avg CPU cycles	1046

Test case: Conversion test OK

Conversion test for General block LookupTable1D.

Test results			
Time step	1	2	3
Mask parameters			
TableData	[1x17]	[1x33]	[1x65]
DimX	17	33	65
x_min	-0.5	-0.5	-0.5
x_max	0.7	0.7	0.7
Controller parameters			
gainX	1789569707	1789569707	1789569707
offsetX	214748365	214748365	214748365
maskX	268435455	134217727	67108863
Table	[1x17]	[1x33]	[1x65]
minX	-1073741824	-1073741824	-1073741824
maxX	1503238554	1503238554	1503238554
sfrX	28	27	26
gainXsfr	30	30	30
idxOffsetX	8	16	32
Exp. gainX	1789569707	1789569707	1789569707
Exp. offsetX	214748365	214748365	214748365
Exp. maskX	268435455	134217727	67108863
Exp. Table	[1x17]	[1x33]	[1x65]
Exp. minX	-1073741824	-1073741824	-1073741824
Exp. maxX	1503238554	1503238554	1503238554
Exp. sfrX	28	27	26
Exp. gainXsfr	30	30	30
Exp. idxOffsetX	8	16	32

Test settings	
Tolerance gainX	±0,0000e+00
Tolerance offsetX	±0,0000e+00
Tolerance maskX	±0,0000e+00
Tolerance Table	±0,0000e+00
Tolerance minX	±0,0000e+00
Tolerance maxX	±0,0000e+00
Tolerance sfrX	±0,0000e+00
Tolerance gainXsfr	±0,0000e+00
Tolerance idxOffsetX	±0,0000e+00

Verification: LookupTable1D FiP32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for General block LookupTable1D.

Test results				
Time step	1	2	...	67
CPU cycles	186	158	...	156
Inputs				
x (DSP)	-2147483648	-2082408386	...	2147483647
x	-1	-0.97	...	1
Parameters				
TableData	[1x257]			
DimX	257			
x_min	-0.8			
x_max	0.7			
Outputs				
Out	0.8	0.8	...	-0.7
Exp. Out	0.8	0.8	...	-0.7
Out (DSP)	1717986917	1717986917	...	-1503238554
Exp. Out (DSP)	1717986918	1717986918	...	-1503238554

Test settings	
Tolerance Out	±9,3132e-10 (±2 LSB)

Test statistics	
Min CPU cycles	156
Max CPU cycles	186
Avg CPU cycles	168

Test case: Conversion test OK

Conversion test for General block LookupTable1D.

Test results			
Time step	1	2	3
Mask parameters			
TableData	[1x17]	[1x33]	[1x65]
DimX	17	33	65
x_min	-0.5	-0.5	-0.5
x_max	0.7	0.7	0.7
Controller parameters			
gainX	1789569707	1789569707	1789569707
offsetX	214748365	214748365	214748365
maskX	268435455	134217727	67108863
Table	[1x17]	[1x33]	[1x65]
minX	-1073741824	-1073741824	-1073741824
maxX	1503238554	1503238554	1503238554
sfrX	28	27	26
gainXsfr	30	30	30
idxOffsetX	8	16	32
Exp. gainX	1789569707	1789569707	1789569707
Exp. offsetX	214748365	214748365	214748365
Exp. maskX	268435455	134217727	67108863
Exp. Table	[1x17]	[1x33]	[1x65]
Exp. minX	-1073741824	-1073741824	-1073741824
Exp. maxX	1503238554	1503238554	1503238554
Exp. sfrX	28	27	26
Exp. gainXsfr	30	30	30
Exp. idxOffsetX	8	16	32

Test settings	
Tolerance gainX	±0,0000e+00
Tolerance offsetX	±0,0000e+00
Tolerance maskX	±0,0000e+00
Tolerance Table	±0,0000e+00
Tolerance minX	±0,0000e+00
Tolerance maxX	±0,0000e+00
Tolerance sfrX	±0,0000e+00
Tolerance gainXsfr	±0,0000e+00
Tolerance idxOffsetX	±0,0000e+00

Verification: LookupTable1D FiP32 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for General block LookupTable1D.

Test results				
Time step	1	2	...	67
CPU cycles	126	126	...	151
Inputs				
x (DSP)	-2147483648	-2082408386	...	2147483647
x	-1	-0.97	...	1
Parameters				
TableData	[1x257]			
DimX	257			
x_min	-0.8			
x_max	0.7			
Outputs				
Out	0.8	0.8	...	-0.7
Exp. Out	0.8	0.8	...	-0.7
Out (DSP)	1717986917	1717986917	...	-1503238554
Exp. Out (DSP)	1717986918	1717986918	...	-1503238554

Test settings	
Tolerance Out	±9,3132e-10 (±2 LSB)

Test statistics	
Min CPU cycles	126
Max CPU cycles	157
Avg CPU cycles	149

Test case: Conversion test OK

Conversion test for General block LookupTable1D.

Test results			
Time step	1	2	3
Mask parameters			
TableData	[1x17]	[1x33]	[1x65]
DimX	17	33	65
x_min	-0.5	-0.5	-0.5
x_max	0.7	0.7	0.7
Controller parameters			
gainX	1789569707	1789569707	1789569707
offsetX	214748365	214748365	214748365
maskX	268435455	134217727	67108863
Table	[1x17]	[1x33]	[1x65]
minX	-1073741824	-1073741824	-1073741824
maxX	1503238554	1503238554	1503238554
sfrX	28	27	26
gainXsfr	30	30	30
idxOffsetX	8	16	32
Exp. gainX	1789569707	1789569707	1789569707
Exp. offsetX	214748365	214748365	214748365
Exp. maskX	268435455	134217727	67108863
Exp. Table	[1x17]	[1x33]	[1x65]
Exp. minX	-1073741824	-1073741824	-1073741824
Exp. maxX	1503238554	1503238554	1503238554
Exp. sfrX	28	27	26
Exp. gainXsfr	30	30	30
Exp. idxOffsetX	8	16	32

Test settings	
Tolerance gainX	±0,0000e+00
Tolerance offsetX	±0,0000e+00
Tolerance maskX	±0,0000e+00
Tolerance Table	±0,0000e+00
Tolerance minX	±0,0000e+00
Tolerance maxX	±0,0000e+00
Tolerance sfrX	±0,0000e+00
Tolerance gainXsfr	±0,0000e+00
Tolerance idxOffsetX	±0,0000e+00

Verification: LookupTable1D Float32 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for General block LookupTable1D.

Test results				
Time step	1	2	...	67
CPU cycles	82	82	...	99
Inputs				
x (DSP)	-1.2	-1.164	...	1.2
x	-1.2	-1.164	...	1.2
Parameters				
TableData	[1x257]			
DimX	257			
x_min	-0.8			
x_max	0.7			
Outputs				
Out	1.04	1.04	...	-0.91
Exp. Out	1.04	1.04	...	-0.91
Out (DSP)	1.04	1.04	...	-0.91
Exp. Out (DSP)	1.04	1.04	...	-0.91

Test settings	
Tolerance Out	±1,8626e-07 (±400 LSB)

Test statistics	
Min CPU cycles	82
Max CPU cycles	122
Avg CPU cycles	110

Test case: Conversion test OK

Conversion test for General block LookupTable1D.

Test results			
Time step	1	2	3
Mask parameters			
TableData	[1x17]	[1x33]	[1x65]
DimX	17	33	65
x_min	-0.8	-0.8	-0.8
x_max	0.7	0.7	0.7
Controller parameters			
gainX	10.667	21.333	42.667
offsetX	-0.8	-0.8	-0.8
Table	[1x17]	[1x33]	[1x65]
dimX	16	32	64
Exp. gainX	10.667	21.333	42.667
Exp. offsetX	-0.8	-0.8	-0.8
Exp. Table	[1x17]	[1x33]	[1x65]
Exp. dimX	16	32	64

Test settings	
Tolerance gainX	±0,0000e+00
Tolerance offsetX	±0,0000e+00
Tolerance Table	±0,0000e+00
Tolerance dimX	±0,0000e+00

Verification: LookupTable1D Float32 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for General block LookupTable1D.

Test results				
Time step	1	2	...	67
CPU cycles	43	43	...	59
Inputs				
x (DSP)	-1.2	-1.164	...	1.2
x	-1.2	-1.164	...	1.2
Parameters				
TableData	[1x257]			
DimX	257			
x_min	-0.8			
x_max	0.7			
Outputs				
Out	1.04	1.04	...	-0.91
Exp. Out	1.04	1.04	...	-0.91
Out (DSP)	1.04	1.04	...	-0.91
Exp. Out (DSP)	1.04	1.04	...	-0.91

Test settings	
Tolerance Out	±1,8626e-07 (±400 LSB)

Test statistics	
Min CPU cycles	43
Max CPU cycles	75
Avg CPU cycles	66

Test case: Conversion test OK

Conversion test for General block LookupTable1D.

Test results			
Time step	1	2	3
Mask parameters			
TableData	[1x17]	[1x33]	[1x65]
DimX	17	33	65
x_min	-0.8	-0.8	-0.8
x_max	0.7	0.7	0.7
Controller parameters			
gainX	10.667	21.333	42.667
offsetX	-0.8	-0.8	-0.8
Table	[1x17]	[1x33]	[1x65]
dimX	16	32	64
Exp. gainX	10.667	21.333	42.667
Exp. offsetX	-0.8	-0.8	-0.8
Exp. Table	[1x17]	[1x33]	[1x65]
Exp. dimX	16	32	64

Test settings	
Tolerance gainX	±0,0000e+00
Tolerance offsetX	±0,0000e+00
Tolerance Table	±0,0000e+00
Tolerance dimX	±0,0000e+00

Verification: LookupTable1D Float32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for General block LookupTable1D.

Test results				
Time step	1	2	...	67
CPU cycles	92	92	...	112
Inputs				
x (DSP)	-1.2	-1.164	...	1.2
x	-1.2	-1.164	...	1.2
Parameters				
TableData	[1x257]			
DimX	257			
x_min	-0.8			
x_max	0.7			
Outputs				
Out	1.04	1.04	...	-0.91
Exp. Out	1.04	1.04	...	-0.91
Out (DSP)	1.04	1.04	...	-0.91
Exp. Out (DSP)	1.04	1.04	...	-0.91

Test settings	
Tolerance Out	±1,8626e-07 (±400 LSB)

Test statistics	
Min CPU cycles	92
Max CPU cycles	118
Avg CPU cycles	110

Test case: Conversion test OK

Conversion test for General block LookupTable1D.

Test results			
Time step	1	2	3
Mask parameters			
TableData	[1x17]	[1x33]	[1x65]
DimX	17	33	65
x_min	-0.8	-0.8	-0.8
x_max	0.7	0.7	0.7
Controller parameters			
gainX	10.667	21.333	42.667
offsetX	-0.8	-0.8	-0.8
Table	[1x17]	[1x33]	[1x65]
dimX	16	32	64
Exp. gainX	10.667	21.333	42.667
Exp. offsetX	-0.8	-0.8	-0.8
Exp. Table	[1x17]	[1x33]	[1x65]
Exp. dimX	16	32	64

Test settings	
Tolerance gainX	±0,0000e+00
Tolerance offsetX	±0,0000e+00
Tolerance Table	±0,0000e+00
Tolerance dimX	±0,0000e+00

Verification: LookupTable1D Float32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for General block LookupTable1D.

Test results				
Time step	1	2	...	67
CPU cycles	497	501	...	625
Inputs				
x (DSP)	-1.2	-1.164	...	1.2
x	-1.2	-1.164	...	1.2
Parameters				
TableData	[1x257]			
DimX	257			
x_min	-0.8			
x_max	0.7			
Outputs				
Out	1.04	1.04	...	-0.91
Exp. Out	1.04	1.04	...	-0.91
Out (DSP)	1.04	1.04	...	-0.91
Exp. Out (DSP)	1.04	1.04	...	-0.91

Test settings	
Tolerance Out	±1,8626e-07 (±400 LSB)

Test statistics	
Min CPU cycles	490
Max CPU cycles	1353
Avg CPU cycles	1027

Test case: Conversion test OK

Conversion test for General block LookupTable1D.

Test results			
Time step	1	2	3
Mask parameters			
TableData	[1x17]	[1x33]	[1x65]
DimX	17	33	65
x_min	-0.8	-0.8	-0.8
x_max	0.7	0.7	0.7
Controller parameters			
gainX	10.667	21.333	42.667
offsetX	-0.8	-0.8	-0.8
Table	[1x17]	[1x33]	[1x65]
dimX	16	32	64
Exp. gainX	10.667	21.333	42.667
Exp. offsetX	-0.8	-0.8	-0.8
Exp. Table	[1x17]	[1x33]	[1x65]
Exp. dimX	16	32	64

Test settings	
Tolerance gainX	±0,0000e+00
Tolerance offsetX	±0,0000e+00
Tolerance Table	±0,0000e+00
Tolerance dimX	±0,0000e+00

Verification: LookupTable1D Float32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for General block LookupTable1D.

Test results				
Time step	1	2	...	67
CPU cycles	205	207	...	240
Inputs				
x (DSP)	-1.2	-1.164	...	1.2
x	-1.2	-1.164	...	1.2
Parameters				
TableData	[1x257]			
DimX	257			
x_min	-0.8			
x_max	0.7			
Outputs				
Out	1.04	1.04	...	-0.91
Exp. Out	1.04	1.04	...	-0.91
Out (DSP)	1.04	1.04	...	-0.91
Exp. Out (DSP)	1.04	1.04	...	-0.91

Test settings	
Tolerance Out	±1,8626e-07 (±400 LSB)

Test statistics	
Min CPU cycles	205
Max CPU cycles	515
Avg CPU cycles	399

Test case: Conversion test OK

Conversion test for General block LookupTable1D.

Test results			
Time step	1	2	3
Mask parameters			
TableData	[1x17]	[1x33]	[1x65]
DimX	17	33	65
x_min	-0.8	-0.8	-0.8
x_max	0.7	0.7	0.7
Controller parameters			
gainX	10.667	21.333	42.667
offsetX	-0.8	-0.8	-0.8
Table	[1x17]	[1x33]	[1x65]
dimX	16	32	64
Exp. gainX	10.667	21.333	42.667
Exp. offsetX	-0.8	-0.8	-0.8
Exp. Table	[1x17]	[1x33]	[1x65]
Exp. dimX	16	32	64

Test settings	
Tolerance gainX	±0,0000e+00
Tolerance offsetX	±0,0000e+00
Tolerance Table	±0,0000e+00
Tolerance dimX	±0,0000e+00

Verification: LookupTable1D Float32 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for General block LookupTable1D.

Test results				
Time step	1	2	...	67
CPU cycles	520	521	...	652
Inputs				
x (DSP)	-1.2	-1.164	...	1.2
x	-1.2	-1.164	...	1.2
Parameters				
TableData	[1x257]			
DimX	257			
x_min	-0.8			
x_max	0.7			
Outputs				
Out	1.04	1.04	...	-0.91
Exp. Out	1.04	1.04	...	-0.91
Out (DSP)	1.04	1.04	...	-0.91
Exp. Out (DSP)	1.04	1.04	...	-0.91

Test settings	
Tolerance Out	±1,8626e-07 (±400 LSB)

Test statistics	
Min CPU cycles	507
Max CPU cycles	1994
Avg CPU cycles	1369

Test case: Conversion test OK

Conversion test for General block LookupTable1D.

Test results			
Time step	1	2	3
Mask parameters			
TableData	[1x17]	[1x33]	[1x65]
DimX	17	33	65
x_min	-0.8	-0.8	-0.8
x_max	0.7	0.7	0.7
Controller parameters			
gainX	10.667	21.333	42.667
offsetX	-0.8	-0.8	-0.8
Table	[1x17]	[1x33]	[1x65]
dimX	16	32	64
Exp. gainX	10.667	21.333	42.667
Exp. offsetX	-0.8	-0.8	-0.8
Exp. Table	[1x17]	[1x33]	[1x65]
Exp. dimX	16	32	64

Test settings	
Tolerance gainX	±0,0000e+00
Tolerance offsetX	±0,0000e+00
Tolerance Table	±0,0000e+00
Tolerance dimX	±0,0000e+00

Verification: LookupTable1D Float32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for General block LookupTable1D.

Test results				
Time step	1	2	...	67
CPU cycles	99	77	...	91
Inputs				
x (DSP)	-1.2	-1.164	...	1.2
x	-1.2	-1.164	...	1.2
Parameters				
TableData	[1x257]			
DimX	257			
x_min	-0.8			
x_max	0.7			
Outputs				
Out	1.04	1.04	...	-0.91
Exp. Out	1.04	1.04	...	-0.91
Out (DSP)	1.04	1.04	...	-0.91
Exp. Out (DSP)	1.04	1.04	...	-0.91

Test settings	
Tolerance Out	±1,8626e-07 (±400 LSB)

Test statistics	
Min CPU cycles	77
Max CPU cycles	112
Avg CPU cycles	98

Test case: Conversion test OK

Conversion test for General block LookupTable1D.

Test results			
Time step	1	2	3
Mask parameters			
TableData	[1x17]	[1x33]	[1x65]
DimX	17	33	65
x_min	-0.8	-0.8	-0.8
x_max	0.7	0.7	0.7
Controller parameters			
gainX	10.667	21.333	42.667
offsetX	-0.8	-0.8	-0.8
Table	[1x17]	[1x33]	[1x65]
dimX	16	32	64
Exp. gainX	10.667	21.333	42.667
Exp. offsetX	-0.8	-0.8	-0.8
Exp. Table	[1x17]	[1x33]	[1x65]
Exp. dimX	16	32	64

Test settings	
Tolerance gainX	±0,0000e+00
Tolerance offsetX	±0,0000e+00
Tolerance Table	±0,0000e+00
Tolerance dimX	±0,0000e+00

Verification: LookupTable1D Float32 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for General block LookupTable1D.

Test results				
Time step	1	2	...	67
CPU cycles	71	71	...	96
Inputs				
x (DSP)	-1.2	-1.164	...	1.2
x	-1.2	-1.164	...	1.2
Parameters				
TableData	[1x257]			
DimX	257			
x_min	-0.8			
x_max	0.7			
Outputs				
Out	1.04	1.04	...	-0.91
Exp. Out	1.04	1.04	...	-0.91
Out (DSP)	1.04	1.04	...	-0.91
Exp. Out (DSP)	1.04	1.04	...	-0.91

Test settings	
Tolerance Out	±1,8626e-07 (±400 LSB)

Test statistics	
Min CPU cycles	71
Max CPU cycles	108
Avg CPU cycles	96

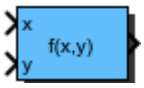
Test case: Conversion test OK

Conversion test for General block LookupTable1D.

Test results			
Time step	1	2	3
Mask parameters			
TableData	[1x17]	[1x33]	[1x65]
DimX	17	33	65
x_min	-0.8	-0.8	-0.8
x_max	0.7	0.7	0.7
Controller parameters			
gainX	10.667	21.333	42.667
offsetX	-0.8	-0.8	-0.8
Table	[1x17]	[1x33]	[1x65]
dimX	16	32	64
Exp. gainX	10.667	21.333	42.667
Exp. offsetX	-0.8	-0.8	-0.8
Exp. Table	[1x17]	[1x33]	[1x65]
Exp. dimX	16	32	64

Test settings	
Tolerance gainX	±0,0000e+00
Tolerance offsetX	±0,0000e+00
Tolerance Table	±0,0000e+00
Tolerance dimX	±0,0000e+00

Block: LookupTable2D



Two dimensional look-up table with selectable number of data points.
Table data must be an array of size DimX*DimY.
If input is out of specified range, output will be cut off (no extrapolation).

Inports	
x	Table index in x direction
y	Table index in y direction

Outports	
Out	Table output

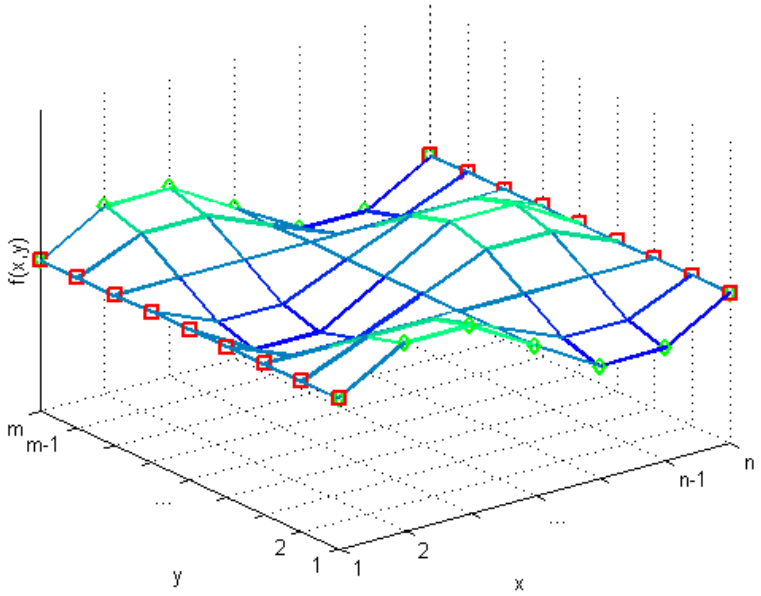
Mask Parameters		
Name	**ID**	**Description**
TableData	1	Look-up table data
DimX	2	Number of data points in x-direction
x_min	3	Minimum input value of x-dimension for look-up table
x_max	4	Maximum input value of x-dimension for look-up table
DimY	5	Number of data points in y-direction
y_min	6	Minimum input value of y-dimension for look-up table
y_max	7	Maximum input value of y-dimension for look-up table

Description:

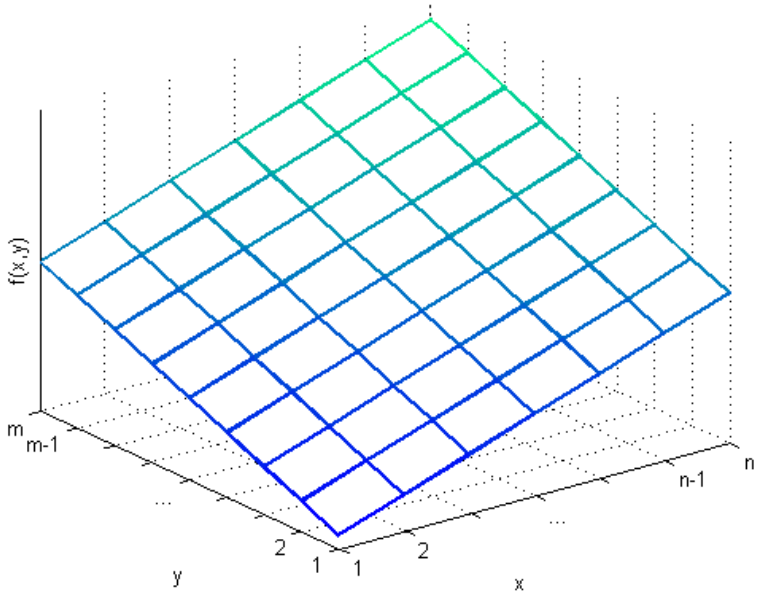
The table of the LookupTable2D block must contain DimX times DimY data points and they have to be arranged as

$$\begin{aligned}\mathrm{TableData} = [&f(x_1,y_1),\ f(x_2,y_1),\ \ldots f(x_{n-1},y_1),\ f(x_n,y_1),\\ &f(x_1,y_2),\ f(x_2,y_2),\ \ldots f(x_{n-1},y_2),\ f(x_n,y_2),\\ &\ldots\\ &f(x_1,y_{m-1}),\ f(x_2,y_{m-1}),\ \ldots f(x_{n-1},y_{m-1}),\ f(x_n,y_{m-1}),\\ &f(x_1,y_m),\ f(x_2,y_m),\ \ldots f(x_{n-1},y_m),\ f(x_n,y_m)]\end{aligned}$$

with n as selected DimX and m as selected DimY values.
For periodic signals, the last entries per dimension must be identical to the first entries in this dimension, see the example in the following figure.



For non-periodic signals there is no restriction regarding the last data points, see the example in the figure below.



Implementations:

FiP16	16 Bit Fixed Point Implementation
FiP32	32 Bit Fixed Point Implementation
Float32	32 Bit Floating Point Implementation
Float64	64 Bit Floating Point Implementation

Implementation: FiP16

16 Bit Fixed Point Implementation

Inports Data Type	
x	int16
y	int16

Outports Data Type	
Out	int16

Implementation: FiP32

32 Bit Fixed Point Implementation

Inports Data Type	
x	int32
y	int32

Outports Data Type	
Out	int32

Implementation: Float32

32 Bit Floating Point Implementation

Inports Data Type	
x	float32
y	float32

Outports Data Type	
Out	float32

Implementation: Float64

64 Bit Floating Point Implementation

Inports Data Type	
x	float64
y	float64

Outports Data Type	
Out	float64

Verification: LookupTable2D FiP16 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for General block LookupTable2D.

Test results						
Time step	1	2	3	4	...	67
CPU cycles	217	217	217	217	...	210
Inputs						
x (DSP)	-32768	-31775	-30782	-29789	...	32767
y (DSP)	26214	25370	24526	23682	...	-29491
x	-1	-0.97	-0.939	-0.909	...	1
y	0.8	0.774	0.748	0.723	...	-0.9
Parameters						
TableData	[1x561]					
DimX	17					
x_min	-0.8					
x_max	0.7					
DimY	33					
y_min	-0.6					
y_max	0.9					
Outputs						
Out	-0	-0.013	-0.026	-0.039	...	0.05
Exp. Out	0	-0.013	-0.026	-0.039	...	0.05
Out (DSP)	-1	-423	-845	-1267	...	1637
Exp. Out (DSP)	0	-422	-844	-1266	...	1638

Test settings	
Tolerance Out	±9,1553e-05 (±3 LSB)

Test statistics	
Min CPU cycles	210
Max CPU cycles	234
Avg CPU cycles	228

Test case: Conversion test OK

Conversion test for General block LookupTable2D.

Test results	
Time step	1
Mask parameters	
TableData	[1x561]
DimX	33
x_min	-1
x_max	1
DimY	17
y_min	-1
y_max	1
Controller parameters	
gainX	16384
maskY	4095
maskX	2047
Table	[1x561]
gainY	16384
maxY	32767
maxX	32767
sfrX	11
sfrY	12
offsetX	0
sizeX	33
offsetY	0
minY	-32767
minX	-32767
gainXsfr	14
idxOffsetY	8
idxOffsetX	16
gainYsfr	14
Exp. gainX	16384
Exp. maskY	4095
Exp. maskX	2047
Exp. Table	[1x561]
Exp. gainY	16384
Exp. maxY	32767
Exp. maxX	32767
Exp. sfrX	11
Exp. sfrY	12
Exp. offsetX	0
Exp. sizeX	33
Exp. offsetY	0
Exp. minY	-32767
Exp. minX	-32767

Test settings	
Tolerance gainX	±0,0000e+00
Tolerance maskY	±0,0000e+00
Tolerance maskX	±0,0000e+00
Tolerance Table	±0,0000e+00
Tolerance gainY	±0,0000e+00
Tolerance maxY	±0,0000e+00
Tolerance maxX	±0,0000e+00
Tolerance sfrX	±0,0000e+00
Tolerance sfrY	±0,0000e+00
Tolerance offsetX	±0,0000e+00
Tolerance sizeX	±0,0000e+00
Tolerance offsetY	±0,0000e+00
Tolerance minY	±0,0000e+00
Tolerance minX	±0,0000e+00
Tolerance gainXsfr	±0,0000e+00
Tolerance idxOffsetY	±0,0000e+00
Tolerance idxOffsetX	±0,0000e+00
Tolerance gainYsfr	±0,0000e+00

Verification: LookupTable2D FiP16 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for General block LookupTable2D.

Test results						
Time step	1	2	3	4	...	67
CPU cycles	133	133	133	133	...	123
Inputs						
x (DSP)	-32768	-31775	-30782	-29789	...	32767
y (DSP)	26214	25370	24526	23682	...	-29491
x	-1	-0.97	-0.939	-0.909	...	1
y	0.8	0.774	0.748	0.723	...	-0.9
Parameters						
TableData	[1x561]					
DimX	17					
x_min	-0.8					
x_max	0.7					
DimY	33					
y_min	-0.6					
y_max	0.9					
Outputs						
Out	-0	-0.013	-0.026	-0.039	...	0.05
Exp. Out	0	-0.013	-0.026	-0.039	...	0.05
Out (DSP)	-1	-423	-845	-1267	...	1637
Exp. Out (DSP)	0	-422	-844	-1266	...	1638

Test settings	
Tolerance Out	±9,1553e-05 (±3 LSB)

Test statistics	
Min CPU cycles	123
Max CPU cycles	151
Avg CPU cycles	144

Test case: Conversion test OK

Conversion test for General block LookupTable2D.

Test results	
Time step	1
Mask parameters	
TableData	[1x561]
DimX	33
x_min	-1
x_max	1
DimY	17
y_min	-1
y_max	1
Controller parameters	
gainX	16384
maskY	4095
maskX	2047
Table	[1x561]
gainY	16384
maxY	32767
maxX	32767
sfrX	11
sfrY	12
offsetX	0
sizeX	33
offsetY	0
minY	-32767
minX	-32767
gainXsfr	14
idxOffsetY	8
idxOffsetX	16
gainYsfr	14
Exp. gainX	16384
Exp. maskY	4095
Exp. maskX	2047
Exp. Table	[1x561]
Exp. gainY	16384
Exp. maxY	32767
Exp. maxX	32767
Exp. sfrX	11
Exp. sfrY	12
Exp. offsetX	0
Exp. sizeX	33
Exp. offsetY	0
Exp. minY	-32767
Exp. minX	-32767

Test settings	
Tolerance gainX	±0,0000e+00
Tolerance maskY	±0,0000e+00
Tolerance maskX	±0,0000e+00
Tolerance Table	±0,0000e+00
Tolerance gainY	±0,0000e+00
Tolerance maxY	±0,0000e+00
Tolerance maxX	±0,0000e+00
Tolerance sfrX	±0,0000e+00
Tolerance sfrY	±0,0000e+00
Tolerance offsetX	±0,0000e+00
Tolerance sizeX	±0,0000e+00
Tolerance offsetY	±0,0000e+00
Tolerance minY	±0,0000e+00
Tolerance minX	±0,0000e+00
Tolerance gainXsfr	±0,0000e+00
Tolerance idxOffsetY	±0,0000e+00
Tolerance idxOffsetX	±0,0000e+00
Tolerance gainYsfr	±0,0000e+00

Verification: LookupTable2D FiP16 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for General block LookupTable2D.

Test results						
Time step	1	2	3	4	...	67
CPU cycles	226	226	226	226	...	185
Inputs						
x (DSP)	-32768	-31775	-30782	-29789	...	32767
y (DSP)	26214	25370	24526	23682	...	-29491
x	-1	-0.97	-0.939	-0.909	...	1
y	0.8	0.774	0.748	0.723	...	-0.9
Parameters						
TableData	[1x561]					
DimX	17					
x_min	-0.8					
x_max	0.7					
DimY	33					
y_min	-0.6					
y_max	0.9					
Outputs						
Out	-0	-0.013	-0.026	-0.039	...	0.05
Exp. Out	0	-0.013	-0.026	-0.039	...	0.05
Out (DSP)	-1	-423	-845	-1267	...	1637
Exp. Out (DSP)	0	-422	-844	-1266	...	1638

Test settings	
Tolerance Out	±9,1553e-05 (±3 LSB)

Test statistics	
Min CPU cycles	185
Max CPU cycles	249
Avg CPU cycles	234

Test case: Conversion test OK

Conversion test for General block LookupTable2D.

Test results	
Time step	1
Mask parameters	
TableData	[1x561]
DimX	33
x_min	-1
x_max	1
DimY	17
y_min	-1
y_max	1
Controller parameters	
gainX	16384
maskY	4095
maskX	2047
Table	[1x561]
gainY	16384
maxY	32767
maxX	32767
sfrX	11
sfrY	12
offsetX	0
sizeX	33
offsetY	0
minY	-32767
minX	-32767
gainXsfr	14
idxOffsetY	8
idxOffsetX	16
gainYsfr	14
Exp. gainX	16384
Exp. maskY	4095
Exp. maskX	2047
Exp. Table	[1x561]
Exp. gainY	16384
Exp. maxY	32767
Exp. maxX	32767
Exp. sfrX	11
Exp. sfrY	12
Exp. offsetX	0
Exp. sizeX	33
Exp. offsetY	0
Exp. minY	-32767
Exp. minX	-32767

Test settings	
Tolerance gainX	±0,0000e+00
Tolerance maskY	±0,0000e+00
Tolerance maskX	±0,0000e+00
Tolerance Table	±0,0000e+00
Tolerance gainY	±0,0000e+00
Tolerance maxY	±0,0000e+00
Tolerance maxX	±0,0000e+00
Tolerance sfrX	±0,0000e+00
Tolerance sfrY	±0,0000e+00
Tolerance offsetX	±0,0000e+00
Tolerance sizeX	±0,0000e+00
Tolerance offsetY	±0,0000e+00
Tolerance minY	±0,0000e+00
Tolerance minX	±0,0000e+00
Tolerance gainXsfr	±0,0000e+00
Tolerance idxOffsetY	±0,0000e+00
Tolerance idxOffsetX	±0,0000e+00
Tolerance gainYsfr	±0,0000e+00

Verification: LookupTable2D FiP16 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for General block LookupTable2D.

Test results						
Time step	1	2	3	4	...	67
CPU cycles	207	207	207	207	...	188
Inputs						
x (DSP)	-32768	-31775	-30782	-29789	...	32767
y (DSP)	26214	25370	24526	23682	...	-29491
x	-1	-0.97	-0.939	-0.909	...	1
y	0.8	0.774	0.748	0.723	...	-0.9
Parameters						
TableData	[1x561]					
DimX	17					
x_min	-0.8					
x_max	0.7					
DimY	33					
y_min	-0.6					
y_max	0.9					
Outputs						
Out	-0	-0.013	-0.026	-0.039	...	0.05
Exp. Out	0	-0.013	-0.026	-0.039	...	0.05
Out (DSP)	-1	-423	-845	-1267	...	1637
Exp. Out (DSP)	0	-422	-844	-1266	...	1638

Test settings	
Tolerance Out	±9,1553e-05 (±3 LSB)

Test statistics	
Min CPU cycles	188
Max CPU cycles	287
Avg CPU cycles	220

Test case: Conversion test OK

Conversion test for General block LookupTable2D.

Test results	
Time step	1
Mask parameters	
TableData	[1x561]
DimX	33
x_min	-1
x_max	1
DimY	17
y_min	-1
y_max	1
Controller parameters	
gainX	16384
maskY	4095
maskX	2047
Table	[1x561]
gainY	16384
maxY	32767
maxX	32767
sfrX	11
sfrY	12
offsetX	0
sizeX	33
offsetY	0
minY	-32767
minX	-32767
gainXsfr	14
idxOffsetY	8
idxOffsetX	16
gainYsfr	14
Exp. gainX	16384
Exp. maskY	4095
Exp. maskX	2047
Exp. Table	[1x561]
Exp. gainY	16384
Exp. maxY	32767
Exp. maxX	32767
Exp. sfrX	11
Exp. sfrY	12
Exp. offsetX	0
Exp. sizeX	33
Exp. offsetY	0
Exp. minY	-32767
Exp. minX	-32767

Test settings	
Tolerance gainX	±0,0000e+00
Tolerance maskY	±0,0000e+00
Tolerance maskX	±0,0000e+00
Tolerance Table	±0,0000e+00
Tolerance gainY	±0,0000e+00
Tolerance maxY	±0,0000e+00
Tolerance maxX	±0,0000e+00
Tolerance sfrX	±0,0000e+00
Tolerance sfrY	±0,0000e+00
Tolerance offsetX	±0,0000e+00
Tolerance sizeX	±0,0000e+00
Tolerance offsetY	±0,0000e+00
Tolerance minY	±0,0000e+00
Tolerance minX	±0,0000e+00
Tolerance gainXsfr	±0,0000e+00
Tolerance idxOffsetY	±0,0000e+00
Tolerance idxOffsetX	±0,0000e+00
Tolerance gainYsfr	±0,0000e+00

Verification: LookupTable2D FiP16 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for General block LookupTable2D.

Test results						
Time step	1	2	3	4	...	67
CPU cycles	124	124	124	124	...	113
Inputs						
x (DSP)	-32768	-31775	-30782	-29789	...	32767
y (DSP)	26214	25370	24526	23682	...	-29491
x	-1	-0.97	-0.939	-0.909	...	1
y	0.8	0.774	0.748	0.723	...	-0.9
Parameters						
TableData	[1x561]					
DimX	17					
x_min	-0.8					
x_max	0.7					
DimY	33					
y_min	-0.6					
y_max	0.9					
Outputs						
Out	-0	-0.013	-0.026	-0.039	...	0.05
Exp. Out	0	-0.013	-0.026	-0.039	...	0.05
Out (DSP)	-1	-423	-845	-1267	...	1637
Exp. Out (DSP)	0	-422	-844	-1266	...	1638

Test settings	
Tolerance Out	±9,1553e-05 (±3 LSB)

Test statistics	
Min CPU cycles	113
Max CPU cycles	142
Avg CPU cycles	135

Test case: Conversion test OK

Conversion test for General block LookupTable2D.

Test results	
Time step	1
Mask parameters	
TableData	[1x561]
DimX	33
x_min	-1
x_max	1
DimY	17
y_min	-1
y_max	1
Controller parameters	
gainX	16384
maskY	4095
maskX	2047
Table	[1x561]
gainY	16384
maxY	32767
maxX	32767
sfrX	11
sfrY	12
offsetX	0
sizeX	33
offsetY	0
minY	-32767
minX	-32767
gainXsfr	14
idxOffsetY	8
idxOffsetX	16
gainYsfr	14
Exp. gainX	16384
Exp. maskY	4095
Exp. maskX	2047
Exp. Table	[1x561]
Exp. gainY	16384
Exp. maxY	32767
Exp. maxX	32767
Exp. sfrX	11
Exp. sfrY	12
Exp. offsetX	0
Exp. sizeX	33
Exp. offsetY	0
Exp. minY	-32767
Exp. minX	-32767

Test settings	
Tolerance gainX	±0,0000e+00
Tolerance maskY	±0,0000e+00
Tolerance maskX	±0,0000e+00
Tolerance Table	±0,0000e+00
Tolerance gainY	±0,0000e+00
Tolerance maxY	±0,0000e+00
Tolerance maxX	±0,0000e+00
Tolerance sfrX	±0,0000e+00
Tolerance sfrY	±0,0000e+00
Tolerance offsetX	±0,0000e+00
Tolerance sizeX	±0,0000e+00
Tolerance offsetY	±0,0000e+00
Tolerance minY	±0,0000e+00
Tolerance minX	±0,0000e+00
Tolerance gainXsfr	±0,0000e+00
Tolerance idxOffsetY	±0,0000e+00
Tolerance idxOffsetX	±0,0000e+00
Tolerance gainYsfr	±0,0000e+00

Verification: LookupTable2D FiP16 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for General block LookupTable2D.

Test results						
Time step	1	2	3	4	...	67
CPU cycles	249	249	249	249	...	223
Inputs						
x (DSP)	-32768	-31775	-30782	-29789	...	32767
y (DSP)	26214	25370	24526	23682	...	-29491
x	-1	-0.97	-0.939	-0.909	...	1
y	0.8	0.774	0.748	0.723	...	-0.9
Parameters						
TableData	[1x561]					
DimX	17					
x_min	-0.8					
x_max	0.7					
DimY	33					
y_min	-0.6					
y_max	0.9					
Outputs						
Out	-0	-0.013	-0.026	-0.039	...	0.05
Exp. Out	0	-0.013	-0.026	-0.039	...	0.05
Out (DSP)	-1	-423	-845	-1267	...	1637
Exp. Out (DSP)	0	-422	-844	-1266	...	1638

Test settings	
Tolerance Out	±9,1553e-05 (±3 LSB)

Test statistics	
Min CPU cycles	223
Max CPU cycles	275
Avg CPU cycles	263

Test case: Conversion test OK

Conversion test for General block LookupTable2D.

Test results	
Time step	1
Mask parameters	
TableData	[1x561]
DimX	33
x_min	-1
x_max	1
DimY	17
y_min	-1
y_max	1
Controller parameters	
gainX	16384
maskY	4095
maskX	2047
Table	[1x561]
gainY	16384
maxY	32767
maxX	32767
sfrX	11
sfrY	12
offsetX	0
sizeX	33
offsetY	0
minY	-32767
minX	-32767
gainXsfr	14
idxOffsetY	8
idxOffsetX	16
gainYsfr	14
Exp. gainX	16384
Exp. maskY	4095
Exp. maskX	2047
Exp. Table	[1x561]
Exp. gainY	16384
Exp. maxY	32767
Exp. maxX	32767
Exp. sfrX	11
Exp. sfrY	12
Exp. offsetX	0
Exp. sizeX	33
Exp. offsetY	0
Exp. minY	-32767
Exp. minX	-32767

Test settings	
Tolerance gainX	±0,0000e+00
Tolerance maskY	±0,0000e+00
Tolerance maskX	±0,0000e+00
Tolerance Table	±0,0000e+00
Tolerance gainY	±0,0000e+00
Tolerance maxY	±0,0000e+00
Tolerance maxX	±0,0000e+00
Tolerance sfrX	±0,0000e+00
Tolerance sfrY	±0,0000e+00
Tolerance offsetX	±0,0000e+00
Tolerance sizeX	±0,0000e+00
Tolerance offsetY	±0,0000e+00
Tolerance minY	±0,0000e+00
Tolerance minX	±0,0000e+00
Tolerance gainXsfr	±0,0000e+00
Tolerance idxOffsetY	±0,0000e+00
Tolerance idxOffsetX	±0,0000e+00
Tolerance gainYsfr	±0,0000e+00

Verification: LookupTable2D FiP16 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for General block LookupTable2D.

Test results						
Time step	1	2	3	4	...	67
CPU cycles	232	178	178	178	...	169
Inputs						
x (DSP)	-32768	-31775	-30782	-29789	...	32767
y (DSP)	26214	25370	24526	23682	...	-29491
x	-1	-0.97	-0.939	-0.909	...	1
y	0.8	0.774	0.748	0.723	...	-0.9
Parameters						
TableData	[1x561]					
DimX	17					
x_min	-0.8					
x_max	0.7					
DimY	33					
y_min	-0.6					
y_max	0.9					
Outputs						
Out	-0	-0.013	-0.026	-0.039	...	0.05
Exp. Out	0	-0.013	-0.026	-0.039	...	0.05
Out (DSP)	-1	-423	-845	-1267	...	1637
Exp. Out (DSP)	0	-422	-844	-1266	...	1638

Test settings	
Tolerance Out	±9,1553e-05 (±3 LSB)

Test statistics	
Min CPU cycles	169
Max CPU cycles	232
Avg CPU cycles	183

Test case: Conversion test OK

Conversion test for General block LookupTable2D.

Test results	
Time step	1
Mask parameters	
TableData	[1x561]
DimX	33
x_min	-1
x_max	1
DimY	17
y_min	-1
y_max	1
Controller parameters	
gainX	16384
maskY	4095
maskX	2047
Table	[1x561]
gainY	16384
maxY	32767
maxX	32767
sfrX	11
sfrY	12
offsetX	0
sizeX	33
offsetY	0
minY	-32767
minX	-32767
gainXsfr	14
idxOffsetY	8
idxOffsetX	16
gainYsfr	14
Exp. gainX	16384
Exp. maskY	4095
Exp. maskX	2047
Exp. Table	[1x561]
Exp. gainY	16384
Exp. maxY	32767
Exp. maxX	32767
Exp. sfrX	11
Exp. sfrY	12
Exp. offsetX	0
Exp. sizeX	33
Exp. offsetY	0
Exp. minY	-32767
Exp. minX	-32767

Test settings	
Tolerance gainX	±0,0000e+00
Tolerance maskY	±0,0000e+00
Tolerance maskX	±0,0000e+00
Tolerance Table	±0,0000e+00
Tolerance gainY	±0,0000e+00
Tolerance maxY	±0,0000e+00
Tolerance maxX	±0,0000e+00
Tolerance sfrX	±0,0000e+00
Tolerance sfrY	±0,0000e+00
Tolerance offsetX	±0,0000e+00
Tolerance sizeX	±0,0000e+00
Tolerance offsetY	±0,0000e+00
Tolerance minY	±0,0000e+00
Tolerance minX	±0,0000e+00
Tolerance gainXsfr	±0,0000e+00
Tolerance idxOffsetY	±0,0000e+00
Tolerance idxOffsetX	±0,0000e+00
Tolerance gainYsfr	±0,0000e+00

Verification: LookupTable2D FiP16 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for General block LookupTable2D.

Test results						
Time step	1	2	3	4	...	67
CPU cycles	197	197	197	197	...	198
Inputs						
x (DSP)	-32768	-31775	-30782	-29789	...	32767
y (DSP)	26214	25370	24526	23682	...	-29491
x	-1	-0.97	-0.939	-0.909	...	1
y	0.8	0.774	0.748	0.723	...	-0.9
Parameters						
TableData	[1x561]					
DimX	17					
x_min	-0.8					
x_max	0.7					
DimY	33					
y_min	-0.6					
y_max	0.9					
Outputs						
Out	-0	-0.013	-0.026	-0.039	...	0.05
Exp. Out	0	-0.013	-0.026	-0.039	...	0.05
Out (DSP)	-1	-423	-845	-1267	...	1637
Exp. Out (DSP)	0	-422	-844	-1266	...	1638

Test settings	
Tolerance Out	±9,1553e-05 (±3 LSB)

Test statistics	
Min CPU cycles	197
Max CPU cycles	217
Avg CPU cycles	209

Test case: Conversion test OK

Conversion test for General block LookupTable2D.

Test results	
Time step	1
Mask parameters	
TableData	[1x561]
DimX	33
x_min	-1
x_max	1
DimY	17
y_min	-1
y_max	1
Controller parameters	
gainX	16384
maskY	4095
maskX	2047
Table	[1x561]
gainY	16384
maxY	32767
maxX	32767
sfrX	11
sfrY	12
offsetX	0
sizeX	33
offsetY	0
minY	-32767
minX	-32767
gainXsfr	14
idxOffsetY	8
idxOffsetX	16
gainYsfr	14
Exp. gainX	16384
Exp. maskY	4095
Exp. maskX	2047
Exp. Table	[1x561]
Exp. gainY	16384
Exp. maxY	32767
Exp. maxX	32767
Exp. sfrX	11
Exp. sfrY	12
Exp. offsetX	0
Exp. sizeX	33
Exp. offsetY	0
Exp. minY	-32767
Exp. minX	-32767

Test settings	
Tolerance gainX	±0,0000e+00
Tolerance maskY	±0,0000e+00
Tolerance maskX	±0,0000e+00
Tolerance Table	±0,0000e+00
Tolerance gainY	±0,0000e+00
Tolerance maxY	±0,0000e+00
Tolerance maxX	±0,0000e+00
Tolerance sfrX	±0,0000e+00
Tolerance sfrY	±0,0000e+00
Tolerance offsetX	±0,0000e+00
Tolerance sizeX	±0,0000e+00
Tolerance offsetY	±0,0000e+00
Tolerance minY	±0,0000e+00
Tolerance minX	±0,0000e+00
Tolerance gainXsfr	±0,0000e+00
Tolerance idxOffsetY	±0,0000e+00
Tolerance idxOffsetX	±0,0000e+00
Tolerance gainYsfr	±0,0000e+00

Verification: LookupTable2D FiP32 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for General block LookupTable2D.

Test results				
Time step	1	2	...	67
CPU cycles	312	312	...	294
Inputs				
x (DSP)	-2147483648	-2082408386	...	2147483647
y (DSP)	1717986918	1662672946	...	-1932735283
x	-1	-0.97	...	1
y	0.8	0.774	...	-0.9
Parameters				
TableData	[1x561]			
DimX	17			
x_min	-0.8			
x_max	0.7			
DimY	33			
y_min	-0.6			
y_max	0.9			
Outputs				
Out	-0	-0.013	...	0.05
Exp. Out	0	-0.013	...	0.05
Out (DSP)	-1	-27656987	...	107374181
Exp. Out (DSP)	0	-27656986	...	107374182

Test settings	
Tolerance Out	±2,3283e-09 (±5 LSB)

Test statistics	
Min CPU cycles	294
Max CPU cycles	342
Avg CPU cycles	330

Test case: Conversion test OK

Conversion test for General block LookupTable2D.

Test results	
Time step	1
Mask parameters	
TableData	[1x561]
DimX	33
x_min	-0.8
x_max	0.7
DimY	17
y_min	-0.6
y_max	0.9
Controller parameters	
gainX	1431655765
maskY	268435455
maskX	134217727
Table	[1x561]
gainY	1431655765
maxY	1932735283
maxX	1503238554
sfrX	27
sfrY	28
offsetX	-107374182
sizeX	33
offsetY	322122547
minY	-1288490189
minX	-1717986918
gainXsfr	30
idxOffsetY	8
idxOffsetX	16
gainYsfr	30
Exp. gainX	1431655765
Exp. maskY	268435455
Exp. maskX	134217727
Exp. Table	[1x561]
Exp. gainY	1431655765
Exp. maxY	1932735283
Exp. maxX	1503238554
Exp. sfrX	27
Exp. sfrY	28
Exp. offsetX	-107374182
Exp. sizeX	33
Exp. offsetY	322122547
Exp. minY	-1288490189
Exp. minX	-1717986918

Test settings	
Tolerance gainX	±0,0000e+00
Tolerance maskY	±0,0000e+00
Tolerance maskX	±0,0000e+00
Tolerance Table	±0,0000e+00
Tolerance gainY	±0,0000e+00
Tolerance maxY	±0,0000e+00
Tolerance maxX	±0,0000e+00
Tolerance sfrX	±0,0000e+00
Tolerance sfrY	±0,0000e+00
Tolerance offsetX	±0,0000e+00
Tolerance sizeX	±0,0000e+00
Tolerance offsetY	±0,0000e+00
Tolerance minY	±0,0000e+00
Tolerance minX	±0,0000e+00
Tolerance gainXsfr	±0,0000e+00
Tolerance idxOffsetY	±0,0000e+00
Tolerance idxOffsetX	±0,0000e+00
Tolerance gainYsfr	±0,0000e+00

Verification: LookupTable2D FiP32 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for General block LookupTable2D.

Test results				
Time step	1	2	...	67
CPU cycles	401	401	...	345
Inputs				
x (DSP)	-2147483648	-2082408386	...	2147483647
y (DSP)	1717986918	1662672946	...	-1932735283
x	-1	-0.97	...	1
y	0.8	0.774	...	-0.9
Parameters				
TableData	[1x561]			
DimX	17			
x_min	-0.8			
x_max	0.7			
DimY	33			
y_min	-0.6			
y_max	0.9			
Outputs				
Out	-0	-0.013	...	0.05
Exp. Out	0	-0.013	...	0.05
Out (DSP)	-1	-27656987	...	107374181
Exp. Out (DSP)	0	-27656986	...	107374182

Test settings	
Tolerance Out	±2,3283e-09 (±5 LSB)

Test statistics	
Min CPU cycles	345
Max CPU cycles	463
Avg CPU cycles	437

Test case: Conversion test OK

Conversion test for General block LookupTable2D.

Test results	
Time step	1
Mask parameters	
TableData	[1x561]
DimX	33
x_min	-0.8
x_max	0.7
DimY	17
y_min	-0.6
y_max	0.9
Controller parameters	
gainX	1431655765
maskY	268435455
maskX	134217727
Table	[1x561]
gainY	1431655765
maxY	1932735283
maxX	1503238554
sfrX	27
sfrY	28
offsetX	-107374182
sizeX	33
offsetY	322122547
minY	-1288490189
minX	-1717986918
gainXsfr	30
idxOffsetY	8
idxOffsetX	16
gainYsfr	30
Exp. gainX	1431655765
Exp. maskY	268435455
Exp. maskX	134217727
Exp. Table	[1x561]
Exp. gainY	1431655765
Exp. maxY	1932735283
Exp. maxX	1503238554
Exp. sfrX	27
Exp. sfrY	28
Exp. offsetX	-107374182
Exp. sizeX	33
Exp. offsetY	322122547
Exp. minY	-1288490189
Exp. minX	-1717986918

Test settings	
Tolerance gainX	±0,0000e+00
Tolerance maskY	±0,0000e+00
Tolerance maskX	±0,0000e+00
Tolerance Table	±0,0000e+00
Tolerance gainY	±0,0000e+00
Tolerance maxY	±0,0000e+00
Tolerance maxX	±0,0000e+00
Tolerance sfrX	±0,0000e+00
Tolerance sfrY	±0,0000e+00
Tolerance offsetX	±0,0000e+00
Tolerance sizeX	±0,0000e+00
Tolerance offsetY	±0,0000e+00
Tolerance minY	±0,0000e+00
Tolerance minX	±0,0000e+00
Tolerance gainXsfr	±0,0000e+00
Tolerance idxOffsetY	±0,0000e+00
Tolerance idxOffsetX	±0,0000e+00
Tolerance gainYsfr	±0,0000e+00

Verification: LookupTable2D FiP32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for General block LookupTable2D.

Test results				
Time step	1	2	...	67
CPU cycles	374	374	...	321
Inputs				
x (DSP)	-2147483648	-2082408386	...	2147483647
y (DSP)	1717986918	1662672946	...	-1932735283
x	-1	-0.97	...	1
y	0.8	0.774	...	-0.9
Parameters				
TableData	[1x561]			
DimX	17			
x_min	-0.8			
x_max	0.7			
DimY	33			
y_min	-0.6			
y_max	0.9			
Outputs				
Out	-0	-0.013	...	0.05
Exp. Out	0	-0.013	...	0.05
Out (DSP)	-1	-27656987	...	107374181
Exp. Out (DSP)	0	-27656986	...	107374182

Test settings	
Tolerance Out	±2,3283e-09 (±5 LSB)

Test statistics	
Min CPU cycles	321
Max CPU cycles	412
Avg CPU cycles	393

Test case: Conversion test OK

Conversion test for General block LookupTable2D.

Test results	
Time step	1
Mask parameters	
TableData	[1x561]
DimX	33
x_min	-0.8
x_max	0.7
DimY	17
y_min	-0.6
y_max	0.9
Controller parameters	
gainX	1431655765
maskY	268435455
maskX	134217727
Table	[1x561]
gainY	1431655765
maxY	1932735283
maxX	1503238554
sfrX	27
sfrY	28
offsetX	-107374182
sizeX	33
offsetY	322122547
minY	-1288490189
minX	-1717986918
gainXsfr	30
idxOffsetY	8
idxOffsetX	16
gainYsfr	30
Exp. gainX	1431655765
Exp. maskY	268435455
Exp. maskX	134217727
Exp. Table	[1x561]
Exp. gainY	1431655765
Exp. maxY	1932735283
Exp. maxX	1503238554
Exp. sfrX	27
Exp. sfrY	28
Exp. offsetX	-107374182
Exp. sizeX	33
Exp. offsetY	322122547
Exp. minY	-1288490189
Exp. minX	-1717986918

Test settings	
Tolerance gainX	±0,0000e+00
Tolerance maskY	±0,0000e+00
Tolerance maskX	±0,0000e+00
Tolerance Table	±0,0000e+00
Tolerance gainY	±0,0000e+00
Tolerance maxY	±0,0000e+00
Tolerance maxX	±0,0000e+00
Tolerance sfrX	±0,0000e+00
Tolerance sfrY	±0,0000e+00
Tolerance offsetX	±0,0000e+00
Tolerance sizeX	±0,0000e+00
Tolerance offsetY	±0,0000e+00
Tolerance minY	±0,0000e+00
Tolerance minX	±0,0000e+00
Tolerance gainXsfr	±0,0000e+00
Tolerance idxOffsetY	±0,0000e+00
Tolerance idxOffsetX	±0,0000e+00
Tolerance gainYsfr	±0,0000e+00

Verification: LookupTable2D FiP32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for General block LookupTable2D.

Test results				
Time step	1	2	...	67
CPU cycles	737	737	...	632
Inputs				
x (DSP)	-2147483648	-2082408386	...	2147483647
y (DSP)	1717986918	1662672946	...	-1932735283
x	-1	-0.97	...	1
y	0.8	0.774	...	-0.9
Parameters				
TableData	[1x561]			
DimX	17			
x_min	-0.8			
x_max	0.7			
DimY	33			
y_min	-0.6			
y_max	0.9			
Outputs				
Out	-0	-0.013	...	0.05
Exp. Out	0	-0.013	...	0.05
Out (DSP)	-1	-27656987	...	107374181
Exp. Out (DSP)	0	-27656986	...	107374182

Test settings	
Tolerance Out	±2,3283e-09 (±5 LSB)

Test statistics	
Min CPU cycles	632
Max CPU cycles	899
Avg CPU cycles	797

Test case: Conversion test OK

Conversion test for General block LookupTable2D.

Test results	
Time step	1
Mask parameters	
TableData	[1x561]
DimX	33
x_min	-0.8
x_max	0.7
DimY	17
y_min	-0.6
y_max	0.9
Controller parameters	
gainX	1431655765
maskY	268435455
maskX	134217727
Table	[1x561]
gainY	1431655765
maxY	1932735283
maxX	1503238554
sfrX	27
sfrY	28
offsetX	-107374182
sizeX	33
offsetY	322122547
minY	-1288490189
minX	-1717986918
gainXsfr	30
idxOffsetY	8
idxOffsetX	16
gainYsfr	30
Exp. gainX	1431655765
Exp. maskY	268435455
Exp. maskX	134217727
Exp. Table	[1x561]
Exp. gainY	1431655765
Exp. maxY	1932735283
Exp. maxX	1503238554
Exp. sfrX	27
Exp. sfrY	28
Exp. offsetX	-107374182
Exp. sizeX	33
Exp. offsetY	322122547
Exp. minY	-1288490189
Exp. minX	-1717986918

Test settings	
Tolerance gainX	±0,0000e+00
Tolerance maskY	±0,0000e+00
Tolerance maskX	±0,0000e+00
Tolerance Table	±0,0000e+00
Tolerance gainY	±0,0000e+00
Tolerance maxY	±0,0000e+00
Tolerance maxX	±0,0000e+00
Tolerance sfrX	±0,0000e+00
Tolerance sfrY	±0,0000e+00
Tolerance offsetX	±0,0000e+00
Tolerance sizeX	±0,0000e+00
Tolerance offsetY	±0,0000e+00
Tolerance minY	±0,0000e+00
Tolerance minX	±0,0000e+00
Tolerance gainXsfr	±0,0000e+00
Tolerance idxOffsetY	±0,0000e+00
Tolerance idxOffsetX	±0,0000e+00
Tolerance gainYsfr	±0,0000e+00

Verification: LookupTable2D FiP32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for General block LookupTable2D.

Test results				
Time step	1	2	...	67
CPU cycles	267	267	...	234
Inputs				
x (DSP)	-2147483648	-2082408386	...	2147483647
y (DSP)	1717986918	1662672946	...	-1932735283
x	-1	-0.97	...	1
y	0.8	0.774	...	-0.9
Parameters				
TableData	[1x561]			
DimX	17			
x_min	-0.8			
x_max	0.7			
DimY	33			
y_min	-0.6			
y_max	0.9			
Outputs				
Out	-0	-0.013	...	0.05
Exp. Out	0	-0.013	...	0.05
Out (DSP)	-1	-27656987	...	107374181
Exp. Out (DSP)	0	-27656986	...	107374182

Test settings	
Tolerance Out	±2,3283e-09 (±5 LSB)

Test statistics	
Min CPU cycles	234
Max CPU cycles	307
Avg CPU cycles	290

Test case: Conversion test OK

Conversion test for General block LookupTable2D.

Test results	
Time step	1
Mask parameters	
TableData	[1x561]
DimX	33
x_min	-0.8
x_max	0.7
DimY	17
y_min	-0.6
y_max	0.9
Controller parameters	
gainX	1431655765
maskY	268435455
maskX	134217727
Table	[1x561]
gainY	1431655765
maxY	1932735283
maxX	1503238554
sfrX	27
sfrY	28
offsetX	-107374182
sizeX	33
offsetY	322122547
minY	-1288490189
minX	-1717986918
gainXsfr	30
idxOffsetY	8
idxOffsetX	16
gainYsfr	30
Exp. gainX	1431655765
Exp. maskY	268435455
Exp. maskX	134217727
Exp. Table	[1x561]
Exp. gainY	1431655765
Exp. maxY	1932735283
Exp. maxX	1503238554
Exp. sfrX	27
Exp. sfrY	28
Exp. offsetX	-107374182
Exp. sizeX	33
Exp. offsetY	322122547
Exp. minY	-1288490189
Exp. minX	-1717986918

Test settings	
Tolerance gainX	±0,0000e+00
Tolerance maskY	±0,0000e+00
Tolerance maskX	±0,0000e+00
Tolerance Table	±0,0000e+00
Tolerance gainY	±0,0000e+00
Tolerance maxY	±0,0000e+00
Tolerance maxX	±0,0000e+00
Tolerance sfrX	±0,0000e+00
Tolerance sfrY	±0,0000e+00
Tolerance offsetX	±0,0000e+00
Tolerance sizeX	±0,0000e+00
Tolerance offsetY	±0,0000e+00
Tolerance minY	±0,0000e+00
Tolerance minX	±0,0000e+00
Tolerance gainXsfr	±0,0000e+00
Tolerance idxOffsetY	±0,0000e+00
Tolerance idxOffsetX	±0,0000e+00
Tolerance gainYsfr	±0,0000e+00

Verification: LookupTable2D FiP32 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for General block LookupTable2D.

Test results				
Time step	1	2	...	67
CPU cycles	2269	2269	...	1853
Inputs				
x (DSP)	-2147483648	-2082408386	...	2147483647
y (DSP)	1717986918	1662672946	...	-1932735283
x	-1	-0.97	...	1
y	0.8	0.774	...	-0.9
Parameters				
TableData	[1x561]			
DimX	17			
x_min	-0.8			
x_max	0.7			
DimY	33			
y_min	-0.6			
y_max	0.9			
Outputs				
Out	-0	-0.013	...	0.05
Exp. Out	0	-0.013	...	0.05
Out (DSP)	-1	-27656987	...	107374181
Exp. Out (DSP)	0	-27656986	...	107374182

Test settings	
Tolerance Out	±2,3283e-09 (±5 LSB)

Test statistics	
Min CPU cycles	1853
Max CPU cycles	2702
Avg CPU cycles	2512

Test case: Conversion test OK

Conversion test for General block LookupTable2D.

Test results	
Time step	1
Mask parameters	
TableData	[1x561]
DimX	33
x_min	-0.8
x_max	0.7
DimY	17
y_min	-0.6
y_max	0.9
Controller parameters	
gainX	1431655765
maskY	268435455
maskX	134217727
Table	[1x561]
gainY	1431655765
maxY	1932735283
maxX	1503238554
sfrX	27
sfrY	28
offsetX	-107374182
sizeX	33
offsetY	322122547
minY	-1288490189
minX	-1717986918
gainXsfr	30
idxOffsetY	8
idxOffsetX	16
gainYsfr	30
Exp. gainX	1431655765
Exp. maskY	268435455
Exp. maskX	134217727
Exp. Table	[1x561]
Exp. gainY	1431655765
Exp. maxY	1932735283
Exp. maxX	1503238554
Exp. sfrX	27
Exp. sfrY	28
Exp. offsetX	-107374182
Exp. sizeX	33
Exp. offsetY	322122547
Exp. minY	-1288490189
Exp. minX	-1717986918

Test settings	
Tolerance gainX	±0,0000e+00
Tolerance maskY	±0,0000e+00
Tolerance maskX	±0,0000e+00
Tolerance Table	±0,0000e+00
Tolerance gainY	±0,0000e+00
Tolerance maxY	±0,0000e+00
Tolerance maxX	±0,0000e+00
Tolerance sfrX	±0,0000e+00
Tolerance sfrY	±0,0000e+00
Tolerance offsetX	±0,0000e+00
Tolerance sizeX	±0,0000e+00
Tolerance offsetY	±0,0000e+00
Tolerance minY	±0,0000e+00
Tolerance minX	±0,0000e+00
Tolerance gainXsfr	±0,0000e+00
Tolerance idxOffsetY	±0,0000e+00
Tolerance idxOffsetX	±0,0000e+00
Tolerance gainYsfr	±0,0000e+00

Verification: LookupTable2D FiP32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for General block LookupTable2D.

Test results				
Time step	1	2	...	67
CPU cycles	396	317	...	298
Inputs				
x (DSP)	-2147483648	-2082408386	...	2147483647
y (DSP)	1717986918	1662672946	...	-1932735283
x	-1	-0.97	...	1
y	0.8	0.774	...	-0.9
Parameters				
TableData	[1x561]			
DimX	17			
x_min	-0.8			
x_max	0.7			
DimY	33			
y_min	-0.6			
y_max	0.9			
Outputs				
Out	-0	-0.013	...	0.05
Exp. Out	0	-0.013	...	0.05
Out (DSP)	-1	-27656987	...	107374181
Exp. Out (DSP)	0	-27656986	...	107374182

Test settings	
Tolerance Out	±2,3283e-09 (±5 LSB)

Test statistics	
Min CPU cycles	298
Max CPU cycles	396
Avg CPU cycles	330

Test case: Conversion test OK

Conversion test for General block LookupTable2D.

Test results	
Time step	1
Mask parameters	
TableData	[1x561]
DimX	33
x_min	-0.8
x_max	0.7
DimY	17
y_min	-0.6
y_max	0.9
Controller parameters	
gainX	1431655765
maskY	268435455
maskX	134217727
Table	[1x561]
gainY	1431655765
maxY	1932735283
maxX	1503238554
sfrX	27
sfrY	28
offsetX	-107374182
sizeX	33
offsetY	322122547
minY	-1288490189
minX	-1717986918
gainXsfr	30
idxOffsetY	8
idxOffsetX	16
gainYsfr	30
Exp. gainX	1431655765
Exp. maskY	268435455
Exp. maskX	134217727
Exp. Table	[1x561]
Exp. gainY	1431655765
Exp. maxY	1932735283
Exp. maxX	1503238554
Exp. sfrX	27
Exp. sfrY	28
Exp. offsetX	-107374182
Exp. sizeX	33
Exp. offsetY	322122547
Exp. minY	-1288490189
Exp. minX	-1717986918

Test settings	
Tolerance gainX	±0,0000e+00
Tolerance maskY	±0,0000e+00
Tolerance maskX	±0,0000e+00
Tolerance Table	±0,0000e+00
Tolerance gainY	±0,0000e+00
Tolerance maxY	±0,0000e+00
Tolerance maxX	±0,0000e+00
Tolerance sfrX	±0,0000e+00
Tolerance sfrY	±0,0000e+00
Tolerance offsetX	±0,0000e+00
Tolerance sizeX	±0,0000e+00
Tolerance offsetY	±0,0000e+00
Tolerance minY	±0,0000e+00
Tolerance minX	±0,0000e+00
Tolerance gainXsfr	±0,0000e+00
Tolerance idxOffsetY	±0,0000e+00
Tolerance idxOffsetX	±0,0000e+00
Tolerance gainYsfr	±0,0000e+00

Verification: LookupTable2D FiP32 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for General block LookupTable2D.

Test results				
Time step	1	2	...	67
CPU cycles	287	287	...	276
Inputs				
x (DSP)	-2147483648	-2082408386	...	2147483647
y (DSP)	1717986918	1662672946	...	-1932735283
x	-1	-0.97	...	1
y	0.8	0.774	...	-0.9
Parameters				
TableData	[1x561]			
DimX	17			
x_min	-0.8			
x_max	0.7			
DimY	33			
y_min	-0.6			
y_max	0.9			
Outputs				
Out	-0	-0.013	...	0.05
Exp. Out	0	-0.013	...	0.05
Out (DSP)	-1	-27656987	...	107374181
Exp. Out (DSP)	0	-27656986	...	107374182

Test settings	
Tolerance Out	±2,3283e-09 (±5 LSB)

Test statistics	
Min CPU cycles	276
Max CPU cycles	324
Avg CPU cycles	309

Test case: Conversion test OK

Conversion test for General block LookupTable2D.

Test results	
Time step	1
Mask parameters	
TableData	[1x561]
DimX	33
x_min	-0.8
x_max	0.7
DimY	17
y_min	-0.6
y_max	0.9
Controller parameters	
gainX	1431655765
maskY	268435455
maskX	134217727
Table	[1x561]
gainY	1431655765
maxY	1932735283
maxX	1503238554
sfrX	27
sfrY	28
offsetX	-107374182
sizeX	33
offsetY	322122547
minY	-1288490189
minX	-1717986918
gainXsfr	30
idxOffsetY	8
idxOffsetX	16
gainYsfr	30
Exp. gainX	1431655765
Exp. maskY	268435455
Exp. maskX	134217727
Exp. Table	[1x561]
Exp. gainY	1431655765
Exp. maxY	1932735283
Exp. maxX	1503238554
Exp. sfrX	27
Exp. sfrY	28
Exp. offsetX	-107374182
Exp. sizeX	33
Exp. offsetY	322122547
Exp. minY	-1288490189
Exp. minX	-1717986918

Test settings	
Tolerance gainX	±0,0000e+00
Tolerance maskY	±0,0000e+00
Tolerance maskX	±0,0000e+00
Tolerance Table	±0,0000e+00
Tolerance gainY	±0,0000e+00
Tolerance maxY	±0,0000e+00
Tolerance maxX	±0,0000e+00
Tolerance sfrX	±0,0000e+00
Tolerance sfrY	±0,0000e+00
Tolerance offsetX	±0,0000e+00
Tolerance sizeX	±0,0000e+00
Tolerance offsetY	±0,0000e+00
Tolerance minY	±0,0000e+00
Tolerance minX	±0,0000e+00
Tolerance gainXsfr	±0,0000e+00
Tolerance idxOffsetY	±0,0000e+00
Tolerance idxOffsetX	±0,0000e+00
Tolerance gainYsfr	±0,0000e+00

Verification: LookupTable2D Float32 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for General block LookupTable2D.

Test results				
Time step	1	2	...	67
CPU cycles	185	185	...	186
Inputs				
x (DSP)	-1.1	-1.067	...	1.1
y (DSP)	1.2	1.161	...	-1.35
x	-1.1	-1.067	...	1.1
y	1.2	1.161	...	-1.35
Parameters				
TableData	[1x561]			
DimX	17			
x_min	-0.8			
x_max	0.7			
DimY	33			
y_min	-0.6			
y_max	0.9			
Outputs				
Out	0.155	0.155	...	0.155
Exp. Out	0.155	0.155	...	0.155
Out (DSP)	0.155	0.155	...	0.155
Exp. Out (DSP)	0.155	0.155	...	0.155

Test settings	
Tolerance Out	±4,6566e-07 (±1000 LSB)

Test statistics	
Min CPU cycles	185
Max CPU cycles	186
Avg CPU cycles	185

Test case: Conversion test OK

Conversion test for General block LookupTable2D.

Test results	
Time step	1
Mask parameters	
TableData	[1x561]
DimX	33
x_min	-0.8
x_max	0.7
DimY	17
y_min	-0.6
y_max	0.9
Controller parameters	
gainX	21.333
offsetX	-0.8
Table	[1x561]
gainY	10.667
offsetY	-0.6
minY	-0.6
minX	-0.8
maxY	0.9
maxX	0.7
dimY	16
dimX	32
Exp. gainX	21.333
Exp. offsetX	-0.8
Exp. Table	[1x561]
Exp. gainY	10.667
Exp. offsetY	-0.6
Exp. minY	-0.6
Exp. minX	-0.8
Exp. maxY	0.9
Exp. maxX	0.7
Exp. dimY	16
Exp. dimX	32

Test settings	
Tolerance gainX	±0,0000e+00
Tolerance offsetX	±0,0000e+00
Tolerance Table	±0,0000e+00
Tolerance gainY	±0,0000e+00
Tolerance offsetY	±0,0000e+00
Tolerance minY	±0,0000e+00
Tolerance minX	±0,0000e+00
Tolerance maxY	±0,0000e+00
Tolerance maxX	±0,0000e+00
Tolerance dimY	±0,0000e+00
Tolerance dimX	±0,0000e+00

Verification: LookupTable2D Float32 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for General block LookupTable2D.

Test results				
Time step	1	2	...	67
CPU cycles	139	139	...	143
Inputs				
x (DSP)	-1.1	-1.067	...	1.1
y (DSP)	1.2	1.161	...	-1.35
x	-1.1	-1.067	...	1.1
y	1.2	1.161	...	-1.35
Parameters				
TableData	[1x561]			
DimX	17			
x_min	-0.8			
x_max	0.7			
DimY	33			
y_min	-0.6			
y_max	0.9			
Outputs				
Out	0.155	0.155	...	0.155
Exp. Out	0.155	0.155	...	0.155
Out (DSP)	0.155	0.155	...	0.155
Exp. Out (DSP)	0.155	0.155	...	0.155

Test settings	
Tolerance Out	±4,6566e-07 (±1000 LSB)

Test statistics	
Min CPU cycles	139
Max CPU cycles	147
Avg CPU cycles	144

Test case: Conversion test OK

Conversion test for General block LookupTable2D.

Test results	
Time step	1
Mask parameters	
TableData	[1x561]
DimX	33
x_min	-0.8
x_max	0.7
DimY	17
y_min	-0.6
y_max	0.9
Controller parameters	
gainX	21.333
offsetX	-0.8
Table	[1x561]
gainY	10.667
offsetY	-0.6
minY	-0.6
minX	-0.8
maxY	0.9
maxX	0.7
dimY	16
dimX	32
Exp. gainX	21.333
Exp. offsetX	-0.8
Exp. Table	[1x561]
Exp. gainY	10.667
Exp. offsetY	-0.6
Exp. minY	-0.6
Exp. minX	-0.8
Exp. maxY	0.9
Exp. maxX	0.7
Exp. dimY	16
Exp. dimX	32

Test settings	
Tolerance gainX	±0,0000e+00
Tolerance offsetX	±0,0000e+00
Tolerance Table	±0,0000e+00
Tolerance gainY	±0,0000e+00
Tolerance offsetY	±0,0000e+00
Tolerance minY	±0,0000e+00
Tolerance minX	±0,0000e+00
Tolerance maxY	±0,0000e+00
Tolerance maxX	±0,0000e+00
Tolerance dimY	±0,0000e+00
Tolerance dimX	±0,0000e+00

Verification: LookupTable2D Float32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for General block LookupTable2D.

Test results				
Time step	1	2	...	67
CPU cycles	219	219	...	224
Inputs				
x (DSP)	-1.1	-1.067	...	1.1
y (DSP)	1.2	1.161	...	-1.35
x	-1.1	-1.067	...	1.1
y	1.2	1.161	...	-1.35
Parameters				
TableData	[1x561]			
DimX	17			
x_min	-0.8			
x_max	0.7			
DimY	33			
y_min	-0.6			
y_max	0.9			
Outputs				
Out	0.155	0.155	...	0.155
Exp. Out	0.155	0.155	...	0.155
Out (DSP)	0.155	0.155	...	0.155
Exp. Out (DSP)	0.155	0.155	...	0.155

Test settings	
Tolerance Out	±4,6566e-07 (±1000 LSB)

Test statistics	
Min CPU cycles	219
Max CPU cycles	224
Avg CPU cycles	223

Test case: Conversion test OK

Conversion test for General block LookupTable2D.

Test results	
Time step	1
Mask parameters	
TableData	[1x561]
DimX	33
x_min	-0.8
x_max	0.7
DimY	17
y_min	-0.6
y_max	0.9
Controller parameters	
gainX	21.333
offsetX	-0.8
Table	[1x561]
gainY	10.667
offsetY	-0.6
minY	-0.6
minX	-0.8
maxY	0.9
maxX	0.7
dimY	16
dimX	32
Exp. gainX	21.333
Exp. offsetX	-0.8
Exp. Table	[1x561]
Exp. gainY	10.667
Exp. offsetY	-0.6
Exp. minY	-0.6
Exp. minX	-0.8
Exp. maxY	0.9
Exp. maxX	0.7
Exp. dimY	16
Exp. dimX	32

Test settings	
Tolerance gainX	±0,0000e+00
Tolerance offsetX	±0,0000e+00
Tolerance Table	±0,0000e+00
Tolerance gainY	±0,0000e+00
Tolerance offsetY	±0,0000e+00
Tolerance minY	±0,0000e+00
Tolerance minX	±0,0000e+00
Tolerance maxY	±0,0000e+00
Tolerance maxX	±0,0000e+00
Tolerance dimY	±0,0000e+00
Tolerance dimX	±0,0000e+00

Verification: LookupTable2D Float32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for General block LookupTable2D.

Test results				
Time step	1	2	...	67
CPU cycles	2921	2921	...	3015
Inputs				
x (DSP)	-1.1	-1.067	...	1.1
y (DSP)	1.2	1.161	...	-1.35
x	-1.1	-1.067	...	1.1
y	1.2	1.161	...	-1.35
Parameters				
TableData	[1x561]			
DimX	17			
x_min	-0.8			
x_max	0.7			
DimY	33			
y_min	-0.6			
y_max	0.9			
Outputs				
Out	0.155	0.155	...	0.155
Exp. Out	0.155	0.155	...	0.155
Out (DSP)	0.155	0.155	...	0.155
Exp. Out (DSP)	0.155	0.155	...	0.155

Test settings	
Tolerance Out	±4,6566e-07 (±1000 LSB)

Test statistics	
Min CPU cycles	2921
Max CPU cycles	3789
Avg CPU cycles	3376

Test case: Conversion test OK

Conversion test for General block LookupTable2D.

Test results	
Time step	1
Mask parameters	
TableData	[1x561]
DimX	33
x_min	-0.8
x_max	0.7
DimY	17
y_min	-0.6
y_max	0.9
Controller parameters	
gainX	21.333
offsetX	-0.8
Table	[1x561]
gainY	10.667
offsetY	-0.6
minY	-0.6
minX	-0.8
maxY	0.9
maxX	0.7
dimY	16
dimX	32
Exp. gainX	21.333
Exp. offsetX	-0.8
Exp. Table	[1x561]
Exp. gainY	10.667
Exp. offsetY	-0.6
Exp. minY	-0.6
Exp. minX	-0.8
Exp. maxY	0.9
Exp. maxX	0.7
Exp. dimY	16
Exp. dimX	32

Test settings	
Tolerance gainX	±0,0000e+00
Tolerance offsetX	±0,0000e+00
Tolerance Table	±0,0000e+00
Tolerance gainY	±0,0000e+00
Tolerance offsetY	±0,0000e+00
Tolerance minY	±0,0000e+00
Tolerance minX	±0,0000e+00
Tolerance maxY	±0,0000e+00
Tolerance maxX	±0,0000e+00
Tolerance dimY	±0,0000e+00
Tolerance dimX	±0,0000e+00

Verification: LookupTable2D Float32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for General block LookupTable2D.

Test results				
Time step	1	2	...	67
CPU cycles	1125	1125	...	1135
Inputs				
x (DSP)	-1.1	-1.067	...	1.1
y (DSP)	1.2	1.161	...	-1.35
x	-1.1	-1.067	...	1.1
y	1.2	1.161	...	-1.35
Parameters				
TableData	[1x561]			
DimX	17			
x_min	-0.8			
x_max	0.7			
DimY	33			
y_min	-0.6			
y_max	0.9			
Outputs				
Out	0.155	0.155	...	0.155
Exp. Out	0.155	0.155	...	0.155
Out (DSP)	0.155	0.155	...	0.155
Exp. Out (DSP)	0.155	0.155	...	0.155

Test settings	
Tolerance Out	±4,6566e-07 (±1000 LSB)

Test statistics	
Min CPU cycles	1125
Max CPU cycles	1431
Avg CPU cycles	1272

Test case: Conversion test OK

Conversion test for General block LookupTable2D.

Test results	
Time step	1
Mask parameters	
TableData	[1x561]
DimX	33
x_min	-0.8
x_max	0.7
DimY	17
y_min	-0.6
y_max	0.9
Controller parameters	
gainX	21.333
offsetX	-0.8
Table	[1x561]
gainY	10.667
offsetY	-0.6
minY	-0.6
minX	-0.8
maxY	0.9
maxX	0.7
dimY	16
dimX	32
Exp. gainX	21.333
Exp. offsetX	-0.8
Exp. Table	[1x561]
Exp. gainY	10.667
Exp. offsetY	-0.6
Exp. minY	-0.6
Exp. minX	-0.8
Exp. maxY	0.9
Exp. maxX	0.7
Exp. dimY	16
Exp. dimX	32

Test settings	
Tolerance gainX	±0,0000e+00
Tolerance offsetX	±0,0000e+00
Tolerance Table	±0,0000e+00
Tolerance gainY	±0,0000e+00
Tolerance offsetY	±0,0000e+00
Tolerance minY	±0,0000e+00
Tolerance minX	±0,0000e+00
Tolerance maxY	±0,0000e+00
Tolerance maxX	±0,0000e+00
Tolerance dimY	±0,0000e+00
Tolerance dimX	±0,0000e+00

Verification: LookupTable2D Float32 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for General block LookupTable2D.

Test results				
Time step	1	2	...	67
CPU cycles	3485	3485	...	4028
Inputs				
x (DSP)	-1.1	-1.067	...	1.1
y (DSP)	1.2	1.161	...	-1.35
x	-1.1	-1.067	...	1.1
y	1.2	1.161	...	-1.35
Parameters				
TableData	[1x561]			
DimX	17			
x_min	-0.8			
x_max	0.7			
DimY	33			
y_min	-0.6			
y_max	0.9			
Outputs				
Out	0.155	0.155	...	0.155
Exp. Out	0.155	0.155	...	0.155
Out (DSP)	0.155	0.155	...	0.155
Exp. Out (DSP)	0.155	0.155	...	0.155

Test settings	
Tolerance Out	±4,6566e-07 (±1000 LSB)

Test statistics	
Min CPU cycles	3485
Max CPU cycles	5208
Avg CPU cycles	4323

Test case: Conversion test OK

Conversion test for General block LookupTable2D.

Test results	
Time step	1
Mask parameters	
TableData	[1x561]
DimX	33
x_min	-0.8
x_max	0.7
DimY	17
y_min	-0.6
y_max	0.9
Controller parameters	
gainX	21.333
offsetX	-0.8
Table	[1x561]
gainY	10.667
offsetY	-0.6
minY	-0.6
minX	-0.8
maxY	0.9
maxX	0.7
dimY	16
dimX	32
Exp. gainX	21.333
Exp. offsetX	-0.8
Exp. Table	[1x561]
Exp. gainY	10.667
Exp. offsetY	-0.6
Exp. minY	-0.6
Exp. minX	-0.8
Exp. maxY	0.9
Exp. maxX	0.7
Exp. dimY	16
Exp. dimX	32

Test settings	
Tolerance gainX	±0,0000e+00
Tolerance offsetX	±0,0000e+00
Tolerance Table	±0,0000e+00
Tolerance gainY	±0,0000e+00
Tolerance offsetY	±0,0000e+00
Tolerance minY	±0,0000e+00
Tolerance minX	±0,0000e+00
Tolerance maxY	±0,0000e+00
Tolerance maxX	±0,0000e+00
Tolerance dimY	±0,0000e+00
Tolerance dimX	±0,0000e+00

Verification: LookupTable2D Float32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for General block LookupTable2D.

Test results				
Time step	1	2	...	67
CPU cycles	218	171	...	171
Inputs				
x (DSP)	-1.1	-1.067	...	1.1
y (DSP)	1.2	1.161	...	-1.35
x	-1.1	-1.067	...	1.1
y	1.2	1.161	...	-1.35
Parameters				
TableData	[1x561]			
DimX	17			
x_min	-0.8			
x_max	0.7			
DimY	33			
y_min	-0.6			
y_max	0.9			
Outputs				
Out	0.155	0.155	...	0.155
Exp. Out	0.155	0.155	...	0.155
Out (DSP)	0.155	0.155	...	0.155
Exp. Out (DSP)	0.155	0.155	...	0.155

Test settings	
Tolerance Out	±4,6566e-07 (±1000 LSB)

Test statistics	
Min CPU cycles	169
Max CPU cycles	218
Avg CPU cycles	174

Test case: Conversion test OK

Conversion test for General block LookupTable2D.

Test results	
Time step	1
Mask parameters	
TableData	[1x561]
DimX	33
x_min	-0.8
x_max	0.7
DimY	17
y_min	-0.6
y_max	0.9
Controller parameters	
gainX	21.333
offsetX	-0.8
Table	[1x561]
gainY	10.667
offsetY	-0.6
minY	-0.6
minX	-0.8
maxY	0.9
maxX	0.7
dimY	16
dimX	32
Exp. gainX	21.333
Exp. offsetX	-0.8
Exp. Table	[1x561]
Exp. gainY	10.667
Exp. offsetY	-0.6
Exp. minY	-0.6
Exp. minX	-0.8
Exp. maxY	0.9
Exp. maxX	0.7
Exp. dimY	16
Exp. dimX	32

Test settings	
Tolerance gainX	±0,0000e+00
Tolerance offsetX	±0,0000e+00
Tolerance Table	±0,0000e+00
Tolerance gainY	±0,0000e+00
Tolerance offsetY	±0,0000e+00
Tolerance minY	±0,0000e+00
Tolerance minX	±0,0000e+00
Tolerance maxY	±0,0000e+00
Tolerance maxX	±0,0000e+00
Tolerance dimY	±0,0000e+00
Tolerance dimX	±0,0000e+00

Verification: LookupTable2D Float32 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for General block LookupTable2D.

Test results				
Time step	1	2	...	67
CPU cycles	165	165	...	168
Inputs				
x (DSP)	-1.1	-1.067	...	1.1
y (DSP)	1.2	1.161	...	-1.35
x	-1.1	-1.067	...	1.1
y	1.2	1.161	...	-1.35
Parameters				
TableData	[1x561]			
DimX	17			
x_min	-0.8			
x_max	0.7			
DimY	33			
y_min	-0.6			
y_max	0.9			
Outputs				
Out	0.155	0.155	...	0.155
Exp. Out	0.155	0.155	...	0.155
Out (DSP)	0.155	0.155	...	0.155
Exp. Out (DSP)	0.155	0.155	...	0.155

Test settings	
Tolerance Out	±4,6566e-07 (±1000 LSB)

Test statistics	
Min CPU cycles	162
Max CPU cycles	174
Avg CPU cycles	165

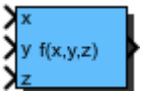
Test case: Conversion test OK

Conversion test for General block LookupTable2D.

Test results	
Time step	1
Mask parameters	
TableData	[1x561]
DimX	33
x_min	-0.8
x_max	0.7
DimY	17
y_min	-0.6
y_max	0.9
Controller parameters	
gainX	21.333
offsetX	-0.8
Table	[1x561]
gainY	10.667
offsetY	-0.6
minY	-0.6
minX	-0.8
maxY	0.9
maxX	0.7
dimY	16
dimX	32
Exp. gainX	21.333
Exp. offsetX	-0.8
Exp. Table	[1x561]
Exp. gainY	10.667
Exp. offsetY	-0.6
Exp. minY	-0.6
Exp. minX	-0.8
Exp. maxY	0.9
Exp. maxX	0.7
Exp. dimY	16
Exp. dimX	32

Test settings	
Tolerance gainX	±0,0000e+00
Tolerance offsetX	±0,0000e+00
Tolerance Table	±0,0000e+00
Tolerance gainY	±0,0000e+00
Tolerance offsetY	±0,0000e+00
Tolerance minY	±0,0000e+00
Tolerance minX	±0,0000e+00
Tolerance maxY	±0,0000e+00
Tolerance maxX	±0,0000e+00
Tolerance dimY	±0,0000e+00
Tolerance dimX	±0,0000e+00

Block: LookupTable3D



Three dimensional look-up table with selectable number of data points.
Table data must be an array of size DimX*DimY*DimZ.
If input is out of specified range, output will be cut off (no extrapolation).

Inports	
x	Table index in x direction
y	Table index in y direction
z	Table index in z direction

Outports	
Out	Table output

Mask Parameters		
Name	**ID**	**Description**
TableData	1	Look-up table data
DimX	2	Number of data points in x-direction
x_min	3	Minimum input value of x-dimension for look-up table
x_max	4	Maximum input value of x-dimension for look-up table
DimY	5	Number of data points in y-direction
y_max	6	Maximum input value of y-dimension for look-up table
y_min	7	Minimum input value of y-dimension for look-up table
DimZ	8	Number of data points in z-direction
z_min	9	Minimum input value of z-dimension for look-up table
z_max	10	Maximum input value of z-dimension for look-up table

Description:

The table of the LookupTable3D block must contain DimX times DimY times DimZ data points and they have to be arranged as

$$
\begin{aligned}
\text{TableData} = [&f(x_1, y_1, z_1),\ f(x_2, y_1, z_1),\ \ldots f(x_{n-1}, y_1, z_1),\ f(x_n, y_1, z_1),\\
&f(x_1, y_2, z_1),\ f(x_2, y_2, z_1),\ \ldots f(x_{n-1}, y_2, z_1),\ f(x_n, y_2, z_1),\\
&\ldots\\
&f(x_1, y_{m-1}, z_1),\ f(x_2, y_{m-1}, z_1),\ \ldots f(x_{n-1}, y_{m-1}, z_1),\ f(x_n, y_{m-1}, z_1),\\
&f(x_1, y_m, z_1),\ f(x_2, y_m, z_1),\ \ldots f(x_{n-1}, y_m, z_1),\ f(x_n, y_m, z_1)\\
&f(x_1, y_1, z_2),\ f(x_2, y_1, z_2),\ \ldots f(x_{n-1}, y_1, z_2),\ f(x_n, y_1, z_2),\\
&f(x_1, y_2, z_2),\ f(x_2, y_2, z_2),\ \ldots f(x_{n-1}, y_2, z_2),\ f(x_n, y_2, z_2),\\
&\ldots\\
&f(x_1, y_{m-1}, z_k),\ f(x_2, y_{m-1}, z_k),\ \ldots f(x_{n-1}, y_{m-1}, z_k),\ f(x_n, y_{m-1}, z_k),\\
&f(x_1, y_m, z_k),\ f(x_2, y_m, z_k),\ \ldots f(x_{n-1}, y_m, z_k),\ f(x_n, y_m, z_k)]
\end{aligned}
$$

with n as selected DimX, m as selected DimY and k as selected DimZ values.
For interpolation of the data, the trilinear interpolation method is used. The interpolation is implemented as

$$f(x, y, z) = \quad c_0 + c_1\Delta x + c_2\Delta y + c_3\Delta z + c_4\Delta x\Delta y + c_5\Delta y\Delta z + c_6\Delta z\Delta x + c_7\Delta x\Delta y\Delta z$$

with Δx, Δy, Δz as relative distances to the starting point f_{000} and with the coefficients

$$
\begin{aligned}
c_0 &= f_{000}\\
c_1 &= f_{100} - f_{000}\\
c_2 &= f_{010} - f_{000}\\
c_3 &= f_{001} - f_{000}\\
c_4 &= f_{110} - f_{010} - f_{100} + f_{000}\\
c_5 &= f_{011} - f_{001} - f_{010} + f_{000}\\
c_6 &= f_{101} - f_{001} - f_{100} + f_{000}\\
c_7 &= f_{111} - f_{011} - f_{101} - f_{110} + f_{100} + f_{001} + f_{010} - f_{000}
\end{aligned}
$$

derived from the lattice points relative to the starting point.

Implementations:

FiP16	16 Bit Fixed Point Implementation
FiP32	32 Bit Fixed Point Implementation
Float32	32 Bit Floating Point Implementation
Float64	64 Bit Floating Point Implementation

Implementation: FiP16

16 Bit Fixed Point Implementation

Inports Data Type	
x	int16
y	int16
z	int16

Outports Data Type	
Out	int16

Implementation: FiP32

32 Bit Fixed Point Implementation

Inports Data Type	
x	int32
y	int32
z	int32

Outports Data Type	
Out	int32

Implementation: Float32

32 Bit Floating Point Implementation

Inports Data Type	
x	float32
y	float32
z	float32

Outports Data Type	
Out	float32

Implementation: Float64

64 Bit Floating Point Implementation

Inports Data Type	
x	float64
y	float64
z	float64

Outports Data Type	
Out	float64

Verification: LookupTable3D FiP16 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for General block LookupTable3D.

Test results						
Time step	1	2	3	4	...	19
CPU cycles	424	424	443	443	...	452
Inputs						
x (DSP)	-32768	-29127	-25486	-21845	...	32767
y (DSP)	-29491	-26396	-23302	-20207	...	26214
z (DSP)	-26214	-23484	-20753	-18022	...	22938
x	-1	-0.889	-0.778	-0.667	...	1
y	-0.9	-0.806	-0.711	-0.617	...	0.8
z	-0.8	-0.717	-0.633	-0.55	...	0.7
Parameters						
TableData	[1x765]					
DimX	9					
x_min	-0.8					
x_max	0.7					
DimY	17					
y_max	0.9					
y_min	-0.6					
DimZ	5					
z_min	-0.9					
z_max	0.95					
Outputs						
Out	0.56	0.502	0.436	0.348	...	0.525
Exp. Out	0.56	0.502	0.436	0.348	...	0.525
Out (DSP)	18346	16435	14292	11410	...	17198
Exp. Out (DSP)	18350	16439	14297	11414	...	17203

Test settings	
Tolerance Out	±3,0518e-04 (±10 LSB)

Test statistics	
Min CPU cycles	424
Max CPU cycles	460
Avg CPU cycles	453

Test case: Conversion test **OK**

Conversion test for General block LookupTable3D.

Test results	
Time step	1
Mask parameters	
TableData	[1x135]
DimX	5
x_min	-0.8
x_max	0.7
DimY	9
y_max	0.9
y_min	-0.6
DimZ	3
z_min	-0.9
z_max	0.95
Controller parameters	
maskY	8191
maskX	16383
maskZ	32767
maxZ	31130
maxY	29491
maxX	22938
sfrX	14
sfrZ	15
sfrY	13
offsetX	-1638
offsetZ	819
offsetY	4915
gainXsfr	14
gainZsfr	14
gainX	21845
gainZ	17712
Table	[1x135]
gainY	21845
sizeX	5
minY	-19661
minX	-26214
minZ	-29491
idxOffsetY	4
idxOffsetX	2
sizeY	9
idxOffsetZ	1
sizeXY	45
gainYsfr	14
Exp. maskY	8191

Test settings	
Tolerance maskY	±0,0000e+00
Tolerance maskX	±0,0000e+00
Tolerance maskZ	±0,0000e+00
Tolerance maxZ	±0,0000e+00
Tolerance maxY	±0,0000e+00
Tolerance maxX	±0,0000e+00
Tolerance sfrX	±0,0000e+00
Tolerance sfrZ	±0,0000e+00
Tolerance sfrY	±0,0000e+00
Tolerance offsetX	±0,0000e+00
Tolerance offsetZ	±0,0000e+00
Tolerance offsetY	±0,0000e+00
Tolerance gainXsfr	±0,0000e+00
Tolerance gainZsfr	±0,0000e+00
Tolerance gainX	±0,0000e+00
Tolerance gainZ	±0,0000e+00
Tolerance Table	±0,0000e+00
Tolerance gainY	±0,0000e+00
Tolerance sizeX	±0,0000e+00
Tolerance minY	±0,0000e+00
Tolerance minX	±0,0000e+00
Tolerance minZ	±0,0000e+00
Tolerance idxOffsetY	±0,0000e+00
Tolerance idxOffsetX	±0,0000e+00
Tolerance sizeY	±0,0000e+00
Tolerance idxOffsetZ	±0,0000e+00
Tolerance sizeXY	±0,0000e+00
Tolerance gainYsfr	±0,0000e+00

Verification: LookupTable3D FiP16 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for General block LookupTable3D.

Test results						
Time step	1	2	3	4	...	19
CPU cycles	247	247	265	265	...	273
Inputs						
x (DSP)	-32768	-29127	-25486	-21845	...	32767
y (DSP)	-29491	-26396	-23302	-20207	...	26214
z (DSP)	-26214	-23484	-20753	-18022	...	22938
x	-1	-0.889	-0.778	-0.667	...	1
y	-0.9	-0.806	-0.711	-0.617	...	0.8
z	-0.8	-0.717	-0.633	-0.55	...	0.7
Parameters						
TableData	[1x765]					
DimX	9					
x_min	-0.8					
x_max	0.7					
DimY	17					
y_max	0.9					
y_min	-0.6					
DimZ	5					
z_min	-0.9					
z_max	0.95					
Outputs						
Out	0.56	0.502	0.436	0.348	...	0.525
Exp. Out	0.56	0.502	0.436	0.348	...	0.525
Out (DSP)	18346	16435	14292	11410	...	17198
Exp. Out (DSP)	18350	16439	14297	11414	...	17203

Test settings	
Tolerance Out	±3,0518e-04 (±10 LSB)

Test statistics	
Min CPU cycles	247
Max CPU cycles	283
Avg CPU cycles	275

Test case: Conversion test **OK**

Conversion test for General block LookupTable3D.

Test results	
Time step	1
Mask parameters	
TableData	[1x135]
DimX	5
x_min	-0.8
x_max	0.7
DimY	9
y_max	0.9
y_min	-0.6
DimZ	3
z_min	-0.9
z_max	0.95
Controller parameters	
maskY	8191
maskX	16383
maskZ	32767
maxZ	31130
maxY	29491
maxX	22938
sfrX	14
sfrZ	15
sfrY	13
offsetX	-1638
offsetZ	819
offsetY	4915
gainXsfr	14
gainZsfr	14
gainX	21845
gainZ	17712
Table	[1x135]
gainY	21845
sizeX	5
minY	-19661
minX	-26214
minZ	-29491
idxOffsetY	4
idxOffsetX	2
sizeY	9
idxOffsetZ	1
sizeXY	45
gainYsfr	14
Exp. maskY	8191

Test settings	
Tolerance maskY	±0,0000e+00
Tolerance maskX	±0,0000e+00
Tolerance maskZ	±0,0000e+00
Tolerance maxZ	±0,0000e+00
Tolerance maxY	±0,0000e+00
Tolerance maxX	±0,0000e+00
Tolerance sfrX	±0,0000e+00
Tolerance sfrZ	±0,0000e+00
Tolerance sfrY	±0,0000e+00
Tolerance offsetX	±0,0000e+00
Tolerance offsetZ	±0,0000e+00
Tolerance offsetY	±0,0000e+00
Tolerance gainXsfr	±0,0000e+00
Tolerance gainZsfr	±0,0000e+00
Tolerance gainX	±0,0000e+00
Tolerance gainZ	±0,0000e+00
Tolerance Table	±0,0000e+00
Tolerance gainY	±0,0000e+00
Tolerance sizeX	±0,0000e+00
Tolerance minY	±0,0000e+00
Tolerance minX	±0,0000e+00
Tolerance minZ	±0,0000e+00
Tolerance idxOffsetY	±0,0000e+00
Tolerance idxOffsetX	±0,0000e+00
Tolerance sizeY	±0,0000e+00
Tolerance idxOffsetZ	±0,0000e+00
Tolerance sizeXY	±0,0000e+00
Tolerance gainYsfr	±0,0000e+00

Verification: LookupTable3D FiP16 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for General block LookupTable3D.

Test results						
Time step	1	2	3	4	...	19
CPU cycles	368	368	395	395	...	394
Inputs						
x (DSP)	-32768	-29127	-25486	-21845	...	32767
y (DSP)	-29491	-26396	-23302	-20207	...	26214
z (DSP)	-26214	-23484	-20753	-18022	...	22938
x	-1	-0.889	-0.778	-0.667	...	1
y	-0.9	-0.806	-0.711	-0.617	...	0.8
z	-0.8	-0.717	-0.633	-0.55	...	0.7
Parameters						
TableData	[1x765]					
DimX	9					
x_min	-0.8					
x_max	0.7					
DimY	17					
y_max	0.9					
y_min	-0.6					
DimZ	5					
z_min	-0.9					
z_max	0.95					
Outputs						
Out	0.56	0.502	0.436	0.348	...	0.525
Exp. Out	0.56	0.502	0.436	0.348	...	0.525
Out (DSP)	18346	16435	14292	11410	...	17198
Exp. Out (DSP)	18350	16439	14297	11414	...	17203

Test settings	
Tolerance Out	±3,0518e-04 (±10 LSB)

Test statistics	
Min CPU cycles	368
Max CPU cycles	430
Avg CPU cycles	411

Test case: Conversion test **OK**

Conversion test for General block LookupTable3D.

Test results	
Time step	1
Mask parameters	
TableData	[1x135]
DimX	5
x_min	-0.8
x_max	0.7
DimY	9
y_max	0.9
y_min	-0.6
DimZ	3
z_min	-0.9
z_max	0.95
Controller parameters	
maskY	8191
maskX	16383
maskZ	32767
maxZ	31130
maxY	29491
maxX	22938
sfrX	14
sfrZ	15
sfrY	13
offsetX	-1638
offsetZ	819
offsetY	4915
gainXsfr	14
gainZsfr	14
gainX	21845
gainZ	17712
Table	[1x135]
gainY	21845
sizeX	5
minY	-19661
minX	-26214
minZ	-29491
idxOffsetY	4
idxOffsetX	2
sizeY	9
idxOffsetZ	1
sizeXY	45
gainYsfr	14
Exp. maskY	8191

Test settings	
Tolerance maskY	±0,0000e+00
Tolerance maskX	±0,0000e+00
Tolerance maskZ	±0,0000e+00
Tolerance maxZ	±0,0000e+00
Tolerance maxY	±0,0000e+00
Tolerance maxX	±0,0000e+00
Tolerance sfrX	±0,0000e+00
Tolerance sfrZ	±0,0000e+00
Tolerance sfrY	±0,0000e+00
Tolerance offsetX	±0,0000e+00
Tolerance offsetZ	±0,0000e+00
Tolerance offsetY	±0,0000e+00
Tolerance gainXsfr	±0,0000e+00
Tolerance gainZsfr	±0,0000e+00
Tolerance gainX	±0,0000e+00
Tolerance gainZ	±0,0000e+00
Tolerance Table	±0,0000e+00
Tolerance gainY	±0,0000e+00
Tolerance sizeX	±0,0000e+00
Tolerance minY	±0,0000e+00
Tolerance minX	±0,0000e+00
Tolerance minZ	±0,0000e+00
Tolerance idxOffsetY	±0,0000e+00
Tolerance idxOffsetX	±0,0000e+00
Tolerance sizeY	±0,0000e+00
Tolerance idxOffsetZ	±0,0000e+00
Tolerance sizeXY	±0,0000e+00
Tolerance gainYsfr	±0,0000e+00

Verification: LookupTable3D FiP16 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for General block LookupTable3D.

Test results						
Time step	1	2	3	4	...	19
CPU cycles	369	369	390	390	...	395
Inputs						
x (DSP)	-32768	-29127	-25486	-21845	...	32767
y (DSP)	-29491	-26396	-23302	-20207	...	26214
z (DSP)	-26214	-23484	-20753	-18022	...	22938
x	-1	-0.889	-0.778	-0.667	...	1
y	-0.9	-0.806	-0.711	-0.617	...	0.8
z	-0.8	-0.717	-0.633	-0.55	...	0.7
Parameters						
TableData	[1x765]					
DimX	9					
x_min	-0.8					
x_max	0.7					
DimY	17					
y_max	0.9					
y_min	-0.6					
DimZ	5					
z_min	-0.9					
z_max	0.95					
Outputs						
Out	0.56	0.502	0.436	0.348	...	0.525
Exp. Out	0.56	0.502	0.436	0.348	...	0.525
Out (DSP)	18346	16435	14292	11410	...	17198
Exp. Out (DSP)	18350	16439	14297	11414	...	17203

Test settings	
Tolerance Out	±3,0518e-04 (±10 LSB)

Test statistics	
Min CPU cycles	369
Max CPU cycles	411
Avg CPU cycles	401

Test case: Conversion test **OK**

Conversion test for General block LookupTable3D.

Test results	
Time step	1
Mask parameters	
TableData	[1x135]
DimX	5
x_min	-0.8
x_max	0.7
DimY	9
y_max	0.9
y_min	-0.6
DimZ	3
z_min	-0.9
z_max	0.95
Controller parameters	
maskY	8191
maskX	16383
maskZ	32767
maxZ	31130
maxY	29491
maxX	22938
sfrX	14
sfrZ	15
sfrY	13
offsetX	-1638
offsetZ	819
offsetY	4915
gainXsfr	14
gainZsfr	14
gainX	21845
gainZ	17712
Table	[1x135]
gainY	21845
sizeX	5
minY	-19661
minX	-26214
minZ	-29491
idxOffsetY	4
idxOffsetX	2
sizeY	9
idxOffsetZ	1
sizeXY	45
gainYsfr	14
Exp. maskY	8191

Test settings	
Tolerance maskY	±0,0000e+00
Tolerance maskX	±0,0000e+00
Tolerance maskZ	±0,0000e+00
Tolerance maxZ	±0,0000e+00
Tolerance maxY	±0,0000e+00
Tolerance maxX	±0,0000e+00
Tolerance sfrX	±0,0000e+00
Tolerance sfrZ	±0,0000e+00
Tolerance sfrY	±0,0000e+00
Tolerance offsetX	±0,0000e+00
Tolerance offsetZ	±0,0000e+00
Tolerance offsetY	±0,0000e+00
Tolerance gainXsfr	±0,0000e+00
Tolerance gainZsfr	±0,0000e+00
Tolerance gainX	±0,0000e+00
Tolerance gainZ	±0,0000e+00
Tolerance Table	±0,0000e+00
Tolerance gainY	±0,0000e+00
Tolerance sizeX	±0,0000e+00
Tolerance minY	±0,0000e+00
Tolerance minX	±0,0000e+00
Tolerance minZ	±0,0000e+00
Tolerance idxOffsetY	±0,0000e+00
Tolerance idxOffsetX	±0,0000e+00
Tolerance sizeY	±0,0000e+00
Tolerance idxOffsetZ	±0,0000e+00
Tolerance sizeXY	±0,0000e+00
Tolerance gainYsfr	±0,0000e+00

Verification: LookupTable3D FiP16 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for General block LookupTable3D.

Test results						
Time step	1	2	3	4	...	19
CPU cycles	222	222	239	239	...	245
Inputs						
x (DSP)	-32768	-29127	-25486	-21845	...	32767
y (DSP)	-29491	-26396	-23302	-20207	...	26214
z (DSP)	-26214	-23484	-20753	-18022	...	22938
x	-1	-0.889	-0.778	-0.667	...	1
y	-0.9	-0.806	-0.711	-0.617	...	0.8
z	-0.8	-0.717	-0.633	-0.55	...	0.7
Parameters						
TableData	[1x765]					
DimX	9					
x_min	-0.8					
x_max	0.7					
DimY	17					
y_max	0.9					
y_min	-0.6					
DimZ	5					
z_min	-0.9					
z_max	0.95					
Outputs						
Out	0.56	0.502	0.436	0.348	...	0.525
Exp. Out	0.56	0.502	0.436	0.348	...	0.525
Out (DSP)	18346	16435	14292	11410	...	17198
Exp. Out (DSP)	18350	16439	14297	11414	...	17203

Test settings	
Tolerance Out	±3,0518e-04 (±10 LSB)

Test statistics	
Min CPU cycles	222
Max CPU cycles	257
Avg CPU cycles	249

Test case: Conversion test **OK**

Conversion test for General block LookupTable3D.

Test results	
Time step	1
Mask parameters	
TableData	[1x135]
DimX	5
x_min	-0.8
x_max	0.7
DimY	9
y_max	0.9
y_min	-0.6
DimZ	3
z_min	-0.9
z_max	0.95
Controller parameters	
maskY	8191
maskX	16383
maskZ	32767
maxZ	31130
maxY	29491
maxX	22938
sfrX	14
sfrZ	15
sfrY	13
offsetX	-1638
offsetZ	819
offsetY	4915
gainXsfr	14
gainZsfr	14
gainX	21845
gainZ	17712
Table	[1x135]
gainY	21845
sizeX	5
minY	-19661
minX	-26214
minZ	-29491
idxOffsetY	4
idxOffsetX	2
sizeY	9
idxOffsetZ	1
sizeXY	45
gainYsfr	14
Exp. maskY	8191

Test settings	
Tolerance maskY	±0,0000e+00
Tolerance maskX	±0,0000e+00
Tolerance maskZ	±0,0000e+00
Tolerance maxZ	±0,0000e+00
Tolerance maxY	±0,0000e+00
Tolerance maxX	±0,0000e+00
Tolerance sfrX	±0,0000e+00
Tolerance sfrZ	±0,0000e+00
Tolerance sfrY	±0,0000e+00
Tolerance offsetX	±0,0000e+00
Tolerance offsetZ	±0,0000e+00
Tolerance offsetY	±0,0000e+00
Tolerance gainXsfr	±0,0000e+00
Tolerance gainZsfr	±0,0000e+00
Tolerance gainX	±0,0000e+00
Tolerance gainZ	±0,0000e+00
Tolerance Table	±0,0000e+00
Tolerance gainY	±0,0000e+00
Tolerance sizeX	±0,0000e+00
Tolerance minY	±0,0000e+00
Tolerance minX	±0,0000e+00
Tolerance minZ	±0,0000e+00
Tolerance idxOffsetY	±0,0000e+00
Tolerance idxOffsetX	±0,0000e+00
Tolerance sizeY	±0,0000e+00
Tolerance idxOffsetZ	±0,0000e+00
Tolerance sizeXY	±0,0000e+00
Tolerance gainYsfr	±0,0000e+00

Verification: LookupTable3D FiP16 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for General block LookupTable3D.

Test results						
Time step	1	2	3	4	...	19
CPU cycles	598	598	630	630	...	628
Inputs						
x (DSP)	-32768	-29127	-25486	-21845	...	32767
y (DSP)	-29491	-26396	-23302	-20207	...	26214
z (DSP)	-26214	-23484	-20753	-18022	...	22938
x	-1	-0.889	-0.778	-0.667	...	1
y	-0.9	-0.806	-0.711	-0.617	...	0.8
z	-0.8	-0.717	-0.633	-0.55	...	0.7
Parameters						
TableData	[1x765]					
DimX	9					
x_min	-0.8					
x_max	0.7					
DimY	17					
y_max	0.9					
y_min	-0.6					
DimZ	5					
z_min	-0.9					
z_max	0.95					
Outputs						
Out	0.56	0.502	0.436	0.348	...	0.525
Exp. Out	0.56	0.502	0.436	0.348	...	0.525
Out (DSP)	18346	16435	14292	11410	...	17198
Exp. Out (DSP)	18350	16439	14297	11414	...	17203

Test settings	
Tolerance Out	±3,0518e-04 (±10 LSB)

Test statistics	
Min CPU cycles	598
Max CPU cycles	657
Avg CPU cycles	643

Test case: Conversion test **OK**

Conversion test for General block LookupTable3D.

Test results	
Time step	1
Mask parameters	
TableData	[1x135]
DimX	5
x_min	-0.8
x_max	0.7
DimY	9
y_max	0.9
y_min	-0.6
DimZ	3
z_min	-0.9
z_max	0.95
Controller parameters	
maskY	8191
maskX	16383
maskZ	32767
maxZ	31130
maxY	29491
maxX	22938
sfrX	14
sfrZ	15
sfrY	13
offsetX	-1638
offsetZ	819
offsetY	4915
gainXsfr	14
gainZsfr	14
gainX	21845
gainZ	17712
Table	[1x135]
gainY	21845
sizeX	5
minY	-19661
minX	-26214
minZ	-29491
idxOffsetY	4
idxOffsetX	2
sizeY	9
idxOffsetZ	1
sizeXY	45
gainYsfr	14
Exp. maskY	8191

Test settings	
Tolerance maskY	±0,0000e+00
Tolerance maskX	±0,0000e+00
Tolerance maskZ	±0,0000e+00
Tolerance maxZ	±0,0000e+00
Tolerance maxY	±0,0000e+00
Tolerance maxX	±0,0000e+00
Tolerance sfrX	±0,0000e+00
Tolerance sfrZ	±0,0000e+00
Tolerance sfrY	±0,0000e+00
Tolerance offsetX	±0,0000e+00
Tolerance offsetZ	±0,0000e+00
Tolerance offsetY	±0,0000e+00
Tolerance gainXsfr	±0,0000e+00
Tolerance gainZsfr	±0,0000e+00
Tolerance gainX	±0,0000e+00
Tolerance gainZ	±0,0000e+00
Tolerance Table	±0,0000e+00
Tolerance gainY	±0,0000e+00
Tolerance sizeX	±0,0000e+00
Tolerance minY	±0,0000e+00
Tolerance minX	±0,0000e+00
Tolerance minZ	±0,0000e+00
Tolerance idxOffsetY	±0,0000e+00
Tolerance idxOffsetX	±0,0000e+00
Tolerance sizeY	±0,0000e+00
Tolerance idxOffsetZ	±0,0000e+00
Tolerance sizeXY	±0,0000e+00
Tolerance gainYsfr	±0,0000e+00

Verification: LookupTable3D FiP16 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for General block LookupTable3D.

Test results						
Time step	1	2	3	4	...	19
CPU cycles	411	323	343	333	...	338
Inputs						
x (DSP)	-32768	-29127	-25486	-21845	...	32767
y (DSP)	-29491	-26396	-23302	-20207	...	26214
z (DSP)	-26214	-23484	-20753	-18022	...	22938
x	-1	-0.889	-0.778	-0.667	...	1
y	-0.9	-0.806	-0.711	-0.617	...	0.8
z	-0.8	-0.717	-0.633	-0.55	...	0.7
Parameters						
TableData	[1x765]					
DimX	9					
x_min	-0.8					
x_max	0.7					
DimY	17					
y_max	0.9					
y_min	-0.6					
DimZ	5					
z_min	-0.9					
z_max	0.95					
Outputs						
Out	0.56	0.502	0.436	0.348	...	0.525
Exp. Out	0.56	0.502	0.436	0.348	...	0.525
Out (DSP)	18346	16435	14292	11410	...	17198
Exp. Out (DSP)	18350	16439	14297	11414	...	17203

Test settings	
Tolerance Out	±3,0518e-04 (±10 LSB)

Test statistics	
Min CPU cycles	323
Max CPU cycles	411
Avg CPU cycles	346

Test case: Conversion test **OK**

Conversion test for General block LookupTable3D.

Test results	
Time step	1
Mask parameters	
TableData	[1x135]
DimX	5
x_min	-0.8
x_max	0.7
DimY	9
y_max	0.9
y_min	-0.6
DimZ	3
z_min	-0.9
z_max	0.95
Controller parameters	
maskY	8191
maskX	16383
maskZ	32767
maxZ	31130
maxY	29491
maxX	22938
sfrX	14
sfrZ	15
sfrY	13
offsetX	-1638
offsetZ	819
offsetY	4915
gainXsfr	14
gainZsfr	14
gainX	21845
gainZ	17712
Table	[1x135]
gainY	21845
sizeX	5
minY	-19661
minX	-26214
minZ	-29491
idxOffsetY	4
idxOffsetX	2
sizeY	9
idxOffsetZ	1
sizeXY	45
gainYsfr	14
Exp. maskY	8191

Test settings	
Tolerance maskY	±0,0000e+00
Tolerance maskX	±0,0000e+00
Tolerance maskZ	±0,0000e+00
Tolerance maxZ	±0,0000e+00
Tolerance maxY	±0,0000e+00
Tolerance maxX	±0,0000e+00
Tolerance sfrX	±0,0000e+00
Tolerance sfrZ	±0,0000e+00
Tolerance sfrY	±0,0000e+00
Tolerance offsetX	±0,0000e+00
Tolerance offsetZ	±0,0000e+00
Tolerance offsetY	±0,0000e+00
Tolerance gainXsfr	±0,0000e+00
Tolerance gainZsfr	±0,0000e+00
Tolerance gainX	±0,0000e+00
Tolerance gainZ	±0,0000e+00
Tolerance Table	±0,0000e+00
Tolerance gainY	±0,0000e+00
Tolerance sizeX	±0,0000e+00
Tolerance minY	±0,0000e+00
Tolerance minX	±0,0000e+00
Tolerance minZ	±0,0000e+00
Tolerance idxOffsetY	±0,0000e+00
Tolerance idxOffsetX	±0,0000e+00
Tolerance sizeY	±0,0000e+00
Tolerance idxOffsetZ	±0,0000e+00
Tolerance sizeXY	±0,0000e+00
Tolerance gainYsfr	±0,0000e+00

Verification: LookupTable3D FiP16 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for General block LookupTable3D.

Test results						
Time step	1	2	3	4	...	19
CPU cycles	389	389	410	410	...	421
Inputs						
x (DSP)	-32768	-29127	-25486	-21845	...	32767
y (DSP)	-29491	-26396	-23302	-20207	...	26214
z (DSP)	-26214	-23484	-20753	-18022	...	22938
x	-1	-0.889	-0.778	-0.667	...	1
y	-0.9	-0.806	-0.711	-0.617	...	0.8
z	-0.8	-0.717	-0.633	-0.55	...	0.7
Parameters						
TableData	[1x765]					
DimX	9					
x_min	-0.8					
x_max	0.7					
DimY	17					
y_max	0.9					
y_min	-0.6					
DimZ	5					
z_min	-0.9					
z_max	0.95					
Outputs						
Out	0.56	0.502	0.436	0.348	...	0.525
Exp. Out	0.56	0.502	0.436	0.348	...	0.525
Out (DSP)	18346	16435	14292	11410	...	17198
Exp. Out (DSP)	18350	16439	14297	11414	...	17203

Test settings	
Tolerance Out	±3,0518e-04 (±10 LSB)

Test statistics	
Min CPU cycles	389
Max CPU cycles	431
Avg CPU cycles	421

Test case: Conversion test **OK**

Conversion test for General block LookupTable3D.

Test results	
Time step	1
Mask parameters	
TableData	[1x135]
DimX	5
x_min	-0.8
x_max	0.7
DimY	9
y_max	0.9
y_min	-0.6
DimZ	3
z_min	-0.9
z_max	0.95
Controller parameters	
maskY	8191
maskX	16383
maskZ	32767
maxZ	31130
maxY	29491
maxX	22938
sfrX	14
sfrZ	15
sfrY	13
offsetX	-1638
offsetZ	819
offsetY	4915
gainXsfr	14
gainZsfr	14
gainX	21845
gainZ	17712
Table	[1x135]
gainY	21845
sizeX	5
minY	-19661
minX	-26214
minZ	-29491
idxOffsetY	4
idxOffsetX	2
sizeY	9
idxOffsetZ	1
sizeXY	45
gainYsfr	14
Exp. maskY	8191

Test settings	
Tolerance maskY	±0,0000e+00
Tolerance maskX	±0,0000e+00
Tolerance maskZ	±0,0000e+00
Tolerance maxZ	±0,0000e+00
Tolerance maxY	±0,0000e+00
Tolerance maxX	±0,0000e+00
Tolerance sfrX	±0,0000e+00
Tolerance sfrZ	±0,0000e+00
Tolerance sfrY	±0,0000e+00
Tolerance offsetX	±0,0000e+00
Tolerance offsetZ	±0,0000e+00
Tolerance offsetY	±0,0000e+00
Tolerance gainXsfr	±0,0000e+00
Tolerance gainZsfr	±0,0000e+00
Tolerance gainX	±0,0000e+00
Tolerance gainZ	±0,0000e+00
Tolerance Table	±0,0000e+00
Tolerance gainY	±0,0000e+00
Tolerance sizeX	±0,0000e+00
Tolerance minY	±0,0000e+00
Tolerance minX	±0,0000e+00
Tolerance minZ	±0,0000e+00
Tolerance idxOffsetY	±0,0000e+00
Tolerance idxOffsetX	±0,0000e+00
Tolerance sizeY	±0,0000e+00
Tolerance idxOffsetZ	±0,0000e+00
Tolerance sizeXY	±0,0000e+00
Tolerance gainYsfr	±0,0000e+00

Verification: LookupTable3D FiP32 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for General block LookupTable3D.

Test results				
Time step	1	2	...	19
CPU cycles	652	652	...	694
Inputs				
x (DSP)	-2147483648	-1908874354	...	2147483647
y (DSP)	-1932735283	-1729917383	...	1717986918
z (DSP)	-1717986918	-1539029948	...	1503238554
x	-1	-0.889	...	1
y	-0.9	-0.806	...	0.8
z	-0.8	-0.717	...	0.7
Parameters				
TableData	[1x765]			
DimX	9			
x_min	-0.8			
x_max	0.7			
DimY	17			
y_max	0.9			
y_min	-0.6			
DimZ	5			
z_min	-0.9			
z_max	0.95			
Outputs				
Out	0.56	0.502	...	0.525
Exp. Out	0.56	0.502	...	0.525
Out (DSP)	1202590840	1077320961	...	1127428909
Exp. Out (DSP)	1202590843	1077320963	...	1127428915

Test settings	
Tolerance Out	±4,6566e-09 (±10 LSB)

Test statistics	
Min CPU cycles	652
Max CPU cycles	711
Avg CPU cycles	698

Test case: Conversion test **OK**

Conversion test for General block LookupTable3D.

Test results	
Time step	1
Mask parameters	
TableData	[1x135]
DimX	5
x_min	-0.8
x_max	0.7
DimY	9
y_max	0.9
y_min	-0.6
DimZ	3
z_min	-0.9
z_max	0.95
Controller parameters	
maskY	536870911
maskX	1073741823
maskZ	2147483647
maxZ	2040109466
maxY	1932735283
maxX	1503238554
sfrX	30
sfrZ	31
sfrY	29
offsetX	-107374182
offsetZ	53687091
offsetY	322122547
gainXsfr	30
gainZsfr	30
gainX	1431655765
gainZ	1160801972
Table	[1x135]
gainY	1431655765
sizeX	5
minY	-1288490189
minX	-1717986918
minZ	-1932735283
idxOffsetY	4
idxOffsetX	2
sizeY	9
idxOffsetZ	1
sizeXY	45
gainYsfr	30
Exp. maskY	536870911

Test settings	
Tolerance maskY	±0,0000e+00
Tolerance maskX	±0,0000e+00
Tolerance maskZ	±0,0000e+00
Tolerance maxZ	±0,0000e+00
Tolerance maxY	±0,0000e+00
Tolerance maxX	±0,0000e+00
Tolerance sfrX	±0,0000e+00
Tolerance sfrZ	±0,0000e+00
Tolerance sfrY	±0,0000e+00
Tolerance offsetX	±0,0000e+00
Tolerance offsetZ	±0,0000e+00
Tolerance offsetY	±0,0000e+00
Tolerance gainXsfr	±0,0000e+00
Tolerance gainZsfr	±0,0000e+00
Tolerance gainX	±0,0000e+00
Tolerance gainZ	±0,0000e+00
Tolerance Table	±0,0000e+00
Tolerance gainY	±0,0000e+00
Tolerance sizeX	±0,0000e+00
Tolerance minY	±0,0000e+00
Tolerance minX	±0,0000e+00
Tolerance minZ	±0,0000e+00
Tolerance idxOffsetY	±0,0000e+00
Tolerance idxOffsetX	±0,0000e+00
Tolerance sizeY	±0,0000e+00
Tolerance idxOffsetZ	±0,0000e+00
Tolerance sizeXY	±0,0000e+00
Tolerance gainYsfr	±0,0000e+00

Verification: LookupTable3D FiP32 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for General block LookupTable3D.

Test results				
Time step	1	2	...	19
CPU cycles	1015	1015	...	1087
Inputs				
x (DSP)	-2147483648	-1908874354	...	2147483647
y (DSP)	-1932735283	-1729917383	...	1717986918
z (DSP)	-1717986918	-1539029948	...	1503238554
x	-1	-0.889	...	1
y	-0.9	-0.806	...	0.8
z	-0.8	-0.717	...	0.7
Parameters				
TableData	[1x765]			
DimX	9			
x_min	-0.8			
x_max	0.7			
DimY	17			
y_max	0.9			
y_min	-0.6			
DimZ	5			
z_min	-0.9			
z_max	0.95			
Outputs				
Out	0.56	0.502	...	0.525
Exp. Out	0.56	0.502	...	0.525
Out (DSP)	1202590840	1077320961	...	1127428909
Exp. Out (DSP)	1202590843	1077320963	...	1127428915

Test settings	
Tolerance Out	±4,6566e-09 (±10 LSB)

Test statistics	
Min CPU cycles	1015
Max CPU cycles	1143
Avg CPU cycles	1113

Test case: Conversion test **OK**

Conversion test for General block LookupTable3D.

Test results	
Time step	1
Mask parameters	
TableData	[1x135]
DimX	5
x_min	-0.8
x_max	0.7
DimY	9
y_max	0.9
y_min	-0.6
DimZ	3
z_min	-0.9
z_max	0.95
Controller parameters	
maskY	536870911
maskX	1073741823
maskZ	2147483647
maxZ	2040109466
maxY	1932735283
maxX	1503238554
sfrX	30
sfrZ	31
sfrY	29
offsetX	-107374182
offsetZ	53687091
offsetY	322122547
gainXsfr	30
gainZsfr	30
gainX	1431655765
gainZ	1160801972
Table	[1x135]
gainY	1431655765
sizeX	5
minY	-1288490189
minX	-1717986918
minZ	-1932735283
idxOffsetY	4
idxOffsetX	2
sizeY	9
idxOffsetZ	1
sizeXY	45
gainYsfr	30
Exp. maskY	536870911

Test settings	
Tolerance maskY	±0,0000e+00
Tolerance maskX	±0,0000e+00
Tolerance maskZ	±0,0000e+00
Tolerance maxZ	±0,0000e+00
Tolerance maxY	±0,0000e+00
Tolerance maxX	±0,0000e+00
Tolerance sfrX	±0,0000e+00
Tolerance sfrZ	±0,0000e+00
Tolerance sfrY	±0,0000e+00
Tolerance offsetX	±0,0000e+00
Tolerance offsetZ	±0,0000e+00
Tolerance offsetY	±0,0000e+00
Tolerance gainXsfr	±0,0000e+00
Tolerance gainZsfr	±0,0000e+00
Tolerance gainX	±0,0000e+00
Tolerance gainZ	±0,0000e+00
Tolerance Table	±0,0000e+00
Tolerance gainY	±0,0000e+00
Tolerance sizeX	±0,0000e+00
Tolerance minY	±0,0000e+00
Tolerance minX	±0,0000e+00
Tolerance minZ	±0,0000e+00
Tolerance idxOffsetY	±0,0000e+00
Tolerance idxOffsetX	±0,0000e+00
Tolerance sizeY	±0,0000e+00
Tolerance idxOffsetZ	±0,0000e+00
Tolerance sizeXY	±0,0000e+00
Tolerance gainYsfr	±0,0000e+00

Verification: LookupTable3D FiP32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for General block LookupTable3D.

Test results				
Time step	1	2	...	19
CPU cycles	830	830	...	863
Inputs				
x (DSP)	-2147483648	-1908874354	...	2147483647
y (DSP)	-1932735283	-1729917383	...	1717986918
z (DSP)	-1717986918	-1539029948	...	1503238554
x	-1	-0.889	...	1
y	-0.9	-0.806	...	0.8
z	-0.8	-0.717	...	0.7
Parameters				
TableData	[1x765]			
DimX	9			
x_min	-0.8			
x_max	0.7			
DimY	17			
y_max	0.9			
y_min	-0.6			
DimZ	5			
z_min	-0.9			
z_max	0.95			
Outputs				
Out	0.56	0.502	...	0.525
Exp. Out	0.56	0.502	...	0.525
Out (DSP)	1202590840	1077320961	...	1127428909
Exp. Out (DSP)	1202590843	1077320963	...	1127428915

Test settings	
Tolerance Out	±4,6566e-09 (±10 LSB)

Test statistics	
Min CPU cycles	830
Max CPU cycles	900
Avg CPU cycles	882

Test case: Conversion test **OK**

Conversion test for General block LookupTable3D.

Test results	
Time step	1
Mask parameters	
TableData	[1x135]
DimX	5
x_min	-0.8
x_max	0.7
DimY	9
y_max	0.9
y_min	-0.6
DimZ	3
z_min	-0.9
z_max	0.95
Controller parameters	
maskY	536870911
maskX	1073741823
maskZ	2147483647
maxZ	2040109466
maxY	1932735283
maxX	1503238554
sfrX	30
sfrZ	31
sfrY	29
offsetX	-107374182
offsetZ	53687091
offsetY	322122547
gainXsfr	30
gainZsfr	30
gainX	1431655765
gainZ	1160801972
Table	[1x135]
gainY	1431655765
sizeX	5
minY	-1288490189
minX	-1717986918
minZ	-1932735283
idxOffsetY	4
idxOffsetX	2
sizeY	9
idxOffsetZ	1
sizeXY	45
gainYsfr	30
Exp. maskY	536870911

Test settings	
Tolerance maskY	±0,0000e+00
Tolerance maskX	±0,0000e+00
Tolerance maskZ	±0,0000e+00
Tolerance maxZ	±0,0000e+00
Tolerance maxY	±0,0000e+00
Tolerance maxX	±0,0000e+00
Tolerance sfrX	±0,0000e+00
Tolerance sfrZ	±0,0000e+00
Tolerance sfrY	±0,0000e+00
Tolerance offsetX	±0,0000e+00
Tolerance offsetZ	±0,0000e+00
Tolerance offsetY	±0,0000e+00
Tolerance gainXsfr	±0,0000e+00
Tolerance gainZsfr	±0,0000e+00
Tolerance gainX	±0,0000e+00
Tolerance gainZ	±0,0000e+00
Tolerance Table	±0,0000e+00
Tolerance gainY	±0,0000e+00
Tolerance sizeX	±0,0000e+00
Tolerance minY	±0,0000e+00
Tolerance minX	±0,0000e+00
Tolerance minZ	±0,0000e+00
Tolerance idxOffsetY	±0,0000e+00
Tolerance idxOffsetX	±0,0000e+00
Tolerance sizeY	±0,0000e+00
Tolerance idxOffsetZ	±0,0000e+00
Tolerance sizeXY	±0,0000e+00
Tolerance gainYsfr	±0,0000e+00

Verification: LookupTable3D FiP32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for General block LookupTable3D.

Test results				
Time step	1	2	...	19
CPU cycles	1713	1713	...	1824
Inputs				
x (DSP)	-2147483648	-1908874354	...	2147483647
y (DSP)	-1932735283	-1729917383	...	1717986918
z (DSP)	-1717986918	-1539029948	...	1503238554
x	-1	-0.889	...	1
y	-0.9	-0.806	...	0.8
z	-0.8	-0.717	...	0.7
Parameters				
TableData	[1x765]			
DimX	9			
x_min	-0.8			
x_max	0.7			
DimY	17			
y_max	0.9			
y_min	-0.6			
DimZ	5			
z_min	-0.9			
z_max	0.95			
Outputs				
Out	0.56	0.502	...	0.525
Exp. Out	0.56	0.502	...	0.525
Out (DSP)	1202590840	1077320961	...	1127428909
Exp. Out (DSP)	1202590843	1077320963	...	1127428915

Test settings	
Tolerance Out	±4,6566e-09 (±10 LSB)

Test statistics	
Min CPU cycles	1713
Max CPU cycles	1919
Avg CPU cycles	1870

Test case: Conversion test **OK**

Conversion test for General block LookupTable3D.

Test results	
Time step	1
Mask parameters	
TableData	[1x135]
DimX	5
x_min	-0.8
x_max	0.7
DimY	9
y_max	0.9
y_min	-0.6
DimZ	3
z_min	-0.9
z_max	0.95
Controller parameters	
maskY	536870911
maskX	1073741823
maskZ	2147483647
maxZ	2040109466
maxY	1932735283
maxX	1503238554
sfrX	30
sfrZ	31
sfrY	29
offsetX	-107374182
offsetZ	53687091
offsetY	322122547
gainXsfr	30
gainZsfr	30
gainX	1431655765
gainZ	1160801972
Table	[1x135]
gainY	1431655765
sizeX	5
minY	-1288490189
minX	-1717986918
minZ	-1932735283
idxOffsetY	4
idxOffsetX	2
sizeY	9
idxOffsetZ	1
sizeXY	45
gainYsfr	30
Exp. maskY	536870911

Test settings	
Tolerance maskY	±0,0000e+00
Tolerance maskX	±0,0000e+00
Tolerance maskZ	±0,0000e+00
Tolerance maxZ	±0,0000e+00
Tolerance maxY	±0,0000e+00
Tolerance maxX	±0,0000e+00
Tolerance sfrX	±0,0000e+00
Tolerance sfrZ	±0,0000e+00
Tolerance sfrY	±0,0000e+00
Tolerance offsetX	±0,0000e+00
Tolerance offsetZ	±0,0000e+00
Tolerance offsetY	±0,0000e+00
Tolerance gainXsfr	±0,0000e+00
Tolerance gainZsfr	±0,0000e+00
Tolerance gainX	±0,0000e+00
Tolerance gainZ	±0,0000e+00
Tolerance Table	±0,0000e+00
Tolerance gainY	±0,0000e+00
Tolerance sizeX	±0,0000e+00
Tolerance minY	±0,0000e+00
Tolerance minX	±0,0000e+00
Tolerance minZ	±0,0000e+00
Tolerance idxOffsetY	±0,0000e+00
Tolerance idxOffsetX	±0,0000e+00
Tolerance sizeY	±0,0000e+00
Tolerance idxOffsetZ	±0,0000e+00
Tolerance sizeXY	±0,0000e+00
Tolerance gainYsfr	±0,0000e+00

Verification: LookupTable3D FiP32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for General block LookupTable3D.

Test results				
Time step	1	2	...	19
CPU cycles	672	672	...	724
Inputs				
x (DSP)	-2147483648	-1908874354	...	2147483647
y (DSP)	-1932735283	-1729917383	...	1717986918
z (DSP)	-1717986918	-1539029948	...	1503238554
x	-1	-0.889	...	1
y	-0.9	-0.806	...	0.8
z	-0.8	-0.717	...	0.7
Parameters				
TableData	[1x765]			
DimX	9			
x_min	-0.8			
x_max	0.7			
DimY	17			
y_max	0.9			
y_min	-0.6			
DimZ	5			
z_min	-0.9			
z_max	0.95			
Outputs				
Out	0.56	0.502	...	0.525
Exp. Out	0.56	0.502	...	0.525
Out (DSP)	1202590840	1077320961	...	1127428909
Exp. Out (DSP)	1202590843	1077320963	...	1127428915

Test settings	
Tolerance Out	±4,6566e-09 (±10 LSB)

Test statistics	
Min CPU cycles	672
Max CPU cycles	758
Avg CPU cycles	739

Test case: Conversion test **OK**

Conversion test for General block LookupTable3D.

Test results	
Time step	1
Mask parameters	
TableData	[1x135]
DimX	5
x_min	-0.8
x_max	0.7
DimY	9
y_max	0.9
y_min	-0.6
DimZ	3
z_min	-0.9
z_max	0.95
Controller parameters	
maskY	536870911
maskX	1073741823
maskZ	2147483647
maxZ	2040109466
maxY	1932735283
maxX	1503238554
sfrX	30
sfrZ	31
sfrY	29
offsetX	-107374182
offsetZ	53687091
offsetY	322122547
gainXsfr	30
gainZsfr	30
gainX	1431655765
gainZ	1160801972
Table	[1x135]
gainY	1431655765
sizeX	5
minY	-1288490189
minX	-1717986918
minZ	-1932735283
idxOffsetY	4
idxOffsetX	2
sizeY	9
idxOffsetZ	1
sizeXY	45
gainYsfr	30
Exp. maskY	536870911

Test settings	
Tolerance maskY	±0,0000e+00
Tolerance maskX	±0,0000e+00
Tolerance maskZ	±0,0000e+00
Tolerance maxZ	±0,0000e+00
Tolerance maxY	±0,0000e+00
Tolerance maxX	±0,0000e+00
Tolerance sfrX	±0,0000e+00
Tolerance sfrZ	±0,0000e+00
Tolerance sfrY	±0,0000e+00
Tolerance offsetX	±0,0000e+00
Tolerance offsetZ	±0,0000e+00
Tolerance offsetY	±0,0000e+00
Tolerance gainXsfr	±0,0000e+00
Tolerance gainZsfr	±0,0000e+00
Tolerance gainX	±0,0000e+00
Tolerance gainZ	±0,0000e+00
Tolerance Table	±0,0000e+00
Tolerance gainY	±0,0000e+00
Tolerance sizeX	±0,0000e+00
Tolerance minY	±0,0000e+00
Tolerance minX	±0,0000e+00
Tolerance minZ	±0,0000e+00
Tolerance idxOffsetY	±0,0000e+00
Tolerance idxOffsetX	±0,0000e+00
Tolerance sizeY	±0,0000e+00
Tolerance idxOffsetZ	±0,0000e+00
Tolerance sizeXY	±0,0000e+00
Tolerance gainYsfr	±0,0000e+00

Verification: LookupTable3D FiP32 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for General block LookupTable3D.

Test results				
Time step	1	2	...	19
CPU cycles	5802	5802	...	6219
Inputs				
x (DSP)	-2147483648	-1908874354	...	2147483647
y (DSP)	-1932735283	-1729917383	...	1717986918
z (DSP)	-1717986918	-1539029948	...	1503238554
x	-1	-0.889	...	1
y	-0.9	-0.806	...	0.8
z	-0.8	-0.717	...	0.7
Parameters				
TableData	[1x765]			
DimX	9			
x_min	-0.8			
x_max	0.7			
DimY	17			
y_max	0.9			
y_min	-0.6			
DimZ	5			
z_min	-0.9			
z_max	0.95			
Outputs				
Out	0.56	0.502	...	0.525
Exp. Out	0.56	0.502	...	0.525
Out (DSP)	1202590840	1077320961	...	1127428909
Exp. Out (DSP)	1202590843	1077320963	...	1127428915

Test settings	
Tolerance Out	±4,6566e-09 (±10 LSB)

Test statistics	
Min CPU cycles	5802
Max CPU cycles	6679
Avg CPU cycles	6445

Test case: Conversion test **OK**

Conversion test for General block LookupTable3D.

Test results	
Time step	1
Mask parameters	
TableData	[1x135]
DimX	5
x_min	-0.8
x_max	0.7
DimY	9
y_max	0.9
y_min	-0.6
DimZ	3
z_min	-0.9
z_max	0.95
Controller parameters	
maskY	536870911
maskX	1073741823
maskZ	2147483647
maxZ	2040109466
maxY	1932735283
maxX	1503238554
sfrX	30
sfrZ	31
sfrY	29
offsetX	-107374182
offsetZ	53687091
offsetY	322122547
gainXsfr	30
gainZsfr	30
gainX	1431655765
gainZ	1160801972
Table	[1x135]
gainY	1431655765
sizeX	5
minY	-1288490189
minX	-1717986918
minZ	-1932735283
idxOffsetY	4
idxOffsetX	2
sizeY	9
idxOffsetZ	1
sizeXY	45
gainYsfr	30
Exp. maskY	536870911

Test settings	
Tolerance maskY	±0,0000e+00
Tolerance maskX	±0,0000e+00
Tolerance maskZ	±0,0000e+00
Tolerance maxZ	±0,0000e+00
Tolerance maxY	±0,0000e+00
Tolerance maxX	±0,0000e+00
Tolerance sfrX	±0,0000e+00
Tolerance sfrZ	±0,0000e+00
Tolerance sfrY	±0,0000e+00
Tolerance offsetX	±0,0000e+00
Tolerance offsetZ	±0,0000e+00
Tolerance offsetY	±0,0000e+00
Tolerance gainXsfr	±0,0000e+00
Tolerance gainZsfr	±0,0000e+00
Tolerance gainX	±0,0000e+00
Tolerance gainZ	±0,0000e+00
Tolerance Table	±0,0000e+00
Tolerance gainY	±0,0000e+00
Tolerance sizeX	±0,0000e+00
Tolerance minY	±0,0000e+00
Tolerance minX	±0,0000e+00
Tolerance minZ	±0,0000e+00
Tolerance idxOffsetY	±0,0000e+00
Tolerance idxOffsetX	±0,0000e+00
Tolerance sizeY	±0,0000e+00
Tolerance idxOffsetZ	±0,0000e+00
Tolerance sizeXY	±0,0000e+00
Tolerance gainYsfr	±0,0000e+00

Verification: LookupTable3D FiP32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for General block LookupTable3D.

Test results				
Time step	1	2	...	19
CPU cycles	1005	849	...	877
Inputs				
x (DSP)	-2147483648	-1908874354	...	2147483647
y (DSP)	-1932735283	-1729917383	...	1717986918
z (DSP)	-1717986918	-1539029948	...	1503238554
x	-1	-0.889	...	1
y	-0.9	-0.806	...	0.8
z	-0.8	-0.717	...	0.7
Parameters				
TableData	[1x765]			
DimX	9			
x_min	-0.8			
x_max	0.7			
DimY	17			
y_max	0.9			
y_min	-0.6			
DimZ	5			
z_min	-0.9			
z_max	0.95			
Outputs				
Out	0.56	0.502	...	0.525
Exp. Out	0.56	0.502	...	0.525
Out (DSP)	1202590840	1077320961	...	1127428909
Exp. Out (DSP)	1202590843	1077320963	...	1127428915

Test settings	
Tolerance Out	±4,6566e-09 (±10 LSB)

Test statistics	
Min CPU cycles	849
Max CPU cycles	1005
Avg CPU cycles	896

Test case: Conversion test **OK**

Conversion test for General block LookupTable3D.

Test results	
Time step	1
Mask parameters	
TableData	[1x135]
DimX	5
x_min	-0.8
x_max	0.7
DimY	9
y_max	0.9
y_min	-0.6
DimZ	3
z_min	-0.9
z_max	0.95
Controller parameters	
maskY	536870911
maskX	1073741823
maskZ	2147483647
maxZ	2040109466
maxY	1932735283
maxX	1503238554
sfrX	30
sfrZ	31
sfrY	29
offsetX	-107374182
offsetZ	53687091
offsetY	322122547
gainXsfr	30
gainZsfr	30
gainX	1431655765
gainZ	1160801972
Table	[1x135]
gainY	1431655765
sizeX	5
minY	-1288490189
minX	-1717986918
minZ	-1932735283
idxOffsetY	4
idxOffsetX	2
sizeY	9
idxOffsetZ	1
sizeXY	45
gainYsfr	30
Exp. maskY	536870911

Test settings	
Tolerance maskY	±0,0000e+00
Tolerance maskX	±0,0000e+00
Tolerance maskZ	±0,0000e+00
Tolerance maxZ	±0,0000e+00
Tolerance maxY	±0,0000e+00
Tolerance maxX	±0,0000e+00
Tolerance sfrX	±0,0000e+00
Tolerance sfrZ	±0,0000e+00
Tolerance sfrY	±0,0000e+00
Tolerance offsetX	±0,0000e+00
Tolerance offsetZ	±0,0000e+00
Tolerance offsetY	±0,0000e+00
Tolerance gainXsfr	±0,0000e+00
Tolerance gainZsfr	±0,0000e+00
Tolerance gainX	±0,0000e+00
Tolerance gainZ	±0,0000e+00
Tolerance Table	±0,0000e+00
Tolerance gainY	±0,0000e+00
Tolerance sizeX	±0,0000e+00
Tolerance minY	±0,0000e+00
Tolerance minX	±0,0000e+00
Tolerance minZ	±0,0000e+00
Tolerance idxOffsetY	±0,0000e+00
Tolerance idxOffsetX	±0,0000e+00
Tolerance sizeY	±0,0000e+00
Tolerance idxOffsetZ	±0,0000e+00
Tolerance sizeXY	±0,0000e+00
Tolerance gainYsfr	±0,0000e+00

Verification: LookupTable3D FiP32 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for General block LookupTable3D.

Test results				
Time step	1	2	...	19
CPU cycles	586	586	...	635
Inputs				
x (DSP)	-2147483648	-1908874354	...	2147483647
y (DSP)	-1932735283	-1729917383	...	1717986918
z (DSP)	-1717986918	-1539029948	...	1503238554
x	-1	-0.889	...	1
y	-0.9	-0.806	...	0.8
z	-0.8	-0.717	...	0.7
Parameters				
TableData	[1x765]			
DimX	9			
x_min	-0.8			
x_max	0.7			
DimY	17			
y_max	0.9			
y_min	-0.6			
DimZ	5			
z_min	-0.9			
z_max	0.95			
Outputs				
Out	0.56	0.502	...	0.525
Exp. Out	0.56	0.502	...	0.525
Out (DSP)	1202590840	1077320961	...	1127428909
Exp. Out (DSP)	1202590843	1077320963	...	1127428915

Test settings	
Tolerance Out	±4,6566e-09 (±10 LSB)

Test statistics	
Min CPU cycles	586
Max CPU cycles	650
Avg CPU cycles	636

Test case: Conversion test **OK**

Conversion test for General block LookupTable3D.

Test results	
Time step	1
Mask parameters	
TableData	[1x135]
DimX	5
x_min	-0.8
x_max	0.7
DimY	9
y_max	0.9
y_min	-0.6
DimZ	3
z_min	-0.9
z_max	0.95
Controller parameters	
maskY	536870911
maskX	1073741823
maskZ	2147483647
maxZ	2040109466
maxY	1932735283
maxX	1503238554
sfrX	30
sfrZ	31
sfrY	29
offsetX	-107374182
offsetZ	53687091
offsetY	322122547
gainXsfr	30
gainZsfr	30
gainX	1431655765
gainZ	1160801972
Table	[1x135]
gainY	1431655765
sizeX	5
minY	-1288490189
minX	-1717986918
minZ	-1932735283
idxOffsetY	4
idxOffsetX	2
sizeY	9
idxOffsetZ	1
sizeXY	45
gainYsfr	30
Exp. maskY	536870911

Test settings	
Tolerance maskY	±0,0000e+00
Tolerance maskX	±0,0000e+00
Tolerance maskZ	±0,0000e+00
Tolerance maxZ	±0,0000e+00
Tolerance maxY	±0,0000e+00
Tolerance maxX	±0,0000e+00
Tolerance sfrX	±0,0000e+00
Tolerance sfrZ	±0,0000e+00
Tolerance sfrY	±0,0000e+00
Tolerance offsetX	±0,0000e+00
Tolerance offsetZ	±0,0000e+00
Tolerance offsetY	±0,0000e+00
Tolerance gainXsfr	±0,0000e+00
Tolerance gainZsfr	±0,0000e+00
Tolerance gainX	±0,0000e+00
Tolerance gainZ	±0,0000e+00
Tolerance Table	±0,0000e+00
Tolerance gainY	±0,0000e+00
Tolerance sizeX	±0,0000e+00
Tolerance minY	±0,0000e+00
Tolerance minX	±0,0000e+00
Tolerance minZ	±0,0000e+00
Tolerance idxOffsetY	±0,0000e+00
Tolerance idxOffsetX	±0,0000e+00
Tolerance sizeY	±0,0000e+00
Tolerance idxOffsetZ	±0,0000e+00
Tolerance sizeXY	±0,0000e+00
Tolerance gainYsfr	±0,0000e+00

Verification: LookupTable3D Float32 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for General block LookupTable3D.

Test results				
Time step	1	2	...	19
CPU cycles	346	346	...	349
Inputs				
x (DSP)	-1.1	-0.978	...	1.1
y (DSP)	-1.35	-1.208	...	1.2
z (DSP)	-2.16	-1.935	...	1.89
x	-1.1	-0.978	...	1.1
y	-1.35	-1.208	...	1.2
z	-2.16	-1.935	...	1.89
Parameters				
TableData	[1x765]			
DimX	9			
x_min	-0.8			
x_max	0.7			
DimY	17			
y_max	0.9			
y_min	-0.6			
DimZ	5			
z_min	-0.9			
z_max	0.95			
Outputs				
Out	1.953	1.953	...	2.356
Exp. Out	1.953	1.953	...	2.356
Out (DSP)	1.953	1.953	...	2.356
Exp. Out (DSP)	1.953	1.953	...	2.356

Test settings	
Tolerance Out	±9,3132e-07 (±2000 LSB)

Test statistics	
Min CPU cycles	346
Max CPU cycles	349
Avg CPU cycles	348

Test case: Conversion test **OK**

Conversion test for General block LookupTable3D.

Test results	
Time step	1
Mask parameters	
TableData	[1x135]
DimX	5
x_min	-0.8
x_max	0.7
DimY	9
y_max	0.9
y_min	-0.6
DimZ	3
z_min	-0.9
z_max	0.95
Controller parameters	
gainX	2.667
gainZ	1.081
Table	[1x135]
gainY	5.333
maxZ	0.95
maxY	0.9
maxX	0.7
offsetX	-0.8
sizeX	5
offsetZ	-0.9
offsetY	-0.6
minY	-0.6
minX	-0.8
minZ	-0.9
dimZ	2
dimY	8
sizeY	9
dimX	4
sizeXY	45
Exp. gainX	2.667
Exp. gainZ	1.081
Exp. Table	[1x135]
Exp. gainY	5.333
Exp. maxZ	0.95
Exp. maxY	0.9
Exp. maxX	0.7
Exp. offsetX	-0.8
Exp. sizeX	5
Exp. offsetZ	-0.9

Test settings	
Tolerance gainX	±0,0000e+00
Tolerance gainZ	±0,0000e+00
Tolerance Table	±0,0000e+00
Tolerance gainY	±0,0000e+00
Tolerance maxZ	±0,0000e+00
Tolerance maxY	±0,0000e+00
Tolerance maxX	±0,0000e+00
Tolerance offsetX	±0,0000e+00
Tolerance sizeX	±0,0000e+00
Tolerance offsetZ	±0,0000e+00
Tolerance offsetY	±0,0000e+00
Tolerance minY	±0,0000e+00
Tolerance minX	±0,0000e+00
Tolerance minZ	±0,0000e+00
Tolerance dimZ	±0,0000e+00
Tolerance dimY	±0,0000e+00
Tolerance sizeY	±0,0000e+00
Tolerance dimX	±0,0000e+00
Tolerance sizeXY	±0,0000e+00

Verification: LookupTable3D Float32 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for General block LookupTable3D.

Test results				
Time step	1	2	...	19
CPU cycles	249	249	...	277
Inputs				
x (DSP)	-1.1	-0.978	...	1.1
y (DSP)	-1.35	-1.208	...	1.2
z (DSP)	-2.16	-1.935	...	1.89
x	-1.1	-0.978	...	1.1
y	-1.35	-1.208	...	1.2
z	-2.16	-1.935	...	1.89
Parameters				
TableData	[1x765]			
DimX	9			
x_min	-0.8			
x_max	0.7			
DimY	17			
y_max	0.9			
y_min	-0.6			
DimZ	5			
z_min	-0.9			
z_max	0.95			
Outputs				
Out	1.953	1.953	...	2.356
Exp. Out	1.953	1.953	...	2.356
Out (DSP)	1.953	1.953	...	2.356
Exp. Out (DSP)	1.953	1.953	...	2.356

Test settings	
Tolerance Out	±9,3132e-07 (±2000 LSB)

Test statistics	
Min CPU cycles	249
Max CPU cycles	277
Avg CPU cycles	266

Test case: Conversion test **OK**

Conversion test for General block LookupTable3D.

Test results	
Time step	1
Mask parameters	
TableData	[1x135]
DimX	5
x_min	-0.8
x_max	0.7
DimY	9
y_max	0.9
y_min	-0.6
DimZ	3
z_min	-0.9
z_max	0.95
Controller parameters	
gainX	2.667
gainZ	1.081
Table	[1x135]
gainY	5.333
maxZ	0.95
maxY	0.9
maxX	0.7
offsetX	-0.8
sizeX	5
offsetZ	-0.9
offsetY	-0.6
minY	-0.6
minX	-0.8
minZ	-0.9
dimZ	2
dimY	8
sizeY	9
dimX	4
sizeXY	45
Exp. gainX	2.667
Exp. gainZ	1.081
Exp. Table	[1x135]
Exp. gainY	5.333
Exp. maxZ	0.95
Exp. maxY	0.9
Exp. maxX	0.7
Exp. offsetX	-0.8
Exp. sizeX	5
Exp. offsetZ	-0.9

Test settings	
Tolerance gainX	±0,0000e+00
Tolerance gainZ	±0,0000e+00
Tolerance Table	±0,0000e+00
Tolerance gainY	±0,0000e+00
Tolerance maxZ	±0,0000e+00
Tolerance maxY	±0,0000e+00
Tolerance maxX	±0,0000e+00
Tolerance offsetX	±0,0000e+00
Tolerance sizeX	±0,0000e+00
Tolerance offsetZ	±0,0000e+00
Tolerance offsetY	±0,0000e+00
Tolerance minY	±0,0000e+00
Tolerance minX	±0,0000e+00
Tolerance minZ	±0,0000e+00
Tolerance dimZ	±0,0000e+00
Tolerance dimY	±0,0000e+00
Tolerance sizeY	±0,0000e+00
Tolerance dimX	±0,0000e+00
Tolerance sizeXY	±0,0000e+00

Verification: LookupTable3D Float32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for General block LookupTable3D.

Test results				
Time step	1	2	...	19
CPU cycles	371	371	...	376
Inputs				
x (DSP)	-1.1	-0.978	...	1.1
y (DSP)	-1.35	-1.208	...	1.2
z (DSP)	-2.16	-1.935	...	1.89
x	-1.1	-0.978	...	1.1
y	-1.35	-1.208	...	1.2
z	-2.16	-1.935	...	1.89
Parameters				
TableData	[1x765]			
DimX	9			
x_min	-0.8			
x_max	0.7			
DimY	17			
y_max	0.9			
y_min	-0.6			
DimZ	5			
z_min	-0.9			
z_max	0.95			
Outputs				
Out	1.953	1.953	...	2.356
Exp. Out	1.953	1.953	...	2.356
Out (DSP)	1.953	1.953	...	2.356
Exp. Out (DSP)	1.953	1.953	...	2.356

Test settings	
Tolerance Out	±9,3132e-07 (±2000 LSB)

Test statistics	
Min CPU cycles	371
Max CPU cycles	376
Avg CPU cycles	375

Test case: Conversion test **OK**

Conversion test for General block LookupTable3D.

Test results	
Time step	1
Mask parameters	
TableData	[1x135]
DimX	5
x_min	-0.8
x_max	0.7
DimY	9
y_max	0.9
y_min	-0.6
DimZ	3
z_min	-0.9
z_max	0.95
Controller parameters	
gainX	2.667
gainZ	1.081
Table	[1x135]
gainY	5.333
maxZ	0.95
maxY	0.9
maxX	0.7
offsetX	-0.8
sizeX	5
offsetZ	-0.9
offsetY	-0.6
minY	-0.6
minX	-0.8
minZ	-0.9
dimZ	2
dimY	8
sizeY	9
dimX	4
sizeXY	45
Exp. gainX	2.667
Exp. gainZ	1.081
Exp. Table	[1x135]
Exp. gainY	5.333
Exp. maxZ	0.95
Exp. maxY	0.9
Exp. maxX	0.7
Exp. offsetX	-0.8
Exp. sizeX	5
Exp. offsetZ	-0.9

Test settings	
Tolerance gainX	±0,0000e+00
Tolerance gainZ	±0,0000e+00
Tolerance Table	±0,0000e+00
Tolerance gainY	±0,0000e+00
Tolerance maxZ	±0,0000e+00
Tolerance maxY	±0,0000e+00
Tolerance maxX	±0,0000e+00
Tolerance offsetX	±0,0000e+00
Tolerance sizeX	±0,0000e+00
Tolerance offsetZ	±0,0000e+00
Tolerance offsetY	±0,0000e+00
Tolerance minY	±0,0000e+00
Tolerance minX	±0,0000e+00
Tolerance minZ	±0,0000e+00
Tolerance dimZ	±0,0000e+00
Tolerance dimY	±0,0000e+00
Tolerance sizeY	±0,0000e+00
Tolerance dimX	±0,0000e+00
Tolerance sizeXY	±0,0000e+00

Verification: LookupTable3D Float32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for General block LookupTable3D.

Test results				
Time step	1	2	...	19
CPU cycles	6805	6748	...	7046
Inputs				
x (DSP)	-1.1	-0.978	...	1.1
y (DSP)	-1.35	-1.208	...	1.2
z (DSP)	-2.16	-1.935	...	1.89
x	-1.1	-0.978	...	1.1
y	-1.35	-1.208	...	1.2
z	-2.16	-1.935	...	1.89
Parameters				
TableData	[1x765]			
DimX	9			
x_min	-0.8			
x_max	0.7			
DimY	17			
y_max	0.9			
y_min	-0.6			
DimZ	5			
z_min	-0.9			
z_max	0.95			
Outputs				
Out	1.953	1.953	...	2.356
Exp. Out	1.953	1.953	...	2.356
Out (DSP)	1.953	1.953	...	2.356
Exp. Out (DSP)	1.953	1.953	...	2.356

Test settings	
Tolerance Out	±9,3132e-07 (±2000 LSB)

Test statistics	
Min CPU cycles	6748
Max CPU cycles	8744
Avg CPU cycles	7726

Test case: Conversion test **OK**

Conversion test for General block LookupTable3D.

Test results	
Time step	1
Mask parameters	
TableData	[1x135]
DimX	5
x_min	-0.8
x_max	0.7
DimY	9
y_max	0.9
y_min	-0.6
DimZ	3
z_min	-0.9
z_max	0.95
Controller parameters	
gainX	2.667
gainZ	1.081
Table	[1x135]
gainY	5.333
maxZ	0.95
maxY	0.9
maxX	0.7
offsetX	-0.8
sizeX	5
offsetZ	-0.9
offsetY	-0.6
minY	-0.6
minX	-0.8
minZ	-0.9
dimZ	2
dimY	8
sizeY	9
dimX	4
sizeXY	45
Exp. gainX	2.667
Exp. gainZ	1.081
Exp. Table	[1x135]
Exp. gainY	5.333
Exp. maxZ	0.95
Exp. maxY	0.9
Exp. maxX	0.7
Exp. offsetX	-0.8
Exp. sizeX	5
Exp. offsetZ	-0.9

Test settings	
Tolerance gainX	±0,0000e+00
Tolerance gainZ	±0,0000e+00
Tolerance Table	±0,0000e+00
Tolerance gainY	±0,0000e+00
Tolerance maxZ	±0,0000e+00
Tolerance maxY	±0,0000e+00
Tolerance maxX	±0,0000e+00
Tolerance offsetX	±0,0000e+00
Tolerance sizeX	±0,0000e+00
Tolerance offsetZ	±0,0000e+00
Tolerance offsetY	±0,0000e+00
Tolerance minY	±0,0000e+00
Tolerance minX	±0,0000e+00
Tolerance minZ	±0,0000e+00
Tolerance dimZ	±0,0000e+00
Tolerance dimY	±0,0000e+00
Tolerance sizeY	±0,0000e+00
Tolerance dimX	±0,0000e+00
Tolerance sizeXY	±0,0000e+00

Verification: LookupTable3D Float32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for General block LookupTable3D.

Test results				
Time step	1	2	...	19
CPU cycles	2531	2531	...	2839
Inputs				
x (DSP)	-1.1	-0.978	...	1.1
y (DSP)	-1.35	-1.208	...	1.2
z (DSP)	-2.16	-1.935	...	1.89
x	-1.1	-0.978	...	1.1
y	-1.35	-1.208	...	1.2
z	-2.16	-1.935	...	1.89
Parameters				
TableData	[1x765]			
DimX	9			
x_min	-0.8			
x_max	0.7			
DimY	17			
y_max	0.9			
y_min	-0.6			
DimZ	5			
z_min	-0.9			
z_max	0.95			
Outputs				
Out	1.953	1.953	...	2.356
Exp. Out	1.953	1.953	...	2.356
Out (DSP)	1.953	1.953	...	2.356
Exp. Out (DSP)	1.953	1.953	...	2.356

Test settings	
Tolerance Out	±9,3132e-07 (±2000 LSB)

Test statistics	
Min CPU cycles	2531
Max CPU cycles	3299
Avg CPU cycles	2957

Test case: Conversion test **OK**

Conversion test for General block LookupTable3D.

Test results	
Time step	1
Mask parameters	
TableData	[1x135]
DimX	5
x_min	-0.8
x_max	0.7
DimY	9
y_max	0.9
y_min	-0.6
DimZ	3
z_min	-0.9
z_max	0.95
Controller parameters	
gainX	2.667
gainZ	1.081
Table	[1x135]
gainY	5.333
maxZ	0.95
maxY	0.9
maxX	0.7
offsetX	-0.8
sizeX	5
offsetZ	-0.9
offsetY	-0.6
minY	-0.6
minX	-0.8
minZ	-0.9
dimZ	2
dimY	8
sizeY	9
dimX	4
sizeXY	45
Exp. gainX	2.667
Exp. gainZ	1.081
Exp. Table	[1x135]
Exp. gainY	5.333
Exp. maxZ	0.95
Exp. maxY	0.9
Exp. maxX	0.7
Exp. offsetX	-0.8
Exp. sizeX	5
Exp. offsetZ	-0.9

Test settings	
Tolerance gainX	±0,0000e+00
Tolerance gainZ	±0,0000e+00
Tolerance Table	±0,0000e+00
Tolerance gainY	±0,0000e+00
Tolerance maxZ	±0,0000e+00
Tolerance maxY	±0,0000e+00
Tolerance maxX	±0,0000e+00
Tolerance offsetX	±0,0000e+00
Tolerance sizeX	±0,0000e+00
Tolerance offsetZ	±0,0000e+00
Tolerance offsetY	±0,0000e+00
Tolerance minY	±0,0000e+00
Tolerance minX	±0,0000e+00
Tolerance minZ	±0,0000e+00
Tolerance dimZ	±0,0000e+00
Tolerance dimY	±0,0000e+00
Tolerance sizeY	±0,0000e+00
Tolerance dimX	±0,0000e+00
Tolerance sizeXY	±0,0000e+00

Verification: LookupTable3D Float32 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for General block LookupTable3D.

Test results				
Time step	1	2	...	19
CPU cycles	8253	8253	...	10165
Inputs				
x (DSP)	-1.1	-0.978	...	1.1
y (DSP)	-1.35	-1.208	...	1.2
z (DSP)	-2.16	-1.935	...	1.89
x	-1.1	-0.978	...	1.1
y	-1.35	-1.208	...	1.2
z	-2.16	-1.935	...	1.89
Parameters				
TableData	[1x765]			
DimX	9			
x_min	-0.8			
x_max	0.7			
DimY	17			
y_max	0.9			
y_min	-0.6			
DimZ	5			
z_min	-0.9			
z_max	0.95			
Outputs				
Out	1.953	1.953	...	2.356
Exp. Out	1.953	1.953	...	2.356
Out (DSP)	1.953	1.953	...	2.356
Exp. Out (DSP)	1.953	1.953	...	2.356

Test settings	
Tolerance Out	±9,3132e-07 (±2000 LSB)

Test statistics	
Min CPU cycles	8253
Max CPU cycles	11431
Avg CPU cycles	9995

Test case: Conversion test **OK**

Conversion test for General block LookupTable3D.

Test results	
Time step	1
Mask parameters	
TableData	[1x135]
DimX	5
x_min	-0.8
x_max	0.7
DimY	9
y_max	0.9
y_min	-0.6
DimZ	3
z_min	-0.9
z_max	0.95
Controller parameters	
gainX	2.667
gainZ	1.081
Table	[1x135]
gainY	5.333
maxZ	0.95
maxY	0.9
maxX	0.7
offsetX	-0.8
sizeX	5
offsetZ	-0.9
offsetY	-0.6
minY	-0.6
minX	-0.8
minZ	-0.9
dimZ	2
dimY	8
sizeY	9
dimX	4
sizeXY	45
Exp. gainX	2.667
Exp. gainZ	1.081
Exp. Table	[1x135]
Exp. gainY	5.333
Exp. maxZ	0.95
Exp. maxY	0.9
Exp. maxX	0.7
Exp. offsetX	-0.8
Exp. sizeX	5
Exp. offsetZ	-0.9

Test settings	
Tolerance gainX	±0,0000e+00
Tolerance gainZ	±0,0000e+00
Tolerance Table	±0,0000e+00
Tolerance gainY	±0,0000e+00
Tolerance maxZ	±0,0000e+00
Tolerance maxY	±0,0000e+00
Tolerance maxX	±0,0000e+00
Tolerance offsetX	±0,0000e+00
Tolerance sizeX	±0,0000e+00
Tolerance offsetZ	±0,0000e+00
Tolerance offsetY	±0,0000e+00
Tolerance minY	±0,0000e+00
Tolerance minX	±0,0000e+00
Tolerance minZ	±0,0000e+00
Tolerance dimZ	±0,0000e+00
Tolerance dimY	±0,0000e+00
Tolerance sizeY	±0,0000e+00
Tolerance dimX	±0,0000e+00
Tolerance sizeXY	±0,0000e+00

Verification: LookupTable3D Float32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for General block LookupTable3D.

Test results				
Time step	1	2	...	19
CPU cycles	362	273	...	291
Inputs				
x (DSP)	-1.1	-0.978	...	1.1
y (DSP)	-1.35	-1.208	...	1.2
z (DSP)	-2.16	-1.935	...	1.89
x	-1.1	-0.978	...	1.1
y	-1.35	-1.208	...	1.2
z	-2.16	-1.935	...	1.89
Parameters				
TableData	[1x765]			
DimX	9			
x_min	-0.8			
x_max	0.7			
DimY	17			
y_max	0.9			
y_min	-0.6			
DimZ	5			
z_min	-0.9			
z_max	0.95			
Outputs				
Out	1.953	1.953	...	2.356
Exp. Out	1.953	1.953	...	2.356
Out (DSP)	1.953	1.953	...	2.356
Exp. Out (DSP)	1.953	1.953	...	2.356

Test settings	
Tolerance Out	±9,3132e-07 (±2000 LSB)

Test statistics	
Min CPU cycles	273
Max CPU cycles	362
Avg CPU cycles	291

Test case: Conversion test **OK**

Conversion test for General block LookupTable3D.

Test results	
Time step	1
Mask parameters	
TableData	[1x135]
DimX	5
x_min	-0.8
x_max	0.7
DimY	9
y_max	0.9
y_min	-0.6
DimZ	3
z_min	-0.9
z_max	0.95
Controller parameters	
gainX	2.667
gainZ	1.081
Table	[1x135]
gainY	5.333
maxZ	0.95
maxY	0.9
maxX	0.7
offsetX	-0.8
sizeX	5
offsetZ	-0.9
offsetY	-0.6
minY	-0.6
minX	-0.8
minZ	-0.9
dimZ	2
dimY	8
sizeY	9
dimX	4
sizeXY	45
Exp. gainX	2.667
Exp. gainZ	1.081
Exp. Table	[1x135]
Exp. gainY	5.333
Exp. maxZ	0.95
Exp. maxY	0.9
Exp. maxX	0.7
Exp. offsetX	-0.8
Exp. sizeX	5
Exp. offsetZ	-0.9

Test settings	
Tolerance gainX	±0,0000e+00
Tolerance gainZ	±0,0000e+00
Tolerance Table	±0,0000e+00
Tolerance gainY	±0,0000e+00
Tolerance maxZ	±0,0000e+00
Tolerance maxY	±0,0000e+00
Tolerance maxX	±0,0000e+00
Tolerance offsetX	±0,0000e+00
Tolerance sizeX	±0,0000e+00
Tolerance offsetZ	±0,0000e+00
Tolerance offsetY	±0,0000e+00
Tolerance minY	±0,0000e+00
Tolerance minX	±0,0000e+00
Tolerance minZ	±0,0000e+00
Tolerance dimZ	±0,0000e+00
Tolerance dimY	±0,0000e+00
Tolerance sizeY	±0,0000e+00
Tolerance dimX	±0,0000e+00
Tolerance sizeXY	±0,0000e+00

Verification: LookupTable3D Float32 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for General block LookupTable3D.

Test results				
Time step	1	2	...	19
CPU cycles	303	303	...	296
Inputs				
x (DSP)	-1.1	-0.978	...	1.1
y (DSP)	-1.35	-1.208	...	1.2
z (DSP)	-2.16	-1.935	...	1.89
x	-1.1	-0.978	...	1.1
y	-1.35	-1.208	...	1.2
z	-2.16	-1.935	...	1.89
Parameters				
TableData	[1x765]			
DimX	9			
x_min	-0.8			
x_max	0.7			
DimY	17			
y_max	0.9			
y_min	-0.6			
DimZ	5			
z_min	-0.9			
z_max	0.95			
Outputs				
Out	1.953	1.953	...	2.356
Exp. Out	1.953	1.953	...	2.356
Out (DSP)	1.953	1.953	...	2.356
Exp. Out (DSP)	1.953	1.953	...	2.356

Test settings	
Tolerance Out	±9,3132e-07 (±2000 LSB)

Test statistics	
Min CPU cycles	291
Max CPU cycles	303
Avg CPU cycles	296

Test case: Conversion test **OK**

Conversion test for General block LookupTable3D.

Test results	
Time step	1
Mask parameters	
TableData	[1x135]
DimX	5
x_min	-0.8
x_max	0.7
DimY	9
y_max	0.9
y_min	-0.6
DimZ	3
z_min	-0.9
z_max	0.95
Controller parameters	
gainX	2.667
gainZ	1.081
Table	[1x135]
gainY	5.333
maxZ	0.95
maxY	0.9
maxX	0.7
offsetX	-0.8
sizeX	5
offsetZ	-0.9
offsetY	-0.6
minY	-0.6
minX	-0.8
minZ	-0.9
dimZ	2
dimY	8
sizeY	9
dimX	4
sizeXY	45
Exp. gainX	2.667
Exp. gainZ	1.081
Exp. Table	[1x135]
Exp. gainY	5.333
Exp. maxZ	0.95
Exp. maxY	0.9
Exp. maxX	0.7
Exp. offsetX	-0.8
Exp. sizeX	5
Exp. offsetZ	-0.9

Test settings	
Tolerance gainX	±0,0000e+00
Tolerance gainZ	±0,0000e+00
Tolerance Table	±0,0000e+00
Tolerance gainY	±0,0000e+00
Tolerance maxZ	±0,0000e+00
Tolerance maxY	±0,0000e+00
Tolerance maxX	±0,0000e+00
Tolerance offsetX	±0,0000e+00
Tolerance sizeX	±0,0000e+00
Tolerance offsetZ	±0,0000e+00
Tolerance offsetY	±0,0000e+00
Tolerance minY	±0,0000e+00
Tolerance minX	±0,0000e+00
Tolerance minZ	±0,0000e+00
Tolerance dimZ	±0,0000e+00
Tolerance dimY	±0,0000e+00
Tolerance sizeY	±0,0000e+00
Tolerance dimX	±0,0000e+00
Tolerance sizeXY	±0,0000e+00

Block: LoopBreaker



Block to break algebraic loops.

Inports	
In	Input In(k)

Outports	
Out	Output Out(k)=In(k-1)

Implementations:

Bool	Boolean Integration
FiP16	16 Bit Fixed Point Implementation
FiP32	32 Bit Fixed Point Implementation
Float32	32 Bit Floating Point Implementation
Float64	64 Bit Floating Point Implementation

Implementation: Bool

Boolean Integration

Inports Data Type	
In	bool

Outports Data Type	
Out	bool

Implementation: FiP16

16 Bit Fixed Point Implementation

Inports Data Type	
In	int16

Outports Data Type	
Out	int16

Implementation: FiP32

32 Bit Fixed Point Implementation

Inports Data Type	
In	int32

Outports Data Type	
Out	int32

Implementation: Float32

32 Bit Floating Point Implementation

Inports Data Type	
In	float32

Outports Data Type	
Out	float32

Implementation: Float64

64 Bit Floating Point Implementation

Inports Data Type	
In	float64

Outports Data Type	
Out	float64

Verification: LoopBreaker FiP16 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test **OK**

Inport test for General block LoopBreaker.

Test results						
Time step	1	2	3	4	...	18
CPU cycles	56	56	56	56	...	56
Inputs						
In (DSP)	0	32767	32767	32767	...	0
In	0	1	1	1.1	...	0
Outputs						
Out	0	1	1	1	...	0
Exp. Out	0	1	1	1	...	0
Out (DSP)	0	32767	32767	32767	...	0
Exp. Out (DSP)	0	32767	32767	32767	...	0

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	56
Max CPU cycles	56
Avg CPU cycles	56

Verification: LoopBreaker FiP16 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for General block LoopBreaker.

Test results						
Time step	1	2	3	4	...	18
CPU cycles	23	23	23	23	...	23
Inputs						
In (DSP)	0	32767	32767	32767	...	0
In	0	1	1	1.1	...	0
Outputs						
Out	0	1	1	1	...	0
Exp. Out	0	1	1	1	...	0
Out (DSP)	0	32767	32767	32767	...	0
Exp. Out (DSP)	0	32767	32767	32767	...	0

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	23
Max CPU cycles	23
Avg CPU cycles	23

Verification: LoopBreaker FiP16 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for General block LoopBreaker.

Test results						
Time step	1	2	3	4	...	18
CPU cycles	57	57	57	57	...	57
Inputs						
In (DSP)	0	32767	32767	32767	...	0
In	0	1	1	1.1	...	0
Outputs						
Out	0	1	1	1	...	0
Exp. Out	0	1	1	1	...	0
Out (DSP)	0	32767	32767	32767	...	0
Exp. Out (DSP)	0	32767	32767	32767	...	0

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	57
Max CPU cycles	57
Avg CPU cycles	57

Verification: LoopBreaker FiP16 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for General block LoopBreaker.

Test results						
Time step	1	2	3	4	...	18
CPU cycles	46	46	46	46	...	46
Inputs						
In (DSP)	0	32767	32767	32767	...	0
In	0	1	1	1.1	...	0
Outputs						
Out	0	1	1	1	...	0
Exp. Out	0	1	1	1	...	0
Out (DSP)	0	32767	32767	32767	...	0
Exp. Out (DSP)	0	32767	32767	32767	...	0

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	46
Max CPU cycles	46
Avg CPU cycles	46

Verification: LoopBreaker FiP16 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for General block LoopBreaker.

Test results						
Time step	1	2	3	4	...	18
CPU cycles	27	27	27	27	...	27
Inputs						
In (DSP)	0	32767	32767	32767	...	0
In	0	1	1	1.1	...	0
Outputs						
Out	0	1	1	1	...	0
Exp. Out	0	1	1	1	...	0
Out (DSP)	0	32767	32767	32767	...	0
Exp. Out (DSP)	0	32767	32767	32767	...	0

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	27
Max CPU cycles	27
Avg CPU cycles	27

Verification: LoopBreaker FiP16 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test **OK**

Inport test for General block LoopBreaker.

Test results						
Time step	1	2	3	4	...	18
CPU cycles	41	41	41	41	...	41
Inputs						
In (DSP)	0	32767	32767	32767	...	0
In	0	1	1	1.1	...	0
Outputs						
Out	0	1	1	1	...	0
Exp. Out	0	1	1	1	...	0
Out (DSP)	0	32767	32767	32767	...	0
Exp. Out (DSP)	0	32767	32767	32767	...	0

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	41
Max CPU cycles	41
Avg CPU cycles	41

Verification: LoopBreaker FiP16 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for General block LoopBreaker.

Test results						
Time step	1	2	3	4	...	18
CPU cycles	63	53	53	53	...	53
Inputs						
In (DSP)	0	32767	32767	32767	...	0
In	0	1	1	1.1	...	0
Outputs						
Out	0	1	1	1	...	0
Exp. Out	0	1	1	1	...	0
Out (DSP)	0	32767	32767	32767	...	0
Exp. Out (DSP)	0	32767	32767	32767	...	0

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	53
Max CPU cycles	63
Avg CPU cycles	53

Verification: LoopBreaker FiP16 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for General block LoopBreaker.

Test results						
Time step	1	2	3	4	...	18
CPU cycles	38	38	38	38	...	38
Inputs						
In (DSP)	0	32767	32767	32767	...	0
In	0	1	1	1.1	...	0
Outputs						
Out	0	1	1	1	...	0
Exp. Out	0	1	1	1	...	0
Out (DSP)	0	32767	32767	32767	...	0
Exp. Out (DSP)	0	32767	32767	32767	...	0

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	38
Max CPU cycles	38
Avg CPU cycles	38

Verification: LoopBreaker FiP32 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for General block LoopBreaker.

Test results				
Time step	1	2	...	18
CPU cycles	56	56	...	56
Inputs				
In (DSP)	0	2147483647	...	0
In	0	1	...	0
Outputs				
Out	0	1	...	0
Exp. Out	0	1	...	0
Out (DSP)	0	2147483647	...	0
Exp. Out (DSP)	0	2147483647	...	0

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	56
Max CPU cycles	56
Avg CPU cycles	56

Verification: LoopBreaker FiP32 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for General block LoopBreaker.

Test results				
Time step	1	2	...	18
CPU cycles	23	23	...	23
Inputs				
In (DSP)	0	2147483647	...	0
In	0	1	...	0
Outputs				
Out	0	1	...	0
Exp. Out	0	1	...	0
Out (DSP)	0	2147483647	...	0
Exp. Out (DSP)	0	2147483647	...	0

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	23
Max CPU cycles	23
Avg CPU cycles	23

Verification: LoopBreaker FiP32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for General block LoopBreaker.

Test results				
Time step	1	2	...	18
CPU cycles	52	52	...	52
Inputs				
In (DSP)	0	2147483647	...	0
In	0	1	...	0
Outputs				
Out	0	1	...	0
Exp. Out	0	1	...	0
Out (DSP)	0	2147483647	...	0
Exp. Out (DSP)	0	2147483647	...	0

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	52
Max CPU cycles	52
Avg CPU cycles	52

Verification: LoopBreaker FiP32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for General block LoopBreaker.

Test results				
Time step	1	2	...	18
CPU cycles	45	45	...	45
Inputs				
In (DSP)	0	2147483647	...	0
In	0	1	...	0
Outputs				
Out	0	1	...	0
Exp. Out	0	1	...	0
Out (DSP)	0	2147483647	...	0
Exp. Out (DSP)	0	2147483647	...	0

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	45
Max CPU cycles	45
Avg CPU cycles	45

Verification: LoopBreaker FiP32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for General block LoopBreaker.

Test results				
Time step	1	2	...	18
CPU cycles	27	27	...	27
Inputs				
In (DSP)	0	2147483647	...	0
In	0	1	...	0
Outputs				
Out	0	1	...	0
Exp. Out	0	1	...	0
Out (DSP)	0	2147483647	...	0
Exp. Out (DSP)	0	2147483647	...	0

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	27
Max CPU cycles	27
Avg CPU cycles	27

Verification: LoopBreaker FiP32 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test **OK**

Inport test for General block LoopBreaker.

Test results				
Time step	1	2	...	18
CPU cycles	43	43	...	43
Inputs				
In (DSP)	0	2147483647	...	0
In	0	1	...	0
Outputs				
Out	0	1	...	0
Exp. Out	0	1	...	0
Out (DSP)	0	2147483647	...	0
Exp. Out (DSP)	0	2147483647	...	0

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	43
Max CPU cycles	43
Avg CPU cycles	43

Verification: LoopBreaker FiP32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for General block LoopBreaker.

Test results				
Time step	1	2	...	18
CPU cycles	53	53	...	53
Inputs				
In (DSP)	0	2147483647	...	0
In	0	1	...	0
Outputs				
Out	0	1	...	0
Exp. Out	0	1	...	0
Out (DSP)	0	2147483647	...	0
Exp. Out (DSP)	0	2147483647	...	0

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	53
Max CPU cycles	53
Avg CPU cycles	53

Verification: LoopBreaker FiP32 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for General block LoopBreaker.

Test results				
Time step	1	2	...	18
CPU cycles	36	36	...	36
Inputs				
In (DSP)	0	2147483647	...	0
In	0	1	...	0
Outputs				
Out	0	1	...	0
Exp. Out	0	1	...	0
Out (DSP)	0	2147483647	...	0
Exp. Out (DSP)	0	2147483647	...	0

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	36
Max CPU cycles	36
Avg CPU cycles	36

Verification: LoopBreaker Float32 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for General block LoopBreaker.

Test results				
Time step	1	2	...	18
CPU cycles	56	56	...	56
Inputs				
In (DSP)	0	1	...	0
In	0	1	...	0
Outputs				
Out	0	1	...	0
Exp. Out	0	1	...	0
Out (DSP)	0	1	...	0
Exp. Out (DSP)	0	1	...	0

Test settings	
Tolerance Out	±3,2596e-08 (±70 LSB)

Test statistics	
Min CPU cycles	56
Max CPU cycles	56
Avg CPU cycles	56

Verification: LoopBreaker Float32 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for General block LoopBreaker.

Test results				
Time step	1	2	...	18
CPU cycles	23	23	...	23
Inputs				
In (DSP)	0	1	...	0
In	0	1	...	0
Outputs				
Out	0	1	...	0
Exp. Out	0	1	...	0
Out (DSP)	0	1	...	0
Exp. Out (DSP)	0	1	...	0

Test settings	
Tolerance Out	±3,2596e-08 (±70 LSB)

Test statistics	
Min CPU cycles	23
Max CPU cycles	23
Avg CPU cycles	23

Verification: LoopBreaker Float32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for General block LoopBreaker.

Test results				
Time step	1	2	...	18
CPU cycles	52	52	...	52
Inputs				
In (DSP)	0	1	...	0
In	0	1	...	0
Outputs				
Out	0	1	...	0
Exp. Out	0	1	...	0
Out (DSP)	0	1	...	0
Exp. Out (DSP)	0	1	...	0

Test settings	
Tolerance Out	±3,2596e-08 (±70 LSB)

Test statistics	
Min CPU cycles	52
Max CPU cycles	52
Avg CPU cycles	52

Verification: LoopBreaker Float32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for General block LoopBreaker.

Test results				
Time step	1	2	...	18
CPU cycles	45	45	...	45
Inputs				
In (DSP)	0	1	...	0
In	0	1	...	0
Outputs				
Out	0	1	...	0
Exp. Out	0	1	...	0
Out (DSP)	0	1	...	0
Exp. Out (DSP)	0	1	...	0

Test settings	
Tolerance Out	±3,2596e-08 (±70 LSB)

Test statistics	
Min CPU cycles	45
Max CPU cycles	45
Avg CPU cycles	45

Verification: LoopBreaker Float32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for General block LoopBreaker.

Test results				
Time step	1	2	...	18
CPU cycles	27	27	...	27
Inputs				
In (DSP)	0	1	...	0
In	0	1	...	0
Outputs				
Out	0	1	...	0
Exp. Out	0	1	...	0
Out (DSP)	0	1	...	0
Exp. Out (DSP)	0	1	...	0

Test settings	
Tolerance Out	±3,2596e-08 (±70 LSB)

Test statistics	
Min CPU cycles	27
Max CPU cycles	27
Avg CPU cycles	27

Verification: LoopBreaker Float32 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for General block LoopBreaker.

Test results				
Time step	1	2	...	18
CPU cycles	43	43	...	43
Inputs				
In (DSP)	0	1	...	0
In	0	1	...	0
Outputs				
Out	0	1	...	0
Exp. Out	0	1	...	0
Out (DSP)	0	1	...	0
Exp. Out (DSP)	0	1	...	0

Test settings	
Tolerance Out	±3,2596e-08 (±70 LSB)

Test statistics	
Min CPU cycles	43
Max CPU cycles	43
Avg CPU cycles	43

Verification: LoopBreaker Float32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for General block LoopBreaker.

Test results				
Time step	1	2	...	18
CPU cycles	53	53	...	53
Inputs				
In (DSP)	0	1	...	0
In	0	1	...	0
Outputs				
Out	0	1	...	0
Exp. Out	0	1	...	0
Out (DSP)	0	1	...	0
Exp. Out (DSP)	0	1	...	0

Test settings	
Tolerance Out	±3,2596e-08 (±70 LSB)

Test statistics	
Min CPU cycles	53
Max CPU cycles	53
Avg CPU cycles	53

Verification: LoopBreaker Float32 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for General block LoopBreaker.

Test results				
Time step	1	2	...	18
CPU cycles	38	38	...	38
Inputs				
In (DSP)	0	1	...	0
In	0	1	...	0
Outputs				
Out	0	1	...	0
Exp. Out	0	1	...	0
Out (DSP)	0	1	...	0
Exp. Out (DSP)	0	1	...	0

Test settings	
Tolerance Out	±3,2596e-08 (±70 LSB)

Test statistics	
Min CPU cycles	38
Max CPU cycles	38
Avg CPU cycles	38

Block: ManualSwitch



Toggling between inputs by double-clicking on block.

Inports	
In1	Input #1
In2	Input #2

Outports	
Out	

Mask Parameters		
Name	**ID**	**Description**
Toggle	1	Toggle

Description:

Doubleclicking of the *ManualSwitch* block changes the routing of the input signals and doesn't open the *Function Block Parameters* dialog. So if changing the implementation is required, one has to open the dialog via *Mask Parameters* command of the context menu.

Developer note: To get the double-click feature the callback function of *OpenFnc* in *Block Properties* is manually altered to

```
if get_param(gcb,'Toggle') == '0'
    set_param(gcb,'Toggle', '1');
else
    set_param(gcb,'Toggle', '0');
end
setBlockData(gcs, gcb);
initSFunction(gcb);
```

Implementations:

Bool	Boolean Implementation
FiP8	8 Bit Fixed Point Implementation
FiP16	16 Bit Fixed Point Implementation
FiP32	32 Bit Fixed Point Implementation
Float32	32 Bit Floating Point Implementation
Float64	64 Bit Floating Point Implementation

Implementation: Bool

Boolean Implementation

Inports Data Type	
In1	bool
In2	bool

Outports Data Type	
Out	bool

Implementation: FiP8

8 Bit Fixed Point Implementation

Inports Data Type	
In1	int8
In2	int8

Outports Data Type	
Out	int8

Implementation: FiP16

16 Bit Fixed Point Implementation

Inports Data Type	
In1	int16
In2	int16

Outports Data Type	
Out	int16

Implementation: FiP32

32 Bit Fixed Point Implementation

Inports Data Type	
In1	int32
In2	int32

Outports Data Type	
Out	int32

Implementation: Float32

32 Bit Floating Point Implementation

Inports Data Type	
In1	float32
In2	float32

Outports Data Type	
Out	float32

Implementation: Float64

64 Bit Floating Point Implementation

Inports Data Type	
In1	float64
In2	float64

Outports Data Type	
Out	float64

Verification: ManualSwitch Bool CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for General block ManualSwitch.

Test results						
Time step	1	2	3	4	...	7
CPU cycles	56	56	56	56	...	56
Inputs						
In1 (DSP)	0	0	0	0	...	1
In2 (DSP)	0	0	0	0	...	1
In1	0	0.1	0.2	0.3	...	1.1
In2	0.1	0.2	0.3	0.4	...	1.2
Parameters						
Toggle	0					
Outputs						
Out	0	0	0	0	...	1
Exp. Out	0	0	0	0	...	1
Out (DSP)	0	0	0	0	...	1
Exp. Out (DSP)	0	0	0	0	...	1

Test settings	
Tolerance Out	±7,8125e-03 (±0 LSB)

Test statistics	
Min CPU cycles	56
Max CPU cycles	56
Avg CPU cycles	56

Test case: Parameter test OK

Parameter test for General block ManualSwitch.

Test results						
Time step	1	2	3	4	...	10
CPU cycles	56	56	56	56	...	56
Inputs						
In1 (DSP)	1					
In2 (DSP)	0					
In1	1					
In2	0					
Parameters						
Toggle	0	0.1	1	2	...	-3
Outputs						
Out	1	0	0	0	...	0
Exp. Out	1	0	0	0	...	0
Out (DSP)	1	0	0	0	...	0
Exp. Out (DSP)	1	0	0	0	...	0

Test settings	
Tolerance Out	±7,8125e-03 (±0 LSB)

Test statistics	
Min CPU cycles	56
Max CPU cycles	56
Avg CPU cycles	56

Test case: Conversion test **OK**

Conversion test for General block ManualSwitch.

Test results						
Time step	1	2	3	4	...	10
Mask parameters						
Toggle	0	0.1	1	2	...	-3
Controller parameters						
Toggle	0	1	1	1	...	1
Exp. Toggle	0	1	1	1	...	1

Test settings	
Tolerance Toggle	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block ManualSwitch.

Test results						
Time step	1	2	3	4	...	10
Mask parameters						
Toggle	0	0.1	1	2	...	-3
Controller parameters						
Toggle	0	1	1	1	...	1
Exp. Toggle	0	1	1	1	...	1

Test settings	
Tolerance Toggle	±0,0000e+00

Test statistics	
Min CPU cycles	793
Max CPU cycles	834
Avg CPU cycles	825

Verification: ManualSwitch Bool CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for General block ManualSwitch.

Test results						
Time step	1	2	3	4	...	7
CPU cycles	23	23	23	23	...	23
Inputs						
In1 (DSP)	0	0	0	0	...	1
In2 (DSP)	0	0	0	0	...	1
In1	0	0.1	0.2	0.3	...	1.1
In2	0.1	0.2	0.3	0.4	...	1.2
Parameters						
Toggle	0					
Outputs						
Out	0	0	0	0	...	1
Exp. Out	0	0	0	0	...	1
Out (DSP)	0	0	0	0	...	1
Exp. Out (DSP)	0	0	0	0	...	1

Test settings	
Tolerance Out	±7,8125e-03 (±0 LSB)

Test statistics	
Min CPU cycles	23
Max CPU cycles	23
Avg CPU cycles	23

Test case: Parameter test OK

Parameter test for General block ManualSwitch.

Test results						
Time step	1	2	3	4	...	10
CPU cycles	23	23	23	23	...	23
Inputs						
In1 (DSP)	1					
In2 (DSP)	0					
In1	1					
In2	0					
Parameters						
Toggle	0	0.1	1	2	...	-3
Outputs						
Out	1	0	0	0	...	0
Exp. Out	1	0	0	0	...	0
Out (DSP)	1	0	0	0	...	0
Exp. Out (DSP)	1	0	0	0	...	0

Test settings	
Tolerance Out	±7,8125e-03 (±0 LSB)

Test statistics	
Min CPU cycles	23
Max CPU cycles	23
Avg CPU cycles	23

Test case: Conversion test **OK**

Conversion test for General block ManualSwitch.

Test results						
Time step	1	2	3	4	...	10
Mask parameters						
Toggle	0	0.1	1	2	...	-3
Controller parameters						
Toggle	0	1	1	1	...	1
Exp. Toggle	0	1	1	1	...	1

Test settings	
Tolerance Toggle	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block ManualSwitch.

Test results						
Time step	1	2	3	4	...	10
Mask parameters						
Toggle	0	0.1	1	2	...	-3
Controller parameters						
Toggle	0	1	1	1	...	1
Exp. Toggle	0	1	1	1	...	1

Test settings	
Tolerance Toggle	±0,0000e+00

Test statistics	
Min CPU cycles	375
Max CPU cycles	399
Avg CPU cycles	393

Verification: ManualSwitch Bool CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for General block ManualSwitch.

Test results						
Time step	1	2	3	4	...	7
CPU cycles	52	52	52	52	...	52
Inputs						
In1 (DSP)	0	0	0	0	...	1
In2 (DSP)	0	0	0	0	...	1
In1	0	0.1	0.2	0.3	...	1.1
In2	0.1	0.2	0.3	0.4	...	1.2
Parameters						
Toggle	0					
Outputs						
Out	0	0	0	0	...	1
Exp. Out	0	0	0	0	...	1
Out (DSP)	0	0	0	0	...	1
Exp. Out (DSP)	0	0	0	0	...	1

Test settings	
Tolerance Out	±7,8125e-03 (±0 LSB)

Test statistics	
Min CPU cycles	52
Max CPU cycles	52
Avg CPU cycles	52

Test case: Parameter test OK

Parameter test for General block ManualSwitch.

Test results						
Time step	1	2	3	4	...	10
CPU cycles	52	52	52	52	...	111
Inputs						
In1 (DSP)	1					
In2 (DSP)	0					
In1	1					
In2	0					
Parameters						
Toggle	0	0.1	1	2	...	-3
Outputs						
Out	1	0	0	0	...	0
Exp. Out	1	0	0	0	...	0
Out (DSP)	1	0	0	0	...	0
Exp. Out (DSP)	1	0	0	0	...	0

Test settings	
Tolerance Out	±7,8125e-03 (±0 LSB)

Test statistics	
Min CPU cycles	52
Max CPU cycles	111
Avg CPU cycles	57

Test case: Conversion test **OK**

Conversion test for General block ManualSwitch.

Test results						
Time step	1	2	3	4	...	10
Mask parameters						
Toggle	0	0.1	1	2	...	-3
Controller parameters						
Toggle	0	1	1	1	...	1
Exp. Toggle	0	1	1	1	...	1

Test settings	
Tolerance Toggle	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block ManualSwitch.

Test results						
Time step	1	2	3	4	...	10
Mask parameters						
Toggle	0	0.1	1	2	...	-3
Controller parameters						
Toggle	0	1	1	1	...	1
Exp. Toggle	0	1	1	1	...	1

Test settings	
Tolerance Toggle	±0,0000e+00

Test statistics	
Min CPU cycles	516
Max CPU cycles	541
Avg CPU cycles	536

Verification: ManualSwitch Bool CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for General block ManualSwitch.

Test results						
Time step	1	2	3	4	...	7
CPU cycles	45	45	45	45	...	45
Inputs						
In1 (DSP)	0	0	0	0	...	1
In2 (DSP)	0	0	0	0	...	1
In1	0	0.1	0.2	0.3	...	1.1
In2	0.1	0.2	0.3	0.4	...	1.2
Parameters						
Toggle	0					
Outputs						
Out	0	0	0	0	...	1
Exp. Out	0	0	0	0	...	1
Out (DSP)	0	0	0	0	...	1
Exp. Out (DSP)	0	0	0	0	...	1

Test settings	
Tolerance Out	±7,8125e-03 (±0 LSB)

Test statistics	
Min CPU cycles	45
Max CPU cycles	45
Avg CPU cycles	45

Test case: Parameter test OK

Parameter test for General block ManualSwitch.

Test results						
Time step	1	2	3	4	...	10
CPU cycles	45	45	45	45	...	45
Inputs						
In1 (DSP)	1					
In2 (DSP)	0					
In1	1					
In2	0					
Parameters						
Toggle	0	0.1	1	2	...	-3
Outputs						
Out	1	0	0	0	...	0
Exp. Out	1	0	0	0	...	0
Out (DSP)	1	0	0	0	...	0
Exp. Out (DSP)	1	0	0	0	...	0

Test settings	
Tolerance Out	±7,8125e-03 (±0 LSB)

Test statistics	
Min CPU cycles	45
Max CPU cycles	45
Avg CPU cycles	45

Test case: Conversion test **OK**

Conversion test for General block ManualSwitch.

Test results						
Time step	1	2	3	4	...	10
Mask parameters						
Toggle	0	0.1	1	2	...	-3
Controller parameters						
Toggle	0	1	1	1	...	1
Exp. Toggle	0	1	1	1	...	1

Test settings	
Tolerance Toggle	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block ManualSwitch.

Test results						
Time step	1	2	3	4	...	10
Mask parameters						
Toggle	0	0.1	1	2	...	-3
Controller parameters						
Toggle	0	1	1	1	...	1
Exp. Toggle	0	1	1	1	...	1

Test settings	
Tolerance Toggle	±0,0000e+00

Test statistics	
Min CPU cycles	602
Max CPU cycles	612
Avg CPU cycles	604

Verification: ManualSwitch Bool CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for General block ManualSwitch.

Test results						
Time step	1	2	3	4	...	7
CPU cycles	27	27	27	27	...	27
Inputs						
In1 (DSP)	0	0	0	0	...	1
In2 (DSP)	0	0	0	0	...	1
In1	0	0.1	0.2	0.3	...	1.1
In2	0.1	0.2	0.3	0.4	...	1.2
Parameters						
Toggle	0					
Outputs						
Out	0	0	0	0	...	1
Exp. Out	0	0	0	0	...	1
Out (DSP)	0	0	0	0	...	1
Exp. Out (DSP)	0	0	0	0	...	1

Test settings	
Tolerance Out	±7,8125e-03 (±0 LSB)

Test statistics	
Min CPU cycles	27
Max CPU cycles	27
Avg CPU cycles	27

Test case: Parameter test OK

Parameter test for General block ManualSwitch.

Test results						
Time step	1	2	3	4	...	10
CPU cycles	27	27	27	27	...	27
Inputs						
In1 (DSP)	1					
In2 (DSP)	0					
In1	1					
In2	0					
Parameters						
Toggle	0	0.1	1	2	...	-3
Outputs						
Out	1	0	0	0	...	0
Exp. Out	1	0	0	0	...	0
Out (DSP)	1	0	0	0	...	0
Exp. Out (DSP)	1	0	0	0	...	0

Test settings	
Tolerance Out	±7,8125e-03 (±0 LSB)

Test statistics	
Min CPU cycles	27
Max CPU cycles	27
Avg CPU cycles	27

Test case: Conversion test **OK**

Conversion test for General block ManualSwitch.

Test results						
Time step	1	2	3	4	...	10
Mask parameters						
Toggle	0	0.1	1	2	...	-3
Controller parameters						
Toggle	0	1	1	1	...	1
Exp. Toggle	0	1	1	1	...	1

Test settings	
Tolerance Toggle	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block ManualSwitch.

Test results						
Time step	1	2	3	4	...	10
Mask parameters						
Toggle	0	0.1	1	2	...	-3
Controller parameters						
Toggle	0	1	1	1	...	1
Exp. Toggle	0	1	1	1	...	1

Test settings	
Tolerance Toggle	±0,0000e+00

Test statistics	
Min CPU cycles	245
Max CPU cycles	279
Avg CPU cycles	266

Verification: ManualSwitch Bool CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test

OK

Inport test for General block ManualSwitch.

Test results						
Time step	1	2	3	4	...	7
CPU cycles	41	41	41	41	...	41
Inputs						
In1 (DSP)	0	0	0	0	...	1
In2 (DSP)	0	0	0	0	...	1
In1	0	0.1	0.2	0.3	...	1.1
In2	0.1	0.2	0.3	0.4	...	1.2
Parameters						
Toggle	0					
Outputs						
Out	0	0	0	0	...	1
Exp. Out	0	0	0	0	...	1
Out (DSP)	0	0	0	0	...	1
Exp. Out (DSP)	0	0	0	0	...	1

Test settings	
Tolerance Out	±7,8125e-03 (±0 LSB)

Test statistics	
Min CPU cycles	41
Max CPU cycles	41
Avg CPU cycles	41

Test case: Parameter test

OK

Parameter test for General block ManualSwitch.

Test results						
Time step	1	2	3	4	...	10
CPU cycles	41	41	41	41	...	41
Inputs						
In1 (DSP)	1					
In2 (DSP)	0					
In1	1					
In2	0					
Parameters						
Toggle	0	0.1	1	2	...	-3
Outputs						
Out	1	0	0	0	...	0
Exp. Out	1	0	0	0	...	0
Out (DSP)	1	0	0	0	...	0
Exp. Out (DSP)	1	0	0	0	...	0

Test settings	
Tolerance Out	±7,8125e-03 (±0 LSB)

Test statistics	
Min CPU cycles	41
Max CPU cycles	41
Avg CPU cycles	41

Test case: Conversion test **OK**

Conversion test for General block ManualSwitch.

Test results						
Time step	1	2	3	4	...	10
Mask parameters						
Toggle	0	0.1	1	2	...	-3
Controller parameters						
Toggle	0	1	1	1	...	1
Exp. Toggle	0	1	1	1	...	1

Test settings	
Tolerance Toggle	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block ManualSwitch.

Test results						
Time step	1	2	3	4	...	10
Mask parameters						
Toggle	0	0.1	1	2	...	-3
Controller parameters						
Toggle	0	1	1	1	...	1
Exp. Toggle	0	1	1	1	...	1

Test settings	
Tolerance Toggle	±0,0000e+00

Test statistics	
Min CPU cycles	520
Max CPU cycles	546
Avg CPU cycles	527

Verification: ManualSwitch Bool CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for General block ManualSwitch.

Test results						
Time step	1	2	3	4	...	7
CPU cycles	53	53	53	53	...	53
Inputs						
In1 (DSP)	0	0	0	0	...	1
In2 (DSP)	0	0	0	0	...	1
In1	0	0.1	0.2	0.3	...	1.1
In2	0.1	0.2	0.3	0.4	...	1.2
Parameters						
Toggle	0					
Outputs						
Out	0	0	0	0	...	1
Exp. Out	0	0	0	0	...	1
Out (DSP)	0	0	0	0	...	1
Exp. Out (DSP)	0	0	0	0	...	1

Test settings	
Tolerance Out	±7,8125e-03 (±0 LSB)

Test statistics	
Min CPU cycles	53
Max CPU cycles	53
Avg CPU cycles	53

Test case: Parameter test OK

Parameter test for General block ManualSwitch.

Test results						
Time step	1	2	3	4	...	10
CPU cycles	53	53	53	53	...	53
Inputs						
In1 (DSP)	1					
In2 (DSP)	0					
In1	1					
In2	0					
Parameters						
Toggle	0	0.1	1	2	...	-3
Outputs						
Out	1	0	0	0	...	0
Exp. Out	1	0	0	0	...	0
Out (DSP)	1	0	0	0	...	0
Exp. Out (DSP)	1	0	0	0	...	0

Test settings	
Tolerance Out	±7,8125e-03 (±0 LSB)

Test statistics	
Min CPU cycles	53
Max CPU cycles	53
Avg CPU cycles	53

Test case: Conversion test **OK**

Conversion test for General block ManualSwitch.

Test results						
Time step	1	2	3	4	...	10
Mask parameters						
Toggle	0	0.1	1	2	...	-3
Controller parameters						
Toggle	0	1	1	1	...	1
Exp. Toggle	0	1	1	1	...	1

Test settings	
Tolerance Toggle	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block ManualSwitch.

Test results						
Time step	1	2	3	4	...	10
Mask parameters						
Toggle	0	0.1	1	2	...	-3
Controller parameters						
Toggle	0	1	1	1	...	1
Exp. Toggle	0	1	1	1	...	1

Test settings	
Tolerance Toggle	±0,0000e+00

Test statistics	
Min CPU cycles	476
Max CPU cycles	516
Avg CPU cycles	484

Verification: ManualSwitch Bool CPU TMS320F28379D

Date of Test 2026-06-22

Target controller TMS320F28379D

Test case: Inport test OK

Inport test for General block ManualSwitch.

Test results						
Time step	1	2	3	4	...	7
CPU cycles	36	36	36	36	...	36
Inputs						
In1 (DSP)	0	0	0	0	...	1
In2 (DSP)	0	0	0	0	...	1
In1	0	0.1	0.2	0.3	...	1.1
In2	0.1	0.2	0.3	0.4	...	1.2
Parameters						
Toggle	0					
Outputs						
Out	0	0	0	0	...	1
Exp. Out	0	0	0	0	...	1
Out (DSP)	0	0	0	0	...	1
Exp. Out (DSP)	0	0	0	0	...	1

Test settings	
Tolerance Out	±7,8125e-03 (±0 LSB)

Test statistics	
Min CPU cycles	36
Max CPU cycles	36
Avg CPU cycles	36

Test case: Parameter test OK

Parameter test for General block ManualSwitch.

Test results						
Time step	1	2	3	4	...	10
CPU cycles	36	36	36	36	...	36
Inputs						
In1 (DSP)	1					
In2 (DSP)	0					
In1	1					
In2	0					
Parameters						
Toggle	0	0.1	1	2	...	-3
Outputs						
Out	1	0	0	0	...	0
Exp. Out	1	0	0	0	...	0
Out (DSP)	1	0	0	0	...	0
Exp. Out (DSP)	1	0	0	0	...	0

Test settings	
Tolerance Out	±7,8125e-03 (±0 LSB)

Test statistics	
Min CPU cycles	36
Max CPU cycles	36
Avg CPU cycles	36

Test case: Conversion test **OK**

Conversion test for General block ManualSwitch.

Test results						
Time step	1	2	3	4	...	10
Mask parameters						
Toggle	0	0.1	1	2	...	-3
Controller parameters						
Toggle	0	1	1	1	...	1
Exp. Toggle	0	1	1	1	...	1

Test settings	
Tolerance Toggle	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block ManualSwitch.

Test results						
Time step	1	2	3	4	...	10
Mask parameters						
Toggle	0	0.1	1	2	...	-3
Controller parameters						
Toggle	0	1	1	1	...	1
Exp. Toggle	0	1	1	1	...	1

Test settings	
Tolerance Toggle	±0,0000e+00

Test statistics	
Min CPU cycles	614
Max CPU cycles	648
Avg CPU cycles	641

Verification: ManualSwitch FiP16 CPU TMS320F28335

Date of Test 2026-06-19

Target controller TMS320F28335

Test case: Inport test OK

Inport test for General block ManualSwitch.

Test results					
Time step	1	2	3	4	5
CPU cycles	56	56	56	56	56
Inputs					
In1 (DSP)	0	3277	6554	9830	13107
In2 (DSP)	3277	6554	9830	13107	16384
In1	0	0.1	0.2	0.3	0.4
In2	0.1	0.2	0.3	0.4	0.5
Parameters					
Toggle					
Outputs					
Out	0	0.1	0.2	0.3	0.4
Exp. Out	0	0.1	0.2	0.3	0.4
Out (DSP)	0	3277	6554	9830	13107
Exp. Out (DSP)	0	3277	6554	9830	13107

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	56
Max CPU cycles	56
Avg CPU cycles	56

Test case: Parameter test OK

Parameter test for General block ManualSwitch.

Test results						
Time step	1	2	3	4	...	10
CPU cycles	56	56	56	56	...	56
Inputs						
In1 (DSP)	9830					
In2 (DSP)	19661					
In1	0.3					
In2	0.6					
Parameters						
Toggle	0	0.1	1	2	...	-3
Outputs						
Out	0.3	0.6	0.6	0.6	...	0.6
Exp. Out	0.3	0.6	0.6	0.6	...	0.6
Out (DSP)	9830	19661	19661	19661	...	19661
Exp. Out (DSP)	9830	19661	19661	19661	...	19661

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	56
Max CPU cycles	56
Avg CPU cycles	56

Test case: Conversion test **OK**

Conversion test for General block ManualSwitch.

Test results						
Time step	1	2	3	4	...	10
Mask parameters						
Toggle	0	0.1	1	2	...	-3
Controller parameters						
Toggle	0	1	1	1	...	1
Exp. Toggle	0	1	1	1	...	1

Test settings	
Tolerance Toggle	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block ManualSwitch.

Test results						
Time step	1	2	3	4	...	10
Mask parameters						
Toggle	0	0.1	1	2	...	-3
Controller parameters						
Toggle	0	1	1	1	...	1
Exp. Toggle	0	1	1	1	...	1

Test settings	
Tolerance Toggle	±0,0000e+00

Test statistics	
Min CPU cycles	778
Max CPU cycles	815
Avg CPU cycles	807

Verification: ManualSwitch FiP16 CPU TM4C123GH6

Date of Test 2026-06-19

Target controller TM4C123GH6

Test case: Inport test OK

Inport test for General block ManualSwitch.

Test results					
Time step	1	2	3	4	5
CPU cycles	23	23	23	23	23
Inputs					
In1 (DSP)	0	3277	6554	9830	13107
In2 (DSP)	3277	6554	9830	13107	16384
In1	0	0.1	0.2	0.3	0.4
In2	0.1	0.2	0.3	0.4	0.5
Parameters					
Toggle					
Outputs					
Out	0	0.1	0.2	0.3	0.4
Exp. Out	0	0.1	0.2	0.3	0.4
Out (DSP)	0	3277	6554	9830	13107
Exp. Out (DSP)	0	3277	6554	9830	13107

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	23
Max CPU cycles	23
Avg CPU cycles	23

Test case: Parameter test OK

Parameter test for General block ManualSwitch.

Test results						
Time step	1	2	3	4	...	10
CPU cycles	23	23	23	23	...	23
Inputs						
In1 (DSP)	9830					
In2 (DSP)	19661					
In1	0.3					
In2	0.6					
Parameters						
Toggle	0	0.1	1	2	...	-3
Outputs						
Out	0.3	0.6	0.6	0.6	...	0.6
Exp. Out	0.3	0.6	0.6	0.6	...	0.6
Out (DSP)	9830	19661	19661	19661	...	19661
Exp. Out (DSP)	9830	19661	19661	19661	...	19661

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	23
Max CPU cycles	23
Avg CPU cycles	23

Test case: Conversion test **OK**

Conversion test for General block ManualSwitch.

Test results						
Time step	1	2	3	4	...	10
Mask parameters						
Toggle	0	0.1	1	2	...	-3
Controller parameters						
Toggle	0	1	1	1	...	1
Exp. Toggle	0	1	1	1	...	1

Test settings	
Tolerance Toggle	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block ManualSwitch.

Test results						
Time step	1	2	3	4	...	10
Mask parameters						
Toggle	0	0.1	1	2	...	-3
Controller parameters						
Toggle	0	1	1	1	...	1
Exp. Toggle	0	1	1	1	...	1

Test settings	
Tolerance Toggle	±0,0000e+00

Test statistics	
Min CPU cycles	375
Max CPU cycles	399
Avg CPU cycles	393

Verification: ManualSwitch FiP16 CPU STM32G474RE

Date of Test 2026-06-19

Target controller STM32G474RE

Test case: Inport test OK

Inport test for General block ManualSwitch.

Test results					
Time step	1	2	3	4	5
CPU cycles	57	57	57	57	57
Inputs					
In1 (DSP)	0	3277	6554	9830	13107
In2 (DSP)	3277	6554	9830	13107	16384
In1	0	0.1	0.2	0.3	0.4
In2	0.1	0.2	0.3	0.4	0.5
Parameters					
Toggle					
Outputs					
Out	0	0.1	0.2	0.3	0.4
Exp. Out	0	0.1	0.2	0.3	0.4
Out (DSP)	0	3277	6554	9830	13107
Exp. Out (DSP)	0	3277	6554	9830	13107

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	57
Max CPU cycles	57
Avg CPU cycles	57

Test case: Parameter test OK

Parameter test for General block ManualSwitch.

Test results						
Time step	1	2	3	4	...	10
CPU cycles	57	57	57	57	...	57
Inputs						
In1 (DSP)	9830					
In2 (DSP)	19661					
In1	0.3					
In2	0.6					
Parameters						
Toggle	0	0.1	1	2	...	-3
Outputs						
Out	0.3	0.6	0.6	0.6	...	0.6
Exp. Out	0.3	0.6	0.6	0.6	...	0.6
Out (DSP)	9830	19661	19661	19661	...	19661
Exp. Out (DSP)	9830	19661	19661	19661	...	19661

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	57
Max CPU cycles	57
Avg CPU cycles	57

Test case: Conversion test **OK**

Conversion test for General block ManualSwitch.

Test results						
Time step	1	2	3	4	...	10
Mask parameters						
Toggle	0	0.1	1	2	...	-3
Controller parameters						
Toggle	0	1	1	1	...	1
Exp. Toggle	0	1	1	1	...	1

Test settings	
Tolerance Toggle	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block ManualSwitch.

Test results						
Time step	1	2	3	4	...	10
Mask parameters						
Toggle	0	0.1	1	2	...	-3
Controller parameters						
Toggle	0	1	1	1	...	1
Exp. Toggle	0	1	1	1	...	1

Test settings	
Tolerance Toggle	±0,0000e+00

Test statistics	
Min CPU cycles	518
Max CPU cycles	543
Avg CPU cycles	538

Verification: ManualSwitch FiP16 CPU STM32F072RB

Date of Test 2026-06-19

Target controller STM32F072RB

Test case: Inport test OK

Inport test for General block ManualSwitch.

Test results					
Time step	1	2	3	4	5
CPU cycles	46	46	46	46	46
Inputs					
In1 (DSP)	0	3277	6554	9830	13107
In2 (DSP)	3277	6554	9830	13107	16384
In1	0	0.1	0.2	0.3	0.4
In2	0.1	0.2	0.3	0.4	0.5
Parameters					
Toggle					
Outputs					
Out	0	0.1	0.2	0.3	0.4
Exp. Out	0	0.1	0.2	0.3	0.4
Out (DSP)	0	3277	6554	9830	13107
Exp. Out (DSP)	0	3277	6554	9830	13107

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	46
Max CPU cycles	46
Avg CPU cycles	46

Test case: Parameter test OK

Parameter test for General block ManualSwitch.

Test results						
Time step	1	2	3	4	...	10
CPU cycles	46	46	46	46	...	46
Inputs						
In1 (DSP)	9830					
In2 (DSP)	19661					
In1	0.3					
In2	0.6					
Parameters						
Toggle	0	0.1	1	2	...	-3
Outputs						
Out	0.3	0.6	0.6	0.6	...	0.6
Exp. Out	0.3	0.6	0.6	0.6	...	0.6
Out (DSP)	9830	19661	19661	19661	...	19661
Exp. Out (DSP)	9830	19661	19661	19661	...	19661

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	46
Max CPU cycles	46
Avg CPU cycles	46

Test case: Conversion test **OK**

Conversion test for General block ManualSwitch.

Test results						
Time step	1	2	3	4	...	10
Mask parameters						
Toggle	0	0.1	1	2	...	-3
Controller parameters						
Toggle	0	1	1	1	...	1
Exp. Toggle	0	1	1	1	...	1

Test settings	
Tolerance Toggle	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block ManualSwitch.

Test results						
Time step	1	2	3	4	...	10
Mask parameters						
Toggle	0	0.1	1	2	...	-3
Controller parameters						
Toggle	0	1	1	1	...	1
Exp. Toggle	0	1	1	1	...	1

Test settings	
Tolerance Toggle	±0,0000e+00

Test statistics	
Min CPU cycles	602
Max CPU cycles	612
Avg CPU cycles	604

Verification: ManualSwitch FiP16 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for General block ManualSwitch.

Test results					
Time step	1	2	3	4	5
CPU cycles	27	27	27	27	27
Inputs					
In1 (DSP)	0	3277	6554	9830	13107
In2 (DSP)	3277	6554	9830	13107	16384
In1	0	0.1	0.2	0.3	0.4
In2	0.1	0.2	0.3	0.4	0.5
Parameters					
Toggle					
Outputs					
Out	0	0.1	0.2	0.3	0.4
Exp. Out	0	0.1	0.2	0.3	0.4
Out (DSP)	0	3277	6554	9830	13107
Exp. Out (DSP)	0	3277	6554	9830	13107

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	27
Max CPU cycles	27
Avg CPU cycles	27

Test case: Parameter test OK

Parameter test for General block ManualSwitch.

Test results						
Time step	1	2	3	4	...	10
CPU cycles	27	27	27	27	...	27
Inputs						
In1 (DSP)	9830					
In2 (DSP)	19661					
In1	0.3					
In2	0.6					
Parameters						
Toggle	0	0.1	1	2	...	-3
Outputs						
Out	0.3	0.6	0.6	0.6	...	0.6
Exp. Out	0.3	0.6	0.6	0.6	...	0.6
Out (DSP)	9830	19661	19661	19661	...	19661
Exp. Out (DSP)	9830	19661	19661	19661	...	19661

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	27
Max CPU cycles	27
Avg CPU cycles	27

Test case: Conversion test **OK**

Conversion test for General block ManualSwitch.

Test results						
Time step	1	2	3	4	...	10
Mask parameters						
Toggle	0	0.1	1	2	...	-3
Controller parameters						
Toggle	0	1	1	1	...	1
Exp. Toggle	0	1	1	1	...	1

Test settings	
Tolerance Toggle	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block ManualSwitch.

Test results						
Time step	1	2	3	4	...	10
Mask parameters						
Toggle	0	0.1	1	2	...	-3
Controller parameters						
Toggle	0	1	1	1	...	1
Exp. Toggle	0	1	1	1	...	1

Test settings	
Tolerance Toggle	±0,0000e+00

Test statistics	
Min CPU cycles	245
Max CPU cycles	279
Avg CPU cycles	266

Verification: ManualSwitch FiP16 CPU dsPIC33EP256MC502

Date of Test 2026-06-19

Target controller dsPIC33EP256MC502

Test case: Inport test OK

Inport test for General block ManualSwitch.

Test results					
Time step	1	2	3	4	5
CPU cycles	41	41	41	41	41
Inputs					
In1 (DSP)	0	3277	6554	9830	13107
In2 (DSP)	3277	6554	9830	13107	16384
In1	0	0.1	0.2	0.3	0.4
In2	0.1	0.2	0.3	0.4	0.5
Parameters					
Toggle					
Outputs					
Out	0	0.1	0.2	0.3	0.4
Exp. Out	0	0.1	0.2	0.3	0.4
Out (DSP)	0	3277	6554	9830	13107
Exp. Out (DSP)	0	3277	6554	9830	13107

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	41
Max CPU cycles	41
Avg CPU cycles	41

Test case: Parameter test OK

Parameter test for General block ManualSwitch.

Test results						
Time step	1	2	3	4	...	10
CPU cycles	41	41	41	41	...	41
Inputs						
In1 (DSP)	9830					
In2 (DSP)	19661					
In1	0.3					
In2	0.6					
Parameters						
Toggle	0	0.1	1	2	...	-3
Outputs						
Out	0.3	0.6	0.6	0.6	...	0.6
Exp. Out	0.3	0.6	0.6	0.6	...	0.6
Out (DSP)	9830	19661	19661	19661	...	19661
Exp. Out (DSP)	9830	19661	19661	19661	...	19661

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	41
Max CPU cycles	41
Avg CPU cycles	41

Test case: Conversion test **OK**

Conversion test for General block ManualSwitch.

Test results						
Time step	1	2	3	4	...	10
Mask parameters						
Toggle	0	0.1	1	2	...	-3
Controller parameters						
Toggle	0	1	1	1	...	1
Exp. Toggle	0	1	1	1	...	1

Test settings	
Tolerance Toggle	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block ManualSwitch.

Test results						
Time step	1	2	3	4	...	10
Mask parameters						
Toggle	0	0.1	1	2	...	-3
Controller parameters						
Toggle	0	1	1	1	...	1
Exp. Toggle	0	1	1	1	...	1

Test settings	
Tolerance Toggle	±0,0000e+00

Test statistics	
Min CPU cycles	520
Max CPU cycles	546
Avg CPU cycles	527

Verification: ManualSwitch FiP16 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for General block ManualSwitch.

Test results					
Time step	1	2	3	4	5
CPU cycles	53	53	53	53	53
Inputs					
In1 (DSP)	0	3277	6554	9830	13107
In2 (DSP)	3277	6554	9830	13107	16384
In1	0	0.1	0.2	0.3	0.4
In2	0.1	0.2	0.3	0.4	0.5
Parameters					
Toggle					
Outputs					
Out	0	0.1	0.2	0.3	0.4
Exp. Out	0	0.1	0.2	0.3	0.4
Out (DSP)	0	3277	6554	9830	13107
Exp. Out (DSP)	0	3277	6554	9830	13107

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	53
Max CPU cycles	53
Avg CPU cycles	53

Test case: Parameter test OK

Parameter test for General block ManualSwitch.

Test results						
Time step	1	2	3	4	...	10
CPU cycles	53	53	53	53	...	53
Inputs						
In1 (DSP)	9830					
In2 (DSP)	19661					
In1	0.3					
In2	0.6					
Parameters						
Toggle	0	0.1	1	2	...	-3
Outputs						
Out	0.3	0.6	0.6	0.6	...	0.6
Exp. Out	0.3	0.6	0.6	0.6	...	0.6
Out (DSP)	9830	19661	19661	19661	...	19661
Exp. Out (DSP)	9830	19661	19661	19661	...	19661

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	53
Max CPU cycles	53
Avg CPU cycles	53

Test case: Conversion test **OK**

Conversion test for General block ManualSwitch.

Test results						
Time step	1	2	3	4	...	10
Mask parameters						
Toggle	0	0.1	1	2	...	-3
Controller parameters						
Toggle	0	1	1	1	...	1
Exp. Toggle	0	1	1	1	...	1

Test settings	
Tolerance Toggle	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block ManualSwitch.

Test results						
Time step	1	2	3	4	...	10
Mask parameters						
Toggle	0	0.1	1	2	...	-3
Controller parameters						
Toggle	0	1	1	1	...	1
Exp. Toggle	0	1	1	1	...	1

Test settings	
Tolerance Toggle	±0,0000e+00

Test statistics	
Min CPU cycles	451
Max CPU cycles	506
Avg CPU cycles	461

Verification: ManualSwitch FiP16 CPU TMS320F28379D

Date of Test 2026-06-22

Target controller TMS320F28379D

Test case: Inport test OK

Inport test for General block ManualSwitch.

Test results					
Time step	1	2	3	4	5
CPU cycles	38	38	38	38	38
Inputs					
In1 (DSP)	0	3277	6554	9830	13107
In2 (DSP)	3277	6554	9830	13107	16384
In1	0	0.1	0.2	0.3	0.4
In2	0.1	0.2	0.3	0.4	0.5
Parameters					
Toggle					
Outputs					
Out	0	0.1	0.2	0.3	0.4
Exp. Out	0	0.1	0.2	0.3	0.4
Out (DSP)	0	3277	6554	9830	13107
Exp. Out (DSP)	0	3277	6554	9830	13107

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	38
Max CPU cycles	38
Avg CPU cycles	38

Test case: Parameter test OK

Parameter test for General block ManualSwitch.

Test results						
Time step	1	2	3	4	...	10
CPU cycles	38	38	38	38	...	38
Inputs						
In1 (DSP)	9830					
In2 (DSP)	19661					
In1	0.3					
In2	0.6					
Parameters						
Toggle	0	0.1	1	2	...	-3
Outputs						
Out	0.3	0.6	0.6	0.6	...	0.6
Exp. Out	0.3	0.6	0.6	0.6	...	0.6
Out (DSP)	9830	19661	19661	19661	...	19661
Exp. Out (DSP)	9830	19661	19661	19661	...	19661

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	38
Max CPU cycles	38
Avg CPU cycles	38

Test case: Conversion test **OK**

Conversion test for General block ManualSwitch.

Test results						
Time step	1	2	3	4	...	10
Mask parameters						
Toggle	0	0.1	1	2	...	-3
Controller parameters						
Toggle	0	1	1	1	...	1
Exp. Toggle	0	1	1	1	...	1

Test settings	
Tolerance Toggle	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block ManualSwitch.

Test results						
Time step	1	2	3	4	...	10
Mask parameters						
Toggle	0	0.1	1	2	...	-3
Controller parameters						
Toggle	0	1	1	1	...	1
Exp. Toggle	0	1	1	1	...	1

Test settings	
Tolerance Toggle	±0,0000e+00

Test statistics	
Min CPU cycles	611
Max CPU cycles	646
Avg CPU cycles	639

Verification: ManualSwitch FiP32 CPU TMS320F28335

Date of Test 2026-06-19

Target controller TMS320F28335

Test case: Inport test OK

Inport test for General block ManualSwitch.

Test results				
Time step	1	2	...	5
CPU cycles	56	56	...	56
Inputs				
In1 (DSP)	0	214748365	...	858993459
In2 (DSP)	214748365	429496730	...	1073741824
In1	0	0.1	...	0.4
In2	0.1	0.2	...	0.5
Parameters				
Toggle	0			
Outputs				
Out	0	0.1	...	0.4
Exp. Out	0	0.1	...	0.4
Out (DSP)	0	214748365	...	858993459
Exp. Out (DSP)	0	214748365	...	858993459

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	56
Max CPU cycles	56
Avg CPU cycles	56

Test case: Parameter test OK

Parameter test for General block ManualSwitch.

Test results				
Time step	1	2	...	10
CPU cycles	56	56	...	56
Inputs				
In1 (DSP)	644245094			
In2 (DSP)	1288490189			
In1	0.3			
In2	0.6			
Parameters				
Toggle	0	0.1	...	-3
Outputs				
Out	0.3	0.6	...	0.6
Exp. Out	0.3	0.6	...	0.6
Out (DSP)	644245094	1288490189	...	1288490189
Exp. Out (DSP)	644245094	1288490189	...	1288490189

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	56
Max CPU cycles	56
Avg CPU cycles	56

Test case: Conversion test **OK**

Conversion test for General block ManualSwitch.

Test results						
Time step	1	2	3	4	...	10
Mask parameters						
Toggle	0	0.1	1	2	...	-3
Controller parameters						
Toggle	0	1	1	1	...	1
Exp. Toggle	0	1	1	1	...	1

Test settings	
Tolerance Toggle	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block ManualSwitch.

Test results						
Time step	1	2	3	4	...	10
Mask parameters						
Toggle	0	0.1	1	2	...	-3
Controller parameters						
Toggle	0	1	1	1	...	1
Exp. Toggle	0	1	1	1	...	1

Test settings	
Tolerance Toggle	±0,0000e+00

Test statistics	
Min CPU cycles	788
Max CPU cycles	829
Avg CPU cycles	820

Verification: ManualSwitch FiP32 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for General block ManualSwitch.

Test results				
Time step	1	2	...	5
CPU cycles	23	23	...	23
Inputs				
In1 (DSP)	0	214748365	...	858993459
In2 (DSP)	214748365	429496730	...	1073741824
In1	0	0.1	...	0.4
In2	0.1	0.2	...	0.5
Parameters				
Toggle	0			
Outputs				
Out	0	0.1	...	0.4
Exp. Out	0	0.1	...	0.4
Out (DSP)	0	214748365	...	858993459
Exp. Out (DSP)	0	214748365	...	858993459

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	23
Max CPU cycles	23
Avg CPU cycles	23

Test case: Parameter test OK

Parameter test for General block ManualSwitch.

Test results				
Time step	1	2	...	10
CPU cycles	23	23	...	23
Inputs				
In1 (DSP)	644245094			
In2 (DSP)	1288490189			
In1	0.3			
In2	0.6			
Parameters				
Toggle	0	0.1	...	-3
Outputs				
Out	0.3	0.6	...	0.6
Exp. Out	0.3	0.6	...	0.6
Out (DSP)	644245094	1288490189	...	1288490189
Exp. Out (DSP)	644245094	1288490189	...	1288490189

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	23
Max CPU cycles	23
Avg CPU cycles	23

Test case: Conversion test **OK**

Conversion test for General block ManualSwitch.

Test results						
Time step	1	2	3	4	...	10
Mask parameters						
Toggle	0	0.1	1	2	...	-3
Controller parameters						
Toggle	0	1	1	1	...	1
Exp. Toggle	0	1	1	1	...	1

Test settings	
Tolerance Toggle	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block ManualSwitch.

Test results						
Time step	1	2	3	4	...	10
Mask parameters						
Toggle	0	0.1	1	2	...	-3
Controller parameters						
Toggle	0	1	1	1	...	1
Exp. Toggle	0	1	1	1	...	1

Test settings	
Tolerance Toggle	±0,0000e+00

Test statistics	
Min CPU cycles	375
Max CPU cycles	399
Avg CPU cycles	393

Verification: ManualSwitch FiP32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for General block ManualSwitch.

Test results				
Time step	1	2	...	5
CPU cycles	57	57	...	57
Inputs				
In1 (DSP)	0	214748365	...	858993459
In2 (DSP)	214748365	429496730	...	1073741824
In1	0	0.1	...	0.4
In2	0.1	0.2	...	0.5
Parameters				
Toggle	0			
Outputs				
Out	0	0.1	...	0.4
Exp. Out	0	0.1	...	0.4
Out (DSP)	0	214748365	...	858993459
Exp. Out (DSP)	0	214748365	...	858993459

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	57
Max CPU cycles	57
Avg CPU cycles	57

Test case: Parameter test OK

Parameter test for General block ManualSwitch.

Test results				
Time step	1	2	...	10
CPU cycles	57	57	...	57
Inputs				
In1 (DSP)	644245094			
In2 (DSP)	1288490189			
In1	0.3			
In2	0.6			
Parameters				
Toggle	0	0.1	...	-3
Outputs				
Out	0.3	0.6	...	0.6
Exp. Out	0.3	0.6	...	0.6
Out (DSP)	644245094	1288490189	...	1288490189
Exp. Out (DSP)	644245094	1288490189	...	1288490189

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	57
Max CPU cycles	57
Avg CPU cycles	57

Test case: Conversion test **OK**

Conversion test for General block ManualSwitch.

Test results						
Time step	1	2	3	4	...	10
Mask parameters						
Toggle	0	0.1	1	2	...	-3
Controller parameters						
Toggle	0	1	1	1	...	1
Exp. Toggle	0	1	1	1	...	1

Test settings	
Tolerance Toggle	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block ManualSwitch.

Test results						
Time step	1	2	3	4	...	10
Mask parameters						
Toggle	0	0.1	1	2	...	-3
Controller parameters						
Toggle	0	1	1	1	...	1
Exp. Toggle	0	1	1	1	...	1

Test settings	
Tolerance Toggle	±0,0000e+00

Test statistics	
Min CPU cycles	511
Max CPU cycles	539
Avg CPU cycles	533

Verification: ManualSwitch FiP32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for General block ManualSwitch.

Test results				
Time step	1	2	...	5
CPU cycles	45	45	...	45
Inputs				
In1 (DSP)	0	214748365	...	858993459
In2 (DSP)	214748365	429496730	...	1073741824
In1	0	0.1	...	0.4
In2	0.1	0.2	...	0.5
Parameters				
Toggle	0			
Outputs				
Out	0	0.1	...	0.4
Exp. Out	0	0.1	...	0.4
Out (DSP)	0	214748365	...	858993459
Exp. Out (DSP)	0	214748365	...	858993459

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	45
Max CPU cycles	45
Avg CPU cycles	45

Test case: Parameter test OK

Parameter test for General block ManualSwitch.

Test results				
Time step	1	2	...	10
CPU cycles	45	45	...	45
Inputs				
In1 (DSP)	644245094			
In2 (DSP)	1288490189			
In1	0.3			
In2	0.6			
Parameters				
Toggle	0	0.1	...	-3
Outputs				
Out	0.3	0.6	...	0.6
Exp. Out	0.3	0.6	...	0.6
Out (DSP)	644245094	1288490189	...	1288490189
Exp. Out (DSP)	644245094	1288490189	...	1288490189

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	45
Max CPU cycles	45
Avg CPU cycles	45

Test case: Conversion test **OK**

Conversion test for General block ManualSwitch.

Test results						
Time step	1	2	3	4	...	10
Mask parameters						
Toggle	0	0.1	1	2	...	-3
Controller parameters						
Toggle	0	1	1	1	...	1
Exp. Toggle	0	1	1	1	...	1

Test settings	
Tolerance Toggle	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block ManualSwitch.

Test results						
Time step	1	2	3	4	...	10
Mask parameters						
Toggle	0	0.1	1	2	...	-3
Controller parameters						
Toggle	0	1	1	1	...	1
Exp. Toggle	0	1	1	1	...	1

Test settings	
Tolerance Toggle	±0,0000e+00

Test statistics	
Min CPU cycles	602
Max CPU cycles	612
Avg CPU cycles	604

Verification: ManualSwitch FiP32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for General block ManualSwitch.

Test results				
Time step	1	2	...	5
CPU cycles	27	27	...	27
Inputs				
In1 (DSP)	0	214748365	...	858993459
In2 (DSP)	214748365	429496730	...	1073741824
In1	0	0.1	...	0.4
In2	0.1	0.2	...	0.5
Parameters				
Toggle	0			
Outputs				
Out	0	0.1	...	0.4
Exp. Out	0	0.1	...	0.4
Out (DSP)	0	214748365	...	858993459
Exp. Out (DSP)	0	214748365	...	858993459

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	27
Max CPU cycles	27
Avg CPU cycles	27

Test case: Parameter test OK

Parameter test for General block ManualSwitch.

Test results				
Time step	1	2	...	10
CPU cycles	27	27	...	27
Inputs				
In1 (DSP)	644245094			
In2 (DSP)	1288490189			
In1	0.3			
In2	0.6			
Parameters				
Toggle	0	0.1	...	-3
Outputs				
Out	0.3	0.6	...	0.6
Exp. Out	0.3	0.6	...	0.6
Out (DSP)	644245094	1288490189	...	1288490189
Exp. Out (DSP)	644245094	1288490189	...	1288490189

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	27
Max CPU cycles	27
Avg CPU cycles	27

Test case: Conversion test **OK**

Conversion test for General block ManualSwitch.

Test results						
Time step	1	2	3	4	...	10
Mask parameters						
Toggle	0	0.1	1	2	...	-3
Controller parameters						
Toggle	0	1	1	1	...	1
Exp. Toggle	0	1	1	1	...	1

Test settings	
Tolerance Toggle	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block ManualSwitch.

Test results						
Time step	1	2	3	4	...	10
Mask parameters						
Toggle	0	0.1	1	2	...	-3
Controller parameters						
Toggle	0	1	1	1	...	1
Exp. Toggle	0	1	1	1	...	1

Test settings	
Tolerance Toggle	±0,0000e+00

Test statistics	
Min CPU cycles	245
Max CPU cycles	279
Avg CPU cycles	266

Verification: ManualSwitch FiP32 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for General block ManualSwitch.

Test results				
Time step	1	2	...	5
CPU cycles	43	43	...	43
Inputs				
In1 (DSP)	0	214748365	...	858993459
In2 (DSP)	214748365	429496730	...	1073741824
In1	0	0.1	...	0.4
In2	0.1	0.2	...	0.5
Parameters				
Toggle	0			
Outputs				
Out	0	0.1	...	0.4
Exp. Out	0	0.1	...	0.4
Out (DSP)	0	214748365	...	858993459
Exp. Out (DSP)	0	214748365	...	858993459

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	43
Max CPU cycles	43
Avg CPU cycles	43

Test case: Parameter test OK

Parameter test for General block ManualSwitch.

Test results				
Time step	1	2	...	10
CPU cycles	43	43	...	43
Inputs				
In1 (DSP)	644245094			
In2 (DSP)	1288490189			
In1	0.3			
In2	0.6			
Parameters				
Toggle	0	0.1	...	-3
Outputs				
Out	0.3	0.6	...	0.6
Exp. Out	0.3	0.6	...	0.6
Out (DSP)	644245094	1288490189	...	1288490189
Exp. Out (DSP)	644245094	1288490189	...	1288490189

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	43
Max CPU cycles	43
Avg CPU cycles	43

Test case: Conversion test **OK**

Conversion test for General block ManualSwitch.

Test results						
Time step	1	2	3	4	...	10
Mask parameters						
Toggle	0	0.1	1	2	...	-3
Controller parameters						
Toggle	0	1	1	1	...	1
Exp. Toggle	0	1	1	1	...	1

Test settings	
Tolerance Toggle	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block ManualSwitch.

Test results						
Time step	1	2	3	4	...	10
Mask parameters						
Toggle	0	0.1	1	2	...	-3
Controller parameters						
Toggle	0	1	1	1	...	1
Exp. Toggle	0	1	1	1	...	1

Test settings	
Tolerance Toggle	±0,0000e+00

Test statistics	
Min CPU cycles	520
Max CPU cycles	546
Avg CPU cycles	527

Verification: ManualSwitch FiP32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for General block ManualSwitch.

Test results				
Time step	1	2	...	5
CPU cycles	53	53	...	53
Inputs				
In1 (DSP)	0	214748365	...	858993459
In2 (DSP)	214748365	429496730	...	1073741824
In1	0	0.1	...	0.4
In2	0.1	0.2	...	0.5
Parameters				
Toggle	0			
Outputs				
Out	0	0.1	...	0.4
Exp. Out	0	0.1	...	0.4
Out (DSP)	0	214748365	...	858993459
Exp. Out (DSP)	0	214748365	...	858993459

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	53
Max CPU cycles	53
Avg CPU cycles	53

Test case: Parameter test OK

Parameter test for General block ManualSwitch.

Test results				
Time step	1	2	...	10
CPU cycles	68	68	...	68
Inputs				
In1 (DSP)	644245094			
In2 (DSP)	1288490189			
In1	0.3			
In2	0.6			
Parameters				
Toggle	0	0.1	...	-3
Outputs				
Out	0.3	0.6	...	0.6
Exp. Out	0.3	0.6	...	0.6
Out (DSP)	644245094	1288490189	...	1288490189
Exp. Out (DSP)	644245094	1288490189	...	1288490189

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	68
Max CPU cycles	68
Avg CPU cycles	68

Test case: Conversion test **OK**

Conversion test for General block ManualSwitch.

Test results						
Time step	1	2	3	4	...	10
Mask parameters						
Toggle	0	0.1	1	2	...	-3
Controller parameters						
Toggle	0	1	1	1	...	1
Exp. Toggle	0	1	1	1	...	1

Test settings	
Tolerance Toggle	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block ManualSwitch.

Test results						
Time step	1	2	3	4	...	10
Mask parameters						
Toggle	0	0.1	1	2	...	-3
Controller parameters						
Toggle	0	1	1	1	...	1
Exp. Toggle	0	1	1	1	...	1

Test settings	
Tolerance Toggle	±0,0000e+00

Test statistics	
Min CPU cycles	453
Max CPU cycles	512
Avg CPU cycles	463

Verification: ManualSwitch FiP32 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for General block ManualSwitch.

Test results				
Time step	1	2	...	5
CPU cycles	36	36	...	36
Inputs				
In1 (DSP)	0	214748365	...	858993459
In2 (DSP)	214748365	429496730	...	1073741824
In1	0	0.1	...	0.4
In2	0.1	0.2	...	0.5
Parameters				
Toggle	0			
Outputs				
Out	0	0.1	...	0.4
Exp. Out	0	0.1	...	0.4
Out (DSP)	0	214748365	...	858993459
Exp. Out (DSP)	0	214748365	...	858993459

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	36
Max CPU cycles	36
Avg CPU cycles	36

Test case: Parameter test OK

Parameter test for General block ManualSwitch.

Test results				
Time step	1	2	...	10
CPU cycles	36	36	...	36
Inputs				
In1 (DSP)	644245094			
In2 (DSP)	1288490189			
In1	0.3			
In2	0.6			
Parameters				
Toggle	0	0.1	...	-3
Outputs				
Out	0.3	0.6	...	0.6
Exp. Out	0.3	0.6	...	0.6
Out (DSP)	644245094	1288490189	...	1288490189
Exp. Out (DSP)	644245094	1288490189	...	1288490189

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	36
Max CPU cycles	36
Avg CPU cycles	36

Test case: Conversion test **OK**

Conversion test for General block ManualSwitch.

Test results						
Time step	1	2	3	4	...	10
Mask parameters						
Toggle	0	0.1	1	2	...	-3
Controller parameters						
Toggle	0	1	1	1	...	1
Exp. Toggle	0	1	1	1	...	1

Test settings	
Tolerance Toggle	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block ManualSwitch.

Test results						
Time step	1	2	3	4	...	10
Mask parameters						
Toggle	0	0.1	1	2	...	-3
Controller parameters						
Toggle	0	1	1	1	...	1
Exp. Toggle	0	1	1	1	...	1

Test settings	
Tolerance Toggle	±0,0000e+00

Test statistics	
Min CPU cycles	606
Max CPU cycles	633
Avg CPU cycles	627

Verification: ManualSwitch Float32 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for General block ManualSwitch.

Test results				
Time step	1	2	...	5
CPU cycles	56	56	...	56
Inputs				
In1 (DSP)	0	0.1	...	0.4
In2 (DSP)	0.1	0.2	...	0.5
In1	0	0.1	...	0.4
In2	0.1	0.2	...	0.5
Parameters				
Toggle	0			
Outputs				
Out	0	0.1	...	0.4
Exp. Out	0	0.1	...	0.4
Out (DSP)	0	0.1	...	0.4
Exp. Out (DSP)	0	0.1	...	0.4

Test settings	
Tolerance Out	±1,5259e-05 (±32768 LSB)

Test statistics	
Min CPU cycles	56
Max CPU cycles	56
Avg CPU cycles	56

Test case: Parameter test OK

Parameter test for General block ManualSwitch.

Test results				
Time step	1	2	...	10
CPU cycles	56	56	...	56
Inputs				
In1 (DSP)	0.3			
In2 (DSP)	0.6			
In1	0.3			
In2	0.6			
Parameters				
Toggle	0	0.1	...	-3
Outputs				
Out	0.3	0.6	...	0.6
Exp. Out	0.3	0.6	...	0.6
Out (DSP)	0.3	0.6	...	0.6
Exp. Out (DSP)	0.3	0.6	...	0.6

Test settings	
Tolerance Out	±1,5259e-05 (±32768 LSB)

Test statistics	
Min CPU cycles	56
Max CPU cycles	56
Avg CPU cycles	56

Test case: Conversion test **OK**

Conversion test for General block ManualSwitch.

Test results						
Time step	1	2	3	4	...	10
Mask parameters						
Toggle	0	0.1	1	2	...	-3
Controller parameters						
Toggle	0	1	1	1	...	1
Exp. Toggle	0	1	1	1	...	1

Test settings	
Tolerance Toggle	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block ManualSwitch.

Test results						
Time step	1	2	3	4	...	10
Mask parameters						
Toggle	0	0.1	1	2	...	-3
Controller parameters						
Toggle	0	1	1	1	...	1
Exp. Toggle	0	1	1	1	...	1

Test settings	
Tolerance Toggle	±0,0000e+00

Test statistics	
Min CPU cycles	778
Max CPU cycles	825
Avg CPU cycles	815

Verification: ManualSwitch Float32 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for General block ManualSwitch.

Test results				
Time step	1	2	...	5
CPU cycles	23	23	...	23
Inputs				
In1 (DSP)	0	0.1	...	0.4
In2 (DSP)	0.1	0.2	...	0.5
In1	0	0.1	...	0.4
In2	0.1	0.2	...	0.5
Parameters				
Toggle	0			
Outputs				
Out	0	0.1	...	0.4
Exp. Out	0	0.1	...	0.4
Out (DSP)	0	0.1	...	0.4
Exp. Out (DSP)	0	0.1	...	0.4

Test settings	
Tolerance Out	±1,5259e-05 (±32768 LSB)

Test statistics	
Min CPU cycles	23
Max CPU cycles	23
Avg CPU cycles	23

Test case: Parameter test OK

Parameter test for General block ManualSwitch.

Test results				
Time step	1	2	...	10
CPU cycles	23	23	...	23
Inputs				
In1 (DSP)	0.3			
In2 (DSP)	0.6			
In1	0.3			
In2	0.6			
Parameters				
Toggle	0	0.1	...	-3
Outputs				
Out	0.3	0.6	...	0.6
Exp. Out	0.3	0.6	...	0.6
Out (DSP)	0.3	0.6	...	0.6
Exp. Out (DSP)	0.3	0.6	...	0.6

Test settings	
Tolerance Out	±1,5259e-05 (±32768 LSB)

Test statistics	
Min CPU cycles	23
Max CPU cycles	23
Avg CPU cycles	23

Test case: Conversion test **OK**

Conversion test for General block ManualSwitch.

Test results						
Time step	1	2	3	4	...	10
Mask parameters						
Toggle	0	0.1	1	2	...	-3
Controller parameters						
Toggle	0	1	1	1	...	1
Exp. Toggle	0	1	1	1	...	1

Test settings	
Tolerance Toggle	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block ManualSwitch.

Test results						
Time step	1	2	3	4	...	10
Mask parameters						
Toggle	0	0.1	1	2	...	-3
Controller parameters						
Toggle	0	1	1	1	...	1
Exp. Toggle	0	1	1	1	...	1

Test settings	
Tolerance Toggle	±0,0000e+00

Test statistics	
Min CPU cycles	375
Max CPU cycles	399
Avg CPU cycles	393

Verification: ManualSwitch Float32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for General block ManualSwitch.

Test results				
Time step	1	2	...	5
CPU cycles	52	52	...	52
Inputs				
In1 (DSP)	0	0.1	...	0.4
In2 (DSP)	0.1	0.2	...	0.5
In1	0	0.1	...	0.4
In2	0.1	0.2	...	0.5
Parameters				
Toggle	0			
Outputs				
Out	0	0.1	...	0.4
Exp. Out	0	0.1	...	0.4
Out (DSP)	0	0.1	...	0.4
Exp. Out (DSP)	0	0.1	...	0.4

Test settings	
Tolerance Out	±1,5259e-05 (±32768 LSB)

Test statistics	
Min CPU cycles	52
Max CPU cycles	52
Avg CPU cycles	52

Test case: Parameter test OK

Parameter test for General block ManualSwitch.

Test results				
Time step	1	2	...	10
CPU cycles	52	52	...	52
Inputs				
In1 (DSP)	0.3			
In2 (DSP)	0.6			
In1	0.3			
In2	0.6			
Parameters				
Toggle	0	0.1	...	-3
Outputs				
Out	0.3	0.6	...	0.6
Exp. Out	0.3	0.6	...	0.6
Out (DSP)	0.3	0.6	...	0.6
Exp. Out (DSP)	0.3	0.6	...	0.6

Test settings	
Tolerance Out	±1,5259e-05 (±32768 LSB)

Test statistics	
Min CPU cycles	52
Max CPU cycles	52
Avg CPU cycles	52

Test case: Conversion test **OK**

Conversion test for General block ManualSwitch.

Test results						
Time step	1	2	3	4	...	10
Mask parameters						
Toggle	0	0.1	1	2	...	-3
Controller parameters						
Toggle	0	1	1	1	...	1
Exp. Toggle	0	1	1	1	...	1

Test settings	
Tolerance Toggle	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block ManualSwitch.

Test results						
Time step	1	2	3	4	...	10
Mask parameters						
Toggle	0	0.1	1	2	...	-3
Controller parameters						
Toggle	0	1	1	1	...	1
Exp. Toggle	0	1	1	1	...	1

Test settings	
Tolerance Toggle	±0,0000e+00

Test statistics	
Min CPU cycles	513
Max CPU cycles	539
Avg CPU cycles	533

Verification: ManualSwitch Float32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for General block ManualSwitch.

Test results				
Time step	1	2	...	5
CPU cycles	45	45	...	45
Inputs				
In1 (DSP)	0	0.1	...	0.4
In2 (DSP)	0.1	0.2	...	0.5
In1	0	0.1	...	0.4
In2	0.1	0.2	...	0.5
Parameters				
Toggle	0			
Outputs				
Out	0	0.1	...	0.4
Exp. Out	0	0.1	...	0.4
Out (DSP)	0	0.1	...	0.4
Exp. Out (DSP)	0	0.1	...	0.4

Test settings	
Tolerance Out	±1,5259e-05 (±32768 LSB)

Test statistics	
Min CPU cycles	45
Max CPU cycles	45
Avg CPU cycles	45

Test case: Parameter test OK

Parameter test for General block ManualSwitch.

Test results				
Time step	1	2	...	10
CPU cycles	45	45	...	45
Inputs				
In1 (DSP)	0.3			
In2 (DSP)	0.6			
In1	0.3			
In2	0.6			
Parameters				
Toggle	0	0.1	...	-3
Outputs				
Out	0.3	0.6	...	0.6
Exp. Out	0.3	0.6	...	0.6
Out (DSP)	0.3	0.6	...	0.6
Exp. Out (DSP)	0.3	0.6	...	0.6

Test settings	
Tolerance Out	±1,5259e-05 (±32768 LSB)

Test statistics	
Min CPU cycles	45
Max CPU cycles	45
Avg CPU cycles	45

Test case: Conversion test **OK**

Conversion test for General block ManualSwitch.

Test results						
Time step	1	2	3	4	...	10
Mask parameters						
Toggle	0	0.1	1	2	...	-3
Controller parameters						
Toggle	0	1	1	1	...	1
Exp. Toggle	0	1	1	1	...	1

Test settings	
Tolerance Toggle	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block ManualSwitch.

Test results						
Time step	1	2	3	4	...	10
Mask parameters						
Toggle	0	0.1	1	2	...	-3
Controller parameters						
Toggle	0	1	1	1	...	1
Exp. Toggle	0	1	1	1	...	1

Test settings	
Tolerance Toggle	±0,0000e+00

Test statistics	
Min CPU cycles	602
Max CPU cycles	612
Avg CPU cycles	604

Verification: ManualSwitch Float32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for General block ManualSwitch.

Test results				
Time step	1	2	...	5
CPU cycles	27	27	...	27
Inputs				
In1 (DSP)	0	0.1	...	0.4
In2 (DSP)	0.1	0.2	...	0.5
In1	0	0.1	...	0.4
In2	0.1	0.2	...	0.5
Parameters				
Toggle	0			
Outputs				
Out	0	0.1	...	0.4
Exp. Out	0	0.1	...	0.4
Out (DSP)	0	0.1	...	0.4
Exp. Out (DSP)	0	0.1	...	0.4

Test settings	
Tolerance Out	±1,5259e-05 (±32768 LSB)

Test statistics	
Min CPU cycles	27
Max CPU cycles	27
Avg CPU cycles	27

Test case: Parameter test OK

Parameter test for General block ManualSwitch.

Test results				
Time step	1	2	...	10
CPU cycles	27	27	...	27
Inputs				
In1 (DSP)	0.3			
In2 (DSP)	0.6			
In1	0.3			
In2	0.6			
Parameters				
Toggle	0	0.1	...	-3
Outputs				
Out	0.3	0.6	...	0.6
Exp. Out	0.3	0.6	...	0.6
Out (DSP)	0.3	0.6	...	0.6
Exp. Out (DSP)	0.3	0.6	...	0.6

Test settings	
Tolerance Out	±1,5259e-05 (±32768 LSB)

Test statistics	
Min CPU cycles	27
Max CPU cycles	27
Avg CPU cycles	27

Test case: Conversion test **OK**

Conversion test for General block ManualSwitch.

Test results						
Time step	1	2	3	4	...	10
Mask parameters						
Toggle	0	0.1	1	2	...	-3
Controller parameters						
Toggle	0	1	1	1	...	1
Exp. Toggle	0	1	1	1	...	1

Test settings	
Tolerance Toggle	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block ManualSwitch.

Test results						
Time step	1	2	3	4	...	10
Mask parameters						
Toggle	0	0.1	1	2	...	-3
Controller parameters						
Toggle	0	1	1	1	...	1
Exp. Toggle	0	1	1	1	...	1

Test settings	
Tolerance Toggle	±0,0000e+00

Test statistics	
Min CPU cycles	245
Max CPU cycles	279
Avg CPU cycles	266

Verification: ManualSwitch Float32 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for General block ManualSwitch.

Test results				
Time step	1	2	...	5
CPU cycles	43	43	...	43
Inputs				
In1 (DSP)	0	0.1	...	0.4
In2 (DSP)	0.1	0.2	...	0.5
In1	0	0.1	...	0.4
In2	0.1	0.2	...	0.5
Parameters				
Toggle	0			
Outputs				
Out	0	0.1	...	0.4
Exp. Out	0	0.1	...	0.4
Out (DSP)	0	0.1	...	0.4
Exp. Out (DSP)	0	0.1	...	0.4

Test settings	
Tolerance Out	±1,5259e-05 (±32768 LSB)

Test statistics	
Min CPU cycles	43
Max CPU cycles	43
Avg CPU cycles	43

Test case: Parameter test OK

Parameter test for General block ManualSwitch.

Test results				
Time step	1	2	...	10
CPU cycles	43	43	...	43
Inputs				
In1 (DSP)	0.3			
In2 (DSP)	0.6			
In1	0.3			
In2	0.6			
Parameters				
Toggle	0	0.1	...	-3
Outputs				
Out	0.3	0.6	...	0.6
Exp. Out	0.3	0.6	...	0.6
Out (DSP)	0.3	0.6	...	0.6
Exp. Out (DSP)	0.3	0.6	...	0.6

Test settings	
Tolerance Out	±1,5259e-05 (±32768 LSB)

Test statistics	
Min CPU cycles	43
Max CPU cycles	43
Avg CPU cycles	43

Test case: Conversion test **OK**

Conversion test for General block ManualSwitch.

Test results						
Time step	1	2	3	4	...	10
Mask parameters						
Toggle	0	0.1	1	2	...	-3
Controller parameters						
Toggle	0	1	1	1	...	1
Exp. Toggle	0	1	1	1	...	1

Test settings	
Tolerance Toggle	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block ManualSwitch.

Test results						
Time step	1	2	3	4	...	10
Mask parameters						
Toggle	0	0.1	1	2	...	-3
Controller parameters						
Toggle	0	1	1	1	...	1
Exp. Toggle	0	1	1	1	...	1

Test settings	
Tolerance Toggle	±0,0000e+00

Test statistics	
Min CPU cycles	520
Max CPU cycles	546
Avg CPU cycles	527

Verification: ManualSwitch Float32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for General block ManualSwitch.

Test results				
Time step	1	2	...	5
CPU cycles	53	53	...	53
Inputs				
In1 (DSP)	0	0.1	...	0.4
In2 (DSP)	0.1	0.2	...	0.5
In1	0	0.1	...	0.4
In2	0.1	0.2	...	0.5
Parameters				
Toggle	0			
Outputs				
Out	0	0.1	...	0.4
Exp. Out	0	0.1	...	0.4
Out (DSP)	0	0.1	...	0.4
Exp. Out (DSP)	0	0.1	...	0.4

Test settings	
Tolerance Out	±1,5259e-05 (±32768 LSB)

Test statistics	
Min CPU cycles	53
Max CPU cycles	53
Avg CPU cycles	53

Test case: Parameter test OK

Parameter test for General block ManualSwitch.

Test results				
Time step	1	2	...	10
CPU cycles	53	53	...	53
Inputs				
In1 (DSP)	0.3			
In2 (DSP)	0.6			
In1	0.3			
In2	0.6			
Parameters				
Toggle	0	0.1	...	-3
Outputs				
Out	0.3	0.6	...	0.6
Exp. Out	0.3	0.6	...	0.6
Out (DSP)	0.3	0.6	...	0.6
Exp. Out (DSP)	0.3	0.6	...	0.6

Test settings	
Tolerance Out	±1,5259e-05 (±32768 LSB)

Test statistics	
Min CPU cycles	53
Max CPU cycles	53
Avg CPU cycles	53

Test case: Conversion test **OK**

Conversion test for General block ManualSwitch.

Test results						
Time step	1	2	3	4	...	10
Mask parameters						
Toggle	0	0.1	1	2	...	-3
Controller parameters						
Toggle	0	1	1	1	...	1
Exp. Toggle	0	1	1	1	...	1

Test settings	
Tolerance Toggle	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block ManualSwitch.

Test results						
Time step	1	2	3	4	...	10
Mask parameters						
Toggle	0	0.1	1	2	...	-3
Controller parameters						
Toggle	0	1	1	1	...	1
Exp. Toggle	0	1	1	1	...	1

Test settings	
Tolerance Toggle	±0,0000e+00

Test statistics	
Min CPU cycles	418
Max CPU cycles	467
Avg CPU cycles	427

Verification: ManualSwitch Float32 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for General block ManualSwitch.

Test results				
Time step	1	2	...	5
CPU cycles	38	38	...	38
Inputs				
In1 (DSP)	0	0.1	...	0.4
In2 (DSP)	0.1	0.2	...	0.5
In1	0	0.1	...	0.4
In2	0.1	0.2	...	0.5
Parameters				
Toggle	0			
Outputs				
Out	0	0.1	...	0.4
Exp. Out	0	0.1	...	0.4
Out (DSP)	0	0.1	...	0.4
Exp. Out (DSP)	0	0.1	...	0.4

Test settings	
Tolerance Out	±1,5259e-05 (±32768 LSB)

Test statistics	
Min CPU cycles	38
Max CPU cycles	38
Avg CPU cycles	38

Test case: Parameter test OK

Parameter test for General block ManualSwitch.

Test results				
Time step	1	2	...	10
CPU cycles	38	38	...	38
Inputs				
In1 (DSP)	0.3			
In2 (DSP)	0.6			
In1	0.3			
In2	0.6			
Parameters				
Toggle	0	0.1	...	-3
Outputs				
Out	0.3	0.6	...	0.6
Exp. Out	0.3	0.6	...	0.6
Out (DSP)	0.3	0.6	...	0.6
Exp. Out (DSP)	0.3	0.6	...	0.6

Test settings	
Tolerance Out	±1,5259e-05 (±32768 LSB)

Test statistics	
Min CPU cycles	38
Max CPU cycles	38
Avg CPU cycles	38

Test case: Conversion test **OK**

Conversion test for General block ManualSwitch.

Test results						
Time step	1	2	3	4	...	10
Mask parameters						
Toggle	0	0.1	1	2	...	-3
Controller parameters						
Toggle	0	1	1	1	...	1
Exp. Toggle	0	1	1	1	...	1

Test settings	
Tolerance Toggle	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block ManualSwitch.

Test results						
Time step	1	2	3	4	...	10
Mask parameters						
Toggle	0	0.1	1	2	...	-3
Controller parameters						
Toggle	0	1	1	1	...	1
Exp. Toggle	0	1	1	1	...	1

Test settings	
Tolerance Toggle	±0,0000e+00

Test statistics	
Min CPU cycles	620
Max CPU cycles	652
Avg CPU cycles	645

Block: Maximum



Outputs the greater value of the two input signals.

Inports	
In1	Input #1
In2	Input #2

Outports	
Out	Maximum of Input #1 and Input #2

Description:

Calculation:

$$\mathrm{Out} = \max\left(\mathrm{In}_1, \mathrm{In}_2\right)$$

Implementations:

FiP16	16 Bit Fixed Point Implementation
FiP32	32 Bit Fixed Point Implementation
Float32	32 Bit Floating Point Implementation
Float64	64 Bit Floating Point Implementation

Implementation: FiP16

16 Bit Fixed Point Implementation

Inports Data Type	
In1	int16
In2	int16

Outports Data Type	
Out	int16

Implementation: FiP32

32 Bit Fixed Point Implementation

Inports Data Type	
In1	int32
In2	int32

Outports Data Type	
Out	int32

Implementation: Float32

32 Bit Floating Point Implementation

Inports Data Type	
In1	float32
In2	float32

Outports Data Type	
Out	float32

Implementation: Float64

64 Bit Floating Point Implementation

Inports Data Type	
In1	float64
In2	float64

Outports Data Type	
Out	float64

Verification: Maximum FiP16 CPU TMS320F28335

Date of Test 2026-06-19

Target controller TMS320F28335

Test case: Inport test OK

Inport test for General block Maximum.

Test results						
Time step	1	2	3	4	...	214
CPU cycles	64	64	64	64	...	63
Inputs						
In1 (DSP)	-32768	-32150	-31531	-30913	...	32767
In2 (DSP)	32767	32150	31531	30913	...	32767
In1	-1	-0.981	-0.962	-0.943	...	1
In2	1	0.981	0.962	0.943	...	1
Outputs						
Out	1	0.981	0.962	0.943	...	1
Exp. Out	1	0.981	0.962	0.943	...	1
Out (DSP)	32767	32150	31531	30913	...	32767
Exp. Out (DSP)	32767	32150	31531	30913	...	32767

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	63
Max CPU cycles	64
Avg CPU cycles	63

Verification: Maximum FiP16 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for General block Maximum.

Test results						
Time step	1	2	3	4	...	214
CPU cycles	27	27	27	27	...	27
Inputs						
In1 (DSP)	-32768	-32150	-31531	-30913	...	32767
In2 (DSP)	32767	32150	31531	30913	...	32767
In1	-1	-0.981	-0.962	-0.943	...	1
In2	1	0.981	0.962	0.943	...	1
Outputs						
Out	1	0.981	0.962	0.943	...	1
Exp. Out	1	0.981	0.962	0.943	...	1
Out (DSP)	32767	32150	31531	30913	...	32767
Exp. Out (DSP)	32767	32150	31531	30913	...	32767

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	27
Max CPU cycles	27
Avg CPU cycles	27

Verification: Maximum FiP16 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for General block Maximum.

Test results						
Time step	1	2	3	4	...	214
CPU cycles	62	62	62	62	...	62
Inputs						
In1 (DSP)	-32768	-32150	-31531	-30913	...	32767
In2 (DSP)	32767	32150	31531	30913	...	32767
In1	-1	-0.981	-0.962	-0.943	...	1
In2	1	0.981	0.962	0.943	...	1
Outputs						
Out	1	0.981	0.962	0.943	...	1
Exp. Out	1	0.981	0.962	0.943	...	1
Out (DSP)	32767	32150	31531	30913	...	32767
Exp. Out (DSP)	32767	32150	31531	30913	...	32767

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	62
Max CPU cycles	62
Avg CPU cycles	62

Verification: Maximum FiP16 CPU STM32F072RB

Date of Test 2026-06-19

Target controller STM32F072RB

Test case: Inport test OK

Inport test for General block Maximum.

Test results						
Time step	1	2	3	4	...	214
CPU cycles	66	66	66	66	...	67
Inputs						
In1 (DSP)	-32768	-32150	-31531	-30913	...	32767
In2 (DSP)	32767	32150	31531	30913	...	32767
In1	-1	-0.981	-0.962	-0.943	...	1
In2	1	0.981	0.962	0.943	...	1
Outputs						
Out	1	0.981	0.962	0.943	...	1
Exp. Out	1	0.981	0.962	0.943	...	1
Out (DSP)	32767	32150	31531	30913	...	32767
Exp. Out (DSP)	32767	32150	31531	30913	...	32767

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	66
Max CPU cycles	67
Avg CPU cycles	66

Verification: Maximum FiP16 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for General block Maximum.

Test results						
Time step	1	2	3	4	...	214
CPU cycles	35	35	35	35	...	35
Inputs						
In1 (DSP)	-32768	-32150	-31531	-30913	...	32767
In2 (DSP)	32767	32150	31531	30913	...	32767
In1	-1	-0.981	-0.962	-0.943	...	1
In2	1	0.981	0.962	0.943	...	1
Outputs						
Out	1	0.981	0.962	0.943	...	1
Exp. Out	1	0.981	0.962	0.943	...	1
Out (DSP)	32767	32150	31531	30913	...	32767
Exp. Out (DSP)	32767	32150	31531	30913	...	32767

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	35
Max CPU cycles	35
Avg CPU cycles	35

Verification: Maximum FiP16 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test — OK

Inport test for General block Maximum.

Test results						
Time step	1	2	3	4	...	214
CPU cycles	46	46	46	46	...	49
Inputs						
In1 (DSP)	-32768	-32150	-31531	-30913	...	32767
In2 (DSP)	32767	32150	31531	30913	...	32767
In1	-1	-0.981	-0.962	-0.943	...	1
In2	1	0.981	0.962	0.943	...	1
Outputs						
Out	1	0.981	0.962	0.943	...	1
Exp. Out	1	0.981	0.962	0.943	...	1
Out (DSP)	32767	32150	31531	30913	...	32767
Exp. Out (DSP)	32767	32150	31531	30913	...	32767

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	46
Max CPU cycles	49
Avg CPU cycles	48

Verification: Maximum FiP16 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for General block Maximum.

Test results						
Time step	1	2	3	4	...	214
CPU cycles	75	64	64	64	...	64
Inputs						
In1 (DSP)	-32768	-32150	-31531	-30913	...	32767
In2 (DSP)	32767	32150	31531	30913	...	32767
In1	-1	-0.981	-0.962	-0.943	...	1
In2	1	0.981	0.962	0.943	...	1
Outputs						
Out	1	0.981	0.962	0.943	...	1
Exp. Out	1	0.981	0.962	0.943	...	1
Out (DSP)	32767	32150	31531	30913	...	32767
Exp. Out (DSP)	32767	32150	31531	30913	...	32767

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	64
Max CPU cycles	75
Avg CPU cycles	64

Verification: Maximum FiP16 CPU TMS320F28379D

Date of Test 2026-06-22

Target controller TMS320F28379D

Test case: Inport test OK

Inport test for General block Maximum.

Test results						
Time step	1	2	3	4	...	214
CPU cycles	49	49	49	49	...	44
Inputs						
In1 (DSP)	-32768	-32150	-31531	-30913	...	32767
In2 (DSP)	32767	32150	31531	30913	...	32767
In1	-1	-0.981	-0.962	-0.943	...	1
In2	1	0.981	0.962	0.943	...	1
Outputs						
Out	1	0.981	0.962	0.943	...	1
Exp. Out	1	0.981	0.962	0.943	...	1
Out (DSP)	32767	32150	31531	30913	...	32767
Exp. Out (DSP)	32767	32150	31531	30913	...	32767

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	44
Max CPU cycles	49
Avg CPU cycles	45

Verification: Maximum FiP32 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for General block Maximum.

Test results				
Time step	1	2	...	214
CPU cycles	66	66	...	65
Inputs				
In1 (DSP)	-2147483648	-2106965089	...	2147483647
In2 (DSP)	2147483647	2106965089	...	2147483647
In1	-1	-0.981	...	1
In2	1	0.981	...	1
Outputs				
Out	1	0.981	...	1
Exp. Out	1	0.981	...	1
Out (DSP)	2147483647	2106965089	...	2147483647
Exp. Out (DSP)	2147483647	2106965089	...	2147483647

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	65
Max CPU cycles	66
Avg CPU cycles	65

Verification: Maximum FiP32 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for General block Maximum.

Test results				
Time step	1	2	...	214
CPU cycles	27	27	...	27
Inputs				
In1 (DSP)	-2147483648	-2106965089	...	2147483647
In2 (DSP)	2147483647	2106965089	...	2147483647
In1	-1	-0.981	...	1
In2	1	0.981	...	1
Outputs				
Out	1	0.981	...	1
Exp. Out	1	0.981	...	1
Out (DSP)	2147483647	2106965089	...	2147483647
Exp. Out (DSP)	2147483647	2106965089	...	2147483647

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	27
Max CPU cycles	27
Avg CPU cycles	27

Verification: Maximum FiP32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for General block Maximum.

Test results				
Time step	1	2	...	214
CPU cycles	57	57	...	57
Inputs				
In1 (DSP)	-2147483648	-2106965089	...	2147483647
In2 (DSP)	2147483647	2106965089	...	2147483647
In1	-1	-0.981	...	1
In2	1	0.981	...	1
Outputs				
Out	1	0.981	...	1
Exp. Out	1	0.981	...	1
Out (DSP)	2147483647	2106965089	...	2147483647
Exp. Out (DSP)	2147483647	2106965089	...	2147483647

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	57
Max CPU cycles	65
Avg CPU cycles	57

Verification: Maximum FiP32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for General block Maximum.

Test results				
Time step	1	2	...	214
CPU cycles	53	53	...	54
Inputs				
In1 (DSP)	-2147483648	-2106965089	...	2147483647
In2 (DSP)	2147483647	2106965089	...	2147483647
In1	-1	-0.981	...	1
In2	1	0.981	...	1
Outputs				
Out	1	0.981	...	1
Exp. Out	1	0.981	...	1
Out (DSP)	2147483647	2106965089	...	2147483647
Exp. Out (DSP)	2147483647	2106965089	...	2147483647

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	53
Max CPU cycles	54
Avg CPU cycles	53

Verification: Maximum FiP32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for General block Maximum.

Test results				
Time step	1	2	...	214
CPU cycles	33	33	...	33
Inputs				
In1 (DSP)	-2147483648	-2106965089	...	2147483647
In2 (DSP)	2147483647	2106965089	...	2147483647
In1	-1	-0.981	...	1
In2	1	0.981	...	1
Outputs				
Out	1	0.981	...	1
Exp. Out	1	0.981	...	1
Out (DSP)	2147483647	2106965089	...	2147483647
Exp. Out (DSP)	2147483647	2106965089	...	2147483647

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	33
Max CPU cycles	33
Avg CPU cycles	33

Verification: Maximum FiP32 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for General block Maximum.

Test results				
Time step	1	2	...	214
CPU cycles	50	50	...	53
Inputs				
In1 (DSP)	-2147483648	-2106965089	...	2147483647
In2 (DSP)	2147483647	2106965089	...	2147483647
In1	-1	-0.981	...	1
In2	1	0.981	...	1
Outputs				
Out	1	0.981	...	1
Exp. Out	1	0.981	...	1
Out (DSP)	2147483647	2106965089	...	2147483647
Exp. Out (DSP)	2147483647	2106965089	...	2147483647

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	50
Max CPU cycles	53
Avg CPU cycles	52

Verification: Maximum FiP32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test — OK

Inport test for General block Maximum.

Test results				
Time step	1	2	...	214
CPU cycles	57	57	...	57
Inputs				
In1 (DSP)	-2147483648	-2106965089	...	2147483647
In2 (DSP)	2147483647	2106965089	...	2147483647
In1	-1	-0.981	...	1
In2	1	0.981	...	1
Outputs				
Out	1	0.981	...	1
Exp. Out	1	0.981	...	1
Out (DSP)	2147483647	2106965089	...	2147483647
Exp. Out (DSP)	2147483647	2106965089	...	2147483647

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	57
Max CPU cycles	57
Avg CPU cycles	57

Verification: Maximum FiP32 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for General block Maximum.

Test results				
Time step	1	2	...	214
CPU cycles	49	49	...	51
Inputs				
In1 (DSP)	-2147483648	-2106965089	...	2147483647
In2 (DSP)	2147483647	2106965089	...	2147483647
In1	-1	-0.981	...	1
In2	1	0.981	...	1
Outputs				
Out	1	0.981	...	1
Exp. Out	1	0.981	...	1
Out (DSP)	2147483647	2106965089	...	2147483647
Exp. Out (DSP)	2147483647	2106965089	...	2147483647

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	49
Max CPU cycles	51
Avg CPU cycles	50

Verification: Maximum Float32 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for General block Maximum.

Test results				
Time step	1	2	...	214
CPU cycles	58	58	...	58
Inputs				
In1 (DSP)	-1	-0.981	...	1
In2 (DSP)	1	0.981	...	1
In1	-1	-0.981	...	1
In2	1	0.981	...	1
Outputs				
Out	1	0.981	...	1
Exp. Out	1	0.981	...	1
Out (DSP)	1	0.981	...	1
Exp. Out (DSP)	1	0.981	...	1

Test settings	
Tolerance Out	±3,2596e-08 (±70 LSB)

Test statistics	
Min CPU cycles	58
Max CPU cycles	58
Avg CPU cycles	58

Verification: Maximum Float32 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for General block Maximum.

Test results				
Time step	1	2	...	214
CPU cycles	31	31	...	33
Inputs				
In1 (DSP)	-1	-0.981	...	1
In2 (DSP)	1	0.981	...	1
In1	-1	-0.981	...	1
In2	1	0.981	...	1
Outputs				
Out	1	0.981	...	1
Exp. Out	1	0.981	...	1
Out (DSP)	1	0.981	...	1
Exp. Out (DSP)	1	0.981	...	1

Test settings	
Tolerance Out	±3,2596e-08 (±70 LSB)

Test statistics	
Min CPU cycles	31
Max CPU cycles	33
Avg CPU cycles	32

Verification: Maximum Float32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for General block Maximum.

Test results				
Time step	1	2	...	214
CPU cycles	72	72	...	72
Inputs				
In1 (DSP)	-1	-0.981	...	1
In2 (DSP)	1	0.981	...	1
In1	-1	-0.981	...	1
In2	1	0.981	...	1
Outputs				
Out	1	0.981	...	1
Exp. Out	1	0.981	...	1
Out (DSP)	1	0.981	...	1
Exp. Out (DSP)	1	0.981	...	1

Test settings	
Tolerance Out	±3,2596e-08 (±70 LSB)

Test statistics	
Min CPU cycles	72
Max CPU cycles	72
Avg CPU cycles	72

Verification: Maximum Float32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for General block Maximum.

Test results				
Time step	1	2	...	214
CPU cycles	136	136	...	150
Inputs				
In1 (DSP)	-1	-0.981	...	1
In2 (DSP)	1	0.981	...	1
In1	-1	-0.981	...	1
In2	1	0.981	...	1
Outputs				
Out	1	0.981	...	1
Exp. Out	1	0.981	...	1
Out (DSP)	1	0.981	...	1
Exp. Out (DSP)	1	0.981	...	1

Test settings	
Tolerance Out	±3,2596e-08 (±70 LSB)

Test statistics	
Min CPU cycles	136
Max CPU cycles	202
Avg CPU cycles	143

Verification: Maximum Float32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for General block Maximum.

Test results				
Time step	1	2	...	214
CPU cycles	85	85	...	85
Inputs				
In1 (DSP)	-1	-0.981	...	1
In2 (DSP)	1	0.981	...	1
In1	-1	-0.981	...	1
In2	1	0.981	...	1
Outputs				
Out	1	0.981	...	1
Exp. Out	1	0.981	...	1
Out (DSP)	1	0.981	...	1
Exp. Out (DSP)	1	0.981	...	1

Test settings	
Tolerance Out	±3,2596e-08 (±70 LSB)

Test statistics	
Min CPU cycles	63
Max CPU cycles	88
Avg CPU cycles	86

Verification: Maximum Float32 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for General block Maximum.

Test results				
Time step	1	2	...	214
CPU cycles	157	157	...	162
Inputs				
In1 (DSP)	-1	-0.981	...	1
In2 (DSP)	1	0.981	...	1
In1	-1	-0.981	...	1
In2	1	0.981	...	1
Outputs				
Out	1	0.981	...	1
Exp. Out	1	0.981	...	1
Out (DSP)	1	0.981	...	1
Exp. Out (DSP)	1	0.981	...	1

Test settings	
Tolerance Out	±3,2596e-08 (±70 LSB)

Test statistics	
Min CPU cycles	157
Max CPU cycles	166
Avg CPU cycles	160

Verification: Maximum Float32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for General block Maximum.

Test results				
Time step	1	2	...	214
CPU cycles	70	59	...	59
Inputs				
In1 (DSP)	-1	-0.981	...	1
In2 (DSP)	1	0.981	...	1
In1	-1	-0.981	...	1
In2	1	0.981	...	1
Outputs				
Out	1	0.981	...	1
Exp. Out	1	0.981	...	1
Out (DSP)	1	0.981	...	1
Exp. Out (DSP)	1	0.981	...	1

Test settings	
Tolerance Out	±3,2596e-08 (±70 LSB)

Test statistics	
Min CPU cycles	59
Max CPU cycles	70
Avg CPU cycles	59

Verification: Maximum Float32 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for General block Maximum.

Test results				
Time step	1	2	...	214
CPU cycles	42	42	...	42
Inputs				
In1 (DSP)	-1	-0.981	...	1
In2 (DSP)	1	0.981	...	1
In1	-1	-0.981	...	1
In2	1	0.981	...	1
Outputs				
Out	1	0.981	...	1
Exp. Out	1	0.981	...	1
Out (DSP)	1	0.981	...	1
Exp. Out (DSP)	1	0.981	...	1

Test settings	
Tolerance Out	±3,2596e-08 (±70 LSB)

Test statistics	
Min CPU cycles	42
Max CPU cycles	42
Avg CPU cycles	42

Block: Minimum



Outputs the lesser value of the two input signals.

Inports	
In1	Input #1
In2	Input #2

Outports	
Out	Minimum of Input #1 and Input #2

Description:

Calculation:

$$\mathrm{Out} = \min\left(\mathrm{In}_1, \mathrm{In}_2\right)$$

Implementations:

FiP16	16 Bit Fixed Point Implementation
FiP32	32 Bit Fixed Point Implementation
Float32	32 Bit Floating Point Implementation
Float64	64 Bit Floating Point Implementation

Implementation: FiP16

16 Bit Fixed Point Implementation

Inports Data Type	
In1	int16
In2	int16

Outports Data Type	
Out	int16

Implementation: FiP32

32 Bit Fixed Point Implementation

Inports Data Type	
In1	int32
In2	int32

Outports Data Type	
Out	int32

Implementation: Float32

32 Bit Floating Point Implementation

Inports Data Type	
In1	float32
In2	float32

Outports Data Type	
Out	float32

Implementation: Float64

64 Bit Floating Point Implementation

Inports Data Type	
In1	float64
In2	float64

Outports Data Type	
Out	float64

Verification: Minimum FiP16 CPU TMS320F28335

Date of Test 2026-06-19

Target controller TMS320F28335

Test case: Inport test OK

Inport test for General block Minimum.

Test results						
Time step	1	2	3	4	...	214
CPU cycles	63	63	63	63	...	63
Inputs						
In1 (DSP)	-32768	-32150	-31531	-30913	...	32767
In2 (DSP)	32767	32150	31531	30913	...	32767
In1	-1	-0.981	-0.962	-0.943	...	1
In2	1	0.981	0.962	0.943	...	1
Outputs						
Out	-1	-0.981	-0.962	-0.943	...	1
Exp. Out	-1	-0.981	-0.962	-0.943	...	1
Out (DSP)	-32768	-32150	-31531	-30913	...	32767
Exp. Out (DSP)	-32768	-32150	-31531	-30913	...	32767

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	63
Max CPU cycles	64
Avg CPU cycles	63

Verification: Minimum FiP16 CPU TM4C123GH6

Date of Test 2026-06-19

Target controller TM4C123GH6

Test case: Inport test OK

Inport test for General block Minimum.

Test results						
Time step	1	2	3	4	...	214
CPU cycles	27	27	27	27	...	27
Inputs						
In1 (DSP)	-32768	-32150	-31531	-30913	...	32767
In2 (DSP)	32767	32150	31531	30913	...	32767
In1	-1	-0.981	-0.962	-0.943	...	1
In2	1	0.981	0.962	0.943	...	1
Outputs						
Out	-1	-0.981	-0.962	-0.943	...	1
Exp. Out	-1	-0.981	-0.962	-0.943	...	1
Out (DSP)	-32768	-32150	-31531	-30913	...	32767
Exp. Out (DSP)	-32768	-32150	-31531	-30913	...	32767

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	27
Max CPU cycles	27
Avg CPU cycles	27

Verification: Minimum FiP16 CPU STM32G474RE

Date of Test 2026-06-19

Target controller STM32G474RE

Test case: Inport test OK

Inport test for General block Minimum.

Test results						
Time step	1	2	3	4	...	214
CPU cycles	62	62	62	62	...	62
Inputs						
In1 (DSP)	-32768	-32150	-31531	-30913	...	32767
In2 (DSP)	32767	32150	31531	30913	...	32767
In1	-1	-0.981	-0.962	-0.943	...	1
In2	1	0.981	0.962	0.943	...	1
Outputs						
Out	-1	-0.981	-0.962	-0.943	...	1
Exp. Out	-1	-0.981	-0.962	-0.943	...	1
Out (DSP)	-32768	-32150	-31531	-30913	...	32767
Exp. Out (DSP)	-32768	-32150	-31531	-30913	...	32767

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	62
Max CPU cycles	115
Avg CPU cycles	62

Verification: Minimum FiP16 CPU STM32F072RB

Date of Test 2026-06-19

Target controller STM32F072RB

Test case: Inport test OK

Inport test for General block Minimum.

Test results						
Time step	1	2	3	4	...	214
CPU cycles	67	67	67	67	...	67
Inputs						
In1 (DSP)	-32768	-32150	-31531	-30913	...	32767
In2 (DSP)	32767	32150	31531	30913	...	32767
In1	-1	-0.981	-0.962	-0.943	...	1
In2	1	0.981	0.962	0.943	...	1
Outputs						
Out	-1	-0.981	-0.962	-0.943	...	1
Exp. Out	-1	-0.981	-0.962	-0.943	...	1
Out (DSP)	-32768	-32150	-31531	-30913	...	32767
Exp. Out (DSP)	-32768	-32150	-31531	-30913	...	32767

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	66
Max CPU cycles	127
Avg CPU cycles	67

Verification: Minimum FiP16 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for General block Minimum.

Test results						
Time step	1	2	3	4	...	214
CPU cycles	35	35	35	35	...	35
Inputs						
In1 (DSP)	-32768	-32150	-31531	-30913	...	32767
In2 (DSP)	32767	32150	31531	30913	...	32767
In1	-1	-0.981	-0.962	-0.943	...	1
In2	1	0.981	0.962	0.943	...	1
Outputs						
Out	-1	-0.981	-0.962	-0.943	...	1
Exp. Out	-1	-0.981	-0.962	-0.943	...	1
Out (DSP)	-32768	-32150	-31531	-30913	...	32767
Exp. Out (DSP)	-32768	-32150	-31531	-30913	...	32767

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	35
Max CPU cycles	35
Avg CPU cycles	35

Verification: Minimum FiP16 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test — OK

Inport test for General block Minimum.

Test results						
Time step	1	2	3	4	...	214
CPU cycles	49	49	49	49	...	49
Inputs						
In1 (DSP)	-32768	-32150	-31531	-30913	...	32767
In2 (DSP)	32767	32150	31531	30913	...	32767
In1	-1	-0.981	-0.962	-0.943	...	1
In2	1	0.981	0.962	0.943	...	1
Outputs						
Out	-1	-0.981	-0.962	-0.943	...	1
Exp. Out	-1	-0.981	-0.962	-0.943	...	1
Out (DSP)	-32768	-32150	-31531	-30913	...	32767
Exp. Out (DSP)	-32768	-32150	-31531	-30913	...	32767

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	46
Max CPU cycles	49
Avg CPU cycles	48

Verification: Minimum FiP16 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for General block Minimum.

Test results						
Time step	1	2	3	4	...	214
CPU cycles	75	64	64	64	...	64
Inputs						
In1 (DSP)	-32768	-32150	-31531	-30913	...	32767
In2 (DSP)	32767	32150	31531	30913	...	32767
In1	-1	-0.981	-0.962	-0.943	...	1
In2	1	0.981	0.962	0.943	...	1
Outputs						
Out	-1	-0.981	-0.962	-0.943	...	1
Exp. Out	-1	-0.981	-0.962	-0.943	...	1
Out (DSP)	-32768	-32150	-31531	-30913	...	32767
Exp. Out (DSP)	-32768	-32150	-31531	-30913	...	32767

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	64
Max CPU cycles	75
Avg CPU cycles	64

Verification: Minimum FiP16 CPU TMS320F28379D

Date of Test 2026-06-22

Target controller TMS320F28379D

Test case: Inport test OK

Inport test for General block Minimum.

Test results						
Time step	1	2	3	4	...	214
CPU cycles	43	43	43	43	...	43
Inputs						
In1 (DSP)	-32768	-32150	-31531	-30913	...	32767
In2 (DSP)	32767	32150	31531	30913	...	32767
In1	-1	-0.981	-0.962	-0.943	...	1
In2	1	0.981	0.962	0.943	...	1
Outputs						
Out	-1	-0.981	-0.962	-0.943	...	1
Exp. Out	-1	-0.981	-0.962	-0.943	...	1
Out (DSP)	-32768	-32150	-31531	-30913	...	32767
Exp. Out (DSP)	-32768	-32150	-31531	-30913	...	32767

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	43
Max CPU cycles	48
Avg CPU cycles	44

Verification: Minimum FiP32 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test — OK

Inport test for General block Minimum.

Test results				
Time step	1	2	...	214
CPU cycles	65	65	...	65
Inputs				
In1 (DSP)	-2147483648	-2106965089	...	2147483647
In2 (DSP)	2147483647	2106965089	...	2147483647
In1	-1	-0.981	...	1
In2	1	0.981	...	1
Outputs				
Out	-1	-0.981	...	1
Exp. Out	-1	-0.981	...	1
Out (DSP)	-2147483648	-2106965089	...	2147483647
Exp. Out (DSP)	-2147483648	-2106965089	...	2147483647

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	65
Max CPU cycles	66
Avg CPU cycles	65

Verification: Minimum FiP32 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test — OK

Inport test for General block Minimum.

Test results				
Time step	1	2	...	214
CPU cycles	27	27	...	27
Inputs				
In1 (DSP)	-2147483648	-2106965089	...	2147483647
In2 (DSP)	2147483647	2106965089	...	2147483647
In1	-1	-0.981	...	1
In2	1	0.981	...	1
Outputs				
Out	-1	-0.981	...	1
Exp. Out	-1	-0.981	...	1
Out (DSP)	-2147483648	-2106965089	...	2147483647
Exp. Out (DSP)	-2147483648	-2106965089	...	2147483647

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	27
Max CPU cycles	27
Avg CPU cycles	27

Verification: Minimum FiP32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for General block Minimum.

Test results				
Time step	1	2	...	214
CPU cycles	62	62	...	62
Inputs				
In1 (DSP)	-2147483648	-2106965089	...	2147483647
In2 (DSP)	2147483647	2106965089	...	2147483647
In1	-1	-0.981	...	1
In2	1	0.981	...	1
Outputs				
Out	-1	-0.981	...	1
Exp. Out	-1	-0.981	...	1
Out (DSP)	-2147483648	-2106965089	...	2147483647
Exp. Out (DSP)	-2147483648	-2106965089	...	2147483647

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	62
Max CPU cycles	65
Avg CPU cycles	62

Verification: Minimum FiP32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for General block Minimum.

Test results				
Time step	1	2	...	214
CPU cycles	54	54	...	54
Inputs				
In1 (DSP)	-2147483648	-2106965089	...	2147483647
In2 (DSP)	2147483647	2106965089	...	2147483647
In1	-1	-0.981	...	1
In2	1	0.981	...	1
Outputs				
Out	-1	-0.981	...	1
Exp. Out	-1	-0.981	...	1
Out (DSP)	-2147483648	-2106965089	...	2147483647
Exp. Out (DSP)	-2147483648	-2106965089	...	2147483647

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	53
Max CPU cycles	54
Avg CPU cycles	53

Verification: Minimum FiP32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test — OK

Inport test for General block Minimum.

Test results				
Time step	1	2	...	214
CPU cycles	33	33	...	33
Inputs				
In1 (DSP)	-2147483648	-2106965089	...	2147483647
In2 (DSP)	2147483647	2106965089	...	2147483647
In1	-1	-0.981	...	1
In2	1	0.981	...	1
Outputs				
Out	-1	-0.981	...	1
Exp. Out	-1	-0.981	...	1
Out (DSP)	-2147483648	-2106965089	...	2147483647
Exp. Out (DSP)	-2147483648	-2106965089	...	2147483647

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	33
Max CPU cycles	33
Avg CPU cycles	33

Verification: Minimum FiP32 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test — OK

Inport test for General block Minimum.

Test results				
Time step	1	2	...	214
CPU cycles	53	53	...	53
Inputs				
In1 (DSP)	-2147483648	-2106965089	...	2147483647
In2 (DSP)	2147483647	2106965089	...	2147483647
In1	-1	-0.981	...	1
In2	1	0.981	...	1
Outputs				
Out	-1	-0.981	...	1
Exp. Out	-1	-0.981	...	1
Out (DSP)	-2147483648	-2106965089	...	2147483647
Exp. Out (DSP)	-2147483648	-2106965089	...	2147483647

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	50
Max CPU cycles	53
Avg CPU cycles	52

Verification: Minimum FiP32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for General block Minimum.

Test results				
Time step	1	2	...	214
CPU cycles	68	57	...	57
Inputs				
In1 (DSP)	-2147483648	-2106965089	...	2147483647
In2 (DSP)	2147483647	2106965089	...	2147483647
In1	-1	-0.981	...	1
In2	1	0.981	...	1
Outputs				
Out	-1	-0.981	...	1
Exp. Out	-1	-0.981	...	1
Out (DSP)	-2147483648	-2106965089	...	2147483647
Exp. Out (DSP)	-2147483648	-2106965089	...	2147483647

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	57
Max CPU cycles	68
Avg CPU cycles	57

Verification: Minimum FiP32 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for General block Minimum.

Test results				
Time step	1	2	...	214
CPU cycles	51	51	...	51
Inputs				
In1 (DSP)	-2147483648	-2106965089	...	2147483647
In2 (DSP)	2147483647	2106965089	...	2147483647
In1	-1	-0.981	...	1
In2	1	0.981	...	1
Outputs				
Out	-1	-0.981	...	1
Exp. Out	-1	-0.981	...	1
Out (DSP)	-2147483648	-2106965089	...	2147483647
Exp. Out (DSP)	-2147483648	-2106965089	...	2147483647

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	49
Max CPU cycles	51
Avg CPU cycles	50

Verification: Minimum Float32 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for General block Minimum.

Test results				
Time step	1	2	...	214
CPU cycles	58	58	...	58
Inputs				
In1 (DSP)	-1	-0.981	...	1
In2 (DSP)	1	0.981	...	1
In1	-1	-0.981	...	1
In2	1	0.981	...	1
Outputs				
Out	-1	-0.981	...	1
Exp. Out	-1	-0.981	...	1
Out (DSP)	-1	-0.981	...	1
Exp. Out (DSP)	-1	-0.981	...	1

Test settings	
Tolerance Out	±3,2596e-08 (±70 LSB)

Test statistics	
Min CPU cycles	58
Max CPU cycles	58
Avg CPU cycles	58

Verification: Minimum Float32 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for General block Minimum.

Test results				
Time step	1	2	...	214
CPU cycles	33	33	...	33
Inputs				
In1 (DSP)	-1	-0.981	...	1
In2 (DSP)	1	0.981	...	1
In1	-1	-0.981	...	1
In2	1	0.981	...	1
Outputs				
Out	-1	-0.981	...	1
Exp. Out	-1	-0.981	...	1
Out (DSP)	-1	-0.981	...	1
Exp. Out (DSP)	-1	-0.981	...	1

Test settings	
Tolerance Out	±3,2596e-08 (±70 LSB)

Test statistics	
Min CPU cycles	31
Max CPU cycles	33
Avg CPU cycles	32

Verification: Minimum Float32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for General block Minimum.

Test results				
Time step	1	2	...	214
CPU cycles	67	67	...	67
Inputs				
In1 (DSP)	-1	-0.981	...	1
In2 (DSP)	1	0.981	...	1
In1	-1	-0.981	...	1
In2	1	0.981	...	1
Outputs				
Out	-1	-0.981	...	1
Exp. Out	-1	-0.981	...	1
Out (DSP)	-1	-0.981	...	1
Exp. Out (DSP)	-1	-0.981	...	1

Test settings	
Tolerance Out	±3,2596e-08 (±70 LSB)

Test statistics	
Min CPU cycles	67
Max CPU cycles	67
Avg CPU cycles	67

Verification: Minimum Float32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for General block Minimum.

Test results				
Time step	1	2	...	214
CPU cycles	142	142	...	150
Inputs				
In1 (DSP)	-1	-0.981	...	1
In2 (DSP)	1	0.981	...	1
In1	-1	-0.981	...	1
In2	1	0.981	...	1
Outputs				
Out	-1	-0.981	...	1
Exp. Out	-1	-0.981	...	1
Out (DSP)	-1	-0.981	...	1
Exp. Out (DSP)	-1	-0.981	...	1

Test settings	
Tolerance Out	±3,2596e-08 (±70 LSB)

Test statistics	
Min CPU cycles	134
Max CPU cycles	150
Avg CPU cycles	145

Verification: Minimum Float32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test — OK

Inport test for General block Minimum.

Test results				
Time step	1	2	...	214
CPU cycles	85	85	...	85
Inputs				
In1 (DSP)	-1	-0.981	...	1
In2 (DSP)	1	0.981	...	1
In1	-1	-0.981	...	1
In2	1	0.981	...	1
Outputs				
Out	-1	-0.981	...	1
Exp. Out	-1	-0.981	...	1
Out (DSP)	-1	-0.981	...	1
Exp. Out (DSP)	-1	-0.981	...	1

Test settings	
Tolerance Out	±3,2596e-08 (±70 LSB)

Test statistics	
Min CPU cycles	63
Max CPU cycles	88
Avg CPU cycles	86

Verification: Minimum Float32 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for General block Minimum.

Test results				
Time step	1	2	...	214
CPU cycles	160	160	...	162
Inputs				
In1 (DSP)	-1	-0.981	...	1
In2 (DSP)	1	0.981	...	1
In1	-1	-0.981	...	1
In2	1	0.981	...	1
Outputs				
Out	-1	-0.981	...	1
Exp. Out	-1	-0.981	...	1
Out (DSP)	-1	-0.981	...	1
Exp. Out (DSP)	-1	-0.981	...	1

Test settings	
Tolerance Out	±3,2596e-08 (±70 LSB)

Test statistics	
Min CPU cycles	157
Max CPU cycles	166
Avg CPU cycles	160

Verification: Minimum Float32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for General block Minimum.

Test results				
Time step	1	2	...	214
CPU cycles	70	59	...	59
Inputs				
In1 (DSP)	-1	-0.981	...	1
In2 (DSP)	1	0.981	...	1
In1	-1	-0.981	...	1
In2	1	0.981	...	1
Outputs				
Out	-1	-0.981	...	1
Exp. Out	-1	-0.981	...	1
Out (DSP)	-1	-0.981	...	1
Exp. Out (DSP)	-1	-0.981	...	1

Test settings	
Tolerance Out	±3,2596e-08 (±70 LSB)

Test statistics	
Min CPU cycles	59
Max CPU cycles	70
Avg CPU cycles	59

Verification: Minimum Float32 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for General block Minimum.

Test results				
Time step	1	2	...	214
CPU cycles	40	40	...	40
Inputs				
In1 (DSP)	-1	-0.981	...	1
In2 (DSP)	1	0.981	...	1
In1	-1	-0.981	...	1
In2	1	0.981	...	1
Outputs				
Out	-1	-0.981	...	1
Exp. Out	-1	-0.981	...	1
Out (DSP)	-1	-0.981	...	1
Exp. Out (DSP)	-1	-0.981	...	1

Test settings	
Tolerance Out	±3,2596e-08 (±70 LSB)

Test statistics	
Min CPU cycles	40
Max CPU cycles	40
Avg CPU cycles	40

Block: Not



Logical inverter block.

Inports	
In	

Outports	
Out	

Implementations:

Bool Boolean Implementation

Implementation: Bool

Boolean Implementation

Inports Data Type	
In	bool

Outports Data Type	
Out	bool

Verification: Not Bool CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test — OK

Inport test for General block Not.

Test results						
Time step	1	2	3	4	...	9
CPU cycles	58	58	58	58	...	58
Inputs						
In (DSP)	0	0	0	0	...	1
In	0	-1	-0.5	-0.2	...	1
Outputs						
Out	1	1	1	1	...	0
Exp. Out	1	1	1	1	...	0
Out (DSP)	1	1	1	1	...	0
Exp. Out (DSP)	1	1	1	1	...	0

Test settings	
Tolerance Out	±0,0000e+00 (±0 LSB)

Test statistics	
Min CPU cycles	58
Max CPU cycles	58
Avg CPU cycles	58

Verification: Not Bool CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test — OK

Inport test for General block Not.

Test results						
Time step	1	2	3	4	...	9
CPU cycles	29	29	29	29	...	29
Inputs						
In (DSP)	0	0	0	0	...	1
In	0	-1	-0.5	-0.2	...	1
Outputs						
Out	1	1	1	1	...	0
Exp. Out	1	1	1	1	...	0
Out (DSP)	1	1	1	1	...	0
Exp. Out (DSP)	1	1	1	1	...	0

Test settings	
Tolerance Out	±0,0000e+00 (±0 LSB)

Test statistics	
Min CPU cycles	29
Max CPU cycles	29
Avg CPU cycles	29

Verification: Not Bool CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for General block Not.

Test results						
Time step	1	2	3	4	...	9
CPU cycles	57	57	57	57	...	57
Inputs						
In (DSP)	0	0	0	0	...	1
In	0	-1	-0.5	-0.2	...	1
Outputs						
Out	1	1	1	1	...	0
Exp. Out	1	1	1	1	...	0
Out (DSP)	1	1	1	1	...	0
Exp. Out (DSP)	1	1	1	1	...	0

Test settings	
Tolerance Out	±0,0000e+00 (±0 LSB)

Test statistics	
Min CPU cycles	57
Max CPU cycles	57
Avg CPU cycles	57

Verification: Not Bool CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for General block Not.

Test results						
Time step	1	2	3	4	...	9
CPU cycles	48	48	48	48	...	48
Inputs						
In (DSP)	0	0	0	0	...	1
In	0	-1	-0.5	-0.2	...	1
Outputs						
Out	1	1	1	1	...	0
Exp. Out	1	1	1	1	...	0
Out (DSP)	1	1	1	1	...	0
Exp. Out (DSP)	1	1	1	1	...	0

Test settings	
Tolerance Out	±0,0000e+00 (±0 LSB)

Test statistics	
Min CPU cycles	48
Max CPU cycles	48
Avg CPU cycles	48

Verification: Not Bool CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for General block Not.

Test results						
Time step	1	2	3	4	...	9
CPU cycles	29	29	29	29	...	29
Inputs						
In (DSP)	0	0	0	0	...	1
In	0	-1	-0.5	-0.2	...	1
Outputs						
Out	1	1	1	1	...	0
Exp. Out	1	1	1	1	...	0
Out (DSP)	1	1	1	1	...	0
Exp. Out (DSP)	1	1	1	1	...	0

Test settings	
Tolerance Out	±0,0000e+00 (±0 LSB)

Test statistics	
Min CPU cycles	29
Max CPU cycles	29
Avg CPU cycles	29

Verification: Not Bool CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test — OK

Inport test for General block Not.

Test results						
Time step	1	2	3	4	...	9
CPU cycles	42	42	42	42	...	42
Inputs						
In (DSP)	0	0	0	0	...	1
In	0	-1	-0.5	-0.2	...	1
Outputs						
Out	1	1	1	1	...	0
Exp. Out	1	1	1	1	...	0
Out (DSP)	1	1	1	1	...	0
Exp. Out (DSP)	1	1	1	1	...	0

Test settings	
Tolerance Out	±0,0000e+00 (±0 LSB)

Test statistics	
Min CPU cycles	42
Max CPU cycles	42
Avg CPU cycles	42

Verification: Not Bool CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test — OK

Inport test for General block Not.

Test results						
Time step	1	2	3	4	...	9
CPU cycles	64	56	56	56	...	56
Inputs						
In (DSP)	0	0	0	0	...	1
In	0	-1	-0.5	-0.2	...	1
Outputs						
Out	1	1	1	1	...	0
Exp. Out	1	1	1	1	...	0
Out (DSP)	1	1	1	1	...	0
Exp. Out (DSP)	1	1	1	1	...	0

Test settings	
Tolerance Out	±0,0000e+00 (±0 LSB)

Test statistics	
Min CPU cycles	56
Max CPU cycles	64
Avg CPU cycles	56

Verification: Not Bool CPU TMS320F28379D

Date of Test 2026-06-22

Target controller TMS320F28379D

Test case: Inport test OK

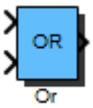
Inport test for General block Not.

Test results						
Time step	1	2	3	4	...	9
CPU cycles	40	40	40	40	...	40
Inputs						
In (DSP)	0	0	0	0	...	1
In	0	-1	-0.5	-0.2	...	1
Outputs						
Out	1	1	1	1	...	0
Exp. Out	1	1	1	1	...	0
Out (DSP)	1	1	1	1	...	0
Exp. Out (DSP)	1	1	1	1	...	0

Test settings	
Tolerance Out	±0,0000e+00 (±0 LSB)

Test statistics	
Min CPU cycles	40
Max CPU cycles	40
Avg CPU cycles	40

Block: Or



Logical OR block.

Inports	
In1	
In2	

Outports	
Out	

Implementations:

Bool Boolean Implementation

Implementation: Bool

Boolean Implementation

Inports Data Type	
In1	bool
In2	bool

Outports Data Type	
Out	bool

Verification: Or Bool CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for General block Or.

Test results						
Time step	1	2	3	4	...	25
CPU cycles	67	67	67	67	...	64
Inputs						
In1 (DSP)	0	0	0	0	...	1
In2 (DSP)	0	0	0	0	...	1
In1	0	-1	-0.5	-0.2	...	1
In2	0	0	0	0	...	1
Outputs						
Out	0	0	0	0	...	1
Exp. Out	0	0	0	0	...	1
Out (DSP)	0	0	0	0	...	1
Exp. Out (DSP)	0	0	0	0	...	1

Test settings	
Tolerance Out	±0,0000e+00 (±0 LSB)

Test statistics	
Min CPU cycles	64
Max CPU cycles	67
Avg CPU cycles	66

Verification: Or Bool CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test — OK

Inport test for General block Or.

Test results						
Time step	1	2	3	4	...	25
CPU cycles	33	33	33	33	...	31
Inputs						
In1 (DSP)	0	0	0	0	...	1
In2 (DSP)	0	0	0	0	...	1
In1	0	-1	-0.5	-0.2	...	1
In2	0	0	0	0	...	1
Outputs						
Out	0	0	0	0	...	1
Exp. Out	0	0	0	0	...	1
Out (DSP)	0	0	0	0	...	1
Exp. Out (DSP)	0	0	0	0	...	1

Test settings	
Tolerance Out	±0,0000e+00 (±0 LSB)

Test statistics	
Min CPU cycles	31
Max CPU cycles	33
Avg CPU cycles	32

Verification: Or Bool CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for General block Or.

Test results						
Time step	1	2	3	4	...	25
CPU cycles	57	57	57	57	...	60
Inputs						
In1 (DSP)	0	0	0	0	...	1
In2 (DSP)	0	0	0	0	...	1
In1	0	-1	-0.5	-0.2	...	1
In2	0	0	0	0	...	1
Outputs						
Out	0	0	0	0	...	1
Exp. Out	0	0	0	0	...	1
Out (DSP)	0	0	0	0	...	1
Exp. Out (DSP)	0	0	0	0	...	1

Test settings	
Tolerance Out	±0,0000e+00 (±0 LSB)

Test statistics	
Min CPU cycles	57
Max CPU cycles	60
Avg CPU cycles	57

Verification: Or Bool CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for General block Or.

Test results						
Time step	1	2	3	4	...	25
CPU cycles	52	52	52	52	...	50
Inputs						
In1 (DSP)	0	0	0	0	...	1
In2 (DSP)	0	0	0	0	...	1
In1	0	-1	-0.5	-0.2	...	1
In2	0	0	0	0	...	1
Outputs						
Out	0	0	0	0	...	1
Exp. Out	0	0	0	0	...	1
Out (DSP)	0	0	0	0	...	1
Exp. Out (DSP)	0	0	0	0	...	1

Test settings	
Tolerance Out	±0,0000e+00 (±0 LSB)

Test statistics	
Min CPU cycles	50
Max CPU cycles	52
Avg CPU cycles	51

Verification: Or Bool CPU PIC32MX170F256

Date of Test 2026-06-19

Target controller PIC32MX170F256

Test case: Inport test OK

Inport test for General block Or.

Test results						
Time step	1	2	3	4	...	25
CPU cycles	35	35	35	35	...	30
Inputs						
In1 (DSP)	0	0	0	0	...	1
In2 (DSP)	0	0	0	0	...	1
In1	0	-1	-0.5	-0.2	...	1
In2	0	0	0	0	...	1
Outputs						
Out	0	0	0	0	...	1
Exp. Out	0	0	0	0	...	1
Out (DSP)	0	0	0	0	...	1
Exp. Out (DSP)	0	0	0	0	...	1

Test settings	
Tolerance Out	±0,0000e+00 (±0 LSB)

Test statistics	
Min CPU cycles	30
Max CPU cycles	35
Avg CPU cycles	34

Verification: Or Bool CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test — OK

Inport test for General block Or.

Test results						
Time step	1	2	3	4	...	25
CPU cycles	45	45	45	45	...	45
Inputs						
In1 (DSP)	0	0	0	0	...	1
In2 (DSP)	0	0	0	0	...	1
In1	0	-1	-0.5	-0.2	...	1
In2	0	0	0	0	...	1
Outputs						
Out	0	0	0	0	...	1
Exp. Out	0	0	0	0	...	1
Out (DSP)	0	0	0	0	...	1
Exp. Out (DSP)	0	0	0	0	...	1

Test settings	
Tolerance Out	±0,0000e+00 (±0 LSB)

Test statistics	
Min CPU cycles	45
Max CPU cycles	45
Avg CPU cycles	45

Verification: Or Bool CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for General block Or.

Test results						
Time step	1	2	3	4	...	25
CPU cycles	60	60	60	60	...	58
Inputs						
In1 (DSP)	0	0	0	0	...	1
In2 (DSP)	0	0	0	0	...	1
In1	0	-1	-0.5	-0.2	...	1
In2	0	0	0	0	...	1
Outputs						
Out	0	0	0	0	...	1
Exp. Out	0	0	0	0	...	1
Out (DSP)	0	0	0	0	...	1
Exp. Out (DSP)	0	0	0	0	...	1

Test settings	
Tolerance Out	±0,0000e+00 (±0 LSB)

Test statistics	
Min CPU cycles	58
Max CPU cycles	60
Avg CPU cycles	59

Verification: Or Bool CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

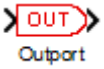
Inport test for General block Or.

Test results						
Time step	1	2	3	4	...	25
CPU cycles	47	47	47	47	...	47
Inputs						
In1 (DSP)	0	0	0	0	...	1
In2 (DSP)	0	0	0	0	...	1
In1	0	-1	-0.5	-0.2	...	1
In2	0	0	0	0	...	1
Outputs						
Out	0	0	0	0	...	1
Exp. Out	0	0	0	0	...	1
Out (DSP)	0	0	0	0	...	1
Exp. Out (DSP)	0	0	0	0	...	1

Test settings	
Tolerance Out	±0,0000e+00 (±0 LSB)

Test statistics	
Min CPU cycles	47
Max CPU cycles	47
Avg CPU cycles	47

Block: Outport

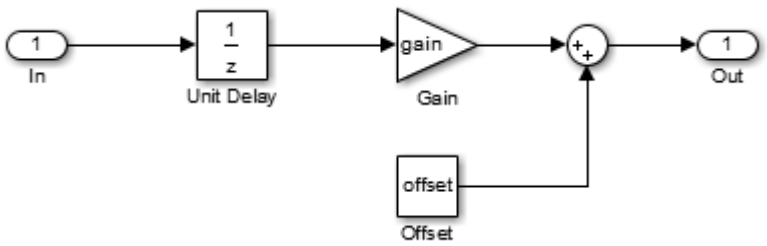


Outports	
OUT	Signal to frame program

Mask Parameters	
ts_fact	Multiplication factor of base sampling time (in integer format)
Gain	Gain value used in simulation
Offset	Offset value used in simulation

Description:

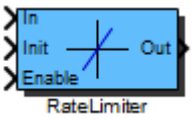
Serves as interface to the frame program. The output of this block is intended for simulation purposes and can be left unconnected if not used. Also the parameters *Gain*, and *Offset* are only used during simulation. The schematic for simulation can be seen in the figure below. The Unit Delay block is only used during simulation and should reflect the time delay caused by a discrete controller.
Note: Currently, *Gain* and *Offset* parameters are only available in Matlab/Simulink.



Data Types:

bool	Boolean
int8	8 Bit Fixed Point
int16	16 Bit Fixed Point
int32	32 Bit Fixed Point
float32	32 Bit Floating Point
float64	64 Bit Floating Point

Block: RateLimiter



Limitation of rising and falling rate.
Function of Enable:
0: rate limiting disabled, signal is passed through
1: rate limiting enabled, signal is rate limited
0->1: preload of output with value from init input

Inports	
In	
Init	Value which is loaded at rising flanke of enable signal
Enable	Enable == 0: Deactivation of block; Out is set to In. Enable != 0: Activation of block; Out is rate limited. Enable 0->1: Preloading of output; Out is set to value of Init input

Outports	
Out	

Mask Parameters		
Name	**ID**	**Description**
Tr	1	Rising time in seconds. Slew rate will be 1/Tr
Tf	2	Falling time in seconds. Slew rate will be 1/Tf
ts_fact	3	Multiplication factor of base sampling time (in integer format)

Description:

Rising and falling time refer to a step from 0 to 1. Entries for *Tr: Rising time* and *Tf: Falling time* smaller than the actual sample time will be limited to the sample time internally.
The 16- and 32-Bit fixed point implementations are based on an internal 32-Bit wide slew-rate variable while the 8-Bit fixed point implementation uses a 16-Bit wide slew-rate variable.

Implementations:

FiP16	16 Bit Fixed Point Implementation
FiP32	32 Bit Fixed Point Implementation
Float32	32 Bit Floating Point Implementation
Float64	64 Bit Floating Point Implementation

Implementation: FiP16

16 Bit Fixed Point Implementation

Inports Data Type	
In	int16
Init	int16
Enable	bool

Outports Data Type	
Out	int16

Implementation: FiP32

32 Bit Fixed Point Implementation

Inports Data Type	
In	int32
Init	int32
Enable	bool

Outports Data Type	
Out	int32

Implementation: Float32

32 Bit Floating Point Implementation

Inports Data Type	
In	float32
Init	float32
Enable	bool

Outports Data Type	
Out	float32

Implementation: Float64

64 Bit Floating Point Implementation

Inports Data Type	
In	float64
Init	float64
Enable	bool

Outports Data Type	
Out	float64

Verification: RateLimiter FiP16 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for General block RateLimiter.

Test results						
Time step	1	2	3	4	...	266
CPU cycles	81	81	81	81	...	125
Inputs						
In (DSP)	0	-32768	-31508	-30247	...	-6554
Init (DSP)	0	9830	9830	9830	...	9830
Enable (DSP)	0	0	0	0	...	1
In	0	-1	-0.962	-0.923	...	-0.2
Init	0	0.3	0.3	0.3	...	0.3
Enable	0	0	0	0	...	1
Parameters						
Tr	0.01					
Tf	0.03					
ts_fact	1					
Outputs						
Out	0	-1	-0.962	-0.923	...	0.423
Exp. Out	0	-1	-0.962	-0.923	...	0.423
Out (DSP)	0	-32768	-31508	-30247	...	13871
Exp. Out (DSP)	0	-32768	-31508	-30247	...	13872

Test settings	
Tolerance Out	±6,1035e-05 (±2 LSB)

Test statistics	
Min CPU cycles	81
Max CPU cycles	125
Avg CPU cycles	106

Test case: Conversion test OK

Conversion test for General block RateLimiter.

Test results				
Time step	1	2	...	37
Mask parameters				
Tr	-10	-9.444	...	10
Tf	-9	-8.5	...	9
ts_fact	3	3	...	3
Controller parameters				
RateUp	2147483647	2147483647	...	64425
RateDown	2147483647	2147483647	...	71583
Exp. RateUp	2147483647	2147483647	...	64425
Exp. RateDown	2147483647	2147483647	...	71583

Test settings	
Tolerance RateUp	±0,0000e+00
Tolerance RateDown	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block RateLimiter.

Test results				
Time step	1	2	...	37
Mask parameters				
Tr	-10	-9.444	...	10
Tf	-9	-8.5	...	9
ts_fact	3	3	...	3
Controller parameters				
RateUp	2147483647	2147483647	...	64424
RateDown	2147483647	2147483647	...	71582
Exp. RateUp	2147483647	2147483647	...	64425
Exp. RateDown	2147483647	2147483647	...	71583

Test settings	
Tolerance RateUp	±1,0000e+00
Tolerance RateDown	±1,0000e+00

Test statistics	
Min CPU cycles	2851
Max CPU cycles	2961
Avg CPU cycles	2905

Verification: RateLimiter FiP16 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for General block RateLimiter.

Test results						
Time step	1	2	3	4	...	266
CPU cycles	51	51	51	51	...	79
Inputs						
In (DSP)	0	-32768	-31508	-30247	...	-6554
Init (DSP)	0	9830	9830	9830	...	9830
Enable (DSP)	0	0	0	0	...	1
In	0	-1	-0.962	-0.923	...	-0.2
Init	0	0.3	0.3	0.3	...	0.3
Enable	0	0	0	0	...	1
Parameters						
Tr	0.01					
Tf	0.03					
ts_fact	1					
Outputs						
Out	0	-1	-0.962	-0.923	...	0.423
Exp. Out	0	-1	-0.962	-0.923	...	0.423
Out (DSP)	0	-32768	-31508	-30247	...	13871
Exp. Out (DSP)	0	-32768	-31508	-30247	...	13872

Test settings	
Tolerance Out	±6,1035e-05 (±2 LSB)

Test statistics	
Min CPU cycles	51
Max CPU cycles	79
Avg CPU cycles	69

Test case: Conversion test OK

Conversion test for General block RateLimiter.

Test results				
Time step	1	2	...	37
Mask parameters				
Tr	-10	-9.444	...	10
Tf	-9	-8.5	...	9
ts_fact	3	3	...	3
Controller parameters				
RateUp	2147483647	2147483647	...	64425
RateDown	2147483647	2147483647	...	71583
Exp. RateUp	2147483647	2147483647	...	64425
Exp. RateDown	2147483647	2147483647	...	71583

Test settings	
Tolerance RateUp	±0,0000e+00
Tolerance RateDown	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block RateLimiter.

Test results				
Time step	1	2	...	37
Mask parameters				
Tr	-10	-9.444	...	10
Tf	-9	-8.5	...	9
ts_fact	3	3	...	3
Controller parameters				
RateUp	2147483647	2147483647	...	64424
RateDown	2147483647	2147483647	...	71582
Exp. RateUp	2147483647	2147483647	...	64425
Exp. RateDown	2147483647	2147483647	...	71583

Test settings	
Tolerance RateUp	±1,0000e+00
Tolerance RateDown	±1,0000e+00

Test statistics	
Min CPU cycles	1087
Max CPU cycles	1097
Avg CPU cycles	1091

Verification: RateLimiter FiP16 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for General block RateLimiter.

Test results						
Time step	1	2	3	4	...	266
CPU cycles	67	67	67	67	...	131
Inputs						
In (DSP)	0	-32768	-31508	-30247	...	-6554
Init (DSP)	0	9830	9830	9830	...	9830
Enable (DSP)	0	0	0	0	...	1
In	0	-1	-0.962	-0.923	...	-0.2
Init	0	0.3	0.3	0.3	...	0.3
Enable	0	0	0	0	...	1
Parameters						
Tr	0.01					
Tf	0.03					
ts_fact	1					
Outputs						
Out	0	-1	-0.962	-0.923	...	0.423
Exp. Out	0	-1	-0.962	-0.923	...	0.423
Out (DSP)	0	-32768	-31508	-30247	...	13871
Exp. Out (DSP)	0	-32768	-31508	-30247	...	13872

Test settings	
Tolerance Out	±6,1035e-05 (±2 LSB)

Test statistics	
Min CPU cycles	67
Max CPU cycles	131
Avg CPU cycles	105

Test case: Conversion test OK

Conversion test for General block RateLimiter.

Test results				
Time step	1	2	...	37
Mask parameters				
Tr	-10	-9.444	...	10
Tf	-9	-8.5	...	9
ts_fact	3	3	...	3
Controller parameters				
RateUp	2147483647	2147483647	...	64425
RateDown	2147483647	2147483647	...	71583
Exp. RateUp	2147483647	2147483647	...	64425
Exp. RateDown	2147483647	2147483647	...	71583

Test settings	
Tolerance RateUp	±0,0000e+00
Tolerance RateDown	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block RateLimiter.

Test results				
Time step	1	2	...	37
Mask parameters				
Tr	-10	-9.444	...	10
Tf	-9	-8.5	...	9
ts_fact	3	3	...	3
Controller parameters				
RateUp	2147483647	2147483647	...	64424
RateDown	2147483647	2147483647	...	71582
Exp. RateUp	2147483647	2147483647	...	64425
Exp. RateDown	2147483647	2147483647	...	71583

Test settings	
Tolerance RateUp	±1,0000e+00
Tolerance RateDown	±1,0000e+00

Test statistics	
Min CPU cycles	1654
Max CPU cycles	1701
Avg CPU cycles	1655

Verification: RateLimiter FiP16 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for General block RateLimiter.

Test results						
Time step	1	2	3	4	...	266
CPU cycles	67	67	67	67	...	105
Inputs						
In (DSP)	0	-32768	-31508	-30247	...	-6554
Init (DSP)	0	9830	9830	9830	...	9830
Enable (DSP)	0	0	0	0	...	1
In	0	-1	-0.962	-0.923	...	-0.2
Init	0	0.3	0.3	0.3	...	0.3
Enable	0	0	0	0	...	1
Parameters						
Tr	0.01					
Tf	0.03					
ts_fact	1					
Outputs						
Out	0	-1	-0.962	-0.923	...	0.423
Exp. Out	0	-1	-0.962	-0.923	...	0.423
Out (DSP)	0	-32768	-31508	-30247	...	13871
Exp. Out (DSP)	0	-32768	-31508	-30247	...	13872

Test settings	
Tolerance Out	±6,1035e-05 (±2 LSB)

Test statistics	
Min CPU cycles	67
Max CPU cycles	166
Avg CPU cycles	91

Test case: Conversion test OK

Conversion test for General block RateLimiter.

Test results				
Time step	1	2	...	37
Mask parameters				
Tr	-10	-9.444	...	10
Tf	-9	-8.5	...	9
ts_fact	3	3	...	3
Controller parameters				
RateUp	2147483647	2147483647	...	64425
RateDown	2147483647	2147483647	...	71583
Exp. RateUp	2147483647	2147483647	...	64425
Exp. RateDown	2147483647	2147483647	...	71583

Test settings	
Tolerance RateUp	±0,0000e+00
Tolerance RateDown	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block RateLimiter.

Test results				
Time step	1	2	...	37
Mask parameters				
Tr	-10	-9.444	...	10
Tf	-9	-8.5	...	9
ts_fact	3	3	...	3
Controller parameters				
RateUp	2147483647	2147483647	...	64424
RateDown	2147483647	2147483647	...	71582
Exp. RateUp	2147483647	2147483647	...	64425
Exp. RateDown	2147483647	2147483647	...	71583

Test settings	
Tolerance RateUp	±1,0000e+00
Tolerance RateDown	±1,0000e+00

Test statistics	
Min CPU cycles	6095
Max CPU cycles	6408
Avg CPU cycles	6238

Verification: RateLimiter FiP16 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for General block RateLimiter.

Test results						
Time step	1	2	3	4	...	266
CPU cycles	41	41	41	41	...	62
Inputs						
In (DSP)	0	-32768	-31508	-30247	...	-6554
Init (DSP)	0	9830	9830	9830	...	9830
Enable (DSP)	0	0	0	0	...	1
In	0	-1	-0.962	-0.923	...	-0.2
Init	0	0.3	0.3	0.3	...	0.3
Enable	0	0	0	0	...	1
Parameters						
Tr	0.01					
Tf	0.03					
ts_fact	1					
Outputs						
Out	0	-1	-0.962	-0.923	...	0.423
Exp. Out	0	-1	-0.962	-0.923	...	0.423
Out (DSP)	0	-32768	-31508	-30247	...	13871
Exp. Out (DSP)	0	-32768	-31508	-30247	...	13872

Test settings	
Tolerance Out	±6,1035e-05 (±2 LSB)

Test statistics	
Min CPU cycles	41
Max CPU cycles	62
Avg CPU cycles	53

Test case: Conversion test OK

Conversion test for General block RateLimiter.

Test results				
Time step	1	2	...	37
Mask parameters				
Tr	-10	-9.444	...	10
Tf	-9	-8.5	...	9
ts_fact	3	3	...	3
Controller parameters				
RateUp	2147483647	2147483647	...	64425
RateDown	2147483647	2147483647	...	71583
Exp. RateUp	2147483647	2147483647	...	64425
Exp. RateDown	2147483647	2147483647	...	71583

Test settings	
Tolerance RateUp	±0,0000e+00
Tolerance RateDown	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block RateLimiter.

Test results				
Time step	1	2	...	37
Mask parameters				
Tr	-10	-9.444	...	10
Tf	-9	-8.5	...	9
ts_fact	3	3	...	3
Controller parameters				
RateUp	2147483647	2147483647	...	64424
RateDown	2147483647	2147483647	...	71582
Exp. RateUp	2147483647	2147483647	...	64425
Exp. RateDown	2147483647	2147483647	...	71583

Test settings	
Tolerance RateUp	±1,0000e+00
Tolerance RateDown	±1,0000e+00

Test statistics	
Min CPU cycles	2067
Max CPU cycles	2100
Avg CPU cycles	2082

Verification: RateLimiter FiP16 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for General block RateLimiter.

Test results						
Time step	1	2	3	4	...	266
CPU cycles	61	61	61	61	...	82
Inputs						
In (DSP)	0	-32768	-31508	-30247	...	-6554
Init (DSP)	0	9830	9830	9830	...	9830
Enable (DSP)	0	0	0	0	...	1
In	0	-1	-0.962	-0.923	...	-0.2
Init	0	0.3	0.3	0.3	...	0.3
Enable	0	0	0	0	...	1
Parameters						
Tr	0.01					
Tf	0.03					
ts_fact	1					
Outputs						
Out	0	-1	-0.962	-0.923	...	0.423
Exp. Out	0	-1	-0.962	-0.923	...	0.423
Out (DSP)	0	-32768	-31508	-30247	...	13871
Exp. Out (DSP)	0	-32768	-31508	-30247	...	13872

Test settings	
Tolerance Out	±6,1035e-05 (±2 LSB)

Test statistics	
Min CPU cycles	60
Max CPU cycles	82
Avg CPU cycles	73

Test case: Conversion test OK

Conversion test for General block RateLimiter.

Test results				
Time step	1	2	...	37
Mask parameters				
Tr	-10	-9.444	...	10
Tf	-9	-8.5	...	9
ts_fact	3	3	...	3
Controller parameters				
RateUp	2147483647	2147483647	...	64425
RateDown	2147483647	2147483647	...	71583
Exp. RateUp	2147483647	2147483647	...	64425
Exp. RateDown	2147483647	2147483647	...	71583

Test settings	
Tolerance RateUp	±0,0000e+00
Tolerance RateDown	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block RateLimiter.

Test results				
Time step	1	2	...	37
Mask parameters				
Tr	-10	-9.444	...	10
Tf	-9	-8.5	...	9
ts_fact	3	3	...	3
Controller parameters				
RateUp	2147483647	2147483647	...	64424
RateDown	2147483647	2147483647	...	71582
Exp. RateUp	2147483647	2147483647	...	64425
Exp. RateDown	2147483647	2147483647	...	71583

Test settings	
Tolerance RateUp	±1,0000e+00
Tolerance RateDown	±1,0000e+00

Test statistics	
Min CPU cycles	4978
Max CPU cycles	5687
Avg CPU cycles	5633

Verification: RateLimiter FiP16 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for General block RateLimiter.

Test results						
Time step	1	2	3	4	...	266
CPU cycles	85	66	66	66	...	96
Inputs						
In (DSP)	0	-32768	-31508	-30247	...	-6554
Init (DSP)	0	9830	9830	9830	...	9830
Enable (DSP)	0	0	0	0	...	1
In	0	-1	-0.962	-0.923	...	-0.2
Init	0	0.3	0.3	0.3	...	0.3
Enable	0	0	0	0	...	1
Parameters						
Tr	0.01					
Tf	0.03					
ts_fact	1					
Outputs						
Out	0	-1	-0.962	-0.923	...	0.423
Exp. Out	0	-1	-0.962	-0.923	...	0.423
Out (DSP)	0	-32768	-31508	-30247	...	13871
Exp. Out (DSP)	0	-32768	-31508	-30247	...	13872

Test settings	
Tolerance Out	±6,1035e-05 (±2 LSB)

Test statistics	
Min CPU cycles	66
Max CPU cycles	96
Avg CPU cycles	84

Test case: Conversion test OK

Conversion test for General block RateLimiter.

Test results				
Time step	1	2	...	37
Mask parameters				
Tr	-10	-9.444	...	10
Tf	-9	-8.5	...	9
ts_fact	3	3	...	3
Controller parameters				
RateUp	2147483647	2147483647	...	64425
RateDown	2147483647	2147483647	...	71583
Exp. RateUp	2147483647	2147483647	...	64425
Exp. RateDown	2147483647	2147483647	...	71583

Test settings	
Tolerance RateUp	±0,0000e+00
Tolerance RateDown	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block RateLimiter.

Test results				
Time step	1	2	...	37
Mask parameters				
Tr	-10	-9.444	...	10
Tf	-9	-8.5	...	9
ts_fact	3	3	...	3
Controller parameters				
RateUp	2147483647	2147483647	...	64424
RateDown	2147483647	2147483647	...	71582
Exp. RateUp	2147483647	2147483647	...	64425
Exp. RateDown	2147483647	2147483647	...	71583

Test settings	
Tolerance RateUp	±1,0000e+00
Tolerance RateDown	±1,0000e+00

Test statistics	
Min CPU cycles	1354
Max CPU cycles	1641
Avg CPU cycles	1361

Verification: RateLimiter FiP16 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for General block RateLimiter.

Test results						
Time step	1	2	3	4	...	266
CPU cycles	66	66	66	66	...	124
Inputs						
In (DSP)	0	-32768	-31508	-30247	...	-6554
Init (DSP)	0	9830	9830	9830	...	9830
Enable (DSP)	0	0	0	0	...	1
In	0	-1	-0.962	-0.923	...	-0.2
Init	0	0.3	0.3	0.3	...	0.3
Enable	0	0	0	0	...	1
Parameters						
Tr	0.01					
Tf	0.03					
ts_fact	1					
Outputs						
Out	0	-1	-0.962	-0.923	...	0.423
Exp. Out	0	-1	-0.962	-0.923	...	0.423
Out (DSP)	0	-32768	-31508	-30247	...	13871
Exp. Out (DSP)	0	-32768	-31508	-30247	...	13872

Test settings	
Tolerance Out	±6,1035e-05 (±2 LSB)

Test statistics	
Min CPU cycles	66
Max CPU cycles	124
Avg CPU cycles	100

Test case: Conversion test OK

Conversion test for General block RateLimiter.

Test results				
Time step	1	2	...	37
Mask parameters				
Tr	-10	-9.444	...	10
Tf	-9	-8.5	...	9
ts_fact	3	3	...	3
Controller parameters				
RateUp	2147483647	2147483647	...	64425
RateDown	2147483647	2147483647	...	71583
Exp. RateUp	2147483647	2147483647	...	64425
Exp. RateDown	2147483647	2147483647	...	71583

Test settings	
Tolerance RateUp	±0,0000e+00
Tolerance RateDown	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block RateLimiter.

Test results				
Time step	1	2	...	37
Mask parameters				
Tr	-10	-9.444	...	10
Tf	-9	-8.5	...	9
ts_fact	3	3	...	3
Controller parameters				
RateUp	2147483647	2147483647	...	64424
RateDown	2147483647	2147483647	...	71582
Exp. RateUp	2147483647	2147483647	...	64425
Exp. RateDown	2147483647	2147483647	...	71583

Test settings	
Tolerance RateUp	±1,0000e+00
Tolerance RateDown	±1,0000e+00

Test statistics	
Min CPU cycles	2164
Max CPU cycles	2242
Avg CPU cycles	2202

Verification: RateLimiter FiP32 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for General block RateLimiter.

Test results				
Time step	1	2	...	266
CPU cycles	82	82	...	168
Inputs				
In (DSP)	0	-2147483648	...	-429496730
Init (DSP)	0	644245094	...	644245094
Enable (DSP)	0	0	...	1
In	0	-1	...	-0.2
Init	0	0.3	...	0.3
Enable	0	0	...	1
Parameters				
Tr	0.01			
Tf	0.03			
ts_fact	1			
Outputs				
Out	0	-1	...	0.423
Exp. Out	0	-1	...	0.423
Out (DSP)	0	-2147483648	...	909101402
Exp. Out (DSP)	0	-2147483648	...	909101411

Test settings	
Tolerance Out	±1,8626e-08 (±40 LSB)

Test statistics	
Min CPU cycles	82
Max CPU cycles	168
Avg CPU cycles	136

Test case: Conversion test OK

Conversion test for General block RateLimiter.

Test results				
Time step	1	2	...	37
Mask parameters				
Tr	-10	-9.444	...	10
Tf	-9	-8.5	...	9
ts_fact	3	3	...	3
Controller parameters				
RateUp	2147483647	2147483647	...	64425
RateDown	2147483647	2147483647	...	71583
Exp. RateUp	2147483647	2147483647	...	64425
Exp. RateDown	2147483647	2147483647	...	71583

Test settings	
Tolerance RateUp	±0,0000e+00
Tolerance RateDown	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block RateLimiter.

Test results				
Time step	1	2	...	37
Mask parameters				
Tr	-10	-9.444	...	10
Tf	-9	-8.5	...	9
ts_fact	3	3	...	3
Controller parameters				
RateUp	2147483647	2147483647	...	64424
RateDown	2147483647	2147483647	...	71582
Exp. RateUp	2147483647	2147483647	...	64425
Exp. RateDown	2147483647	2147483647	...	71583

Test settings	
Tolerance RateUp	±3,0000e+00
Tolerance RateDown	±3,0000e+00

Test statistics	
Min CPU cycles	2851
Max CPU cycles	2961
Avg CPU cycles	2905

Verification: RateLimiter FiP32 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for General block RateLimiter.

Test results				
Time step	1	2	...	266
CPU cycles	49	49	...	81
Inputs				
In (DSP)	0	-2147483648	...	-429496730
Init (DSP)	0	644245094	...	644245094
Enable (DSP)	0	0	...	1
In	0	-1	...	-0.2
Init	0	0.3	...	0.3
Enable	0	0	...	1
Parameters				
Tr	0.01			
Tf	0.03			
ts_fact	1			
Outputs				
Out	0	-1	...	0.423
Exp. Out	0	-1	...	0.423
Out (DSP)	0	-2147483648	...	909101402
Exp. Out (DSP)	0	-2147483648	...	909101411

Test settings	
Tolerance Out	±1,8626e-08 (±40 LSB)

Test statistics	
Min CPU cycles	49
Max CPU cycles	81
Avg CPU cycles	70

Test case: Conversion test OK

Conversion test for General block RateLimiter.

Test results				
Time step	1	2	...	37
Mask parameters				
Tr	-10	-9.444	...	10
Tf	-9	-8.5	...	9
ts_fact	3	3	...	3
Controller parameters				
RateUp	2147483647	2147483647	...	64425
RateDown	2147483647	2147483647	...	71583
Exp. RateUp	2147483647	2147483647	...	64425
Exp. RateDown	2147483647	2147483647	...	71583

Test settings	
Tolerance RateUp	±0,0000e+00
Tolerance RateDown	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block RateLimiter.

Test results				
Time step	1	2	...	37
Mask parameters				
Tr	-10	-9.444	...	10
Tf	-9	-8.5	...	9
ts_fact	3	3	...	3
Controller parameters				
RateUp	2147483647	2147483647	...	64424
RateDown	2147483647	2147483647	...	71582
Exp. RateUp	2147483647	2147483647	...	64425
Exp. RateDown	2147483647	2147483647	...	71583

Test settings	
Tolerance RateUp	±3,0000e+00
Tolerance RateDown	±3,0000e+00

Test statistics	
Min CPU cycles	1087
Max CPU cycles	1097
Avg CPU cycles	1091

Verification: RateLimiter FiP32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for General block RateLimiter.

Test results				
Time step	1	2	...	266
CPU cycles	57	57	...	124
Inputs				
In (DSP)	0	-2147483648	...	-429496730
Init (DSP)	0	644245094	...	644245094
Enable (DSP)	0	0	...	1
In	0	-1	...	-0.2
Init	0	0.3	...	0.3
Enable	0	0	...	1
Parameters				
Tr	0.01			
Tf	0.03			
ts_fact	1			
Outputs				
Out	0	-1	...	0.423
Exp. Out	0	-1	...	0.423
Out (DSP)	0	-2147483648	...	909101402
Exp. Out (DSP)	0	-2147483648	...	909101411

Test settings	
Tolerance Out	±1,8626e-08 (±40 LSB)

Test statistics	
Min CPU cycles	57
Max CPU cycles	124
Avg CPU cycles	101

Test case: Conversion test OK

Conversion test for General block RateLimiter.

Test results				
Time step	1	2	...	37
Mask parameters				
Tr	-10	-9.444	...	10
Tf	-9	-8.5	...	9
ts_fact	3	3	...	3
Controller parameters				
RateUp	2147483647	2147483647	...	64425
RateDown	2147483647	2147483647	...	71583
Exp. RateUp	2147483647	2147483647	...	64425
Exp. RateDown	2147483647	2147483647	...	71583

Test settings	
Tolerance RateUp	±0,0000e+00
Tolerance RateDown	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block RateLimiter.

Test results				
Time step	1	2	...	37
Mask parameters				
Tr	-10	-9.444	...	10
Tf	-9	-8.5	...	9
ts_fact	3	3	...	3
Controller parameters				
RateUp	2147483647	2147483647	...	64424
RateDown	2147483647	2147483647	...	71582
Exp. RateUp	2147483647	2147483647	...	64425
Exp. RateDown	2147483647	2147483647	...	71583

Test settings	
Tolerance RateUp	±3,0000e+00
Tolerance RateDown	±3,0000e+00

Test statistics	
Min CPU cycles	1654
Max CPU cycles	1659
Avg CPU cycles	1654

Verification: RateLimiter FiP32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for General block RateLimiter.

Test results				
Time step	1	2	...	266
CPU cycles	72	72	...	121
Inputs				
In (DSP)	0	-2147483648	...	-429496730
Init (DSP)	0	644245094	...	644245094
Enable (DSP)	0	0	...	1
In	0	-1	...	-0.2
Init	0	0.3	...	0.3
Enable	0	0	...	1
Parameters				
Tr	0.01			
Tf	0.03			
ts_fact	1			
Outputs				
Out	0	-1	...	0.423
Exp. Out	0	-1	...	0.423
Out (DSP)	0	-2147483648	...	909101402
Exp. Out (DSP)	0	-2147483648	...	909101411

Test settings	
Tolerance Out	±1,8626e-08 (±40 LSB)

Test statistics	
Min CPU cycles	72
Max CPU cycles	183
Avg CPU cycles	106

Test case: Conversion test OK

Conversion test for General block RateLimiter.

Test results				
Time step	1	2	...	37
Mask parameters				
Tr	-10	-9.444	...	10
Tf	-9	-8.5	...	9
ts_fact	3	3	...	3
Controller parameters				
RateUp	2147483647	2147483647	...	64425
RateDown	2147483647	2147483647	...	71583
Exp. RateUp	2147483647	2147483647	...	64425
Exp. RateDown	2147483647	2147483647	...	71583

Test settings	
Tolerance RateUp	±0,0000e+00
Tolerance RateDown	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block RateLimiter.

Test results				
Time step	1	2	...	37
Mask parameters				
Tr	-10	-9.444	...	10
Tf	-9	-8.5	...	9
ts_fact	3	3	...	3
Controller parameters				
RateUp	2147483647	2147483647	...	64424
RateDown	2147483647	2147483647	...	71582
Exp. RateUp	2147483647	2147483647	...	64425
Exp. RateDown	2147483647	2147483647	...	71583

Test settings	
Tolerance RateUp	±3,0000e+00
Tolerance RateDown	±3,0000e+00

Test statistics	
Min CPU cycles	6095
Max CPU cycles	6411
Avg CPU cycles	6235

Verification: RateLimiter FiP32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for General block RateLimiter.

Test results				
Time step	1	2	...	266
CPU cycles	38	38	...	69
Inputs				
In (DSP)	0	-2147483648	...	-429496730
Init (DSP)	0	644245094	...	644245094
Enable (DSP)	0	0	...	1
In	0	-1	...	-0.2
Init	0	0.3	...	0.3
Enable	0	0	...	1
Parameters				
Tr	0.01			
Tf	0.03			
ts_fact	1			
Outputs				
Out	0	-1	...	0.423
Exp. Out	0	-1	...	0.423
Out (DSP)	0	-2147483648	...	909101402
Exp. Out (DSP)	0	-2147483648	...	909101411

Test settings	
Tolerance Out	±1,8626e-08 (±40 LSB)

Test statistics	
Min CPU cycles	38
Max CPU cycles	69
Avg CPU cycles	57

Test case: Conversion test OK

Conversion test for General block RateLimiter.

Test results				
Time step	1	2	...	37
Mask parameters				
Tr	-10	-9.444	...	10
Tf	-9	-8.5	...	9
ts_fact	3	3	...	3
Controller parameters				
RateUp	2147483647	2147483647	...	64425
RateDown	2147483647	2147483647	...	71583
Exp. RateUp	2147483647	2147483647	...	64425
Exp. RateDown	2147483647	2147483647	...	71583

Test settings	
Tolerance RateUp	±0,0000e+00
Tolerance RateDown	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block RateLimiter.

Test results				
Time step	1	2	...	37
Mask parameters				
Tr	-10	-9.444	...	10
Tf	-9	-8.5	...	9
ts_fact	3	3	...	3
Controller parameters				
RateUp	2147483647	2147483647	...	64424
RateDown	2147483647	2147483647	...	71582
Exp. RateUp	2147483647	2147483647	...	64425
Exp. RateDown	2147483647	2147483647	...	71583

Test settings	
Tolerance RateUp	±3,0000e+00
Tolerance RateDown	±3,0000e+00

Test statistics	
Min CPU cycles	2067
Max CPU cycles	2100
Avg CPU cycles	2082

Verification: RateLimiter FiP32 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for General block RateLimiter.

Test results				
Time step	1	2	...	266
CPU cycles	66	66	...	141
Inputs				
In (DSP)	0	-2147483648	...	-429496730
Init (DSP)	0	644245094	...	644245094
Enable (DSP)	0	0	...	1
In	0	-1	...	-0.2
Init	0	0.3	...	0.3
Enable	0	0	...	1
Parameters				
Tr	0.01			
Tf	0.03			
ts_fact	1			
Outputs				
Out	0	-1	...	0.423
Exp. Out	0	-1	...	0.423
Out (DSP)	0	-2147483648	...	909101402
Exp. Out (DSP)	0	-2147483648	...	909101411

Test settings	
Tolerance Out	±1,8626e-08 (±40 LSB)

Test statistics	
Min CPU cycles	66
Max CPU cycles	141
Avg CPU cycles	111

Test case: Conversion test OK

Conversion test for General block RateLimiter.

Test results				
Time step	1	2	...	37
Mask parameters				
Tr	-10	-9.444	...	10
Tf	-9	-8.5	...	9
ts_fact	3	3	...	3
Controller parameters				
RateUp	2147483647	2147483647	...	64425
RateDown	2147483647	2147483647	...	71583
Exp. RateUp	2147483647	2147483647	...	64425
Exp. RateDown	2147483647	2147483647	...	71583

Test settings	
Tolerance RateUp	±0,0000e+00
Tolerance RateDown	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block RateLimiter.

Test results				
Time step	1	2	...	37
Mask parameters				
Tr	-10	-9.444	...	10
Tf	-9	-8.5	...	9
ts_fact	3	3	...	3
Controller parameters				
RateUp	2147483647	2147483647	...	64424
RateDown	2147483647	2147483647	...	71582
Exp. RateUp	2147483647	2147483647	...	64425
Exp. RateDown	2147483647	2147483647	...	71583

Test settings	
Tolerance RateUp	±3,0000e+00
Tolerance RateDown	±3,0000e+00

Test statistics	
Min CPU cycles	4978
Max CPU cycles	5687
Avg CPU cycles	5633

Verification: RateLimiter FiP32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for General block RateLimiter.

Test results				
Time step	1	2	...	266
CPU cycles	76	64	...	105
Inputs				
In (DSP)	0	-2147483648	...	-429496730
Init (DSP)	0	644245094	...	644245094
Enable (DSP)	0	0	...	1
In	0	-1	...	-0.2
Init	0	0.3	...	0.3
Enable	0	0	...	1
Parameters				
Tr	0.01			
Tf	0.03			
ts_fact	1			
Outputs				
Out	0	-1	...	0.423
Exp. Out	0	-1	...	0.423
Out (DSP)	0	-2147483648	...	909101402
Exp. Out (DSP)	0	-2147483648	...	909101411

Test settings	
Tolerance Out	±1,8626e-08 (±40 LSB)

Test statistics	
Min CPU cycles	64
Max CPU cycles	105
Avg CPU cycles	91

Test case: Conversion test OK

Conversion test for General block RateLimiter.

Test results				
Time step	1	2	...	37
Mask parameters				
Tr	-10	-9.444	...	10
Tf	-9	-8.5	...	9
ts_fact	3	3	...	3
Controller parameters				
RateUp	2147483647	2147483647	...	64425
RateDown	2147483647	2147483647	...	71583
Exp. RateUp	2147483647	2147483647	...	64425
Exp. RateDown	2147483647	2147483647	...	71583

Test settings	
Tolerance RateUp	±0,0000e+00
Tolerance RateDown	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block RateLimiter.

Test results				
Time step	1	2	...	37
Mask parameters				
Tr	-10	-9.444	...	10
Tf	-9	-8.5	...	9
ts_fact	3	3	...	3
Controller parameters				
RateUp	2147483647	2147483647	...	64424
RateDown	2147483647	2147483647	...	71582
Exp. RateUp	2147483647	2147483647	...	64425
Exp. RateDown	2147483647	2147483647	...	71583

Test settings	
Tolerance RateUp	±3,0000e+00
Tolerance RateDown	±3,0000e+00

Test statistics	
Min CPU cycles	1391
Max CPU cycles	1646
Avg CPU cycles	1398

Verification: RateLimiter FiP32 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for General block RateLimiter.

Test results				
Time step	1	2	...	266
CPU cycles	61	61	...	142
Inputs				
In (DSP)	0	-2147483648	...	-429496730
Init (DSP)	0	644245094	...	644245094
Enable (DSP)	0	0	...	1
In	0	-1	...	-0.2
Init	0	0.3	...	0.3
Enable	0	0	...	1
Parameters				
Tr	0.01			
Tf	0.03			
ts_fact	1			
Outputs				
Out	0	-1	...	0.423
Exp. Out	0	-1	...	0.423
Out (DSP)	0	-2147483648	...	909101402
Exp. Out (DSP)	0	-2147483648	...	909101411

Test settings	
Tolerance Out	±1,8626e-08 (±40 LSB)

Test statistics	
Min CPU cycles	61
Max CPU cycles	154
Avg CPU cycles	115

Test case: Conversion test OK

Conversion test for General block RateLimiter.

Test results				
Time step	1	2	...	37
Mask parameters				
Tr	-10	-9.444	...	10
Tf	-9	-8.5	...	9
ts_fact	3	3	...	3
Controller parameters				
RateUp	2147483647	2147483647	...	64425
RateDown	2147483647	2147483647	...	71583
Exp. RateUp	2147483647	2147483647	...	64425
Exp. RateDown	2147483647	2147483647	...	71583

Test settings	
Tolerance RateUp	±0,0000e+00
Tolerance RateDown	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block RateLimiter.

Test results				
Time step	1	2	...	37
Mask parameters				
Tr	-10	-9.444	...	10
Tf	-9	-8.5	...	9
ts_fact	3	3	...	3
Controller parameters				
RateUp	2147483647	2147483647	...	64424
RateDown	2147483647	2147483647	...	71582
Exp. RateUp	2147483647	2147483647	...	64425
Exp. RateDown	2147483647	2147483647	...	71583

Test settings	
Tolerance RateUp	±3,0000e+00
Tolerance RateDown	±3,0000e+00

Test statistics	
Min CPU cycles	2162
Max CPU cycles	2240
Avg CPU cycles	2200

Verification: RateLimiter Float32 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for General block RateLimiter.

Test results				
Time step	1	2	...	213
CPU cycles	72	72	...	111
Inputs				
In (DSP)	0	-1	...	-0.8
Init (DSP)	0	0.3	...	0.3
Enable (DSP)	0	0	...	1
In	0	-1	...	-0.8
Init	0	0.3	...	0.3
Enable	0	0	...	1
Parameters				
Tr	0.01			
Tf	0.03			
ts_fact	1			
Outputs				
Out	0	-1	...	0.423
Exp. Out	0	-1	...	0.423
Out (DSP)	0	-1	...	0.423
Exp. Out (DSP)	0	-1	...	0.423

Test settings	
Tolerance Out	±1,9558e-07 (±420 LSB)

Test statistics	
Min CPU cycles	72
Max CPU cycles	111
Avg CPU cycles	95

Test case: Conversion test OK

Conversion test for General block RateLimiter.

Test results				
Time step	1	2	...	37
Mask parameters				
Tr	-10	-9.444	...	10
Tf	-9	-8.5	...	9
ts_fact	3	3	...	3
Controller parameters				
RateUp	1	1	...	0
RateDown	1	1	...	0
Exp. RateUp	1	1	...	0
Exp. RateDown	1	1	...	0

Test settings	
Tolerance RateUp	±0,0000e+00
Tolerance RateDown	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block RateLimiter.

Test results				
Time step	1	2	...	37
Mask parameters				
Tr	-10	-9.444	...	10
Tf	-9	-8.5	...	9
ts_fact	3	3	...	3
Controller parameters				
RateUp	1	1	...	0
RateDown	1	1	...	0
Exp. RateUp	1	1	...	0
Exp. RateDown	1	1	...	0

Test settings	
Tolerance RateUp	±3,0000e-09
Tolerance RateDown	±3,0000e-09

Test statistics	
Min CPU cycles	2418
Max CPU cycles	2452
Avg CPU cycles	2418

Verification: RateLimiter Float32 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for General block RateLimiter.

Test results				
Time step	1	2	...	213
CPU cycles	41	41	...	81
Inputs				
In (DSP)	0	-1	...	-0.8
Init (DSP)	0	0.3	...	0.3
Enable (DSP)	0	0	...	1
In	0	-1	...	-0.8
Init	0	0.3	...	0.3
Enable	0	0	...	1
Parameters				
Tr	0.01			
Tf	0.03			
ts_fact	1			
Outputs				
Out	0	-1	...	0.423
Exp. Out	0	-1	...	0.423
Out (DSP)	0	-1	...	0.423
Exp. Out (DSP)	0	-1	...	0.423

Test settings	
Tolerance Out	±1,9558e-07 (±420 LSB)

Test statistics	
Min CPU cycles	41
Max CPU cycles	81
Avg CPU cycles	67

Test case: Conversion test OK

Conversion test for General block RateLimiter.

Test results				
Time step	1	2	...	37
Mask parameters				
Tr	-10	-9.444	...	10
Tf	-9	-8.5	...	9
ts_fact	3	3	...	3
Controller parameters				
RateUp	1	1	...	0
RateDown	1	1	...	0
Exp. RateUp	1	1	...	0
Exp. RateDown	1	1	...	0

Test settings	
Tolerance RateUp	±0,0000e+00
Tolerance RateDown	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block RateLimiter.

Test results				
Time step	1	2	...	37
Mask parameters				
Tr	-10	-9.444	...	10
Tf	-9	-8.5	...	9
ts_fact	3	3	...	3
Controller parameters				
RateUp	1	1	...	0
RateDown	1	1	...	0
Exp. RateUp	1	1	...	0
Exp. RateDown	1	1	...	0

Test settings	
Tolerance RateUp	±3,0000e-09
Tolerance RateDown	±3,0000e-09

Test statistics	
Min CPU cycles	927
Max CPU cycles	927
Avg CPU cycles	927

Verification: RateLimiter Float32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for General block RateLimiter.

Test results				
Time step	1	2	...	213
CPU cycles	57	57	...	115
Inputs				
In (DSP)	0	-1	...	-0.8
Init (DSP)	0	0.3	...	0.3
Enable (DSP)	0	0	...	1
In	0	-1	...	-0.8
Init	0	0.3	...	0.3
Enable	0	0	...	1
Parameters				
Tr	0.01			
Tf	0.03			
ts_fact	1			
Outputs				
Out	0	-1	...	0.423
Exp. Out	0	-1	...	0.423
Out (DSP)	0	-1	...	0.423
Exp. Out (DSP)	0	-1	...	0.423

Test settings	
Tolerance Out	±1,9558e-07 (±420 LSB)

Test statistics	
Min CPU cycles	57
Max CPU cycles	175
Avg CPU cycles	94

Test case: Conversion test OK

Conversion test for General block RateLimiter.

Test results				
Time step	1	2	...	37
Mask parameters				
Tr	-10	-9.444	...	10
Tf	-9	-8.5	...	9
ts_fact	3	3	...	3
Controller parameters				
RateUp	1	1	...	0
RateDown	1	1	...	0
Exp. RateUp	1	1	...	0
Exp. RateDown	1	1	...	0

Test settings	
Tolerance RateUp	±0,0000e+00
Tolerance RateDown	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block RateLimiter.

Test results				
Time step	1	2	...	37
Mask parameters				
Tr	-10	-9.444	...	10
Tf	-9	-8.5	...	9
ts_fact	3	3	...	3
Controller parameters				
RateUp	1	1	...	0
RateDown	1	1	...	0
Exp. RateUp	1	1	...	0
Exp. RateDown	1	1	...	0

Test settings	
Tolerance RateUp	±3,0000e-09
Tolerance RateDown	±3,0000e-09

Test statistics	
Min CPU cycles	957
Max CPU cycles	962
Avg CPU cycles	957

Verification: RateLimiter Float32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for General block RateLimiter.

Test results				
Time step	1	2	...	213
CPU cycles	79	79	...	618
Inputs				
In (DSP)	0	-1	...	-0.8
Init (DSP)	0	0.3	...	0.3
Enable (DSP)	0	0	...	1
In	0	-1	...	-0.8
Init	0	0.3	...	0.3
Enable	0	0	...	1
Parameters				
Tr	0.01			
Tf	0.03			
ts_fact	1			
Outputs				
Out	0	-1	...	0.423
Exp. Out	0	-1	...	0.423
Out (DSP)	0	-1	...	0.423
Exp. Out (DSP)	0	-1	...	0.423

Test settings	
Tolerance Out	±1,9558e-07 (±420 LSB)

Test statistics	
Min CPU cycles	79
Max CPU cycles	676
Avg CPU cycles	418

Test case: Conversion test OK

Conversion test for General block RateLimiter.

Test results				
Time step	1	2	...	37
Mask parameters				
Tr	-10	-9.444	...	10
Tf	-9	-8.5	...	9
ts_fact	3	3	...	3
Controller parameters				
RateUp	1	1	...	0
RateDown	1	1	...	0
Exp. RateUp	1	1	...	0
Exp. RateDown	1	1	...	0

Test settings	
Tolerance RateUp	±0,0000e+00
Tolerance RateDown	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block RateLimiter.

Test results				
Time step	1	2	...	37
Mask parameters				
Tr	-10	-9.444	...	10
Tf	-9	-8.5	...	9
ts_fact	3	3	...	3
Controller parameters				
RateUp	1	1	...	0
RateDown	1	1	...	0
Exp. RateUp	1	1	...	0
Exp. RateDown	1	1	...	0

Test settings	
Tolerance RateUp	±3,0000e-09
Tolerance RateDown	±3,0000e-09

Test statistics	
Min CPU cycles	3110
Max CPU cycles	3216
Avg CPU cycles	3175

Verification: RateLimiter Float32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for General block RateLimiter.

Test results				
Time step	1	2	...	213
CPU cycles	66	66	...	311
Inputs				
In (DSP)	0	-1	...	-0.8
Init (DSP)	0	0.3	...	0.3
Enable (DSP)	0	0	...	1
In	0	-1	...	-0.8
Init	0	0.3	...	0.3
Enable	0	0	...	1
Parameters				
Tr	0.01			
Tf	0.03			
ts_fact	1			
Outputs				
Out	0	-1	...	0.423
Exp. Out	0	-1	...	0.423
Out (DSP)	0	-1	...	0.423
Exp. Out (DSP)	0	-1	...	0.423

Test settings	
Tolerance Out	±1,9558e-07 (±420 LSB)

Test statistics	
Min CPU cycles	66
Max CPU cycles	313
Avg CPU cycles	211

Test case: Conversion test OK

Conversion test for General block RateLimiter.

Test results				
Time step	1	2	...	37
Mask parameters				
Tr	-10	-9.444	...	10
Tf	-9	-8.5	...	9
ts_fact	3	3	...	3
Controller parameters				
RateUp	1	1	...	0
RateDown	1	1	...	0
Exp. RateUp	1	1	...	0
Exp. RateDown	1	1	...	0

Test settings	
Tolerance RateUp	±0,0000e+00
Tolerance RateDown	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block RateLimiter.

Test results				
Time step	1	2	...	37
Mask parameters				
Tr	-10	-9.444	...	10
Tf	-9	-8.5	...	9
ts_fact	3	3	...	3
Controller parameters				
RateUp	1	1	...	0
RateDown	1	1	...	0
Exp. RateUp	1	1	...	0
Exp. RateDown	1	1	...	0

Test settings	
Tolerance RateUp	±3,0000e-09
Tolerance RateDown	±3,0000e-09

Test statistics	
Min CPU cycles	972
Max CPU cycles	1013
Avg CPU cycles	991

Verification: RateLimiter Float32 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for General block RateLimiter.

Test results				
Time step	1	2	...	213
CPU cycles	71	71	...	809
Inputs				
In (DSP)	0	-1	...	-0.8
Init (DSP)	0	0.3	...	0.3
Enable (DSP)	0	0	...	1
In	0	-1	...	-0.8
Init	0	0.3	...	0.3
Enable	0	0	...	1
Parameters				
Tr	0.01			
Tf	0.03			
ts_fact	1			
Outputs				
Out	0	-1	...	0.423
Exp. Out	0	-1	...	0.423
Out (DSP)	0	-1	...	0.423
Exp. Out (DSP)	0	-1	...	0.423

Test settings	
Tolerance Out	±1,9558e-07 (±420 LSB)

Test statistics	
Min CPU cycles	71
Max CPU cycles	849
Avg CPU cycles	545

Test case: Conversion test OK

Conversion test for General block RateLimiter.

Test results				
Time step	1	2	...	37
Mask parameters				
Tr	-10	-9.444	...	10
Tf	-9	-8.5	...	9
ts_fact	3	3	...	3
Controller parameters				
RateUp	1	1	...	0
RateDown	1	1	...	0
Exp. RateUp	1	1	...	0
Exp. RateDown	1	1	...	0

Test settings	
Tolerance RateUp	±0,0000e+00
Tolerance RateDown	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block RateLimiter.

Test results				
Time step	1	2	...	37
Mask parameters				
Tr	-10	-9.444	...	10
Tf	-9	-8.5	...	9
ts_fact	3	3	...	3
Controller parameters				
RateUp	1	1	...	0
RateDown	1	1	...	0
Exp. RateUp	1	1	...	0
Exp. RateDown	1	1	...	0

Test settings	
Tolerance RateUp	±3,0000e-09
Tolerance RateDown	±3,0000e-09

Test statistics	
Min CPU cycles	3463
Max CPU cycles	4224
Avg CPU cycles	4149

Verification: RateLimiter Float32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for General block RateLimiter.

Test results				
Time step	1	2	...	213
CPU cycles	92	66	...	84
Inputs				
In (DSP)	0	-1	...	-0.8
Init (DSP)	0	0.3	...	0.3
Enable (DSP)	0	0	...	1
In	0	-1	...	-0.8
Init	0	0.3	...	0.3
Enable	0	0	...	1
Parameters				
Tr	0.01			
Tf	0.03			
ts_fact	1			
Outputs				
Out	0	-1	...	0.423
Exp. Out	0	-1	...	0.423
Out (DSP)	0	-1	...	0.423
Exp. Out (DSP)	0	-1	...	0.423

Test settings	
Tolerance Out	±1,9558e-07 (±420 LSB)

Test statistics	
Min CPU cycles	66
Max CPU cycles	92
Avg CPU cycles	76

Test case: Conversion test OK

Conversion test for General block RateLimiter.

Test results				
Time step	1	2	...	37
Mask parameters				
Tr	-10	-9.444	...	10
Tf	-9	-8.5	...	9
ts_fact	3	3	...	3
Controller parameters				
RateUp	1	1	...	0
RateDown	1	1	...	0
Exp. RateUp	1	1	...	0
Exp. RateDown	1	1	...	0

Test settings	
Tolerance RateUp	±0,0000e+00
Tolerance RateDown	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block RateLimiter.

Test results				
Time step	1	2	...	37
Mask parameters				
Tr	-10	-9.444	...	10
Tf	-9	-8.5	...	9
ts_fact	3	3	...	3
Controller parameters				
RateUp	1	1	...	0
RateDown	1	1	...	0
Exp. RateUp	1	1	...	0
Exp. RateDown	1	1	...	0

Test settings	
Tolerance RateUp	±3,0000e-09
Tolerance RateDown	±3,0000e-09

Test statistics	
Min CPU cycles	787
Max CPU cycles	938
Avg CPU cycles	791

Verification: RateLimiter Float32 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for General block RateLimiter.

Test results				
Time step	1	2	...	213
CPU cycles	57	57	...	109
Inputs				
In (DSP)	0	-1	...	-0.8
Init (DSP)	0	0.3	...	0.3
Enable (DSP)	0	0	...	1
In	0	-1	...	-0.8
Init	0	0.3	...	0.3
Enable	0	0	...	1
Parameters				
Tr	0.01			
Tf	0.03			
ts_fact	1			
Outputs				
Out	0	-1	...	0.423
Exp. Out	0	-1	...	0.423
Out (DSP)	0	-1	...	0.423
Exp. Out (DSP)	0	-1	...	0.423

Test settings	
Tolerance Out	±1,9558e-07 (±420 LSB)

Test statistics	
Min CPU cycles	57
Max CPU cycles	109
Avg CPU cycles	88

Test case: Conversion test OK

Conversion test for General block RateLimiter.

Test results				
Time step	1	2	...	37
Mask parameters				
Tr	-10	-9.444	...	10
Tf	-9	-8.5	...	9
ts_fact	3	3	...	3
Controller parameters				
RateUp	1	1	...	0
RateDown	1	1	...	0
Exp. RateUp	1	1	...	0
Exp. RateDown	1	1	...	0

Test settings	
Tolerance RateUp	±0,0000e+00
Tolerance RateDown	±0,0000e+00

Test case: Conversion-on-Target test **OK**

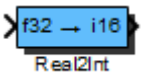
Conversion-on-Target test for General block RateLimiter.

Test results				
Time step	1	2	...	37
Mask parameters				
Tr	-10	-9.444	...	10
Tf	-9	-8.5	...	9
ts_fact	3	3	...	3
Controller parameters				
RateUp	1	1	...	0
RateDown	1	1	...	0
Exp. RateUp	1	1	...	0
Exp. RateDown	1	1	...	0

Test settings	
Tolerance RateUp	±3,0000e-09
Tolerance RateDown	±3,0000e-09

Test statistics	
Min CPU cycles	1858
Max CPU cycles	1864
Avg CPU cycles	1858

Block: Real2Int



Conversion block from real (floating point) datatypes to integer (fixed point) datatypes.
Out = In / Scale

Inports	
In	Real input

Outports	
Out	Integer output

Mask Parameters		
Name	**ID**	**Description**
Scale	1	Scaling factor from real to integer

Implementations:

Float32_FiP8	32 Floating Point to 8 Bit Fixed Point Implementation
Float32_FiP16	32 Floating Point to 16 Bit Fixed Point Implementation
Float32_FiP32	32 Floating Point to 32 Bit Fixed Point Implementation
Float64_FiP8	64 Floating Point to 8 Bit Fixed Point Implementation
Float64_FiP16	64 Floating Point to 16 Bit Fixed Point Implementation
Float64_FiP32	64 Floating Point to 32 Bit Fixed Point Implementation
Float32_Bool	32 Floating Point to Boolean Implementation
Float64_Bool	64 Floating Point to Boolean Implementation

Implementation: Float32_FiP8

32 Floating Point to 8 Bit Fixed Point Implementation

Inports Data Type	
In	float32

Outports Data Type	
Out	int8

Implementation: Float32_FiP16

32 Floating Point to 16 Bit Fixed Point Implementation

Inports Data Type	
In	float32

Outports Data Type	
Out	int16

Implementation: Float32_FiP32

32 Floating Point to 32 Bit Fixed Point Implementation

Inports Data Type	
In	float32

Outports Data Type	
Out	int32

Implementation: Float64_FiP8

64 Floating Point to 8 Bit Fixed Point Implementation

Inports Data Type	
In	float64

Outports Data Type	
Out	int8

Implementation: Float64_FiP16

64 Floating Point to 16 Bit Fixed Point Implementation

Inports Data Type	
In	float64

Outports Data Type	
Out	int16

Implementation: Float64_FiP32

64 Floating Point to 32 Bit Fixed Point Implementation

Inports Data Type	
In	float64

Outports Data Type	
Out	int32

Implementation: Float32_Bool

32 Floating Point to Boolean Implementation

Inports Data Type	
In	float32

Outports Data Type	
Out	bool

Implementation: Float64_Bool

64 Floating Point to Boolean Implementation

Inports Data Type	
In	float64

Outports Data Type	
Out	bool

Verification: Real2Int Float32_FiP16 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for General block Real2Int.

Test results				
Time step	1	2	...	113
CPU cycles	82	82	...	82
Inputs				
In (DSP)	-31	-30.446	...	31
In	-31	-30.446	...	31
Parameters				
Scale	73.5			
Outputs				
Out	-0.422	-0.414	...	0.422
Exp. Out	-0.422	-0.414	...	0.422
Out (DSP)	-13820	-13573	...	13820
Exp. Out (DSP)	-13821	-13574	...	13821

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	82
Max CPU cycles	82
Avg CPU cycles	82

Test case: Parameter test OK

Parameter test for General block Real2Int.

Test results				
Time step	1	2	...	14
CPU cycles	82	82	...	82
Inputs				
In (DSP)	0.1			
In	0.1			
Parameters				
Scale	-10	-5	...	10
Outputs				
Out	-0.01	-0.02	...	0.01
Exp. Out	-0.01	-0.02	...	0.01
Out (DSP)	-327	-655	...	327
Exp. Out (DSP)	-328	-655	...	328

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	78
Max CPU cycles	82
Avg CPU cycles	81

Test case: Conversion test **OK**

Conversion test for General block Real2Int.

Test results				
Time step	1	2	...	14
Mask parameters				
Scale	-10	-5	...	10
Controller parameters				
scale	-3276.8	-6553.6	...	3276.8
Exp. scale	-3276.8	-6553.6	...	3276.8

Test settings	
Tolerance scale	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block Real2Int.

Test results				
Time step	1	2	...	14
Mask parameters				
Scale	-10	-5	...	10
Controller parameters				
scale	-3276.8	-6553.6	...	3276.8
Exp. scale	-3276.8	-6553.6	...	3276.8

Test settings	
Tolerance scale	±5,0000e-04

Test statistics	
Min CPU cycles	1095
Max CPU cycles	1095
Avg CPU cycles	1095

Verification: Real2Int Float32_FiP16 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for General block Real2Int.

Test results				
Time step	1	2	...	113
CPU cycles	41	41	...	41
Inputs				
In (DSP)	-31	-30.446	...	31
In	-31	-30.446	...	31
Parameters				
Scale	73.5			
Outputs				
Out	-0.422	-0.414	...	0.422
Exp. Out	-0.422	-0.414	...	0.422
Out (DSP)	-13820	-13573	...	13820
Exp. Out (DSP)	-13821	-13574	...	13821

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	41
Max CPU cycles	41
Avg CPU cycles	41

Test case: Parameter test OK

Parameter test for General block Real2Int.

Test results				
Time step	1	2	...	14
CPU cycles	41	41	...	41
Inputs				
In (DSP)	0.1			
In	0.1			
Parameters				
Scale	-10	-5	...	10
Outputs				
Out	-0.01	-0.02	...	0.01
Exp. Out	-0.01	-0.02	...	0.01
Out (DSP)	-327	-655	...	327
Exp. Out (DSP)	-328	-655	...	328

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	37
Max CPU cycles	43
Avg CPU cycles	40

Test case: Conversion test **OK**

Conversion test for General block Real2Int.

Test results				
Time step	1	2	...	14
Mask parameters				
Scale	-10	-5	...	10
Controller parameters				
scale	-3276.8	-6553.6	...	3276.8
Exp. scale	-3276.8	-6553.6	...	3276.8

Test settings	
Tolerance scale	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block Real2Int.

Test results				
Time step	1	2	...	14
Mask parameters				
Scale	-10	-5	...	10
Controller parameters				
scale	-3276.8	-6553.6	...	3276.8
Exp. scale	-3276.8	-6553.6	...	3276.8

Test settings	
Tolerance scale	±5,0000e-04

Test statistics	
Min CPU cycles	415
Max CPU cycles	415
Avg CPU cycles	415

Verification: Real2Int Float32_FiP16 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for General block Real2Int.

Test results				
Time step	1	2	...	113
CPU cycles	82	82	...	82
Inputs				
In (DSP)	-31	-30.446	...	31
In	-31	-30.446	...	31
Parameters				
Scale	73.5			
Outputs				
Out	-0.422	-0.414	...	0.422
Exp. Out	-0.422	-0.414	...	0.422
Out (DSP)	-13820	-13573	...	13820
Exp. Out (DSP)	-13821	-13574	...	13821

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	82
Max CPU cycles	82
Avg CPU cycles	82

Test case: Parameter test OK

Parameter test for General block Real2Int.

Test results				
Time step	1	2	...	14
CPU cycles	82	82	...	82
Inputs				
In (DSP)	0.1			
In	0.1			
Parameters				
Scale	-10	-5	...	10
Outputs				
Out	-0.01	-0.02	...	0.01
Exp. Out	-0.01	-0.02	...	0.01
Out (DSP)	-327	-655	...	327
Exp. Out (DSP)	-328	-655	...	328

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	82
Max CPU cycles	82
Avg CPU cycles	82

Test case: Conversion test **OK**

Conversion test for General block Real2Int.

Test results				
Time step	1	2	...	14
Mask parameters				
Scale	-10	-5	...	10
Controller parameters				
scale	-3276.8	-6553.6	...	3276.8
Exp. scale	-3276.8	-6553.6	...	3276.8

Test settings	
Tolerance scale	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block Real2Int.

Test results				
Time step	1	2	...	14
Mask parameters				
Scale	-10	-5	...	10
Controller parameters				
scale	-3276.8	-6553.6	...	3276.8
Exp. scale	-3276.8	-6553.6	...	3276.8

Test settings	
Tolerance scale	±5,0000e-04

Test statistics	
Min CPU cycles	492
Max CPU cycles	492
Avg CPU cycles	492

Verification: Real2Int Float32_FiP16 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for General block Real2Int.

Test results				
Time step	1	2	...	113
CPU cycles	276	276	...	278
Inputs				
In (DSP)	-31	-30.446	...	31
In	-31	-30.446	...	31
Parameters				
Scale	73.5			
Outputs				
Out	-0.422	-0.414	...	0.422
Exp. Out	-0.422	-0.414	...	0.422
Out (DSP)	-13820	-13573	...	13820
Exp. Out (DSP)	-13821	-13574	...	13821

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	205
Max CPU cycles	282
Avg CPU cycles	277

Test case: Parameter test OK

Parameter test for General block Real2Int.

Test results				
Time step	1	2	...	14
CPU cycles	276	276	...	278
Inputs				
In (DSP)	0.1			
In	0.1			
Parameters				
Scale	-10	-5	...	10
Outputs				
Out	-0.01	-0.02	...	0.01
Exp. Out	-0.01	-0.02	...	0.01
Out (DSP)	-327	-655	...	327
Exp. Out (DSP)	-328	-655	...	328

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	275
Max CPU cycles	281
Avg CPU cycles	278

Test case: Conversion test **OK**

Conversion test for General block Real2Int.

Test results				
Time step	1	2	...	14
Mask parameters				
Scale	-10	-5	...	10
Controller parameters				
scale	-3276.8	-6553.6	...	3276.8
Exp. scale	-3276.8	-6553.6	...	3276.8

Test settings	
Tolerance scale	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block Real2Int.

Test results				
Time step	1	2	...	14
Mask parameters				
Scale	-10	-5	...	10
Controller parameters				
scale	-3276.8	-6553.6	...	3276.8
Exp. scale	-3276.8	-6553.6	...	3276.8

Test settings	
Tolerance scale	±5,0000e-04

Test statistics	
Min CPU cycles	1254
Max CPU cycles	1272
Avg CPU cycles	1261

Verification: Real2Int Float32_FiP16 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for General block Real2Int.

Test results				
Time step	1	2	...	113
CPU cycles	115	116	...	114
Inputs				
In (DSP)	-31	-30.446	...	31
In	-31	-30.446	...	31
Parameters				
Scale	73.5			
Outputs				
Out	-0.422	-0.414	...	0.422
Exp. Out	-0.422	-0.414	...	0.422
Out (DSP)	-13820	-13573	...	13820
Exp. Out (DSP)	-13821	-13574	...	13821

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	97
Max CPU cycles	118
Avg CPU cycles	115

Test case: Parameter test OK

Parameter test for General block Real2Int.

Test results				
Time step	1	2	...	14
CPU cycles	116	116	...	115
Inputs				
In (DSP)	0.1			
In	0.1			
Parameters				
Scale	-10	-5	...	10
Outputs				
Out	-0.01	-0.02	...	0.01
Exp. Out	-0.01	-0.02	...	0.01
Out (DSP)	-327	-655	...	327
Exp. Out (DSP)	-328	-655	...	328

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	114
Max CPU cycles	117
Avg CPU cycles	115

Test case: Conversion test **OK**

Conversion test for General block Real2Int.

Test results				
Time step	1	2	...	14
Mask parameters				
Scale	-10	-5	...	10
Controller parameters				
scale	-3276.8	-6553.6	...	3276.8
Exp. scale	-3276.8	-6553.6	...	3276.8

Test settings	
Tolerance scale	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block Real2Int.

Test results				
Time step	1	2	...	14
Mask parameters				
Scale	-10	-5	...	10
Controller parameters				
scale	-3276.8	-6553.6	...	3276.8
Exp. scale	-3276.8	-6553.6	...	3276.8

Test settings	
Tolerance scale	±5,0000e-04

Test statistics	
Min CPU cycles	396
Max CPU cycles	422
Avg CPU cycles	409

Verification: Real2Int Float32_FiP16 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for General block Real2Int.

Test results				
Time step	1	2	...	113
CPU cycles	323	327	...	324
Inputs				
In (DSP)	-31	-30.446	...	31
In	-31	-30.446	...	31
Parameters				
Scale	73.5			
Outputs				
Out	-0.422	-0.414	...	0.422
Exp. Out	-0.422	-0.414	...	0.422
Out (DSP)	-13820	-13573	...	13820
Exp. Out (DSP)	-13821	-13574	...	13821

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	209
Max CPU cycles	371
Avg CPU cycles	333

Test case: Parameter test OK

Parameter test for General block Real2Int.

Test results				
Time step	1	2	...	14
CPU cycles	362	355	...	363
Inputs				
In (DSP)	0.1			
In	0.1			
Parameters				
Scale	-10	-5	...	10
Outputs				
Out	-0.01	-0.02	...	0.01
Exp. Out	-0.01	-0.02	...	0.01
Out (DSP)	-327	-655	...	327
Exp. Out (DSP)	-328	-655	...	328

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	308
Max CPU cycles	363
Avg CPU cycles	337

Test case: Conversion test **OK**

Conversion test for General block Real2Int.

Test results				
Time step	1	2	...	14
Mask parameters				
Scale	-10	-5	...	10
Controller parameters				
scale	-3276.8	-6553.6	...	3276.8
Exp. scale	-3276.8	-6553.6	...	3276.8

Test settings	
Tolerance scale	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block Real2Int.

Test results				
Time step	1	2	...	14
Mask parameters				
Scale	-10	-5	...	10
Controller parameters				
scale	-3276.8	-6553.6	...	3276.8
Exp. scale	-3276.8	-6553.6	...	3276.8

Test settings	
Tolerance scale	±5,0000e-04

Test statistics	
Min CPU cycles	1305
Max CPU cycles	1369
Avg CPU cycles	1331

Verification: Real2Int Float32_FiP16 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for General block Real2Int.

Test results				
Time step	1	2	...	113
CPU cycles	91	80	...	80
Inputs				
In (DSP)	-31	-30.446	...	31
In	-31	-30.446	...	31
Parameters				
Scale	73.5			
Outputs				
Out	-0.422	-0.414	...	0.422
Exp. Out	-0.422	-0.414	...	0.422
Out (DSP)	-13820	-13573	...	13820
Exp. Out (DSP)	-13821	-13574	...	13821

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	80
Max CPU cycles	91
Avg CPU cycles	80

Test case: Parameter test OK

Parameter test for General block Real2Int.

Test results				
Time step	1	2	...	14
CPU cycles	91	91	...	91
Inputs				
In (DSP)	0.1			
In	0.1			
Parameters				
Scale	-10	-5	...	10
Outputs				
Out	-0.01	-0.02	...	0.01
Exp. Out	-0.01	-0.02	...	0.01
Out (DSP)	-327	-655	...	327
Exp. Out (DSP)	-328	-655	...	328

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	91
Max CPU cycles	91
Avg CPU cycles	91

Test case: Conversion test **OK**

Conversion test for General block Real2Int.

Test results				
Time step	1	2	...	14
Mask parameters				
Scale	-10	-5	...	10
Controller parameters				
scale	-3276.8	-6553.6	...	3276.8
Exp. scale	-3276.8	-6553.6	...	3276.8

Test settings	
Tolerance scale	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block Real2Int.

Test results				
Time step	1	2	...	14
Mask parameters				
Scale	-10	-5	...	10
Controller parameters				
scale	-3276.8	-6553.6	...	3276.8
Exp. scale	-3276.8	-6553.6	...	3276.8

Test settings	
Tolerance scale	±5,0000e-04

Test statistics	
Min CPU cycles	398
Max CPU cycles	464
Avg CPU cycles	402

Verification: Real2Int Float32_FiP16 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for General block Real2Int.

Test results				
Time step	1	2	...	113
CPU cycles	65	65	...	65
Inputs				
In (DSP)	-31	-30.446	...	31
In	-31	-30.446	...	31
Parameters				
Scale	73.5			
Outputs				
Out	-0.422	-0.414	...	0.422
Exp. Out	-0.422	-0.414	...	0.422
Out (DSP)	-13820	-13573	...	13820
Exp. Out (DSP)	-13821	-13574	...	13821

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	65
Max CPU cycles	65
Avg CPU cycles	65

Test case: Parameter test OK

Parameter test for General block Real2Int.

Test results				
Time step	1	2	...	14
CPU cycles	65	65	...	65
Inputs				
In (DSP)	0.1			
In	0.1			
Parameters				
Scale	-10	-5	...	10
Outputs				
Out	-0.01	-0.02	...	0.01
Exp. Out	-0.01	-0.02	...	0.01
Out (DSP)	-327	-655	...	327
Exp. Out (DSP)	-328	-655	...	328

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	64
Max CPU cycles	65
Avg CPU cycles	64

Test case: Conversion test **OK**

Conversion test for General block Real2Int.

Test results				
Time step	1	2	...	14
Mask parameters				
Scale	-10	-5	...	10
Controller parameters				
scale	-3276.8	-6553.6	...	3276.8
Exp. scale	-3276.8	-6553.6	...	3276.8

Test settings	
Tolerance scale	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block Real2Int.

Test results				
Time step	1	2	...	14
Mask parameters				
Scale	-10	-5	...	10
Controller parameters				
scale	-3276.8	-6553.6	...	3276.8
Exp. scale	-3276.8	-6553.6	...	3276.8

Test settings	
Tolerance scale	±5,0000e-04

Test statistics	
Min CPU cycles	884
Max CPU cycles	884
Avg CPU cycles	884

Verification: Real2Int Float32_FiP32 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for General block Real2Int.

Test results				
Time step	1	2	...	113
CPU cycles	244	244	...	251
Inputs				
In (DSP)	-31	-30.446	...	31
In	-31	-30.446	...	31
Parameters				
Scale	73.5			
Outputs				
Out	-0.422	-0.414	...	0.422
Exp. Out	-0.422	-0.414	...	0.422
Out (DSP)	-905741376	-889567424	...	905741376
Exp. Out (DSP)	-905741403	-889567449	...	905741403

Test settings	
Tolerance Out	±4,6566e-08 (±100 LSB)

Test statistics	
Min CPU cycles	202
Max CPU cycles	251
Avg CPU cycles	247

Test case: Parameter test OK

Parameter test for General block Real2Int.

Test results				
Time step	1	2	...	14
CPU cycles	244	244	...	251
Inputs				
In (DSP)	0.1			
In	0.1			
Parameters				
Scale	-10	-5	...	10
Outputs				
Out	-0.01	-0.02	...	0.01
Exp. Out	-0.01	-0.02	...	0.01
Out (DSP)	-21474838	-42949676	...	21474838
Exp. Out (DSP)	-21474836	-42949673	...	21474836

Test settings	
Tolerance Out	±3,7253e-09 (±8 LSB)

Test statistics	
Min CPU cycles	204
Max CPU cycles	251
Avg CPU cycles	244

Test case: Conversion test **OK**

Conversion test for General block Real2Int.

Test results				
Time step	1	2	...	14
Mask parameters				
Scale	-10	-5	...	10
Controller parameters				
scale	-214748364.8	-429496729.6	...	214748364.8
Exp. scale	-214748364.8	-429496729.6	...	214748364.8

Test settings	
Tolerance scale	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block Real2Int.

Test results				
Time step	1	2	...	14
Mask parameters				
Scale	-10	-5	...	10
Controller parameters				
scale	-214748352	-429496704	...	214748352
Exp. scale	-214748364.8	-429496729.6	...	214748364.8

Test settings	
Tolerance scale	±5,0000e+01

Test statistics	
Min CPU cycles	1083
Max CPU cycles	1083
Avg CPU cycles	1083

Verification: Real2Int Float32_FiP32 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for General block Real2Int.

Test results				
Time step	1	2	...	113
CPU cycles	111	111	...	109
Inputs				
In (DSP)	-31	-30.446	...	31
In	-31	-30.446	...	31
Parameters				
Scale	73.5			
Outputs				
Out	-0.422	-0.414	...	0.422
Exp. Out	-0.422	-0.414	...	0.422
Out (DSP)	-905741376	-889567424	...	905741376
Exp. Out (DSP)	-905741403	-889567449	...	905741403

Test settings	
Tolerance Out	±4,6566e-08 (±100 LSB)

Test statistics	
Min CPU cycles	83
Max CPU cycles	111
Avg CPU cycles	109

Test case: Parameter test OK

Parameter test for General block Real2Int.

Test results				
Time step	1	2	...	14
CPU cycles	111	111	...	109
Inputs				
In (DSP)	0.1			
In	0.1			
Parameters				
Scale	-10	-5	...	10
Outputs				
Out	-0.01	-0.02	...	0.01
Exp. Out	-0.01	-0.02	...	0.01
Out (DSP)	-21474838	-42949676	...	21474838
Exp. Out (DSP)	-21474836	-42949673	...	21474836

Test settings	
Tolerance Out	±3,7253e-09 (±8 LSB)

Test statistics	
Min CPU cycles	103
Max CPU cycles	115
Avg CPU cycles	109

Test case: Conversion test OK

Conversion test for General block Real2Int.

Test results				
Time step	1	2	...	14
Mask parameters				
Scale	-10	-5	...	10
Controller parameters				
scale	-214748364.8	-429496729.6	...	214748364.8
Exp. scale	-214748364.8	-429496729.6	...	214748364.8

Test settings	
Tolerance scale	±0,0000e+00

Test case: Conversion-on-Target test OK

Conversion-on-Target test for General block Real2Int.

Test results				
Time step	1	2	...	14
Mask parameters				
Scale	-10	-5	...	10
Controller parameters				
scale	-214748368	-429496736	...	214748368
Exp. scale	-214748364.8	-429496729.6	...	214748364.8

Test settings	
Tolerance scale	±5,0000e+01

Test statistics	
Min CPU cycles	415
Max CPU cycles	415
Avg CPU cycles	415

Verification: Real2Int Float32_FiP32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for General block Real2Int.

Test results				
Time step	1	2	...	113
CPU cycles	530	530	...	516
Inputs				
In (DSP)	-31	-30.446	...	31
In	-31	-30.446	...	31
Parameters				
Scale	73.5			
Outputs				
Out	-0.422	-0.414	...	0.422
Exp. Out	-0.422	-0.414	...	0.422
Out (DSP)	-905741376	-889567424	...	905741376
Exp. Out (DSP)	-905741403	-889567449	...	905741403

Test settings	
Tolerance Out	±4,6566e-08 (±100 LSB)

Test statistics	
Min CPU cycles	471
Max CPU cycles	569
Avg CPU cycles	523

Test case: Parameter test OK

Parameter test for General block Real2Int.

Test results				
Time step	1	2	...	14
CPU cycles	530	530	...	516
Inputs				
In (DSP)	0.1			
In	0.1			
Parameters				
Scale	-10	-5	...	10
Outputs				
Out	-0.01	-0.02	...	0.01
Exp. Out	-0.01	-0.02	...	0.01
Out (DSP)	-21474838	-42949676	...	21474838
Exp. Out (DSP)	-21474836	-42949673	...	21474836

Test settings	
Tolerance Out	±3,7253e-09 (±8 LSB)

Test statistics	
Min CPU cycles	516
Max CPU cycles	530
Avg CPU cycles	523

Test case: Conversion test **OK**

Conversion test for General block Real2Int.

Test results				
Time step	1	2	...	14
Mask parameters				
Scale	-10	-5	...	10
Controller parameters				
scale	-214748364.8	-429496729.6	...	214748364.8
Exp. scale	-214748364.8	-429496729.6	...	214748364.8

Test settings	
Tolerance scale	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block Real2Int.

Test results				
Time step	1	2	...	14
Mask parameters				
Scale	-10	-5	...	10
Controller parameters				
scale	-214748368	-429496736	...	214748368
Exp. scale	-214748364.8	-429496729.6	...	214748364.8

Test settings	
Tolerance scale	±5,0000e+01

Test statistics	
Min CPU cycles	484
Max CPU cycles	484
Avg CPU cycles	484

Verification: Real2Int Float32_FiP32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for General block Real2Int.

Test results				
Time step	1	2	...	113
CPU cycles	1496	1496	...	1487
Inputs				
In (DSP)	-31	-30.446	...	31
In	-31	-30.446	...	31
Parameters				
Scale	73.5			
Outputs				
Out	-0.422	-0.414	...	0.422
Exp. Out	-0.422	-0.414	...	0.422
Out (DSP)	-905741376	-889567424	...	905741376
Exp. Out (DSP)	-905741403	-889567449	...	905741403

Test settings	
Tolerance Out	±4,6566e-08 (±100 LSB)

Test statistics	
Min CPU cycles	1174
Max CPU cycles	1556
Avg CPU cycles	1492

Test case: Parameter test OK

Parameter test for General block Real2Int.

Test results				
Time step	1	2	...	14
CPU cycles	1555	1496	...	1487
Inputs				
In (DSP)	0.1			
In	0.1			
Parameters				
Scale	-10	-5	...	10
Outputs				
Out	-0.01	-0.02	...	0.01
Exp. Out	-0.01	-0.02	...	0.01
Out (DSP)	-21474838	-42949676	...	21474838
Exp. Out (DSP)	-21474836	-42949673	...	21474836

Test settings	
Tolerance Out	±3,7253e-09 (±8 LSB)

Test statistics	
Min CPU cycles	1487
Max CPU cycles	1624
Avg CPU cycles	1515

Test case: Conversion test **OK**

Conversion test for General block Real2Int.

Test results				
Time step	1	2	...	14
Mask parameters				
Scale	-10	-5	...	10
Controller parameters				
scale	-214748364.8	-429496729.6	...	214748364.8
Exp. scale	-214748364.8	-429496729.6	...	214748364.8

Test settings	
Tolerance scale	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block Real2Int.

Test results				
Time step	1	2	...	14
Mask parameters				
Scale	-10	-5	...	10
Controller parameters				
scale	-214748368	-429496736	...	214748368
Exp. scale	-214748364.8	-429496729.6	...	214748364.8

Test settings	
Tolerance scale	±5,0000e+01

Test statistics	
Min CPU cycles	1254
Max CPU cycles	1314
Avg CPU cycles	1266

Verification: Real2Int Float32_FiP32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for General block Real2Int.

Test results				
Time step	1	2	...	113
CPU cycles	471	472	...	466
Inputs				
In (DSP)	-31	-30.446	...	31
In	-31	-30.446	...	31
Parameters				
Scale	73.5			
Outputs				
Out	-0.422	-0.414	...	0.422
Exp. Out	-0.422	-0.414	...	0.422
Out (DSP)	-905741376	-889567424	...	905741376
Exp. Out (DSP)	-905741403	-889567449	...	905741403

Test settings	
Tolerance Out	±4,6566e-08 (±100 LSB)

Test statistics	
Min CPU cycles	379
Max CPU cycles	474
Avg CPU cycles	468

Test case: Parameter test OK

Parameter test for General block Real2Int.

Test results				
Time step	1	2	...	14
CPU cycles	472	472	...	467
Inputs				
In (DSP)	0.1			
In	0.1			
Parameters				
Scale	-10	-5	...	10
Outputs				
Out	-0.01	-0.02	...	0.01
Exp. Out	-0.01	-0.02	...	0.01
Out (DSP)	-21474838	-42949676	...	21474838
Exp. Out (DSP)	-21474836	-42949673	...	21474836

Test settings	
Tolerance Out	±3,7253e-09 (±8 LSB)

Test statistics	
Min CPU cycles	466
Max CPU cycles	473
Avg CPU cycles	469

Test case: Conversion test **OK**

Conversion test for General block Real2Int.

Test results				
Time step	1	2	...	14
Mask parameters				
Scale	-10	-5	...	10
Controller parameters				
scale	-214748364.8	-429496729.6	...	214748364.8
Exp. scale	-214748364.8	-429496729.6	...	214748364.8

Test settings	
Tolerance scale	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block Real2Int.

Test results				
Time step	1	2	...	14
Mask parameters				
Scale	-10	-5	...	10
Controller parameters				
scale	-214748368	-429496736	...	214748368
Exp. scale	-214748364.8	-429496729.6	...	214748364.8

Test settings	
Tolerance scale	±5,0000e+01

Test statistics	
Min CPU cycles	396
Max CPU cycles	422
Avg CPU cycles	409

Verification: Real2Int Float32_FiP32 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for General block Real2Int.

Test results				
Time step	1	2	...	113
CPU cycles	325	329	...	324
Inputs				
In (DSP)	-31	-30.446	...	31
In	-31	-30.446	...	31
Parameters				
Scale	73.5			
Outputs				
Out	-0.422	-0.414	...	0.422
Exp. Out	-0.422	-0.414	...	0.422
Out (DSP)	-905741376	-889567424	...	905741376
Exp. Out (DSP)	-905741403	-889567449	...	905741403

Test settings	
Tolerance Out	±4,6566e-08 (±100 LSB)

Test statistics	
Min CPU cycles	223
Max CPU cycles	329
Avg CPU cycles	316

Test case: Parameter test OK

Parameter test for General block Real2Int.

Test results				
Time step	1	2	...	14
CPU cycles	284	293	...	283
Inputs				
In (DSP)	0.1			
In	0.1			
Parameters				
Scale	-10	-5	...	10
Outputs				
Out	-0.01	-0.02	...	0.01
Exp. Out	-0.01	-0.02	...	0.01
Out (DSP)	-21474838	-42949676	...	21474838
Exp. Out (DSP)	-21474836	-42949673	...	21474836

Test settings	
Tolerance Out	±3,7253e-09 (±8 LSB)

Test statistics	
Min CPU cycles	283
Max CPU cycles	344
Avg CPU cycles	311

Test case: Conversion test **OK**

Conversion test for General block Real2Int.

Test results				
Time step	1	2	...	14
Mask parameters				
Scale	-10	-5	...	10
Controller parameters				
scale	-214748364.8	-429496729.6	...	214748364.8
Exp. scale	-214748364.8	-429496729.6	...	214748364.8

Test settings	
Tolerance scale	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block Real2Int.

Test results				
Time step	1	2	...	14
Mask parameters				
Scale	-10	-5	...	10
Controller parameters				
scale	-214748368	-429496736	...	214748368
Exp. scale	-214748364.8	-429496729.6	...	214748364.8

Test settings	
Tolerance scale	±5,0000e+01

Test statistics	
Min CPU cycles	1305
Max CPU cycles	1369
Avg CPU cycles	1331

Verification: Real2Int Float32_FiP32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for General block Real2Int.

Test results				
Time step	1	2	...	113
CPU cycles	455	341	...	326
Inputs				
In (DSP)	-31	-30.446	...	31
In	-31	-30.446	...	31
Parameters				
Scale	73.5			
Outputs				
Out	-0.422	-0.414	...	0.422
Exp. Out	-0.422	-0.414	...	0.422
Out (DSP)	-905741376	-889567424	...	905741376
Exp. Out (DSP)	-905741403	-889567449	...	905741403

Test settings	
Tolerance Out	±4,6566e-08 (±100 LSB)

Test statistics	
Min CPU cycles	319
Max CPU cycles	455
Avg CPU cycles	334

Test case: Parameter test OK

Parameter test for General block Real2Int.

Test results				
Time step	1	2	...	14
CPU cycles	356	356	...	341
Inputs				
In (DSP)	0.1			
In	0.1			
Parameters				
Scale	-10	-5	...	10
Outputs				
Out	-0.01	-0.02	...	0.01
Exp. Out	-0.01	-0.02	...	0.01
Out (DSP)	-21474838	-42949676	...	21474838
Exp. Out (DSP)	-21474836	-42949673	...	21474836

Test settings	
Tolerance Out	±3,7253e-09 (±8 LSB)

Test statistics	
Min CPU cycles	341
Max CPU cycles	356
Avg CPU cycles	348

Test case: Conversion test OK

Conversion test for General block Real2Int.

Test results				
Time step	1	2	...	14
Mask parameters				
Scale	-10	-5	...	10
Controller parameters				
scale	-214748364.8	-429496729.6	...	214748364.8
Exp. scale	-214748364.8	-429496729.6	...	214748364.8

Test settings	
Tolerance scale	±0,0000e+00

Test case: Conversion-on-Target test OK

Conversion-on-Target test for General block Real2Int.

Test results				
Time step	1	2	...	14
Mask parameters				
Scale	-10	-5	...	10
Controller parameters				
scale	-214748368	-429496736	...	214748368
Exp. scale	-214748364.8	-429496729.6	...	214748364.8

Test settings	
Tolerance scale	±5,0000e+01

Test statistics	
Min CPU cycles	403
Max CPU cycles	448
Avg CPU cycles	406

Verification: Real2Int Float32_FiP32 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for General block Real2Int.

Test results				
Time step	1	2	...	113
CPU cycles	204	204	...	212
Inputs				
In (DSP)	-31	-30.446	...	31
In	-31	-30.446	...	31
Parameters				
Scale	73.5			
Outputs				
Out	-0.422	-0.414	...	0.422
Exp. Out	-0.422	-0.414	...	0.422
Out (DSP)	-905741376	-889567424	...	905741376
Exp. Out (DSP)	-905741403	-889567449	...	905741403

Test settings	
Tolerance Out	±4,6566e-08 (±100 LSB)

Test statistics	
Min CPU cycles	172
Max CPU cycles	212
Avg CPU cycles	207

Test case: Parameter test OK

Parameter test for General block Real2Int.

Test results				
Time step	1	2	...	14
CPU cycles	204	204	...	212
Inputs				
In (DSP)	0.1			
In	0.1			
Parameters				
Scale	-10	-5	...	10
Outputs				
Out	-0.01	-0.02	...	0.01
Exp. Out	-0.01	-0.02	...	0.01
Out (DSP)	-21474838	-42949676	...	21474838
Exp. Out (DSP)	-21474836	-42949673	...	21474836

Test settings	
Tolerance Out	±3,7253e-09 (±8 LSB)

Test statistics	
Min CPU cycles	174
Max CPU cycles	212
Avg CPU cycles	205

Test case: Conversion test **OK**

Conversion test for General block Real2Int.

Test results				
Time step	1	2	...	14
Mask parameters				
Scale	-10	-5	...	10
Controller parameters				
scale	-214748364.8	-429496729.6	...	214748364.8
Exp. scale	-214748364.8	-429496729.6	...	214748364.8

Test settings	
Tolerance scale	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block Real2Int.

Test results				
Time step	1	2	...	14
Mask parameters				
Scale	-10	-5	...	10
Controller parameters				
scale	-214748352	-429496704	...	214748352
Exp. scale	-214748364.8	-429496729.6	...	214748364.8

Test settings	
Tolerance scale	±5,0000e+01

Test statistics	
Min CPU cycles	879
Max CPU cycles	879
Avg CPU cycles	879

Verification: Real2Int Float32_Bool CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for General block Real2Int.

Test results				
Time step	1	2	...	5
CPU cycles	61	61	...	61
Inputs				
In (DSP)	3.1	0.31	...	3.3
In	3.1	0.31	...	3.3
Parameters				
Scale	7.35			
Outputs				
Out	1	1	...	1
Exp. Out	1	1	...	1
Out (DSP)	1	1	...	1
Exp. Out (DSP)	1	1	...	1

Test settings	
Tolerance Out	±4,6566e-10 (±0 LSB)

Test statistics	
Min CPU cycles	61
Max CPU cycles	61
Avg CPU cycles	61

Test case: Parameter test OK

Parameter test for General block Real2Int.

Test results				
Time step	1	2	...	14
CPU cycles	61	61	...	61
Inputs				
In (DSP)	0.1			
In	0.1			
Parameters				
Scale	-10	-5	...	10
Outputs				
Out	1	1	...	1
Exp. Out	1	1	...	1
Out (DSP)	1	1	...	1
Exp. Out (DSP)	1	1	...	1

Test settings	
Tolerance Out	±4,6566e-10 (±0 LSB)

Test statistics	
Min CPU cycles	61
Max CPU cycles	61
Avg CPU cycles	61

Verification: Real2Int Float32_Bool CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for General block Real2Int.

Test results				
Time step	1	2	...	5
CPU cycles	29	29	...	29
Inputs				
In (DSP)	3.1	0.31	...	3.3
In	3.1	0.31	...	3.3
Parameters				
Scale	7.35			
Outputs				
Out	1	1	...	1
Exp. Out	1	1	...	1
Out (DSP)	1	1	...	1
Exp. Out (DSP)	1	1	...	1

Test settings	
Tolerance Out	±4,6566e-10 (±0 LSB)

Test statistics	
Min CPU cycles	29
Max CPU cycles	29
Avg CPU cycles	29

Test case: Parameter test OK

Parameter test for General block Real2Int.

Test results				
Time step	1	2	...	14
CPU cycles	29	29	...	29
Inputs				
In (DSP)	0.1			
In	0.1			
Parameters				
Scale	-10	-5	...	10
Outputs				
Out	1	1	...	1
Exp. Out	1	1	...	1
Out (DSP)	1	1	...	1
Exp. Out (DSP)	1	1	...	1

Test settings	
Tolerance Out	±4,6566e-10 (±0 LSB)

Test statistics	
Min CPU cycles	29
Max CPU cycles	29
Avg CPU cycles	29

Verification: Real2Int Float32_Bool CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for General block Real2Int.

Test results				
Time step	1	2	...	5
CPU cycles	67	67	...	67
Inputs				
In (DSP)	3.1	0.31	...	3.3
In	3.1	0.31	...	3.3
Parameters				
Scale	7.35			
Outputs				
Out	1	1	...	1
Exp. Out	1	1	...	1
Out (DSP)	1	1	...	1
Exp. Out (DSP)	1	1	...	1

Test settings	
Tolerance Out	±4,6566e-10 (±0 LSB)

Test statistics	
Min CPU cycles	67
Max CPU cycles	67
Avg CPU cycles	67

Test case: Parameter test OK

Parameter test for General block Real2Int.

Test results				
Time step	1	2	...	14
CPU cycles	67	67	...	67
Inputs				
In (DSP)	0.1			
In	0.1			
Parameters				
Scale	-10	-5	...	10
Outputs				
Out	1	1	...	1
Exp. Out	1	1	...	1
Out (DSP)	1	1	...	1
Exp. Out (DSP)	1	1	...	1

Test settings	
Tolerance Out	±4,6566e-10 (±0 LSB)

Test statistics	
Min CPU cycles	67
Max CPU cycles	67
Avg CPU cycles	67

Verification: Real2Int Float32_Bool CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for General block Real2Int.

Test results				
Time step	1	2	...	5
CPU cycles	132	132	...	132
Inputs				
In (DSP)	3.1	0.31	...	3.3
In	3.1	0.31	...	3.3
Parameters				
Scale	7.35			
Outputs				
Out	1	1	...	1
Exp. Out	1	1	...	1
Out (DSP)	1	1	...	1
Exp. Out (DSP)	1	1	...	1

Test settings	
Tolerance Out	±4,6566e-10 (±0 LSB)

Test statistics	
Min CPU cycles	127
Max CPU cycles	132
Avg CPU cycles	131

Test case: Parameter test OK

Parameter test for General block Real2Int.

Test results				
Time step	1	2	...	14
CPU cycles	132	132	...	132
Inputs				
In (DSP)	0.1			
In	0.1			
Parameters				
Scale	-10	-5	...	10
Outputs				
Out	1	1	...	1
Exp. Out	1	1	...	1
Out (DSP)	1	1	...	1
Exp. Out (DSP)	1	1	...	1

Test settings	
Tolerance Out	±4,6566e-10 (±0 LSB)

Test statistics	
Min CPU cycles	132
Max CPU cycles	132
Avg CPU cycles	132

Verification: Real2Int Float32_Bool CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for General block Real2Int.

Test results				
Time step	1	2	...	5
CPU cycles	74	74	...	74
Inputs				
In (DSP)	3.1	0.31	...	3.3
In	3.1	0.31	...	3.3
Parameters				
Scale	7.35			
Outputs				
Out	1	1	...	1
Exp. Out	1	1	...	1
Out (DSP)	1	1	...	1
Exp. Out (DSP)	1	1	...	1

Test settings	
Tolerance Out	±4,6566e-10 (±0 LSB)

Test statistics	
Min CPU cycles	50
Max CPU cycles	74
Avg CPU cycles	69

Test case: Parameter test OK

Parameter test for General block Real2Int.

Test results				
Time step	1	2	...	14
CPU cycles	74	74	...	74
Inputs				
In (DSP)	0.1			
In	0.1			
Parameters				
Scale	-10	-5	...	10
Outputs				
Out	1	1	...	1
Exp. Out	1	1	...	1
Out (DSP)	1	1	...	1
Exp. Out (DSP)	1	1	...	1

Test settings	
Tolerance Out	±4,6566e-10 (±0 LSB)

Test statistics	
Min CPU cycles	74
Max CPU cycles	74
Avg CPU cycles	74

Verification: Real2Int Float32_Bool CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test

OK

Inport test for General block Real2Int.

Test results				
Time step	1	2	...	5
CPU cycles	151	151	...	151
Inputs				
In (DSP)	3.1	0.31	...	3.3
In	3.1	0.31	...	3.3
Parameters				
Scale	7.35			
Outputs				
Out	1	1	...	1
Exp. Out	1	1	...	1
Out (DSP)	1	1	...	1
Exp. Out (DSP)	1	1	...	1

Test settings	
Tolerance Out	±4,6566e-10 (±0 LSB)

Test statistics	
Min CPU cycles	151
Max CPU cycles	155
Avg CPU cycles	151

Test case: Parameter test

OK

Parameter test for General block Real2Int.

Test results				
Time step	1	2	...	14
CPU cycles	151	151	...	151
Inputs				
In (DSP)	0.1			
In	0.1			
Parameters				
Scale	-10	-5	...	10
Outputs				
Out	1	1	...	1
Exp. Out	1	1	...	1
Out (DSP)	1	1	...	1
Exp. Out (DSP)	1	1	...	1

Test settings	
Tolerance Out	±4,6566e-10 (±0 LSB)

Test statistics	
Min CPU cycles	151
Max CPU cycles	151
Avg CPU cycles	151

Verification: Real2Int Float32_Bool CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for General block Real2Int.

Test results				
Time step	1	2	...	5
CPU cycles	70	70	...	70
Inputs				
In (DSP)	3.1	0.31	...	3.3
In	3.1	0.31	...	3.3
Parameters				
Scale	7.35			
Outputs				
Out	1	1	...	1
Exp. Out	1	1	...	1
Out (DSP)	1	1	...	1
Exp. Out (DSP)	1	1	...	1

Test settings	
Tolerance Out	±4,6566e-10 (±0 LSB)

Test statistics	
Min CPU cycles	70
Max CPU cycles	70
Avg CPU cycles	70

Test case: Parameter test OK

Parameter test for General block Real2Int.

Test results				
Time step	1	2	...	14
CPU cycles	70	70	...	70
Inputs				
In (DSP)	0.1			
In	0.1			
Parameters				
Scale	-10	-5	...	10
Outputs				
Out	1	1	...	1
Exp. Out	1	1	...	1
Out (DSP)	1	1	...	1
Exp. Out (DSP)	1	1	...	1

Test settings	
Tolerance Out	±4,6566e-10 (±0 LSB)

Test statistics	
Min CPU cycles	70
Max CPU cycles	70
Avg CPU cycles	70

Verification: Real2Int Float32_Bool CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for General block Real2Int.

Test results				
Time step	1	2	...	5
CPU cycles	43	43	...	43
Inputs				
In (DSP)	3.1	0.31	...	3.3
In	3.1	0.31	...	3.3
Parameters				
Scale	7.35			
Outputs				
Out	1	1	...	1
Exp. Out	1	1	...	1
Out (DSP)	1	1	...	1
Exp. Out (DSP)	1	1	...	1

Test settings	
Tolerance Out	±4,6566e-10 (±0 LSB)

Test statistics	
Min CPU cycles	43
Max CPU cycles	43
Avg CPU cycles	43

Test case: Parameter test OK

Parameter test for General block Real2Int.

Test results				
Time step	1	2	...	14
CPU cycles	43	43	...	43
Inputs				
In (DSP)	0.1			
In	0.1			
Parameters				
Scale	-10	-5	...	10
Outputs				
Out	1	1	...	1
Exp. Out	1	1	...	1
Out (DSP)	1	1	...	1
Exp. Out (DSP)	1	1	...	1

Test settings	
Tolerance Out	±4,6566e-10 (±0 LSB)

Test statistics	
Min CPU cycles	43
Max CPU cycles	43
Avg CPU cycles	43

Block: Saturation



Saturation of output to adjustable upper and lower limit.

Inports	
In	Input

Outports	
Out	Limited output

Mask Parameters		
Name	**ID**	**Description**
max	1	Upper Limit
min	2	Lower Limit

Description:

If the entry for *Upper Limit* is lower than the entry for *Lower Limit* then the limits will be swapped internally.

Implementations:

FiP16 16 Bit Fixed Point Implementation
FiP32 32 Bit Fixed Point Implementation
Float32 32 Bit Floating Point Implementation
Float64 64 Bit Floating Point Implementation

Implementation: FiP16

16 Bit Fixed Point Implementation

Inports Data Type	
In	int16

Outports Data Type	
Out	int16

Implementation: FiP32

32 Bit Fixed Point Implementation

Inports Data Type	
In	int32

Outports Data Type	
Out	int32

Implementation: Float32

32 Bit Floating Point Implementation

Inports Data Type	
In	float32

Outports Data Type	
Out	float32

Implementation: Float64

64 Bit Floating Point Implementation

Inports Data Type	
In	float64

Outports Data Type	
Out	float64

Verification: Saturation FiP16 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for General block Saturation.

Test results						
Time step	1	2	3	4	...	137
CPU cycles	64	64	64	64	...	64
Inputs						
In (DSP)	0	-1513	-3023	-4527	...	0
In	-0	-0.046	-0.092	-0.138	...	0
Parameters						
max	0.8					
min	-0.3					
Outputs						
Out	0	-0.046	-0.092	-0.138	...	0
Exp. Out	-0	-0.046	-0.092	-0.138	...	0
Out (DSP)	0	-1513	-3023	-4527	...	0
Exp. Out (DSP)	0	-1513	-3023	-4527	...	0

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	64
Max CPU cycles	64
Avg CPU cycles	64

Verification: Saturation FiP16 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for General block Saturation.

Test results						
Time step	1	2	3	4	...	137
CPU cycles	33	33	33	33	...	33
Inputs						
In (DSP)	0	-1513	-3023	-4527	...	0
In	-0	-0.046	-0.092	-0.138	...	0
Parameters						
max	0.8					
min	-0.3					
Outputs						
Out	0	-0.046	-0.092	-0.138	...	0
Exp. Out	-0	-0.046	-0.092	-0.138	...	0
Out (DSP)	0	-1513	-3023	-4527	...	0
Exp. Out (DSP)	0	-1513	-3023	-4527	...	0

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	29
Max CPU cycles	33
Avg CPU cycles	32

Verification: Saturation FiP16 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for General block Saturation.

Test results						
Time step	1	2	3	4	...	137
CPU cycles	63	63	63	63	...	63
Inputs						
In (DSP)	0	-1513	-3023	-4527	...	0
In	-0	-0.046	-0.092	-0.138	...	0
Parameters						
max	0.8					
min	-0.3					
Outputs						
Out	0	-0.046	-0.092	-0.138	...	0
Exp. Out	-0	-0.046	-0.092	-0.138	...	0
Out (DSP)	0	-1513	-3023	-4527	...	0
Exp. Out (DSP)	0	-1513	-3023	-4527	...	0

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	63
Max CPU cycles	70
Avg CPU cycles	65

Verification: Saturation FiP16 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for General block Saturation.

Test results						
Time step	1	2	3	4	...	137
CPU cycles	59	59	59	59	...	59
Inputs						
In (DSP)	0	-1513	-3023	-4527	...	0
In	-0	-0.046	-0.092	-0.138	...	0
Parameters						
max	0.8					
min	-0.3					
Outputs						
Out	0	-0.046	-0.092	-0.138	...	0
Exp. Out	-0	-0.046	-0.092	-0.138	...	0
Out (DSP)	0	-1513	-3023	-4527	...	0
Exp. Out (DSP)	0	-1513	-3023	-4527	...	0

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	57
Max CPU cycles	59
Avg CPU cycles	58

Verification: Saturation FiP16 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for General block Saturation.

Test results						
Time step	1	2	3	4	...	137
CPU cycles	38	38	38	38	...	38
Inputs						
In (DSP)	0	-1513	-3023	-4527	...	0
In	-0	-0.046	-0.092	-0.138	...	0
Parameters						
max	0.8					
min	-0.3					
Outputs						
Out	0	-0.046	-0.092	-0.138	...	0
Exp. Out	-0	-0.046	-0.092	-0.138	...	0
Out (DSP)	0	-1513	-3023	-4527	...	0
Exp. Out (DSP)	0	-1513	-3023	-4527	...	0

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	34
Max CPU cycles	40
Avg CPU cycles	38

Verification: Saturation FiP16 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for General block Saturation.

Test results						
Time step	1	2	3	4	...	137
CPU cycles	50	50	50	50	...	50
Inputs						
In (DSP)	0	-1513	-3023	-4527	...	0
In	-0	-0.046	-0.092	-0.138	...	0
Parameters						
max	0.8					
min	-0.3					
Outputs						
Out	0	-0.046	-0.092	-0.138	...	0
Exp. Out	-0	-0.046	-0.092	-0.138	...	0
Out (DSP)	0	-1513	-3023	-4527	...	0
Exp. Out (DSP)	0	-1513	-3023	-4527	...	0

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	48
Max CPU cycles	50
Avg CPU cycles	48

Verification: Saturation FiP16 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for General block Saturation.

Test results						
Time step	1	2	3	4	...	137
CPU cycles	75	64	64	64	...	64
Inputs						
In (DSP)	0	-1513	-3023	-4527	...	0
In	-0	-0.046	-0.092	-0.138	...	0
Parameters						
max	0.8					
min	-0.3					
Outputs						
Out	0	-0.046	-0.092	-0.138	...	0
Exp. Out	-0	-0.046	-0.092	-0.138	...	0
Out (DSP)	0	-1513	-3023	-4527	...	0
Exp. Out (DSP)	0	-1513	-3023	-4527	...	0

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	59
Max CPU cycles	75
Avg CPU cycles	63

Verification: Saturation FiP16 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test

OK

Inport test for General block Saturation.

Test results						
Time step	1	2	3	4	...	137
CPU cycles	44	44	44	44	...	44
Inputs						
In (DSP)	0	-1513	-3023	-4527	...	0
In	-0	-0.046	-0.092	-0.138	...	0
Parameters						
max	0.8					
min	-0.3					
Outputs						
Out	0	-0.046	-0.092	-0.138	...	0
Exp. Out	-0	-0.046	-0.092	-0.138	...	0
Out (DSP)	0	-1513	-3023	-4527	...	0
Exp. Out (DSP)	0	-1513	-3023	-4527	...	0

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	44
Max CPU cycles	52
Avg CPU cycles	45

Verification: Saturation FiP32 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for General block Saturation.

Test results				
Time step	1	2	...	137
CPU cycles	68	68	...	68
Inputs				
In (DSP)	0	-99178222	...	0
In	-0	-0.046	...	0
Parameters				
max	0.8			
min	-0.3			
Outputs				
Out	0	-0.046	...	0
Exp. Out	-0	-0.046	...	0
Out (DSP)	0	-99178222	...	0
Exp. Out (DSP)	0	-99178222	...	0

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	63
Max CPU cycles	70
Avg CPU cycles	67

Verification: Saturation FiP32 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for General block Saturation.

Test results				
Time step	1	2	...	137
CPU cycles	31	31	...	31
Inputs				
In (DSP)	0	-99178222	...	0
In	-0	-0.046	...	0
Parameters				
max	0.8			
min	-0.3			
Outputs				
Out	0	-0.046	...	0
Exp. Out	-0	-0.046	...	0
Out (DSP)	0	-99178222	...	0
Exp. Out (DSP)	0	-99178222	...	0

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	27
Max CPU cycles	31
Avg CPU cycles	30

Verification: Saturation FiP32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for General block Saturation.

Test results				
Time step	1	2	...	137
CPU cycles	62	62	...	62
Inputs				
In (DSP)	0	-99178222	...	0
In	-0	-0.046	...	0
Parameters				
max	0.8			
min	-0.3			
Outputs				
Out	0	-0.046	...	0
Exp. Out	-0	-0.046	...	0
Out (DSP)	0	-99178222	...	0
Exp. Out (DSP)	0	-99178222	...	0

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	62
Max CPU cycles	62
Avg CPU cycles	62

Verification: Saturation FiP32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for General block Saturation.

Test results				
Time step	1	2	...	137
CPU cycles	56	56	...	56
Inputs				
In (DSP)	0	-99178222	...	0
In	-0	-0.046	...	0
Parameters				
max	0.8			
min	-0.3			
Outputs				
Out	0	-0.046	...	0
Exp. Out	-0	-0.046	...	0
Out (DSP)	0	-99178222	...	0
Exp. Out (DSP)	0	-99178222	...	0

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	54
Max CPU cycles	56
Avg CPU cycles	55

Verification: Saturation FiP32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for General block Saturation.

Test results				
Time step	1	2	...	137
CPU cycles	38	38	...	38
Inputs				
In (DSP)	0	-99178222	...	0
In	-0	-0.046	...	0
Parameters				
max	0.8			
min	-0.3			
Outputs				
Out	0	-0.046	...	0
Exp. Out	-0	-0.046	...	0
Out (DSP)	0	-99178222	...	0
Exp. Out (DSP)	0	-99178222	...	0

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	34
Max CPU cycles	40
Avg CPU cycles	38

Verification: Saturation FiP32 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for General block Saturation.

Test results				
Time step	1	2	...	137
CPU cycles	56	56	...	56
Inputs				
In (DSP)	0	-99178222	...	0
In	-0	-0.046	...	0
Parameters				
max	0.8			
min	-0.3			
Outputs				
Out	0	-0.046	...	0
Exp. Out	-0	-0.046	...	0
Out (DSP)	0	-99178222	...	0
Exp. Out (DSP)	0	-99178222	...	0

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	53
Max CPU cycles	56
Avg CPU cycles	55

Verification: Saturation FiP32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for General block Saturation.

Test results				
Time step	1	2	...	137
CPU cycles	61	61	...	61
Inputs				
In (DSP)	0	-99178222	...	0
In	-0	-0.046	...	0
Parameters				
max	0.8			
min	-0.3			
Outputs				
Out	0	-0.046	...	0
Exp. Out	-0	-0.046	...	0
Out (DSP)	0	-99178222	...	0
Exp. Out (DSP)	0	-99178222	...	0

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	57
Max CPU cycles	61
Avg CPU cycles	60

Verification: Saturation FiP32 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for General block Saturation.

Test results				
Time step	1	2	...	137
CPU cycles	48	48	...	48
Inputs				
In (DSP)	0	-99178222	...	0
In	-0	-0.046	...	0
Parameters				
max	0.8			
min	-0.3			
Outputs				
Out	0	-0.046	...	0
Exp. Out	-0	-0.046	...	0
Out (DSP)	0	-99178222	...	0
Exp. Out (DSP)	0	-99178222	...	0

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	46
Max CPU cycles	53
Avg CPU cycles	49

Verification: Saturation Float32 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for General block Saturation.

Test results				
Time step	1	2	...	137
CPU cycles	70	70	...	70
Inputs				
In (DSP)	-0	-0.046	...	0
In	-0	-0.046	...	0
Parameters				
max	0.8			
min	-0.3			
Outputs				
Out	-0	-0.046	...	0
Exp. Out	-0	-0.046	...	0
Out (DSP)	-0	-0.046	...	0
Exp. Out (DSP)	-0	-0.046	...	0

Test settings	
Tolerance Out	±2,7940e-08 (±60 LSB)

Test statistics	
Min CPU cycles	66
Max CPU cycles	70
Avg CPU cycles	69

Verification: Saturation Float32 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for General block Saturation.

Test results				
Time step	1	2	...	137
CPU cycles	39	39	...	39
Inputs				
In (DSP)	-0	-0.046	...	0
In	-0	-0.046	...	0
Parameters				
max	0.8			
min	-0.3			
Outputs				
Out	-0	-0.046	...	0
Exp. Out	-0	-0.046	...	0
Out (DSP)	-0	-0.046	...	0
Exp. Out (DSP)	-0	-0.046	...	0

Test settings	
Tolerance Out	±2,7940e-08 (±60 LSB)

Test statistics	
Min CPU cycles	33
Max CPU cycles	39
Avg CPU cycles	37

Verification: Saturation Float32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for General block Saturation.

Test results				
Time step	1	2	...	137
CPU cycles	73	73	...	73
Inputs				
In (DSP)	-0	-0.046	...	0
In	-0	-0.046	...	0
Parameters				
max	0.8			
min	-0.3			
Outputs				
Out	-0	-0.046	...	0
Exp. Out	-0	-0.046	...	0
Out (DSP)	-0	-0.046	...	0
Exp. Out (DSP)	-0	-0.046	...	0

Test settings	
Tolerance Out	±2,7940e-08 (±60 LSB)

Test statistics	
Min CPU cycles	73
Max CPU cycles	77
Avg CPU cycles	75

Verification: Saturation Float32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for General block Saturation.

Test results				
Time step	1	2	...	137
CPU cycles	223	223	...	229
Inputs				
In (DSP)	-0	-0.046	...	0
In	-0	-0.046	...	0
Parameters				
max	0.8			
min	-0.3			
Outputs				
Out	-0	-0.046	...	0
Exp. Out	-0	-0.046	...	0
Out (DSP)	-0	-0.046	...	0
Exp. Out (DSP)	-0	-0.046	...	0

Test settings	
Tolerance Out	±2,7940e-08 (±60 LSB)

Test statistics	
Min CPU cycles	154
Max CPU cycles	290
Avg CPU cycles	214

Verification: Saturation Float32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for General block Saturation.

Test results				
Time step	1	2	...	137
CPU cycles	124	124	...	122
Inputs				
In (DSP)	-0	-0.046	...	0
In	-0	-0.046	...	0
Parameters				
max	0.8			
min	-0.3			
Outputs				
Out	-0	-0.046	...	0
Exp. Out	-0	-0.046	...	0
Out (DSP)	-0	-0.046	...	0
Exp. Out (DSP)	-0	-0.046	...	0

Test settings	
Tolerance Out	±2,7940e-08 (±60 LSB)

Test statistics	
Min CPU cycles	86
Max CPU cycles	125
Avg CPU cycles	116

Verification: Saturation Float32 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for General block Saturation.

Test results				
Time step	1	2	...	137
CPU cycles	260	260	...	260
Inputs				
In (DSP)	-0	-0.046	...	0
In	-0	-0.046	...	0
Parameters				
max	0.8			
min	-0.3			
Outputs				
Out	-0	-0.046	...	0
Exp. Out	-0	-0.046	...	0
Out (DSP)	-0	-0.046	...	0
Exp. Out (DSP)	-0	-0.046	...	0

Test settings	
Tolerance Out	±2,7940e-08 (±60 LSB)

Test statistics	
Min CPU cycles	164
Max CPU cycles	264
Avg CPU cycles	241

Verification: Saturation Float32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for General block Saturation.

Test results				
Time step	1	2	...	137
CPU cycles	76	64	...	64
Inputs				
In (DSP)	-0	-0.046	...	0
In	-0	-0.046	...	0
Parameters				
max	0.8			
min	-0.3			
Outputs				
Out	-0	-0.046	...	0
Exp. Out	-0	-0.046	...	0
Out (DSP)	-0	-0.046	...	0
Exp. Out (DSP)	-0	-0.046	...	0

Test settings	
Tolerance Out	±2,7940e-08 (±60 LSB)

Test statistics	
Min CPU cycles	61
Max CPU cycles	76
Avg CPU cycles	63

Verification: Saturation Float32 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for General block Saturation.

Test results				
Time step	1	2	...	137
CPU cycles	55	55	...	55
Inputs				
In (DSP)	-0	-0.046	...	0
In	-0	-0.046	...	0
Parameters				
max	0.8			
min	-0.3			
Outputs				
Out	-0	-0.046	...	0
Exp. Out	-0	-0.046	...	0
Out (DSP)	-0	-0.046	...	0
Exp. Out (DSP)	-0	-0.046	...	0

Test settings	
Tolerance Out	±2,7940e-08 (±60 LSB)

Test statistics	
Min CPU cycles	53
Max CPU cycles	55
Avg CPU cycles	54

Block: SaveSignal



Makes the incoming signal accessible for reading with parameter numbers.

Inports	
In	Input signal to be saved

Implementations:

Bool	Boolean Implementation
FiP8	8 Bit Fixed Point Implementation
FiP16	16 Bit Fixed Point Implementation
FiP32	32 Bit Fixed Point Implementation
Float32	32 Bit Floating Point Implementation
Float64	64 Bit Floating Point Implementation

Implementation: Bool

Boolean Implementation

Inports Data Type	
In	bool

Implementation: FiP8

8 Bit Fixed Point Implementation

Inports Data Type	
In	int8

Implementation: FiP16

16 Bit Fixed Point Implementation

Inports Data Type	
In	int16

Implementation: FiP32

32 Bit Fixed Point Implementation

Inports Data Type	
In	int32

Implementation: Float32

32 Bit Floating Point Implementation

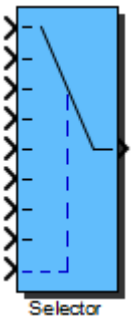
Inports Data Type	
In	float32

Implementation: Float64

64 Bit Floating Point Implementation

Inports Data Type	
In	float64

Block: Selector



Passing through of input signal selected by the select inport:
Select = 0 (DSP): Out = In0
Select = 1 (DSP): Out = In1
...
Select = 7 (DSP): Out = In7

Inports	
In0	Input #0
In1	Input #1
In2	Input #2
In3	Input #3
In4	Input #4
In5	Input #5
In6	Input #6
In7	Input #7
Select	Input select

Outports	
Out	Selected input signal

Implementations:

FiP8	8 Bit Fixed Point Implementation
FiP16	16 Bit Fixed Point Implementation
FiP32	32 Bit Fixed Point Implementation
Float32	32 Bit Floating Point Implementation
Float64	64 Bit Floating Point Implementation

Implementation: FiP8

8 Bit Fixed Point Implementation

Inports Data Type	
In0	int8
In1	int8
In2	int8
In3	int8
In4	int8
In5	int8
In6	int8
In7	int8
Select	int8

Outports Data Type	
Out	int8

Implementation: FiP16

16 Bit Fixed Point Implementation

Inports Data Type	
In0	int16
In1	int16
In2	int16
In3	int16
In4	int16
In5	int16
In6	int16
In7	int16
Select	int8

Outports Data Type	
Out	int16

Implementation: FiP32

32 Bit Fixed Point Implementation

Inports Data Type	
In0	int32
In1	int32
In2	int32
In3	int32
In4	int32
In5	int32
In6	int32
In7	int32
Select	int8

Outports Data Type	
Out	int32

Implementation: Float32

32 Bit Floating Point Implementation

Inports Data Type	
In0	float32
In1	float32
In2	float32
In3	float32
In4	float32
In5	float32
In6	float32
In7	float32
Select	int8

Outports Data Type	
Out	float32

Implementation: Float64

64 Bit Floating Point Implementation

Inports Data Type	
In0	float64
In1	float64
In2	float64
In3	float64
In4	float64
In5	float64
In6	float64
In7	float64
Select	int8

Outports Data Type	
Out	float64

Verification: Selector FiP16 CPU TMS320F28335

Date of Test 2026-06-19

Target controller TMS320F28335

Test case: Inport test OK

Inport test for General block Selector.

Test results						
Time step	1	2	3	4	...	16
CPU cycles	68	68	68	68	...	68
Inputs						
In0 (DSP)	3277	-3277	3277	-3277	...	-3277
In1 (DSP)	6554	-6554	6554	-6554	...	-6554
In2 (DSP)	9830	-9830	9830	-9830	...	-9830
In3 (DSP)	13107	-13107	13107	-13107	...	-13107
In4 (DSP)	16384	-16384	16384	-16384	...	-16384
In5 (DSP)	19661	-19661	19661	-19661	...	-19661
In6 (DSP)	22938	-22938	22938	-22938	...	-22938
In7 (DSP)	26214	-26214	26214	-26214	...	-26214
Select (DSP)	0	0	1	1	...	7
In0	0.1	-0.1	0.1	-0.1	...	-0.1
In1	0.2	-0.2	0.2	-0.2	...	-0.2
In2	0.3	-0.3	0.3	-0.3	...	-0.3
In3	0.4	-0.4	0.4	-0.4	...	-0.4
In4	0.5	-0.5	0.5	-0.5	...	-0.5
In5	0.6	-0.6	0.6	-0.6	...	-0.6
In6	0.7	-0.7	0.7	-0.7	...	-0.7
In7	0.8	-0.8	0.8	-0.8	...	-0.8
Select	0	0	0.008	0.008	...	0.055
Outputs						
Out	0.1	-0.1	0.2	-0.2	...	-0.8
Exp. Out	0.1	-0.1	0.2	-0.2	...	-0.8
Out (DSP)	3277	-3277	6554	-6554	...	-26214
Exp. Out (DSP)	3277	-3277	6554	-6554	...	-26214

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	68
Max CPU cycles	68
Avg CPU cycles	68

Verification: Selector FiP16 CPU TM4C123GH6

Date of Test 2026-06-19

Target controller TM4C123GH6

Test case: Inport test OK

Inport test for General block Selector.

Test results						
Time step	1	2	3	4	...	16
CPU cycles	29	29	29	29	...	29
Inputs						
In0 (DSP)	3277	-3277	3277	-3277	...	-3277
In1 (DSP)	6554	-6554	6554	-6554	...	-6554
In2 (DSP)	9830	-9830	9830	-9830	...	-9830
In3 (DSP)	13107	-13107	13107	-13107	...	-13107
In4 (DSP)	16384	-16384	16384	-16384	...	-16384
In5 (DSP)	19661	-19661	19661	-19661	...	-19661
In6 (DSP)	22938	-22938	22938	-22938	...	-22938
In7 (DSP)	26214	-26214	26214	-26214	...	-26214
Select (DSP)	0	0	1	1	...	7
In0	0.1	-0.1	0.1	-0.1	...	-0.1
In1	0.2	-0.2	0.2	-0.2	...	-0.2
In2	0.3	-0.3	0.3	-0.3	...	-0.3
In3	0.4	-0.4	0.4	-0.4	...	-0.4
In4	0.5	-0.5	0.5	-0.5	...	-0.5
In5	0.6	-0.6	0.6	-0.6	...	-0.6
In6	0.7	-0.7	0.7	-0.7	...	-0.7
In7	0.8	-0.8	0.8	-0.8	...	-0.8
Select	0	0	0.008	0.008	...	0.055
Outputs						
Out	0.1	-0.1	0.2	-0.2	...	-0.8
Exp. Out	0.1	-0.1	0.2	-0.2	...	-0.8
Out (DSP)	3277	-3277	6554	-6554	...	-26214
Exp. Out (DSP)	3277	-3277	6554	-6554	...	-26214

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	29
Max CPU cycles	29
Avg CPU cycles	29

Verification: Selector FiP16 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for General block Selector.

Test results						
Time step	1	2	3	4	...	16
CPU cycles	62	62	62	62	...	62
Inputs						
In0 (DSP)	3277	-3277	3277	-3277	...	-3277
In1 (DSP)	6554	-6554	6554	-6554	...	-6554
In2 (DSP)	9830	-9830	9830	-9830	...	-9830
In3 (DSP)	13107	-13107	13107	-13107	...	-13107
In4 (DSP)	16384	-16384	16384	-16384	...	-16384
In5 (DSP)	19661	-19661	19661	-19661	...	-19661
In6 (DSP)	22938	-22938	22938	-22938	...	-22938
In7 (DSP)	26214	-26214	26214	-26214	...	-26214
Select (DSP)	0	0	1	1	...	7
In0	0.1	-0.1	0.1	-0.1	...	-0.1
In1	0.2	-0.2	0.2	-0.2	...	-0.2
In2	0.3	-0.3	0.3	-0.3	...	-0.3
In3	0.4	-0.4	0.4	-0.4	...	-0.4
In4	0.5	-0.5	0.5	-0.5	...	-0.5
In5	0.6	-0.6	0.6	-0.6	...	-0.6
In6	0.7	-0.7	0.7	-0.7	...	-0.7
In7	0.8	-0.8	0.8	-0.8	...	-0.8
Select	0	0	0.008	0.008	...	0.055
Outputs						
Out	0.1	-0.1	0.2	-0.2	...	-0.8
Exp. Out	0.1	-0.1	0.2	-0.2	...	-0.8
Out (DSP)	3277	-3277	6554	-6554	...	-26214
Exp. Out (DSP)	3277	-3277	6554	-6554	...	-26214

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	62
Max CPU cycles	62
Avg CPU cycles	62

Verification: Selector FiP16 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for General block Selector.

Test results						
Time step	1	2	3	4	...	16
CPU cycles	55	55	55	55	...	55
Inputs						
In0 (DSP)	3277	-3277	3277	-3277	...	-3277
In1 (DSP)	6554	-6554	6554	-6554	...	-6554
In2 (DSP)	9830	-9830	9830	-9830	...	-9830
In3 (DSP)	13107	-13107	13107	-13107	...	-13107
In4 (DSP)	16384	-16384	16384	-16384	...	-16384
In5 (DSP)	19661	-19661	19661	-19661	...	-19661
In6 (DSP)	22938	-22938	22938	-22938	...	-22938
In7 (DSP)	26214	-26214	26214	-26214	...	-26214
Select (DSP)	0	0	1	1	...	7
In0	0.1	-0.1	0.1	-0.1	...	-0.1
In1	0.2	-0.2	0.2	-0.2	...	-0.2
In2	0.3	-0.3	0.3	-0.3	...	-0.3
In3	0.4	-0.4	0.4	-0.4	...	-0.4
In4	0.5	-0.5	0.5	-0.5	...	-0.5
In5	0.6	-0.6	0.6	-0.6	...	-0.6
In6	0.7	-0.7	0.7	-0.7	...	-0.7
In7	0.8	-0.8	0.8	-0.8	...	-0.8
Select	0	0	0.008	0.008	...	0.055
Outputs						
Out	0.1	-0.1	0.2	-0.2	...	-0.8
Exp. Out	0.1	-0.1	0.2	-0.2	...	-0.8
Out (DSP)	3277	-3277	6554	-6554	...	-26214
Exp. Out (DSP)	3277	-3277	6554	-6554	...	-26214

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	55
Max CPU cycles	55
Avg CPU cycles	55

Verification: Selector FiP16 CPU PIC32MX170F256

Date of Test 2026-06-19

Target controller PIC32MX170F256

Test case: Inport test OK

Inport test for General block Selector.

Test results						
Time step	1	2	3	4	...	16
CPU cycles	36	36	36	36	...	36
Inputs						
In0 (DSP)	3277	-3277	3277	-3277	...	-3277
In1 (DSP)	6554	-6554	6554	-6554	...	-6554
In2 (DSP)	9830	-9830	9830	-9830	...	-9830
In3 (DSP)	13107	-13107	13107	-13107	...	-13107
In4 (DSP)	16384	-16384	16384	-16384	...	-16384
In5 (DSP)	19661	-19661	19661	-19661	...	-19661
In6 (DSP)	22938	-22938	22938	-22938	...	-22938
In7 (DSP)	26214	-26214	26214	-26214	...	-26214
Select (DSP)	0	0	1	1	...	7
In0	0.1	-0.1	0.1	-0.1	...	-0.1
In1	0.2	-0.2	0.2	-0.2	...	-0.2
In2	0.3	-0.3	0.3	-0.3	...	-0.3
In3	0.4	-0.4	0.4	-0.4	...	-0.4
In4	0.5	-0.5	0.5	-0.5	...	-0.5
In5	0.6	-0.6	0.6	-0.6	...	-0.6
In6	0.7	-0.7	0.7	-0.7	...	-0.7
In7	0.8	-0.8	0.8	-0.8	...	-0.8
Select	0	0	0.008	0.008	...	0.055
Outputs						
Out	0.1	-0.1	0.2	-0.2	...	-0.8
Exp. Out	0.1	-0.1	0.2	-0.2	...	-0.8
Out (DSP)	3277	-3277	6554	-6554	...	-26214
Exp. Out (DSP)	3277	-3277	6554	-6554	...	-26214

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	36
Max CPU cycles	36
Avg CPU cycles	36

Verification: Selector FiP16 CPU dsPIC33EP256MC502

Date of Test 2026-06-19

Target controller dsPIC33EP256MC502

Test case: Inport test OK

Inport test for General block Selector.

Test results						
Time step	1	2	3	4	...	16
CPU cycles	48	48	48	48	...	48
Inputs						
In0 (DSP)	3277	-3277	3277	-3277	...	-3277
In1 (DSP)	6554	-6554	6554	-6554	...	-6554
In2 (DSP)	9830	-9830	9830	-9830	...	-9830
In3 (DSP)	13107	-13107	13107	-13107	...	-13107
In4 (DSP)	16384	-16384	16384	-16384	...	-16384
In5 (DSP)	19661	-19661	19661	-19661	...	-19661
In6 (DSP)	22938	-22938	22938	-22938	...	-22938
In7 (DSP)	26214	-26214	26214	-26214	...	-26214
Select (DSP)	0	0	1	1	...	7
In0	0.1	-0.1	0.1	-0.1	...	-0.1
In1	0.2	-0.2	0.2	-0.2	...	-0.2
In2	0.3	-0.3	0.3	-0.3	...	-0.3
In3	0.4	-0.4	0.4	-0.4	...	-0.4
In4	0.5	-0.5	0.5	-0.5	...	-0.5
In5	0.6	-0.6	0.6	-0.6	...	-0.6
In6	0.7	-0.7	0.7	-0.7	...	-0.7
In7	0.8	-0.8	0.8	-0.8	...	-0.8
Select	0	0	0.008	0.008	...	0.055
Outputs						
Out	0.1	-0.1	0.2	-0.2	...	-0.8
Exp. Out	0.1	-0.1	0.2	-0.2	...	-0.8
Out (DSP)	3277	-3277	6554	-6554	...	-26214
Exp. Out (DSP)	3277	-3277	6554	-6554	...	-26214

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	48
Max CPU cycles	48
Avg CPU cycles	48

Verification: Selector FiP16 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for General block Selector.

Test results						
Time step	1	2	3	4	...	16
CPU cycles	70	62	62	62	...	62
Inputs						
In0 (DSP)	3277	-3277	3277	-3277	...	-3277
In1 (DSP)	6554	-6554	6554	-6554	...	-6554
In2 (DSP)	9830	-9830	9830	-9830	...	-9830
In3 (DSP)	13107	-13107	13107	-13107	...	-13107
In4 (DSP)	16384	-16384	16384	-16384	...	-16384
In5 (DSP)	19661	-19661	19661	-19661	...	-19661
In6 (DSP)	22938	-22938	22938	-22938	...	-22938
In7 (DSP)	26214	-26214	26214	-26214	...	-26214
Select (DSP)	0	0	1	1	...	7
In0	0.1	-0.1	0.1	-0.1	...	-0.1
In1	0.2	-0.2	0.2	-0.2	...	-0.2
In2	0.3	-0.3	0.3	-0.3	...	-0.3
In3	0.4	-0.4	0.4	-0.4	...	-0.4
In4	0.5	-0.5	0.5	-0.5	...	-0.5
In5	0.6	-0.6	0.6	-0.6	...	-0.6
In6	0.7	-0.7	0.7	-0.7	...	-0.7
In7	0.8	-0.8	0.8	-0.8	...	-0.8
Select	0	0	0.008	0.008	...	0.055
Outputs						
Out	0.1	-0.1	0.2	-0.2	...	-0.8
Exp. Out	0.1	-0.1	0.2	-0.2	...	-0.8
Out (DSP)	3277	-3277	6554	-6554	...	-26214
Exp. Out (DSP)	3277	-3277	6554	-6554	...	-26214

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	62
Max CPU cycles	70
Avg CPU cycles	62

Verification: Selector FiP16 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for General block Selector.

Test results						
Time step	1	2	3	4	...	16
CPU cycles	51	51	51	51	...	51
Inputs						
In0 (DSP)	3277	-3277	3277	-3277	...	-3277
In1 (DSP)	6554	-6554	6554	-6554	...	-6554
In2 (DSP)	9830	-9830	9830	-9830	...	-9830
In3 (DSP)	13107	-13107	13107	-13107	...	-13107
In4 (DSP)	16384	-16384	16384	-16384	...	-16384
In5 (DSP)	19661	-19661	19661	-19661	...	-19661
In6 (DSP)	22938	-22938	22938	-22938	...	-22938
In7 (DSP)	26214	-26214	26214	-26214	...	-26214
Select (DSP)	0	0	1	1	...	7
In0	0.1	-0.1	0.1	-0.1	...	-0.1
In1	0.2	-0.2	0.2	-0.2	...	-0.2
In2	0.3	-0.3	0.3	-0.3	...	-0.3
In3	0.4	-0.4	0.4	-0.4	...	-0.4
In4	0.5	-0.5	0.5	-0.5	...	-0.5
In5	0.6	-0.6	0.6	-0.6	...	-0.6
In6	0.7	-0.7	0.7	-0.7	...	-0.7
In7	0.8	-0.8	0.8	-0.8	...	-0.8
Select	0	0	0.008	0.008	...	0.055
Outputs						
Out	0.1	-0.1	0.2	-0.2	...	-0.8
Exp. Out	0.1	-0.1	0.2	-0.2	...	-0.8
Out (DSP)	3277	-3277	6554	-6554	...	-26214
Exp. Out (DSP)	3277	-3277	6554	-6554	...	-26214

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	51
Max CPU cycles	51
Avg CPU cycles	51

Verification: Selector FiP32 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for General block Selector.

Test results				
Time step	1	2	...	16
CPU cycles	68	68	...	68
Inputs				
In0 (DSP)	214748365	-214748365	...	-214748365
In1 (DSP)	429496730	-429496730	...	-429496730
In2 (DSP)	644245094	-644245094	...	-644245094
In3 (DSP)	858993459	-858993459	...	-858993459
In4 (DSP)	1073741824	-1073741824	...	-1073741824
In5 (DSP)	1288490189	-1288490189	...	-1288490189
In6 (DSP)	1503238554	-1503238554	...	-1503238554
In7 (DSP)	1717986918	-1717986918	...	-1717986918
Select (DSP)	0	0	...	7
In0	0.1	-0.1	...	-0.1
In1	0.2	-0.2	...	-0.2
In2	0.3	-0.3	...	-0.3
In3	0.4	-0.4	...	-0.4
In4	0.5	-0.5	...	-0.5
In5	0.6	-0.6	...	-0.6
In6	0.7	-0.7	...	-0.7
In7	0.8	-0.8	...	-0.8
Select	0	0	...	0.055
Outputs				
Out	0.1	-0.1	...	-0.8
Exp. Out	0.1	-0.1	...	-0.8
Out (DSP)	214748365	-214748365	...	-1717986918
Exp. Out (DSP)	214748365	-214748365	...	-1717986918

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	68
Max CPU cycles	68
Avg CPU cycles	68

Verification: Selector FiP32 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for General block Selector.

Test results				
Time step	1	2	...	16
CPU cycles	29	29	...	29
Inputs				
In0 (DSP)	214748365	-214748365	...	-214748365
In1 (DSP)	429496730	-429496730	...	-429496730
In2 (DSP)	644245094	-644245094	...	-644245094
In3 (DSP)	858993459	-858993459	...	-858993459
In4 (DSP)	1073741824	-1073741824	...	-1073741824
In5 (DSP)	1288490189	-1288490189	...	-1288490189
In6 (DSP)	1503238554	-1503238554	...	-1503238554
In7 (DSP)	1717986918	-1717986918	...	-1717986918
Select (DSP)	0	0	...	7
In0	0.1	-0.1	...	-0.1
In1	0.2	-0.2	...	-0.2
In2	0.3	-0.3	...	-0.3
In3	0.4	-0.4	...	-0.4
In4	0.5	-0.5	...	-0.5
In5	0.6	-0.6	...	-0.6
In6	0.7	-0.7	...	-0.7
In7	0.8	-0.8	...	-0.8
Select	0	0	...	0.055
Outputs				
Out	0.1	-0.1	...	-0.8
Exp. Out	0.1	-0.1	...	-0.8
Out (DSP)	214748365	-214748365	...	-1717986918
Exp. Out (DSP)	214748365	-214748365	...	-1717986918

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	29
Max CPU cycles	29
Avg CPU cycles	29

Verification: Selector FiP32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for General block Selector.

Test results				
Time step	1	2	...	16
CPU cycles	62	62	...	62
Inputs				
In0 (DSP)	214748365	-214748365	...	-214748365
In1 (DSP)	429496730	-429496730	...	-429496730
In2 (DSP)	644245094	-644245094	...	-644245094
In3 (DSP)	858993459	-858993459	...	-858993459
In4 (DSP)	1073741824	-1073741824	...	-1073741824
In5 (DSP)	1288490189	-1288490189	...	-1288490189
In6 (DSP)	1503238554	-1503238554	...	-1503238554
In7 (DSP)	1717986918	-1717986918	...	-1717986918
Select (DSP)	0	0	...	7
In0	0.1	-0.1	...	-0.1
In1	0.2	-0.2	...	-0.2
In2	0.3	-0.3	...	-0.3
In3	0.4	-0.4	...	-0.4
In4	0.5	-0.5	...	-0.5
In5	0.6	-0.6	...	-0.6
In6	0.7	-0.7	...	-0.7
In7	0.8	-0.8	...	-0.8
Select	0	0	...	0.055
Outputs				
Out	0.1	-0.1	...	-0.8
Exp. Out	0.1	-0.1	...	-0.8
Out (DSP)	214748365	-214748365	...	-1717986918
Exp. Out (DSP)	214748365	-214748365	...	-1717986918

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	62
Max CPU cycles	62
Avg CPU cycles	62

Verification: Selector FiP32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for General block Selector.

Test results				
Time step	1	2	...	16
CPU cycles	54	54	...	54
Inputs				
In0 (DSP)	214748365	-214748365	...	-214748365
In1 (DSP)	429496730	-429496730	...	-429496730
In2 (DSP)	644245094	-644245094	...	-644245094
In3 (DSP)	858993459	-858993459	...	-858993459
In4 (DSP)	1073741824	-1073741824	...	-1073741824
In5 (DSP)	1288490189	-1288490189	...	-1288490189
In6 (DSP)	1503238554	-1503238554	...	-1503238554
In7 (DSP)	1717986918	-1717986918	...	-1717986918
Select (DSP)	0	0	...	7
In0	0.1	-0.1	...	-0.1
In1	0.2	-0.2	...	-0.2
In2	0.3	-0.3	...	-0.3
In3	0.4	-0.4	...	-0.4
In4	0.5	-0.5	...	-0.5
In5	0.6	-0.6	...	-0.6
In6	0.7	-0.7	...	-0.7
In7	0.8	-0.8	...	-0.8
Select	0	0	...	0.055
Outputs				
Out	0.1	-0.1	...	-0.8
Exp. Out	0.1	-0.1	...	-0.8
Out (DSP)	214748365	-214748365	...	-1717986918
Exp. Out (DSP)	214748365	-214748365	...	-1717986918

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	54
Max CPU cycles	54
Avg CPU cycles	54

Verification: Selector FiP32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for General block Selector.

Test results				
Time step	1	2	...	16
CPU cycles	36	36	...	36
Inputs				
In0 (DSP)	214748365	-214748365	...	-214748365
In1 (DSP)	429496730	-429496730	...	-429496730
In2 (DSP)	644245094	-644245094	...	-644245094
In3 (DSP)	858993459	-858993459	...	-858993459
In4 (DSP)	1073741824	-1073741824	...	-1073741824
In5 (DSP)	1288490189	-1288490189	...	-1288490189
In6 (DSP)	1503238554	-1503238554	...	-1503238554
In7 (DSP)	1717986918	-1717986918	...	-1717986918
Select (DSP)	0	0	...	7
In0	0.1	-0.1	...	-0.1
In1	0.2	-0.2	...	-0.2
In2	0.3	-0.3	...	-0.3
In3	0.4	-0.4	...	-0.4
In4	0.5	-0.5	...	-0.5
In5	0.6	-0.6	...	-0.6
In6	0.7	-0.7	...	-0.7
In7	0.8	-0.8	...	-0.8
Select	0	0	...	0.055
Outputs				
Out	0.1	-0.1	...	-0.8
Exp. Out	0.1	-0.1	...	-0.8
Out (DSP)	214748365	-214748365	...	-1717986918
Exp. Out (DSP)	214748365	-214748365	...	-1717986918

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	36
Max CPU cycles	36
Avg CPU cycles	36

Verification: Selector FiP32 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for General block Selector.

Test results				
Time step	1	2	...	16
CPU cycles	50	50	...	50
Inputs				
In0 (DSP)	214748365	-214748365	...	-214748365
In1 (DSP)	429496730	-429496730	...	-429496730
In2 (DSP)	644245094	-644245094	...	-644245094
In3 (DSP)	858993459	-858993459	...	-858993459
In4 (DSP)	1073741824	-1073741824	...	-1073741824
In5 (DSP)	1288490189	-1288490189	...	-1288490189
In6 (DSP)	1503238554	-1503238554	...	-1503238554
In7 (DSP)	1717986918	-1717986918	...	-1717986918
Select (DSP)	0	0	...	7
In0	0.1	-0.1	...	-0.1
In1	0.2	-0.2	...	-0.2
In2	0.3	-0.3	...	-0.3
In3	0.4	-0.4	...	-0.4
In4	0.5	-0.5	...	-0.5
In5	0.6	-0.6	...	-0.6
In6	0.7	-0.7	...	-0.7
In7	0.8	-0.8	...	-0.8
Select	0	0	...	0.055
Outputs				
Out	0.1	-0.1	...	-0.8
Exp. Out	0.1	-0.1	...	-0.8
Out (DSP)	214748365	-214748365	...	-1717986918
Exp. Out (DSP)	214748365	-214748365	...	-1717986918

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	50
Max CPU cycles	50
Avg CPU cycles	50

Verification: Selector FiP32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for General block Selector.

Test results				
Time step	1	2	...	16
CPU cycles	70	62	...	62
Inputs				
In0 (DSP)	214748365	-214748365	...	-214748365
In1 (DSP)	429496730	-429496730	...	-429496730
In2 (DSP)	644245094	-644245094	...	-644245094
In3 (DSP)	858993459	-858993459	...	-858993459
In4 (DSP)	1073741824	-1073741824	...	-1073741824
In5 (DSP)	1288490189	-1288490189	...	-1288490189
In6 (DSP)	1503238554	-1503238554	...	-1503238554
In7 (DSP)	1717986918	-1717986918	...	-1717986918
Select (DSP)	0	0	...	7
In0	0.1	-0.1	...	-0.1
In1	0.2	-0.2	...	-0.2
In2	0.3	-0.3	...	-0.3
In3	0.4	-0.4	...	-0.4
In4	0.5	-0.5	...	-0.5
In5	0.6	-0.6	...	-0.6
In6	0.7	-0.7	...	-0.7
In7	0.8	-0.8	...	-0.8
Select	0	0	...	0.055
Outputs				
Out	0.1	-0.1	...	-0.8
Exp. Out	0.1	-0.1	...	-0.8
Out (DSP)	214748365	-214748365	...	-1717986918
Exp. Out (DSP)	214748365	-214748365	...	-1717986918

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	62
Max CPU cycles	70
Avg CPU cycles	62

Verification: Selector FiP32 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for General block Selector.

Test results				
Time step	1	2	...	16
CPU cycles	49	49	...	49
Inputs				
In0 (DSP)	214748365	-214748365	...	-214748365
In1 (DSP)	429496730	-429496730	...	-429496730
In2 (DSP)	644245094	-644245094	...	-644245094
In3 (DSP)	858993459	-858993459	...	-858993459
In4 (DSP)	1073741824	-1073741824	...	-1073741824
In5 (DSP)	1288490189	-1288490189	...	-1288490189
In6 (DSP)	1503238554	-1503238554	...	-1503238554
In7 (DSP)	1717986918	-1717986918	...	-1717986918
Select (DSP)	0	0	...	7
In0	0.1	-0.1	...	-0.1
In1	0.2	-0.2	...	-0.2
In2	0.3	-0.3	...	-0.3
In3	0.4	-0.4	...	-0.4
In4	0.5	-0.5	...	-0.5
In5	0.6	-0.6	...	-0.6
In6	0.7	-0.7	...	-0.7
In7	0.8	-0.8	...	-0.8
Select	0	0	...	0.055
Outputs				
Out	0.1	-0.1	...	-0.8
Exp. Out	0.1	-0.1	...	-0.8
Out (DSP)	214748365	-214748365	...	-1717986918
Exp. Out (DSP)	214748365	-214748365	...	-1717986918

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	49
Max CPU cycles	49
Avg CPU cycles	49

Verification: Selector Float32 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for General block Selector.

Test results				
Time step	1	2	...	16
CPU cycles	68	68	...	68
Inputs				
In0 (DSP)	0.1	-0.1	...	-0.1
In1 (DSP)	0.2	-0.2	...	-0.2
In2 (DSP)	0.3	-0.3	...	-0.3
In3 (DSP)	0.4	-0.4	...	-0.4
In4 (DSP)	0.5	-0.5	...	-0.5
In5 (DSP)	0.6	-0.6	...	-0.6
In6 (DSP)	0.7	-0.7	...	-0.7
In7 (DSP)	0.8	-0.8	...	-0.8
Select (DSP)	0	0	...	7
In0	0.1	-0.1	...	-0.1
In1	0.2	-0.2	...	-0.2
In2	0.3	-0.3	...	-0.3
In3	0.4	-0.4	...	-0.4
In4	0.5	-0.5	...	-0.5
In5	0.6	-0.6	...	-0.6
In6	0.7	-0.7	...	-0.7
In7	0.8	-0.8	...	-0.8
Select	0	0	...	0.055
Outputs				
Out	0.1	-0.1	...	-0.8
Exp. Out	0.1	-0.1	...	-0.8
Out (DSP)	0.1	-0.1	...	-0.8
Exp. Out (DSP)	0.1	-0.1	...	-0.8

Test settings	
Tolerance Out	±3,2596e-08 (±70 LSB)

Test statistics	
Min CPU cycles	68
Max CPU cycles	68
Avg CPU cycles	68

Verification: Selector Float32 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for General block Selector.

Test results				
Time step	1	2	...	16
CPU cycles	29	29	...	29
Inputs				
In0 (DSP)	0.1	-0.1	...	-0.1
In1 (DSP)	0.2	-0.2	...	-0.2
In2 (DSP)	0.3	-0.3	...	-0.3
In3 (DSP)	0.4	-0.4	...	-0.4
In4 (DSP)	0.5	-0.5	...	-0.5
In5 (DSP)	0.6	-0.6	...	-0.6
In6 (DSP)	0.7	-0.7	...	-0.7
In7 (DSP)	0.8	-0.8	...	-0.8
Select (DSP)	0	0	...	7
In0	0.1	-0.1	...	-0.1
In1	0.2	-0.2	...	-0.2
In2	0.3	-0.3	...	-0.3
In3	0.4	-0.4	...	-0.4
In4	0.5	-0.5	...	-0.5
In5	0.6	-0.6	...	-0.6
In6	0.7	-0.7	...	-0.7
In7	0.8	-0.8	...	-0.8
Select	0	0	...	0.055
Outputs				
Out	0.1	-0.1	...	-0.8
Exp. Out	0.1	-0.1	...	-0.8
Out (DSP)	0.1	-0.1	...	-0.8
Exp. Out (DSP)	0.1	-0.1	...	-0.8

Test settings	
Tolerance Out	±3,2596e-08 (±70 LSB)

Test statistics	
Min CPU cycles	29
Max CPU cycles	29
Avg CPU cycles	29

Verification: Selector Float32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for General block Selector.

Test results				
Time step	1	2	...	16
CPU cycles	62	62	...	62
Inputs				
In0 (DSP)	0.1	-0.1	...	-0.1
In1 (DSP)	0.2	-0.2	...	-0.2
In2 (DSP)	0.3	-0.3	...	-0.3
In3 (DSP)	0.4	-0.4	...	-0.4
In4 (DSP)	0.5	-0.5	...	-0.5
In5 (DSP)	0.6	-0.6	...	-0.6
In6 (DSP)	0.7	-0.7	...	-0.7
In7 (DSP)	0.8	-0.8	...	-0.8
Select (DSP)	0	0	...	7
In0	0.1	-0.1	...	-0.1
In1	0.2	-0.2	...	-0.2
In2	0.3	-0.3	...	-0.3
In3	0.4	-0.4	...	-0.4
In4	0.5	-0.5	...	-0.5
In5	0.6	-0.6	...	-0.6
In6	0.7	-0.7	...	-0.7
In7	0.8	-0.8	...	-0.8
Select	0	0	...	0.055
Outputs				
Out	0.1	-0.1	...	-0.8
Exp. Out	0.1	-0.1	...	-0.8
Out (DSP)	0.1	-0.1	...	-0.8
Exp. Out (DSP)	0.1	-0.1	...	-0.8

Test settings	
Tolerance Out	±3,2596e-08 (±70 LSB)

Test statistics	
Min CPU cycles	62
Max CPU cycles	62
Avg CPU cycles	62

Verification: Selector Float32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for General block Selector.

Test results				
Time step	1	2	...	16
CPU cycles	54	54	...	54
Inputs				
In0 (DSP)	0.1	-0.1	...	-0.1
In1 (DSP)	0.2	-0.2	...	-0.2
In2 (DSP)	0.3	-0.3	...	-0.3
In3 (DSP)	0.4	-0.4	...	-0.4
In4 (DSP)	0.5	-0.5	...	-0.5
In5 (DSP)	0.6	-0.6	...	-0.6
In6 (DSP)	0.7	-0.7	...	-0.7
In7 (DSP)	0.8	-0.8	...	-0.8
Select (DSP)	0	0	...	7
In0	0.1	-0.1	...	-0.1
In1	0.2	-0.2	...	-0.2
In2	0.3	-0.3	...	-0.3
In3	0.4	-0.4	...	-0.4
In4	0.5	-0.5	...	-0.5
In5	0.6	-0.6	...	-0.6
In6	0.7	-0.7	...	-0.7
In7	0.8	-0.8	...	-0.8
Select	0	0	...	0.055
Outputs				
Out	0.1	-0.1	...	-0.8
Exp. Out	0.1	-0.1	...	-0.8
Out (DSP)	0.1	-0.1	...	-0.8
Exp. Out (DSP)	0.1	-0.1	...	-0.8

Test settings	
Tolerance Out	±3,2596e-08 (±70 LSB)

Test statistics	
Min CPU cycles	54
Max CPU cycles	54
Avg CPU cycles	54

Verification: Selector Float32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for General block Selector.

Test results				
Time step	1	2	...	16
CPU cycles	36	36	...	36
Inputs				
In0 (DSP)	0.1	-0.1	...	-0.1
In1 (DSP)	0.2	-0.2	...	-0.2
In2 (DSP)	0.3	-0.3	...	-0.3
In3 (DSP)	0.4	-0.4	...	-0.4
In4 (DSP)	0.5	-0.5	...	-0.5
In5 (DSP)	0.6	-0.6	...	-0.6
In6 (DSP)	0.7	-0.7	...	-0.7
In7 (DSP)	0.8	-0.8	...	-0.8
Select (DSP)	0	0	...	7
In0	0.1	-0.1	...	-0.1
In1	0.2	-0.2	...	-0.2
In2	0.3	-0.3	...	-0.3
In3	0.4	-0.4	...	-0.4
In4	0.5	-0.5	...	-0.5
In5	0.6	-0.6	...	-0.6
In6	0.7	-0.7	...	-0.7
In7	0.8	-0.8	...	-0.8
Select	0	0	...	0.055
Outputs				
Out	0.1	-0.1	...	-0.8
Exp. Out	0.1	-0.1	...	-0.8
Out (DSP)	0.1	-0.1	...	-0.8
Exp. Out (DSP)	0.1	-0.1	...	-0.8

Test settings	
Tolerance Out	±3,2596e-08 (±70 LSB)

Test statistics	
Min CPU cycles	36
Max CPU cycles	36
Avg CPU cycles	36

Verification: Selector Float32 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for General block Selector.

Test results				
Time step	1	2	...	16
CPU cycles	50	50	...	50
Inputs				
In0 (DSP)	0.1	-0.1	...	-0.1
In1 (DSP)	0.2	-0.2	...	-0.2
In2 (DSP)	0.3	-0.3	...	-0.3
In3 (DSP)	0.4	-0.4	...	-0.4
In4 (DSP)	0.5	-0.5	...	-0.5
In5 (DSP)	0.6	-0.6	...	-0.6
In6 (DSP)	0.7	-0.7	...	-0.7
In7 (DSP)	0.8	-0.8	...	-0.8
Select (DSP)	0	0	...	7
In0	0.1	-0.1	...	-0.1
In1	0.2	-0.2	...	-0.2
In2	0.3	-0.3	...	-0.3
In3	0.4	-0.4	...	-0.4
In4	0.5	-0.5	...	-0.5
In5	0.6	-0.6	...	-0.6
In6	0.7	-0.7	...	-0.7
In7	0.8	-0.8	...	-0.8
Select	0	0	...	0.055
Outputs				
Out	0.1	-0.1	...	-0.8
Exp. Out	0.1	-0.1	...	-0.8
Out (DSP)	0.1	-0.1	...	-0.8
Exp. Out (DSP)	0.1	-0.1	...	-0.8

Test settings	
Tolerance Out	±3,2596e-08 (±70 LSB)

Test statistics	
Min CPU cycles	50
Max CPU cycles	50
Avg CPU cycles	50

Verification: Selector Float32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for General block Selector.

Test results				
Time step	1	2	...	16
CPU cycles	62	62	...	62
Inputs				
In0 (DSP)	0.1	-0.1	...	-0.1
In1 (DSP)	0.2	-0.2	...	-0.2
In2 (DSP)	0.3	-0.3	...	-0.3
In3 (DSP)	0.4	-0.4	...	-0.4
In4 (DSP)	0.5	-0.5	...	-0.5
In5 (DSP)	0.6	-0.6	...	-0.6
In6 (DSP)	0.7	-0.7	...	-0.7
In7 (DSP)	0.8	-0.8	...	-0.8
Select (DSP)	0	0	...	7
In0	0.1	-0.1	...	-0.1
In1	0.2	-0.2	...	-0.2
In2	0.3	-0.3	...	-0.3
In3	0.4	-0.4	...	-0.4
In4	0.5	-0.5	...	-0.5
In5	0.6	-0.6	...	-0.6
In6	0.7	-0.7	...	-0.7
In7	0.8	-0.8	...	-0.8
Select	0	0	...	0.055
Outputs				
Out	0.1	-0.1	...	-0.8
Exp. Out	0.1	-0.1	...	-0.8
Out (DSP)	0.1	-0.1	...	-0.8
Exp. Out (DSP)	0.1	-0.1	...	-0.8

Test settings	
Tolerance Out	±3,2596e-08 (±70 LSB)

Test statistics	
Min CPU cycles	62
Max CPU cycles	62
Avg CPU cycles	62

Verification: Selector Float32 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

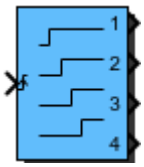
Inport test for General block Selector.

Test results				
Time step	1	2	...	16
CPU cycles	48	48	...	48
Inputs				
In0 (DSP)	0.1	-0.1	...	-0.1
In1 (DSP)	0.2	-0.2	...	-0.2
In2 (DSP)	0.3	-0.3	...	-0.3
In3 (DSP)	0.4	-0.4	...	-0.4
In4 (DSP)	0.5	-0.5	...	-0.5
In5 (DSP)	0.6	-0.6	...	-0.6
In6 (DSP)	0.7	-0.7	...	-0.7
In7 (DSP)	0.8	-0.8	...	-0.8
Select (DSP)	0	0	...	7
In0	0.1	-0.1	...	-0.1
In1	0.2	-0.2	...	-0.2
In2	0.3	-0.3	...	-0.3
In3	0.4	-0.4	...	-0.4
In4	0.5	-0.5	...	-0.5
In5	0.6	-0.6	...	-0.6
In6	0.7	-0.7	...	-0.7
In7	0.8	-0.8	...	-0.8
Select	0	0	...	0.055
Outputs				
Out	0.1	-0.1	...	-0.8
Exp. Out	0.1	-0.1	...	-0.8
Out (DSP)	0.1	-0.1	...	-0.8
Exp. Out (DSP)	0.1	-0.1	...	-0.8

Test settings	
Tolerance Out	±3,2596e-08 (±70 LSB)

Test statistics	
Min CPU cycles	48
Max CPU cycles	48
Avg CPU cycles	48

Block: Sequencer



Generation of time delayed (enable) sequence.

Inports	
Start	Start signal. Rising flank triggers sequence

Outports	
Out1	Output #1
Out2	Output #2
Out3	Output #3
Out4	Output #4

Mask Parameters		
Name	**ID**	**Description**
Delay1	1	Time delay for output 1
Delay2	2	Time delay for output 2
Delay3	3	Time delay for output 3
Delay4	4	Time delay for output 4
ts_fact	5	Multiplication factor of base sampling time (in integer format)

Implementations:

Bool	Boolean Implementation
FiP8	8 Bit Fixed Point Implementation
FiP16	16 Bit Fixed Point Implementation
FiP32	32 Bit Fixed Point Implementation
Float32	32 Bit Floating Point Implementation
Float64	64 Bit Floating Point Implementation

Implementation: Bool

Boolean Implementation

Inports Data Type	
Start	bool

Outports Data Type	
Out1	bool
Out2	bool
Out3	bool
Out4	bool

Implementation: FiP8

8 Bit Fixed Point Implementation

Inports Data Type	
Start	int8

Outports Data Type	
Out1	int8
Out2	int8
Out3	int8
Out4	int8

Implementation: FiP16

16 Bit Fixed Point Implementation

Inports Data Type	
Start	int16

Outports Data Type	
Out1	int16
Out2	int16
Out3	int16
Out4	int16

Implementation: FiP32

32 Bit Fixed Point Implementation

Inports Data Type	
Start	int32

Outports Data Type	
Out1	int32
Out2	int32
Out3	int32
Out4	int32

Implementation: Float32

32 Bit Floating Point Implementation

Inports Data Type	
Start	float32

Outports Data Type	
Out1	float32
Out2	float32
Out3	float32
Out4	float32

Implementation: Float64

64 Bit Floating Point Implementation

Inports Data Type	
Start	float64

Outports Data Type	
Out1	float64
Out2	float64
Out3	float64
Out4	float64

Verification: Sequencer Bool CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for General block Sequencer.

Test results						
Time step	1	2	3	4	...	16
CPU cycles	72	115	113	111	...	72
Inputs						
Start (DSP)	0	1	1	1	...	0
Start	0	1	1	1	...	0
Parameters						
Delay1	0					
Delay2	0					
Delay3	0.001					
Delay4	0					
ts_fact	1					
Outputs						
Out1	0	0	1	1	...	0
Out2	0	0	0	1	...	0
Out3	0	0	0	0	...	0
Out4	0	1	1	1	...	0
Exp. Out1	0	0	1	1	...	0
Exp. Out2	0	0	0	1	...	0
Exp. Out3	0	0	0	0	...	0
Exp. Out4	0	1	1	1	...	0
Out1 (DSP)	0	0	1	1	...	0
Out2 (DSP)	0	0	0	1	...	0
Out3 (DSP)	0	0	0	0	...	0
Out4 (DSP)	0	1	1	1	...	0
Exp. Out1 (DSP)	0	0	1	1	...	0
Exp. Out2 (DSP)	0	0	0	1	...	0
Exp. Out3 (DSP)	0	0	0	0	...	0
Exp. Out4 (DSP)	0	1	1	1	...	0

Test settings	
Tolerance Out1	±0,0000e+00 (±0 LSB)
Tolerance Out2	±0,0000e+00 (±0 LSB)
Tolerance Out3	±0,0000e+00 (±0 LSB)
Tolerance Out4	±0,0000e+00 (±0 LSB)

Test statistics	
Min CPU cycles	72
Max CPU cycles	115
Avg CPU cycles	106

Test case: Conversion test **OK**

Conversion test for General block Sequencer.

Test results			
Time step	1	2	3
Mask parameters			
Delay1	0.1	0.1	0.1
Delay2	0.2	0.2	0.2
Delay3	1	1	1
Delay4	1.7	1.7	1.7
ts_fact	1	2	10
Controller parameters			
delay3	10000	5000	1000
delay4	17000	8500	1700
delay1	1000	500	100
delay2	2000	1000	200
Exp. delay3	10000	5000	1000
Exp. delay4	17000	8500	1700
Exp. delay1	1000	500	100
Exp. delay2	2000	1000	200

Test settings	
Tolerance delay3	±0,0000e+00
Tolerance delay4	±0,0000e+00
Tolerance delay1	±0,0000e+00
Tolerance delay2	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block Sequencer.

Test results			
Time step	1	2	3
Mask parameters			
Delay1	0.1	0.1	0.1
Delay2	0.2	0.2	0.2
Delay3	1	1	1
Delay4	1.7	1.7	1.7
ts_fact	1	2	10
Controller parameters			
delay3	10000	5000	1000
delay4	17000	8500	1700
delay1	1000	500	100
delay2	2000	1000	200
Exp. delay3	10000	5000	1000
Exp. delay4	17000	8500	1700
Exp. delay1	1000	500	100
Exp. delay2	2000	1000	200

Test settings	
Tolerance delay3	±0,0000e+00
Tolerance delay4	±0,0000e+00
Tolerance delay1	±0,0000e+00
Tolerance delay2	±0,0000e+00

Test statistics	
Min CPU cycles	3591
Max CPU cycles	3598
Avg CPU cycles	3595

Verification: Sequencer Bool CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for General block Sequencer.

Test results						
Time step	1	2	3	4	...	16
CPU cycles	53	77	77	77	...	53
Inputs						
Start (DSP)	0	1	1	1	...	0
Start	0	1	1	1	...	0
Parameters						
Delay1	0					
Delay2	0					
Delay3	0.001					
Delay4	0					
ts_fact	1					
Outputs						
Out1	0	0	1	1	...	0
Out2	0	0	0	1	...	0
Out3	0	0	0	0	...	0
Out4	0	1	1	1	...	0
Exp. Out1	0	0	1	1	...	0
Exp. Out2	0	0	0	1	...	0
Exp. Out3	0	0	0	0	...	0
Exp. Out4	0	1	1	1	...	0
Out1 (DSP)	0	0	1	1	...	0
Out2 (DSP)	0	0	0	1	...	0
Out3 (DSP)	0	0	0	0	...	0
Out4 (DSP)	0	1	1	1	...	0
Exp. Out1 (DSP)	0	0	1	1	...	0
Exp. Out2 (DSP)	0	0	0	1	...	0
Exp. Out3 (DSP)	0	0	0	0	...	0
Exp. Out4 (DSP)	0	1	1	1	...	0

Test settings	
Tolerance Out1	±0,0000e+00 (±0 LSB)
Tolerance Out2	±0,0000e+00 (±0 LSB)
Tolerance Out3	±0,0000e+00 (±0 LSB)
Tolerance Out4	±0,0000e+00 (±0 LSB)

Test statistics	
Min CPU cycles	53
Max CPU cycles	77
Avg CPU cycles	74

Test case: Conversion test **OK**

Conversion test for General block Sequencer.

Test results			
Time step	1	2	3
Mask parameters			
Delay1	0.1	0.1	0.1
Delay2	0.2	0.2	0.2
Delay3	1	1	1
Delay4	1.7	1.7	1.7
ts_fact	1	2	10
Controller parameters			
delay3	10000	5000	1000
delay4	17000	8500	1700
delay1	1000	500	100
delay2	2000	1000	200
Exp. delay3	10000	5000	1000
Exp. delay4	17000	8500	1700
Exp. delay1	1000	500	100
Exp. delay2	2000	1000	200

Test settings	
Tolerance delay3	±0,0000e+00
Tolerance delay4	±0,0000e+00
Tolerance delay1	±0,0000e+00
Tolerance delay2	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block Sequencer.

Test results			
Time step	1	2	3
Mask parameters			
Delay1	0.1	0.1	0.1
Delay2	0.2	0.2	0.2
Delay3	1	1	1
Delay4	1.7	1.7	1.7
ts_fact	1	2	10
Controller parameters			
delay3	10000	5000	1000
delay4	17000	8500	1700
delay1	1000	500	100
delay2	2000	1000	200
Exp. delay3	10000	5000	1000
Exp. delay4	17000	8500	1700
Exp. delay1	1000	500	100
Exp. delay2	2000	1000	200

Test settings	
Tolerance delay3	±0,0000e+00
Tolerance delay4	±0,0000e+00
Tolerance delay1	±0,0000e+00
Tolerance delay2	±0,0000e+00

Test statistics	
Min CPU cycles	1209
Max CPU cycles	1209
Avg CPU cycles	1209

Verification: Sequencer Bool CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test **OK**

Inport test for General block Sequencer.

Test results						
Time step	1	2	3	4	...	16
CPU cycles	86	106	145	145	...	86
Inputs						
Start (DSP)	0	1	1	1	...	0
Start	0	1	1	1	...	0
Parameters						
Delay1	0					
Delay2	0					
Delay3	0.001					
Delay4	0					
ts_fact	1					
Outputs						
Out1	0	0	1	1	...	0
Out2	0	0	0	1	...	0
Out3	0	0	0	0	...	0
Out4	0	1	1	1	...	0
Exp. Out1	0	0	1	1	...	0
Exp. Out2	0	0	0	1	...	0
Exp. Out3	0	0	0	0	...	0
Exp. Out4	0	1	1	1	...	0
Out1 (DSP)	0	0	1	1	...	0
Out2 (DSP)	0	0	0	1	...	0
Out3 (DSP)	0	0	0	0	...	0
Out4 (DSP)	0	1	1	1	...	0
Exp. Out1 (DSP)	0	0	1	1	...	0
Exp. Out2 (DSP)	0	0	0	1	...	0
Exp. Out3 (DSP)	0	0	0	0	...	0
Exp. Out4 (DSP)	0	1	1	1	...	0

Test settings	
Tolerance Out1	±0,0000e+00 (±0 LSB)
Tolerance Out2	±0,0000e+00 (±0 LSB)
Tolerance Out3	±0,0000e+00 (±0 LSB)
Tolerance Out4	±0,0000e+00 (±0 LSB)

Test statistics	
Min CPU cycles	86
Max CPU cycles	145
Avg CPU cycles	135

Test case: Conversion test **OK**

Conversion test for General block Sequencer.

Test results			
Time step	1	2	3
Mask parameters			
Delay1	0.1	0.1	0.1
Delay2	0.2	0.2	0.2
Delay3	1	1	1
Delay4	1.7	1.7	1.7
ts_fact	1	2	10
Controller parameters			
delay3	10000	5000	1000
delay4	17000	8500	1700
delay1	1000	500	100
delay2	2000	1000	200
Exp. delay3	10000	5000	1000
Exp. delay4	17000	8500	1700
Exp. delay1	1000	500	100
Exp. delay2	2000	1000	200

Test settings	
Tolerance delay3	±0,0000e+00
Tolerance delay4	±0,0000e+00
Tolerance delay1	±0,0000e+00
Tolerance delay2	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block Sequencer.

Test results			
Time step	1	2	3
Mask parameters			
Delay1	0.1	0.1	0.1
Delay2	0.2	0.2	0.2
Delay3	1	1	1
Delay4	1.7	1.7	1.7
ts_fact	1	2	10
Controller parameters			
delay3	10000	5000	1000
delay4	17000	8500	1700
delay1	1000	500	100
delay2	2000	1000	200
Exp. delay3	10000	5000	1000
Exp. delay4	17000	8500	1700
Exp. delay1	1000	500	100
Exp. delay2	2000	1000	200

Test settings	
Tolerance delay3	±0,0000e+00
Tolerance delay4	±0,0000e+00
Tolerance delay1	±0,0000e+00
Tolerance delay2	±0,0000e+00

Test statistics	
Min CPU cycles	1272
Max CPU cycles	1315
Avg CPU cycles	1286

Verification: Sequencer Bool CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test **OK**

Inport test for General block Sequencer.

Test results						
Time step	1	2	3	4	...	16
CPU cycles	77	100	120	120	...	77
Inputs						
Start (DSP)	0	1	1	1	...	0
Start	0	1	1	1	...	0
Parameters						
Delay1	0					
Delay2	0					
Delay3	0.001					
Delay4	0					
ts_fact	1					
Outputs						
Out1	0	0	1	1	...	0
Out2	0	0	0	1	...	0
Out3	0	0	0	0	...	0
Out4	0	1	1	1	...	0
Exp. Out1	0	0	1	1	...	0
Exp. Out2	0	0	0	1	...	0
Exp. Out3	0	0	0	0	...	0
Exp. Out4	0	1	1	1	...	0
Out1 (DSP)	0	0	1	1	...	0
Out2 (DSP)	0	0	0	1	...	0
Out3 (DSP)	0	0	0	0	...	0
Out4 (DSP)	0	1	1	1	...	0
Exp. Out1 (DSP)	0	0	1	1	...	0
Exp. Out2 (DSP)	0	0	0	1	...	0
Exp. Out3 (DSP)	0	0	0	0	...	0
Exp. Out4 (DSP)	0	1	1	1	...	0

Test settings	
Tolerance Out1	±0,0000e+00 (±0 LSB)
Tolerance Out2	±0,0000e+00 (±0 LSB)
Tolerance Out3	±0,0000e+00 (±0 LSB)
Tolerance Out4	±0,0000e+00 (±0 LSB)

Test statistics	
Min CPU cycles	77
Max CPU cycles	120
Avg CPU cycles	113

Test case: Conversion test **OK**

Conversion test for General block Sequencer.

Test results			
Time step	1	2	3
Mask parameters			
Delay1	0.1	0.1	0.1
Delay2	0.2	0.2	0.2
Delay3	1	1	1
Delay4	1.7	1.7	1.7
ts_fact	1	2	10
Controller parameters			
delay3	10000	5000	1000
delay4	17000	8500	1700
delay1	1000	500	100
delay2	2000	1000	200
Exp. delay3	10000	5000	1000
Exp. delay4	17000	8500	1700
Exp. delay1	1000	500	100
Exp. delay2	2000	1000	200

Test settings	
Tolerance delay3	±0,0000e+00
Tolerance delay4	±0,0000e+00
Tolerance delay1	±0,0000e+00
Tolerance delay2	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block Sequencer.

Test results			
Time step	1	2	3
Mask parameters			
Delay1	0.1	0.1	0.1
Delay2	0.2	0.2	0.2
Delay3	1	1	1
Delay4	1.7	1.7	1.7
ts_fact	1	2	10
Controller parameters			
delay3	10000	5000	1000
delay4	17000	8500	1700
delay1	1000	500	100
delay2	2000	1000	200
Exp. delay3	10000	5000	1000
Exp. delay4	17000	8500	1700
Exp. delay1	1000	500	100
Exp. delay2	2000	1000	200

Test settings	
Tolerance delay3	±0,0000e+00
Tolerance delay4	±0,0000e+00
Tolerance delay1	±0,0000e+00
Tolerance delay2	±0,0000e+00

Test statistics	
Min CPU cycles	5808
Max CPU cycles	5817
Avg CPU cycles	5814

Verification: Sequencer Bool CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for General block Sequencer.

Test results						
Time step	1	2	3	4	...	16
CPU cycles	42	58	68	68	...	42
Inputs						
Start (DSP)	0	1	1	1	...	0
Start	0	1	1	1	...	0
Parameters						
Delay1	0					
Delay2	0					
Delay3	0.001					
Delay4	0					
ts_fact	1					
Outputs						
Out1	0	0	1	1	...	0
Out2	0	0	0	1	...	0
Out3	0	0	0	0	...	0
Out4	0	1	1	1	...	0
Exp. Out1	0	0	1	1	...	0
Exp. Out2	0	0	0	1	...	0
Exp. Out3	0	0	0	0	...	0
Exp. Out4	0	1	1	1	...	0
Out1 (DSP)	0	0	1	1	...	0
Out2 (DSP)	0	0	0	1	...	0
Out3 (DSP)	0	0	0	0	...	0
Out4 (DSP)	0	1	1	1	...	0
Exp. Out1 (DSP)	0	0	1	1	...	0
Exp. Out2 (DSP)	0	0	0	1	...	0
Exp. Out3 (DSP)	0	0	0	0	...	0
Exp. Out4 (DSP)	0	1	1	1	...	0

Test settings	
Tolerance Out1	±0,0000e+00 (±0 LSB)
Tolerance Out2	±0,0000e+00 (±0 LSB)
Tolerance Out3	±0,0000e+00 (±0 LSB)
Tolerance Out4	±0,0000e+00 (±0 LSB)

Test statistics	
Min CPU cycles	42
Max CPU cycles	68
Avg CPU cycles	64

Test case: Conversion test **OK**

Conversion test for General block Sequencer.

Test results			
Time step	1	2	3
Mask parameters			
Delay1	0.1	0.1	0.1
Delay2	0.2	0.2	0.2
Delay3	1	1	1
Delay4	1.7	1.7	1.7
ts_fact	1	2	10
Controller parameters			
delay3	10000	5000	1000
delay4	17000	8500	1700
delay1	1000	500	100
delay2	2000	1000	200
Exp. delay3	10000	5000	1000
Exp. delay4	17000	8500	1700
Exp. delay1	1000	500	100
Exp. delay2	2000	1000	200

Test settings	
Tolerance delay3	±0,0000e+00
Tolerance delay4	±0,0000e+00
Tolerance delay1	±0,0000e+00
Tolerance delay2	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block Sequencer.

Test results			
Time step	1	2	3
Mask parameters			
Delay1	0.1	0.1	0.1
Delay2	0.2	0.2	0.2
Delay3	1	1	1
Delay4	1.7	1.7	1.7
ts_fact	1	2	10
Controller parameters			
delay3	10000	5000	1000
delay4	17000	8500	1700
delay1	1000	500	100
delay2	2000	1000	200
Exp. delay3	10000	5000	1000
Exp. delay4	17000	8500	1700
Exp. delay1	1000	500	100
Exp. delay2	2000	1000	200

Test settings	
Tolerance delay3	±0,0000e+00
Tolerance delay4	±0,0000e+00
Tolerance delay1	±0,0000e+00
Tolerance delay2	±0,0000e+00

Test statistics	
Min CPU cycles	1852
Max CPU cycles	1853
Avg CPU cycles	1852

Verification: Sequencer Bool CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for General block Sequencer.

Test results						
Time step	1	2	3	4	...	16
CPU cycles	54	72	90	85	...	54
Inputs						
Start (DSP)	0	1	1	1	...	0
Start	0	1	1	1	...	0
Parameters						
Delay1	0					
Delay2	0					
Delay3	0.001					
Delay4	0					
ts_fact	1					
Outputs						
Out1	0	0	1	1	...	0
Out2	0	0	0	1	...	0
Out3	0	0	0	0	...	0
Out4	0	1	1	1	...	0
Exp. Out1	0	0	1	1	...	0
Exp. Out2	0	0	0	1	...	0
Exp. Out3	0	0	0	0	...	0
Exp. Out4	0	1	1	1	...	0
Out1 (DSP)	0	0	1	1	...	0
Out2 (DSP)	0	0	0	1	...	0
Out3 (DSP)	0	0	0	0	...	0
Out4 (DSP)	0	1	1	1	...	0
Exp. Out1 (DSP)	0	0	1	1	...	0
Exp. Out2 (DSP)	0	0	0	1	...	0
Exp. Out3 (DSP)	0	0	0	0	...	0
Exp. Out4 (DSP)	0	1	1	1	...	0

Test settings	
Tolerance Out1	±0,0000e+00 (±0 LSB)
Tolerance Out2	±0,0000e+00 (±0 LSB)
Tolerance Out3	±0,0000e+00 (±0 LSB)
Tolerance Out4	±0,0000e+00 (±0 LSB)

Test statistics	
Min CPU cycles	54
Max CPU cycles	90
Avg CPU cycles	77

Test case: Conversion test **OK**

Conversion test for General block Sequencer.

Test results			
Time step	1	2	3
Mask parameters			
Delay1	0.1	0.1	0.1
Delay2	0.2	0.2	0.2
Delay3	1	1	1
Delay4	1.7	1.7	1.7
ts_fact	1	2	10
Controller parameters			
delay3	10000	5000	1000
delay4	17000	8500	1700
delay1	1000	500	100
delay2	2000	1000	200
Exp. delay3	10000	5000	1000
Exp. delay4	17000	8500	1700
Exp. delay1	1000	500	100
Exp. delay2	2000	1000	200

Test settings	
Tolerance delay3	±0,0000e+00
Tolerance delay4	±0,0000e+00
Tolerance delay1	±0,0000e+00
Tolerance delay2	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block Sequencer.

Test results			
Time step	1	2	3
Mask parameters			
Delay1	0.1	0.1	0.1
Delay2	0.2	0.2	0.2
Delay3	1	1	1
Delay4	1.7	1.7	1.7
ts_fact	1	2	10
Controller parameters			
delay3	10000	5000	1000
delay4	17000	8500	1700
delay1	1000	500	100
delay2	2000	1000	200
Exp. delay3	10000	5000	1000
Exp. delay4	17000	8500	1700
Exp. delay1	1000	500	100
Exp. delay2	2000	1000	200

Test settings	
Tolerance delay3	±0,0000e+00
Tolerance delay4	±0,0000e+00
Tolerance delay1	±0,0000e+00
Tolerance delay2	±0,0000e+00

Test statistics	
Min CPU cycles	7397
Max CPU cycles	7489
Avg CPU cycles	7437

Verification: Sequencer Bool CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for General block Sequencer.

Test results						
Time step	1	2	3	4	...	16
CPU cycles	107	99	109	102	...	79
Inputs						
Start (DSP)	0	1	1	1	...	0
Start	0	1	1	1	...	0
Parameters						
Delay1	0					
Delay2	0					
Delay3	0.001					
Delay4	0					
ts_fact	1					
Outputs						
Out1	0	0	1	1	...	0
Out2	0	0	0	1	...	0
Out3	0	0	0	0	...	0
Out4	0	1	1	1	...	0
Exp. Out1	0	0	1	1	...	0
Exp. Out2	0	0	0	1	...	0
Exp. Out3	0	0	0	0	...	0
Exp. Out4	0	1	1	1	...	0
Out1 (DSP)	0	0	1	1	...	0
Out2 (DSP)	0	0	0	1	...	0
Out3 (DSP)	0	0	0	0	...	0
Out4 (DSP)	0	1	1	1	...	0
Exp. Out1 (DSP)	0	0	1	1	...	0
Exp. Out2 (DSP)	0	0	0	1	...	0
Exp. Out3 (DSP)	0	0	0	0	...	0
Exp. Out4 (DSP)	0	1	1	1	...	0

Test settings	
Tolerance Out1	±0,0000e+00 (±0 LSB)
Tolerance Out2	±0,0000e+00 (±0 LSB)
Tolerance Out3	±0,0000e+00 (±0 LSB)
Tolerance Out4	±0,0000e+00 (±0 LSB)

Test statistics	
Min CPU cycles	79
Max CPU cycles	109
Avg CPU cycles	101

Test case: Conversion test **OK**

Conversion test for General block Sequencer.

Test results			
Time step	1	2	3
Mask parameters			
Delay1	0.1	0.1	0.1
Delay2	0.2	0.2	0.2
Delay3	1	1	1
Delay4	1.7	1.7	1.7
ts_fact	1	2	10
Controller parameters			
delay3	10000	5000	1000
delay4	17000	8500	1700
delay1	1000	500	100
delay2	2000	1000	200
Exp. delay3	10000	5000	1000
Exp. delay4	17000	8500	1700
Exp. delay1	1000	500	100
Exp. delay2	2000	1000	200

Test settings	
Tolerance delay3	±0,0000e+00
Tolerance delay4	±0,0000e+00
Tolerance delay1	±0,0000e+00
Tolerance delay2	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block Sequencer.

Test results			
Time step	1	2	3
Mask parameters			
Delay1	0.1	0.1	0.1
Delay2	0.2	0.2	0.2
Delay3	1	1	1
Delay4	1.7	1.7	1.7
ts_fact	1	2	10
Controller parameters			
delay3	10000	5000	1000
delay4	17000	8500	1700
delay1	1000	500	100
delay2	2000	1000	200
Exp. delay3	10000	5000	1000
Exp. delay4	17000	8500	1700
Exp. delay1	1000	500	100
Exp. delay2	2000	1000	200

Test settings	
Tolerance delay3	±0,0000e+00
Tolerance delay4	±0,0000e+00
Tolerance delay1	±0,0000e+00
Tolerance delay2	±0,0000e+00

Test statistics	
Min CPU cycles	1037
Max CPU cycles	1300
Avg CPU cycles	1136

Verification: Sequencer Bool CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for General block Sequencer.

Test results						
Time step	1	2	3	4	...	16
CPU cycles	55	111	107	99	...	55
Inputs						
Start (DSP)	0	1	1	1	...	0
Start	0	1	1	1	...	0
Parameters						
Delay1	0					
Delay2	0					
Delay3	0.001					
Delay4	0					
ts_fact	1					
Outputs						
Out1	0	0	1	1	...	0
Out2	0	0	0	1	...	0
Out3	0	0	0	0	...	0
Out4	0	1	1	1	...	0
Exp. Out1	0	0	1	1	...	0
Exp. Out2	0	0	0	1	...	0
Exp. Out3	0	0	0	0	...	0
Exp. Out4	0	1	1	1	...	0
Out1 (DSP)	0	0	1	1	...	0
Out2 (DSP)	0	0	0	1	...	0
Out3 (DSP)	0	0	0	0	...	0
Out4 (DSP)	0	1	1	1	...	0
Exp. Out1 (DSP)	0	0	1	1	...	0
Exp. Out2 (DSP)	0	0	0	1	...	0
Exp. Out3 (DSP)	0	0	0	0	...	0
Exp. Out4 (DSP)	0	1	1	1	...	0

Test settings	
Tolerance Out1	±0,0000e+00 (±0 LSB)
Tolerance Out2	±0,0000e+00 (±0 LSB)
Tolerance Out3	±0,0000e+00 (±0 LSB)
Tolerance Out4	±0,0000e+00 (±0 LSB)

Test statistics	
Min CPU cycles	55
Max CPU cycles	111
Avg CPU cycles	94

Test case: Conversion test **OK**

Conversion test for General block Sequencer.

Test results			
Time step	1	2	3
Mask parameters			
Delay1	0.1	0.1	0.1
Delay2	0.2	0.2	0.2
Delay3	1	1	1
Delay4	1.7	1.7	1.7
ts_fact	1	2	10
Controller parameters			
delay3	10000	5000	1000
delay4	17000	8500	1700
delay1	1000	500	100
delay2	2000	1000	200
Exp. delay3	10000	5000	1000
Exp. delay4	17000	8500	1700
Exp. delay1	1000	500	100
Exp. delay2	2000	1000	200

Test settings	
Tolerance delay3	±0,0000e+00
Tolerance delay4	±0,0000e+00
Tolerance delay1	±0,0000e+00
Tolerance delay2	±0,0000e+00

Test case: Conversion-on-Target test **OK**

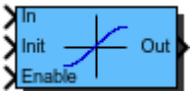
Conversion-on-Target test for General block Sequencer.

Test results			
Time step	1	2	3
Mask parameters			
Delay1	0.1	0.1	0.1
Delay2	0.2	0.2	0.2
Delay3	1	1	1
Delay4	1.7	1.7	1.7
ts_fact	1	2	10
Controller parameters			
delay3	10000	5000	1000
delay4	17000	8500	1700
delay1	1000	500	100
delay2	2000	1000	200
Exp. delay3	10000	5000	1000
Exp. delay4	17000	8500	1700
Exp. delay1	1000	500	100
Exp. delay2	2000	1000	200

Test settings	
Tolerance delay3	±0,0000e+00
Tolerance delay4	±0,0000e+00
Tolerance delay1	±0,0000e+00
Tolerance delay2	±0,0000e+00

Test statistics	
Min CPU cycles	2737
Max CPU cycles	2742
Avg CPU cycles	2740

Block: Sin2Limiter



Limitation of rising and falling rate with sin^2 characteristic.
Note: A running limitation process can not be interrupted!
Function of Enable:
0: rate limiting disabled, signal is set to zero
1: rate limiting enabled, signal is rate limited
0->1: preload of output with value from init input

Inports	
In	
Init	Value which is loaded at rising flanke of enable signal
Enable	Enable == 0: Deactivation of block; Out is set to zero. Enable != 0: Activation of block; Out is rate limited. Enable 0->1: Preloading of output; Out is set to value of Init input

Outports	
Out	

Mask Parameters		
Name	**ID**	**Description**
Tr	1	Rising time in seconds. Slew rate will be 1/Tr
Tf	2	Falling time in seconds. Slew rate will be 1/Tf
ts_fact	3	Multiplication factor of base sampling time (in integer format)

Description:

Rising and falling time refer to a step from 0 to 1. Entries for *Tr: Rising time* and *Tf: Falling time* smaller than the actual sample time will be limited to the sample time internally.

Implementations:

FiP16 16 Bit Fixed Point Implementation
FiP32 32 Bit Fixed Point Implementation
Float32 32 Bit Floating Point Implementation
Float64 64 Bit Floating Point Implementation

Implementation: FiP16

16 Bit Fixed Point Implementation

Inports Data Type	
In	int16
Init	int16
Enable	bool

Outports Data Type	
Out	int16

Implementation: FiP32

32 Bit Fixed Point Implementation

Inports Data Type	
In	int32
Init	int32
Enable	bool

Outports Data Type	
Out	int32

Implementation: Float32

32 Bit Floating Point Implementation

Inports Data Type	
In	float32
Init	float32
Enable	bool

Outports Data Type	
Out	float32

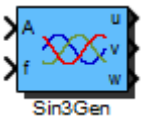
Implementation: Float64

64 Bit Floating Point Implementation

Inports Data Type	
In	float64
Init	float64
Enable	bool

Outports Data Type	
Out	float64

Block: Sin3Gen



Generation of a 3 sine waves with amplitude (A) and frequency (f).

Inports	
A	Amplitude
f	Frequency

Outports	
u	Sine wave output phase u
v	Sine wave output phase v
w	Sine wave output phase w

Mask Parameters		
Name	**ID**	**Description**
fmax	1	Maximum Frequency in Hz
Offset	2	Offset
ts_fact	3	Multiplication factor of base sampling time (in integer format)

Description:

Calculation fixed point implementation:

$$
\begin{aligned}
u_k &= A_k \sin\left(2 f_k f_{\max} k T_\mathrm{s}\right) + A_\mathrm{offset} \\
v_k &= A_k \sin\left(2 f_k f_{\max} k T_\mathrm{s} - \frac{2\pi}{3}\right) + A_\mathrm{offset} \\
w_k &= A_k \sin\left(2 f_k f_{\max} k T_\mathrm{s} + \frac{2\pi}{3}\right) + A_\mathrm{offset}
\end{aligned}
$$

For sine calculation a lookup table with 256 entries is used. This results in a short computation time but with the downside of reduced accuracy for the FiP32 implementation.

Calculation floating point implementation (parameter *f_max* is ignored):

$$
\begin{aligned}
u_k &= A_k \sin\left(2\pi f_k k T_\mathrm{s}\right) + A_\mathrm{offset} \\
v_k &= A_k \sin\left(2\pi f_k k T_\mathrm{s} - \frac{2\pi}{3}\right) + A_\mathrm{offset} \\
w_k &= A_k \sin\left(2\pi f_k k T_\mathrm{s} + \frac{2\pi}{3}\right) + A_\mathrm{offset}
\end{aligned}
$$

Implementations:

FiP16	16 Bit Fixed Point Implementation
FiP32	32 Bit Fixed Point Implementation
Float32	32 Bit Floating Point Implementation
Float64	64 Bit Floating Point Implementation

Implementation: FiP16

16 Bit Fixed Point Implementation

Inports Data Type	
A	int16
f	int16

Outports Data Type	
u	int16
v	int16
w	int16

Implementation: FiP32

32 Bit Fixed Point Implementation

Inports Data Type	
A	int32
f	int32

Outports Data Type	
u	int32
v	int32
w	int32

Implementation: Float32

32 Bit Floating Point Implementation

Inports Data Type	
A	float32
f	float32

Outports Data Type	
u	float32
v	float32
w	float32

Implementation: Float64

64 Bit Floating Point Implementation

Inports Data Type	
A	float64
f	float64

Outports Data Type	
u	float64
v	float64
w	float64

Verification: Sin3Gen FiP16 CPU TMS320F28335

Date of Test 2026-06-19

Target controller TMS320F28335

Test case: Inport test OK

Inport test for General block Sin3Gen.

Test results						
Time step	1	2	3	4	...	200
CPU cycles	230	230	230	230	...	230
Inputs						
A (DSP)	164	328	492	655	...	32767
f (DSP)	32767	32767	32767	32767	...	32767
A	0.005	0.01	0.015	0.02	...	1
f	1	1	1	1	...	1
Parameters						
fmax	200					
Offset	0.13					
ts_fact	1					
Outputs						
u	0.131	0.133	0.136	0.14	...	0.135
v	0.125	0.12	0.115	0.11	...	-0.739
w	0.134	0.137	0.139	0.14	...	0.993
Exp. u	0.131	0.132	0.136	0.14	...	0.13
Exp. v	0.125	0.12	0.115	0.11	...	-0.736
Exp. w	0.134	0.137	0.139	0.14	...	0.996
u (DSP)	4281	4342	4441	4576	...	4435
v (DSP)	4109	3944	3773	3605	...	-24204
w (DSP)	4391	4494	4566	4599	...	32545
Exp. u (DSP)	4280	4341	4441	4576	...	4260
Exp. v (DSP)	4109	3944	3774	3605	...	-24118
Exp. w (DSP)	4390	4494	4565	4599	...	32638

Test settings	
Tolerance u	±5,3711e-03 (±176 LSB)
Tolerance v	±5,3711e-03 (±176 LSB)
Tolerance w	±5,3711e-03 (±176 LSB)

Test statistics	
Min CPU cycles	227
Max CPU cycles	230
Avg CPU cycles	229

Verification: Sin3Gen FiP16 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for General block Sin3Gen.

Test results						
Time step	1	2	3	4	...	200
CPU cycles	181	181	181	181	...	181
Inputs						
A (DSP)	164	328	492	655	...	32767
f (DSP)	32767	32767	32767	32767	...	32767
A	0.005	0.01	0.015	0.02	...	1
f	1	1	1	1	...	1
Parameters						
fmax	200					
Offset	0.13					
ts_fact	1					
Outputs						
u	0.131	0.133	0.136	0.14	...	0.135
v	0.125	0.12	0.115	0.11	...	-0.739
w	0.134	0.137	0.139	0.14	...	0.993
Exp. u	0.131	0.132	0.136	0.14	...	0.13
Exp. v	0.125	0.12	0.115	0.11	...	-0.736
Exp. w	0.134	0.137	0.139	0.14	...	0.996
u (DSP)	4281	4342	4441	4576	...	4435
v (DSP)	4109	3944	3773	3605	...	-24204
w (DSP)	4391	4494	4566	4599	...	32545
Exp. u (DSP)	4280	4341	4441	4576	...	4260
Exp. v (DSP)	4109	3944	3774	3605	...	-24118
Exp. w (DSP)	4390	4494	4565	4599	...	32638

Test settings	
Tolerance u	±5,3711e-03 (±176 LSB)
Tolerance v	±5,3711e-03 (±176 LSB)
Tolerance w	±5,3711e-03 (±176 LSB)

Test statistics	
Min CPU cycles	175
Max CPU cycles	181
Avg CPU cycles	180

Verification: Sin3Gen FiP16 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for General block Sin3Gen.

Test results						
Time step	1	2	3	4	...	200
CPU cycles	215	211	211	216	...	216
Inputs						
A (DSP)	164	328	492	655	...	32767
f (DSP)	32767	32767	32767	32767	...	32767
A	0.005	0.01	0.015	0.02	...	1
f	1	1	1	1	...	1
Parameters						
fmax	200					
Offset	0.13					
ts_fact	1					
Outputs						
u	0.131	0.133	0.136	0.14	...	0.135
v	0.125	0.12	0.115	0.11	...	-0.739
w	0.134	0.137	0.139	0.14	...	0.993
Exp. u	0.131	0.132	0.136	0.14	...	0.13
Exp. v	0.125	0.12	0.115	0.11	...	-0.736
Exp. w	0.134	0.137	0.139	0.14	...	0.996
u (DSP)	4281	4342	4441	4576	...	4435
v (DSP)	4109	3944	3773	3605	...	-24204
w (DSP)	4391	4494	4566	4599	...	32545
Exp. u (DSP)	4280	4341	4441	4576	...	4260
Exp. v (DSP)	4109	3944	3774	3605	...	-24118
Exp. w (DSP)	4390	4494	4565	4599	...	32638

Test settings	
Tolerance u	±5,3711e-03 (±176 LSB)
Tolerance v	±5,3711e-03 (±176 LSB)
Tolerance w	±5,3711e-03 (±176 LSB)

Test statistics	
Min CPU cycles	211
Max CPU cycles	216
Avg CPU cycles	214

Verification: Sin3Gen FiP16 CPU STM32F072RB

Date of Test 2026-06-19

Target controller STM32F072RB

Test case: Inport test OK

Inport test for General block Sin3Gen.

Test results						
Time step	1	2	3	4	...	200
CPU cycles	249	249	249	249	...	249
Inputs						
A (DSP)	164	328	492	655	...	32767
f (DSP)	32767	32767	32767	32767	...	32767
A	0.005	0.01	0.015	0.02	...	1
f	1	1	1	1	...	1
Parameters						
fmax	200					
Offset	0.13					
ts_fact	1					
Outputs						
u	0.131	0.133	0.136	0.14	...	0.135
v	0.125	0.12	0.115	0.11	...	-0.739
w	0.134	0.137	0.139	0.14	...	0.993
Exp. u	0.131	0.132	0.136	0.14	...	0.13
Exp. v	0.125	0.12	0.115	0.11	...	-0.736
Exp. w	0.134	0.137	0.139	0.14	...	0.996
u (DSP)	4281	4342	4441	4576	...	4435
v (DSP)	4109	3944	3773	3605	...	-24204
w (DSP)	4391	4494	4566	4599	...	32545
Exp. u (DSP)	4280	4341	4441	4576	...	4260
Exp. v (DSP)	4109	3944	3774	3605	...	-24118
Exp. w (DSP)	4390	4494	4565	4599	...	32638

Test settings	
Tolerance u	±5,3711e-03 (±176 LSB)
Tolerance v	±5,3711e-03 (±176 LSB)
Tolerance w	±5,3711e-03 (±176 LSB)

Test statistics	
Min CPU cycles	249
Max CPU cycles	308
Avg CPU cycles	249

Verification: Sin3Gen FiP16 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for General block Sin3Gen.

Test results						
Time step	1	2	3	4	...	200
CPU cycles	139	139	139	139	...	139
Inputs						
A (DSP)	164	328	492	655	...	32767
f (DSP)	32767	32767	32767	32767	...	32767
A	0.005	0.01	0.015	0.02	...	1
f	1	1	1	1	...	1
Parameters						
fmax	200					
Offset	0.13					
ts_fact	1					
Outputs						
u	0.131	0.133	0.136	0.14	...	0.135
v	0.125	0.12	0.115	0.11	...	-0.739
w	0.134	0.137	0.139	0.14	...	0.993
Exp. u	0.131	0.132	0.136	0.14	...	0.13
Exp. v	0.125	0.12	0.115	0.11	...	-0.736
Exp. w	0.134	0.137	0.139	0.14	...	0.996
u (DSP)	4281	4342	4441	4576	...	4435
v (DSP)	4109	3944	3773	3605	...	-24204
w (DSP)	4391	4494	4566	4599	...	32545
Exp. u (DSP)	4280	4341	4441	4576	...	4260
Exp. v (DSP)	4109	3944	3774	3605	...	-24118
Exp. w (DSP)	4390	4494	4565	4599	...	32638

Test settings	
Tolerance u	±5,3711e-03 (±176 LSB)
Tolerance v	±5,3711e-03 (±176 LSB)
Tolerance w	±5,3711e-03 (±176 LSB)

Test statistics	
Min CPU cycles	139
Max CPU cycles	139
Avg CPU cycles	139

Verification: Sin3Gen FiP16 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for General block Sin3Gen.

Test results						
Time step	1	2	3	4	...	200
CPU cycles	228	228	228	228	...	228
Inputs						
A (DSP)	164	328	492	655	...	32767
f (DSP)	32767	32767	32767	32767	...	32767
A	0.005	0.01	0.015	0.02	...	1
f	1	1	1	1	...	1
Parameters						
fmax	200					
Offset	0.13					
ts_fact	1					
Outputs						
u	0.131	0.133	0.136	0.14	...	0.135
v	0.125	0.12	0.115	0.11	...	-0.739
w	0.134	0.137	0.139	0.14	...	0.993
Exp. u	0.131	0.132	0.136	0.14	...	0.13
Exp. v	0.125	0.12	0.115	0.11	...	-0.736
Exp. w	0.134	0.137	0.139	0.14	...	0.996
u (DSP)	4281	4342	4441	4576	...	4435
v (DSP)	4109	3944	3773	3605	...	-24204
w (DSP)	4391	4494	4566	4599	...	32545
Exp. u (DSP)	4280	4341	4441	4576	...	4260
Exp. v (DSP)	4109	3944	3774	3605	...	-24118
Exp. w (DSP)	4390	4494	4565	4599	...	32638

Test settings	
Tolerance u	±5,3711e-03 (±176 LSB)
Tolerance v	±5,3711e-03 (±176 LSB)
Tolerance w	±5,3711e-03 (±176 LSB)

Test statistics	
Min CPU cycles	227
Max CPU cycles	228
Avg CPU cycles	227

Verification: Sin3Gen FiP16 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test — OK

Inport test for General block Sin3Gen.

Test results						
Time step	1	2	3	4	...	200
CPU cycles	257	211	211	211	...	211
Inputs						
A (DSP)	164	328	492	655	...	32767
f (DSP)	32767	32767	32767	32767	...	32767
A	0.005	0.01	0.015	0.02	...	1
f	1	1	1	1	...	1
Parameters						
fmax	200					
Offset	0.13					
ts_fact	1					
Outputs						
u	0.131	0.133	0.136	0.14	...	0.135
v	0.125	0.12	0.115	0.11	...	-0.739
w	0.134	0.137	0.139	0.14	...	0.993
Exp. u	0.131	0.132	0.136	0.14	...	0.13
Exp. v	0.125	0.12	0.115	0.11	...	-0.736
Exp. w	0.134	0.137	0.139	0.14	...	0.996
u (DSP)	4281	4342	4441	4576	...	4435
v (DSP)	4109	3944	3773	3605	...	-24204
w (DSP)	4391	4494	4566	4599	...	32545
Exp. u (DSP)	4280	4341	4441	4576	...	4260
Exp. v (DSP)	4109	3944	3774	3605	...	-24118
Exp. w (DSP)	4390	4494	4565	4599	...	32638

Test settings	
Tolerance u	±5,3711e-03 (±176 LSB)
Tolerance v	±5,3711e-03 (±176 LSB)
Tolerance w	±5,3711e-03 (±176 LSB)

Test statistics	
Min CPU cycles	211
Max CPU cycles	257
Avg CPU cycles	211

Verification: Sin3Gen FiP16 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for General block Sin3Gen.

Test results						
Time step	1	2	3	4	...	200
CPU cycles	202	202	202	205	...	202
Inputs						
A (DSP)	164	328	492	655	...	32767
f (DSP)	32767	32767	32767	32767	...	32767
A	0.005	0.01	0.015	0.02	...	1
f	1	1	1	1	...	1
Parameters						
fmax	200					
Offset	0.13					
ts_fact	1					
Outputs						
u	0.131	0.133	0.136	0.14	...	0.135
v	0.125	0.12	0.115	0.11	...	-0.739
w	0.134	0.137	0.139	0.14	...	0.993
Exp. u	0.131	0.132	0.136	0.14	...	0.13
Exp. v	0.125	0.12	0.115	0.11	...	-0.736
Exp. w	0.134	0.137	0.139	0.14	...	0.996
u (DSP)	4281	4342	4441	4576	...	4435
v (DSP)	4109	3944	3773	3605	...	-24204
w (DSP)	4391	4494	4566	4599	...	32545
Exp. u (DSP)	4280	4341	4441	4576	...	4260
Exp. v (DSP)	4109	3944	3774	3605	...	-24118
Exp. w (DSP)	4390	4494	4565	4599	...	32638

Test settings	
Tolerance u	±5,3711e-03 (±176 LSB)
Tolerance v	±5,3711e-03 (±176 LSB)
Tolerance w	±5,3711e-03 (±176 LSB)

Test statistics	
Min CPU cycles	196
Max CPU cycles	208
Avg CPU cycles	203

Verification: Sin3Gen FiP32 CPU TMS320F28335

Date of Test 2026-06-19

Target controller TMS320F28335

Test case: Inport test OK

Inport test for General block Sin3Gen.

Test results				
Time step	1	2	...	200
CPU cycles	627	627	...	627
Inputs				
A (DSP)	10737418	21474836	...	2147483647
f (DSP)	2147483647	2147483647	...	2147483647
A	0.005	0.01	...	1
f	1	1	...	1
Parameters				
fmax	200			
Offset	0.13			
ts_fact	1			
Outputs				
u	0.131	0.132	...	0.13
v	0.125	0.12	...	-0.736
w	0.134	0.137	...	0.996
Exp. u	0.131	0.132	...	0.13
Exp. v	0.125	0.12	...	-0.736
Exp. w	0.134	0.137	...	0.996
u (DSP)	280518584	284513150	...	279172924
v (DSP)	269274943	258489642	...	-1580478263
w (DSP)	287724911	294514926	...	2138823959
Exp. u (DSP)	280518630	284513449	...	279172874
Exp. v (DSP)	269274444	258489116	...	-1580602519
Exp. w (DSP)	287725549	294516058	...	2138948268

Test settings	
Tolerance u	±6,9849e-05 (±150000 LSB)
Tolerance v	±6,9849e-05 (±150000 LSB)
Tolerance w	±6,9849e-05 (±150000 LSB)

Test statistics	
Min CPU cycles	575
Max CPU cycles	627
Avg CPU cycles	624

Verification: Sin3Gen FiP32 CPU TM4C123GH6

Date of Test 2026-06-19

Target controller TM4C123GH6

Test case: Inport test OK

Inport test for General block Sin3Gen.

Test results				
Time step	1	2	...	200
CPU cycles	189	189	...	189
Inputs				
A (DSP)	10737418	21474836	...	2147483647
f (DSP)	2147483647	2147483647	...	2147483647
A	0.005	0.01	...	1
f	1	1	...	1
Parameters				
fmax	200			
Offset	0.13			
ts_fact	1			
Outputs				
u	0.131	0.132	...	0.13
v	0.125	0.12	...	-0.736
w	0.134	0.137	...	0.996
Exp. u	0.131	0.132	...	0.13
Exp. v	0.125	0.12	...	-0.736
Exp. w	0.134	0.137	...	0.996
u (DSP)	280518584	284513150	...	279172924
v (DSP)	269274943	258489642	...	-1580478263
w (DSP)	287724911	294514926	...	2138823959
Exp. u (DSP)	280518630	284513449	...	279172874
Exp. v (DSP)	269274444	258489116	...	-1580602519
Exp. w (DSP)	287725549	294516058	...	2138948268

Test settings	
Tolerance u	±6,9849e-05 (±150000 LSB)
Tolerance v	±6,9849e-05 (±150000 LSB)
Tolerance w	±6,9849e-05 (±150000 LSB)

Test statistics	
Min CPU cycles	183
Max CPU cycles	189
Avg CPU cycles	188

Verification: Sin3Gen FiP32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for General block Sin3Gen.

Test results				
Time step	1	2	...	200
CPU cycles	288	283	...	283
Inputs				
A (DSP)	10737418	21474836	...	2147483647
f (DSP)	2147483647	2147483647	...	2147483647
A	0.005	0.01	...	1
f	1	1	...	1
Parameters				
fmax	200			
Offset	0.13			
ts_fact	1			
Outputs				
u	0.131	0.132	...	0.13
v	0.125	0.12	...	-0.736
w	0.134	0.137	...	0.996
Exp. u	0.131	0.132	...	0.13
Exp. v	0.125	0.12	...	-0.736
Exp. w	0.134	0.137	...	0.996
u (DSP)	280518584	284513150	...	279172924
v (DSP)	269274943	258489642	...	-1580478263
w (DSP)	287724911	294514926	...	2138823959
Exp. u (DSP)	280518630	284513449	...	279172874
Exp. v (DSP)	269274444	258489116	...	-1580602519
Exp. w (DSP)	287725549	294516058	...	2138948268

Test settings	
Tolerance u	±6,9849e-05 (±150000 LSB)
Tolerance v	±6,9849e-05 (±150000 LSB)
Tolerance w	±6,9849e-05 (±150000 LSB)

Test statistics	
Min CPU cycles	283
Max CPU cycles	288
Avg CPU cycles	285

Verification: Sin3Gen FiP32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for General block Sin3Gen.

Test results				
Time step	1	2	...	200
CPU cycles	789	789	...	795
Inputs				
A (DSP)	10737418	21474836	...	2147483647
f (DSP)	2147483647	2147483647	...	2147483647
A	0.005	0.01	...	1
f	1	1	...	1
Parameters				
fmax	200			
Offset	0.13			
ts_fact	1			
Outputs				
u	0.131	0.132	...	0.13
v	0.125	0.12	...	-0.736
w	0.134	0.137	...	0.996
Exp. u	0.131	0.132	...	0.13
Exp. v	0.125	0.12	...	-0.736
Exp. w	0.134	0.137	...	0.996
u (DSP)	280518584	284513150	...	279172924
v (DSP)	269274943	258489642	...	-1580478263
w (DSP)	287724911	294514926	...	2138823959
Exp. u (DSP)	280518630	284513449	...	279172874
Exp. v (DSP)	269274444	258489116	...	-1580602519
Exp. w (DSP)	287725549	294516058	...	2138948268

Test settings	
Tolerance u	±6,9849e-05 (±150000 LSB)
Tolerance v	±6,9849e-05 (±150000 LSB)
Tolerance w	±6,9849e-05 (±150000 LSB)

Test statistics	
Min CPU cycles	789
Max CPU cycles	862
Avg CPU cycles	795

Verification: Sin3Gen FiP32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for General block Sin3Gen.

Test results				
Time step	1	2	...	200
CPU cycles	215	215	...	213
Inputs				
A (DSP)	10737418	21474836	...	2147483647
f (DSP)	2147483647	2147483647	...	2147483647
A	0.005	0.01	...	1
f	1	1	...	1
Parameters				
fmax	200			
Offset	0.13			
ts_fact	1			
Outputs				
u	0.131	0.132	...	0.13
v	0.125	0.12	...	-0.736
w	0.134	0.137	...	0.996
Exp. u	0.131	0.132	...	0.13
Exp. v	0.125	0.12	...	-0.736
Exp. w	0.134	0.137	...	0.996
u (DSP)	280518584	284513150	...	279172924
v (DSP)	269274943	258489642	...	-1580478263
w (DSP)	287724911	294514926	...	2138823959
Exp. u (DSP)	280518630	284513449	...	279172874
Exp. v (DSP)	269274444	258489116	...	-1580602519
Exp. w (DSP)	287725549	294516058	...	2138948268

Test settings	
Tolerance u	±6,9849e-05 (±150000 LSB)
Tolerance v	±6,9849e-05 (±150000 LSB)
Tolerance w	±6,9849e-05 (±150000 LSB)

Test statistics	
Min CPU cycles	213
Max CPU cycles	218
Avg CPU cycles	214

Verification: Sin3Gen FiP32 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for General block Sin3Gen.

Test results				
Time step	1	2	...	200
CPU cycles	1164	1164	...	1164
Inputs				
A (DSP)	10737418	21474836	...	2147483647
f (DSP)	2147483647	2147483647	...	2147483647
A	0.005	0.01	...	1
f	1	1	...	1
Parameters				
fmax	200			
Offset	0.13			
ts_fact	1			
Outputs				
u	0.131	0.132	...	0.13
v	0.125	0.12	...	-0.736
w	0.134	0.137	...	0.996
Exp. u	0.131	0.132	...	0.13
Exp. v	0.125	0.12	...	-0.736
Exp. w	0.134	0.137	...	0.996
u (DSP)	280518584	284513150	...	279172924
v (DSP)	269274943	258489642	...	-1580478263
w (DSP)	287724911	294514926	...	2138823959
Exp. u (DSP)	280518630	284513449	...	279172874
Exp. v (DSP)	269274444	258489116	...	-1580602519
Exp. w (DSP)	287725549	294516058	...	2138948268

Test settings	
Tolerance u	±6,9849e-05 (±150000 LSB)
Tolerance v	±6,9849e-05 (±150000 LSB)
Tolerance w	±6,9849e-05 (±150000 LSB)

Test statistics	
Min CPU cycles	1157
Max CPU cycles	1172
Avg CPU cycles	1164

Verification: Sin3Gen FiP32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for General block Sin3Gen.

Test results				
Time step	1	2	...	200
CPU cycles	379	297	...	299
Inputs				
A (DSP)	10737418	21474836	...	2147483647
f (DSP)	2147483647	2147483647	...	2147483647
A	0.005	0.01	...	1
f	1	1	...	1
Parameters				
fmax	200			
Offset	0.13			
ts_fact	1			
Outputs				
u	0.131	0.132	...	0.13
v	0.125	0.12	...	-0.736
w	0.134	0.137	...	0.996
Exp. u	0.131	0.132	...	0.13
Exp. v	0.125	0.12	...	-0.736
Exp. w	0.134	0.137	...	0.996
u (DSP)	280518584	284513150	...	279172924
v (DSP)	269274943	258489642	...	-1580478263
w (DSP)	287724911	294514926	...	2138823959
Exp. u (DSP)	280518630	284513449	...	279172874
Exp. v (DSP)	269274444	258489116	...	-1580602519
Exp. w (DSP)	287725549	294516058	...	2138948268

Test settings	
Tolerance u	±6,9849e-05 (±150000 LSB)
Tolerance v	±6,9849e-05 (±150000 LSB)
Tolerance w	±6,9849e-05 (±150000 LSB)

Test statistics	
Min CPU cycles	297
Max CPU cycles	379
Avg CPU cycles	298

Verification: Sin3Gen FiP32 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

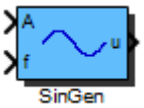
Inport test for General block Sin3Gen.

Test results				
Time step	1	2	...	200
CPU cycles	551	542	...	547
Inputs				
A (DSP)	10737418	21474836	...	2147483647
f (DSP)	2147483647	2147483647	...	2147483647
A	0.005	0.01	...	1
f	1	1	...	1
Parameters				
fmax	200			
Offset	0.13			
ts_fact	1			
Outputs				
u	0.131	0.132	...	0.13
v	0.125	0.12	...	-0.736
w	0.134	0.137	...	0.996
Exp. u	0.131	0.132	...	0.13
Exp. v	0.125	0.12	...	-0.736
Exp. w	0.134	0.137	...	0.996
u (DSP)	280518584	284513150	...	279172924
v (DSP)	269274943	258489642	...	-1580478263
w (DSP)	287724911	294514926	...	2138823959
Exp. u (DSP)	280518630	284513449	...	279172874
Exp. v (DSP)	269274444	258489116	...	-1580602519
Exp. w (DSP)	287725549	294516058	...	2138948268

Test settings	
Tolerance u	±6,9849e-05 (±150000 LSB)
Tolerance v	±6,9849e-05 (±150000 LSB)
Tolerance w	±6,9849e-05 (±150000 LSB)

Test statistics	
Min CPU cycles	496
Max CPU cycles	551
Avg CPU cycles	543

Block: SinGen



Generation of a sine wave with amplitude (A) and frequency (f).

Inports	
A	Amplitude
f	Frequency

Outports	
u	Sine wave output

Mask Parameters		
Name	**ID**	**Description**
fmax	1	Maximum Frequency in Hz
Offset	2	Offset
Phase	3	Phase [-Pi..Pi]
ts_fact	4	Multiplication factor of base sampling time (in integer format)

Description:

Calculation fixed point implementation:

$$u_k = A_k \sin\left(2 f_k f_{\max} k T_\mathrm{s} + \phi_\mathrm{phase}\right) + A_\mathrm{offset}$$

For sine calculation a lookup table with 256 entries is used. This results in a short computation time but with the downside of reduced accuracy for the FiP32 implementation.

Calculation floating point implementation (parameter *f_max* is ignored):

$$u_k = A_k \sin\left(2\pi f_k k T_\mathrm{s} + \phi_\mathrm{phase}\right) + A_\mathrm{offset}$$

Implementations:

FiP16 16 Bit Fixed Point Implementation
FiP32 32 Bit Fixed Point Implementation
Float32 32 Bit Floating Point Implementation
Float64 64 Bit Floating Point Implementation

Implementation: FiP16

16 Bit Fixed Point Implementation

Inports Data Type	
A	int16
f	int16

Outports Data Type	
u	int16

Implementation: FiP32

32 Bit Fixed Point Implementation

Inports Data Type	
A	int32
f	int32

Outports Data Type	
u	int32

Implementation: Float32

32 Bit Floating Point Implementation

Inports Data Type	
A	float32
f	float32

Outports Data Type	
u	float32

Implementation: Float64

64 Bit Floating Point Implementation

Inports Data Type	
A	float64
f	float64

Outports Data Type	
u	float64

Verification: SinGen FiP16 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for General block SinGen.

Test results						
Time step	1	2	3	4	...	200
CPU cycles	117	117	117	117	...	117
Inputs						
A (DSP)	164	328	492	655	...	32767
f (DSP)	32767	32767	32767	32767	...	32767
A	0.005	0.01	0.015	0.02	...	1
f	1	1	1	1	...	1
Parameters						
fmax	200					
Offset	0.13					
Phase	0					
ts_fact	1					
Outputs						
u	0.131	0.133	0.136	0.14	...	0.135
Exp. u	0.131	0.132	0.136	0.14	...	0.13
u (DSP)	4281	4342	4441	4576	...	4435
Exp. u (DSP)	4280	4341	4441	4576	...	4260

Test settings	
Tolerance u	±5,3711e-03 (±176 LSB)

Test statistics	
Min CPU cycles	117
Max CPU cycles	117
Avg CPU cycles	117

Verification: SinGen FiP16 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test — OK

Inport test for General block SinGen.

Test results						
Time step	1	2	3	4	...	200
CPU cycles	87	87	87	87	...	87
Inputs						
A (DSP)	164	328	492	655	...	32767
f (DSP)	32767	32767	32767	32767	...	32767
A	0.005	0.01	0.015	0.02	...	1
f	1	1	1	1	...	1
Parameters						
fmax	200					
Offset	0.13					
Phase	0					
ts_fact	1					
Outputs						
u	0.131	0.133	0.136	0.14	...	0.135
Exp. u	0.131	0.132	0.136	0.14	...	0.13
u (DSP)	4281	4342	4441	4576	...	4435
Exp. u (DSP)	4280	4341	4441	4576	...	4260

Test settings	
Tolerance u	±5,3711e-03 (±176 LSB)

Test statistics	
Min CPU cycles	87
Max CPU cycles	87
Avg CPU cycles	87

Verification: SinGen FiP16 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test **OK**

Inport test for General block SinGen.

Test results						
Time step	1	2	3	4	...	200
CPU cycles	136	130	130	130	...	130
Inputs						
A (DSP)	164	328	492	655	...	32767
f (DSP)	32767	32767	32767	32767	...	32767
A	0.005	0.01	0.015	0.02	...	1
f	1	1	1	1	...	1
Parameters						
fmax	200					
Offset	0.13					
Phase	0					
ts_fact	1					
Outputs						
u	0.131	0.133	0.136	0.14	...	0.135
Exp. u	0.131	0.132	0.136	0.14	...	0.13
u (DSP)	4281	4342	4441	4576	...	4435
Exp. u (DSP)	4280	4341	4441	4576	...	4260

Test settings	
Tolerance u	±5,3711e-03 (±176 LSB)

Test statistics	
Min CPU cycles	130
Max CPU cycles	136
Avg CPU cycles	131

Verification: SinGen FiP16 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for General block SinGen.

Test results						
Time step	1	2	3	4	...	200
CPU cycles	117	117	117	117	...	117
Inputs						
A (DSP)	164	328	492	655	...	32767
f (DSP)	32767	32767	32767	32767	...	32767
A	0.005	0.01	0.015	0.02	...	1
f	1	1	1	1	...	1
Parameters						
fmax	200					
Offset	0.13					
Phase	0					
ts_fact	1					
Outputs						
u	0.131	0.133	0.136	0.14	...	0.135
Exp. u	0.131	0.132	0.136	0.14	...	0.13
u (DSP)	4281	4342	4441	4576	...	4435
Exp. u (DSP)	4280	4341	4441	4576	...	4260

Test settings	
Tolerance u	±5,3711e-03 (±176 LSB)

Test statistics	
Min CPU cycles	117
Max CPU cycles	117
Avg CPU cycles	117

Verification: SinGen FiP16 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for General block SinGen.

Test results						
Time step	1	2	3	4	...	200
CPU cycles	80	80	80	80	...	80
Inputs						
A (DSP)	164	328	492	655	...	32767
f (DSP)	32767	32767	32767	32767	...	32767
A	0.005	0.01	0.015	0.02	...	1
f	1	1	1	1	...	1
Parameters						
fmax	200					
Offset	0.13					
Phase	0					
ts_fact	1					
Outputs						
u	0.131	0.133	0.136	0.14	...	0.135
Exp. u	0.131	0.132	0.136	0.14	...	0.13
u (DSP)	4281	4342	4441	4576	...	4435
Exp. u (DSP)	4280	4341	4441	4576	...	4260

Test settings	
Tolerance u	±5,3711e-03 (±176 LSB)

Test statistics	
Min CPU cycles	80
Max CPU cycles	80
Avg CPU cycles	80

Verification: SinGen FiP16 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for General block SinGen.

Test results						
Time step	1	2	3	4	...	200
CPU cycles	108	108	108	108	...	108
Inputs						
A (DSP)	164	328	492	655	...	32767
f (DSP)	32767	32767	32767	32767	...	32767
A	0.005	0.01	0.015	0.02	...	1
f	1	1	1	1	...	1
Parameters						
fmax	200					
Offset	0.13					
Phase	0					
ts_fact	1					
Outputs						
u	0.131	0.133	0.136	0.14	...	0.135
Exp. u	0.131	0.132	0.136	0.14	...	0.13
u (DSP)	4281	4342	4441	4576	...	4435
Exp. u (DSP)	4280	4341	4441	4576	...	4260

Test settings	
Tolerance u	±5,3711e-03 (±176 LSB)

Test statistics	
Min CPU cycles	108
Max CPU cycles	108
Avg CPU cycles	108

Verification: SinGen FiP16 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for General block SinGen.

Test results						
Time step	1	2	3	4	...	200
CPU cycles	148	123	123	123	...	123
Inputs						
A (DSP)	164	328	492	655	...	32767
f (DSP)	32767	32767	32767	32767	...	32767
A	0.005	0.01	0.015	0.02	...	1
f	1	1	1	1	...	1
Parameters						
fmax	200					
Offset	0.13					
Phase	0					
ts_fact	1					
Outputs						
u	0.131	0.133	0.136	0.14	...	0.135
Exp. u	0.131	0.132	0.136	0.14	...	0.13
u (DSP)	4281	4342	4441	4576	...	4435
Exp. u (DSP)	4280	4341	4441	4576	...	4260

Test settings	
Tolerance u	±5,3711e-03 (±176 LSB)

Test statistics	
Min CPU cycles	123
Max CPU cycles	148
Avg CPU cycles	123

Verification: SinGen FiP16 CPU TMS320F28379D

Date of Test 2026-06-22

Target controller TMS320F28379D

Test case: Inport test OK

Inport test for General block SinGen.

Test results						
Time step	1	2	3	4	...	200
CPU cycles	98	98	98	98	...	98
Inputs						
A (DSP)	164	328	492	655	...	32767
f (DSP)	32767	32767	32767	32767	...	32767
A	0.005	0.01	0.015	0.02	...	1
f	1	1	1	1	...	1
Parameters						
fmax	200					
Offset	0.13					
Phase	0					
ts_fact	1					
Outputs						
u	0.131	0.133	0.136	0.14	...	0.135
Exp. u	0.131	0.132	0.136	0.14	...	0.13
u (DSP)	4281	4342	4441	4576	...	4435
Exp. u (DSP)	4280	4341	4441	4576	...	4260

Test settings	
Tolerance u	±5,3711e-03 (±176 LSB)

Test statistics	
Min CPU cycles	98
Max CPU cycles	101
Avg CPU cycles	98

Verification: SinGen FiP32 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for General block SinGen.

Test results				
Time step	1	2	...	200
CPU cycles	244	244	...	244
Inputs				
A (DSP)	10737418	21474836	...	2147483647
f (DSP)	2147483647	2147483647	...	2147483647
A	0.005	0.01	...	1
f	1	1	...	1
Parameters				
fmax	200			
Offset	0.13			
Phase	0			
ts_fact	1			
Outputs				
u	0.131	0.132	...	0.13
Exp. u	0.131	0.132	...	0.13
u (DSP)	280518584	284513150	...	279172924
Exp. u (DSP)	280518630	284513449	...	279172874

Test settings	
Tolerance u	±6,9849e-05 (±150000 LSB)

Test statistics	
Min CPU cycles	244
Max CPU cycles	244
Avg CPU cycles	244

Verification: SinGen FiP32 CPU TM4C123GH6

Date of Test 2026-06-19

Target controller TM4C123GH6

Test case: Inport test OK

Inport test for General block SinGen.

Test results				
Time step	1	2	...	200
CPU cycles	97	97	...	97
Inputs				
A (DSP)	10737418	21474836	...	2147483647
f (DSP)	2147483647	2147483647	...	2147483647
A	0.005	0.01	...	1
f	1	1	...	1
Parameters				
fmax	200			
Offset	0.13			
Phase	0			
ts_fact	1			
Outputs				
u	0.131	0.132	...	0.13
Exp. u	0.131	0.132	...	0.13
u (DSP)	280518584	284513150	...	279172924
Exp. u (DSP)	280518630	284513449	...	279172874

Test settings	
Tolerance u	±6,9849e-05 (±150000 LSB)

Test statistics	
Min CPU cycles	97
Max CPU cycles	97
Avg CPU cycles	97

Verification: SinGen FiP32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for General block SinGen.

Test results				
Time step	1	2	...	200
CPU cycles	159	154	...	154
Inputs				
A (DSP)	10737418	21474836	...	2147483647
f (DSP)	2147483647	2147483647	...	2147483647
A	0.005	0.01	...	1
f	1	1	...	1
Parameters				
fmax	200			
Offset	0.13			
Phase	0			
ts_fact	1			
Outputs				
u	0.131	0.132	...	0.13
Exp. u	0.131	0.132	...	0.13
u (DSP)	280518584	284513150	...	279172924
Exp. u (DSP)	280518630	284513449	...	279172874

Test settings	
Tolerance u	±6,9849e-05 (±150000 LSB)

Test statistics	
Min CPU cycles	154
Max CPU cycles	159
Avg CPU cycles	156

Verification: SinGen FiP32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for General block SinGen.

Test results				
Time step	1	2	...	200
CPU cycles	343	343	...	343
Inputs				
A (DSP)	10737418	21474836	...	2147483647
f (DSP)	2147483647	2147483647	...	2147483647
A	0.005	0.01	...	1
f	1	1	...	1
Parameters				
fmax	200			
Offset	0.13			
Phase	0			
ts_fact	1			
Outputs				
u	0.131	0.132	...	0.13
Exp. u	0.131	0.132	...	0.13
u (DSP)	280518584	284513150	...	279172924
Exp. u (DSP)	280518630	284513449	...	279172874

Test settings	
Tolerance u	±6,9849e-05 (±150000 LSB)

Test statistics	
Min CPU cycles	343
Max CPU cycles	402
Avg CPU cycles	344

Verification: SinGen FiP32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for General block SinGen.

Test results				
Time step	1	2	...	200
CPU cycles	107	107	...	105
Inputs				
A (DSP)	10737418	21474836	...	2147483647
f (DSP)	2147483647	2147483647	...	2147483647
A	0.005	0.01	...	1
f	1	1	...	1
Parameters				
fmax	200			
Offset	0.13			
Phase	0			
ts_fact	1			
Outputs				
u	0.131	0.132	...	0.13
Exp. u	0.131	0.132	...	0.13
u (DSP)	280518584	284513150	...	279172924
Exp. u (DSP)	280518630	284513449	...	279172874

Test settings	
Tolerance u	±6,9849e-05 (±150000 LSB)

Test statistics	
Min CPU cycles	105
Max CPU cycles	108
Avg CPU cycles	107

Verification: SinGen FiP32 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for General block SinGen.

Test results				
Time step	1	2	...	200
CPU cycles	482	482	...	482
Inputs				
A (DSP)	10737418	21474836	...	2147483647
f (DSP)	2147483647	2147483647	...	2147483647
A	0.005	0.01	...	1
f	1	1	...	1
Parameters				
fmax	200			
Offset	0.13			
Phase	0			
ts_fact	1			
Outputs				
u	0.131	0.132	...	0.13
Exp. u	0.131	0.132	...	0.13
u (DSP)	280518584	284513150	...	279172924
Exp. u (DSP)	280518630	284513449	...	279172874

Test settings	
Tolerance u	±6,9849e-05 (±150000 LSB)

Test statistics	
Min CPU cycles	482
Max CPU cycles	496
Avg CPU cycles	489

Verification: SinGen FiP32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for General block SinGen.

Test results				
Time step	1	2	...	200
CPU cycles	190	155	...	155
Inputs				
A (DSP)	10737418	21474836	...	2147483647
f (DSP)	2147483647	2147483647	...	2147483647
A	0.005	0.01	...	1
f	1	1	...	1
Parameters				
fmax	200			
Offset	0.13			
Phase	0			
ts_fact	1			
Outputs				
u	0.131	0.132	...	0.13
Exp. u	0.131	0.132	...	0.13
u (DSP)	280518584	284513150	...	279172924
Exp. u (DSP)	280518630	284513449	...	279172874

Test settings	
Tolerance u	±6,9849e-05 (±150000 LSB)

Test statistics	
Min CPU cycles	155
Max CPU cycles	190
Avg CPU cycles	155

Verification: SinGen FiP32 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test — OK

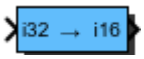
Inport test for General block SinGen.

Test results				
Time step	1	2	...	200
CPU cycles	212	208	...	208
Inputs				
A (DSP)	10737418	21474836	...	2147483647
f (DSP)	2147483647	2147483647	...	2147483647
A	0.005	0.01	...	1
f	1	1	...	1
Parameters				
fmax	200			
Offset	0.13			
Phase	0			
ts_fact	1			
Outputs				
u	0.131	0.132	...	0.13
Exp. u	0.131	0.132	...	0.13
u (DSP)	280518584	284513150	...	279172924
Exp. u (DSP)	280518630	284513449	...	279172874

Test settings	
Tolerance u	±6,9849e-05 (±150000 LSB)

Test statistics	
Min CPU cycles	208
Max CPU cycles	212
Avg CPU cycles	208

Block: TypeConv



Data Type Conversion

Inports	
In	

Outports	
Out	

Implementations:

FiP8_16	8 to 16 Bit Fixed Point Implementation
FiP8_32	8 to 32 Bit Fixed Point Implementation
FiP16_8	16 to 8 Bit Fixed Point Implementation
FiP16_32	16 to 32 Bit Fixed Point Implementation
FiP32_8	32 to 8 Bit Fixed Point Implementation
FiP32_16	32 to 16 Bit Fixed Point Implementation
Bool_FiP16	Boolean to 16 Bit Fixed Point Implementation
Bool_FiP32	Boolean to 32 Bit Fixed Point Implementation
FiP16_Bool	16 Bit Fixed Point to Boolean Implementation
FiP32_Bool	32 Bit Fixed Point to Boolean Implementation

Implementation: FiP8_16

8 to 16 Bit Fixed Point Implementation

Inports Data Type	
In	int8

Outports Data Type	
Out	int16

Implementation: FiP8_32

8 to 32 Bit Fixed Point Implementation

Inports Data Type	
In	int8

Outports Data Type	
Out	int32

Implementation: FiP16_8

16 to 8 Bit Fixed Point Implementation

Inports Data Type	
In	int16

Outports Data Type	
Out	int8

Implementation: FiP16_32

16 to 32 Bit Fixed Point Implementation

Inports Data Type	
In	int16

Outports Data Type	
Out	int32

Implementation: FiP32_8

32 to 8 Bit Fixed Point Implementation

Inports Data Type	
In	int32

Outports Data Type	
Out	int8

Implementation: FiP32_16

32 to 16 Bit Fixed Point Implementation

Inports Data Type	
In	int32

Outports Data Type	
Out	int16

Implementation: Bool_FiP16

Boolean to 16 Bit Fixed Point Implementation

Inports Data Type	
In	bool

Outports Data Type	
Out	int16

Implementation: Bool_FiP32

Boolean to 32 Bit Fixed Point Implementation

Inports Data Type	
In	bool

Outports Data Type	
Out	int32

Implementation: FiP16_Bool

16 Bit Fixed Point to Boolean Implementation

Inports Data Type	
In	int16

Outports Data Type	
Out	bool

Implementation: FiP32_Bool

32 Bit Fixed Point to Boolean Implementation

Inports Data Type	
In	int32

Outports Data Type	
Out	bool

Verification: TypeConv FiP8_16 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for General block TypeConv.

Test results						
Time step	1	2	3	4	...	8
CPU cycles	56	56	56	56	...	56
Inputs						
In (DSP)	0	26	64	127	...	-127
In	0	0.2	0.5	0.992	...	-0.992
Outputs						
Out	0	0.203	0.5	0.992	...	-0.992
Exp. Out	0	0.2	0.5	0.992	...	-0.992
Out (DSP)	0	6656	16384	32512	...	-32512
Exp. Out (DSP)	0	6553	16384	32512	...	-32512

Test settings	
Tolerance Out	±7,8125e-03 (±256 LSB)

Test statistics	
Min CPU cycles	56
Max CPU cycles	56
Avg CPU cycles	56

Verification: TypeConv FiP8_16 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for General block TypeConv.

Test results						
Time step	1	2	3	4	...	8
CPU cycles	25	25	25	25	...	25
Inputs						
In (DSP)	0	26	64	127	...	-127
In	0	0.2	0.5	0.992	...	-0.992
Outputs						
Out	0	0.203	0.5	0.992	...	-0.992
Exp. Out	0	0.2	0.5	0.992	...	-0.992
Out (DSP)	0	6656	16384	32512	...	-32512
Exp. Out (DSP)	0	6553	16384	32512	...	-32512

Test settings	
Tolerance Out	±7,8125e-03 (±256 LSB)

Test statistics	
Min CPU cycles	25
Max CPU cycles	25
Avg CPU cycles	25

Verification: TypeConv FiP8_16 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test **OK**

Inport test for General block TypeConv.

Test results						
Time step	1	2	3	4	...	8
CPU cycles	57	57	57	57	...	57
Inputs						
In (DSP)	0	26	64	127	...	-127
In	0	0.2	0.5	0.992	...	-0.992
Outputs						
Out	0	0.203	0.5	0.992	...	-0.992
Exp. Out	0	0.2	0.5	0.992	...	-0.992
Out (DSP)	0	6656	16384	32512	...	-32512
Exp. Out (DSP)	0	6553	16384	32512	...	-32512

Test settings	
Tolerance Out	±7,8125e-03 (±256 LSB)

Test statistics	
Min CPU cycles	57
Max CPU cycles	57
Avg CPU cycles	57

Verification: TypeConv FiP8_16 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test **OK**

Inport test for General block TypeConv.

Test results						
Time step	1	2	3	4	...	8
CPU cycles	48	48	48	48	...	48
Inputs						
In (DSP)	0	26	64	127	...	-127
In	0	0.2	0.5	0.992	...	-0.992
Outputs						
Out	0	0.203	0.5	0.992	...	-0.992
Exp. Out	0	0.2	0.5	0.992	...	-0.992
Out (DSP)	0	6656	16384	32512	...	-32512
Exp. Out (DSP)	0	6553	16384	32512	...	-32512

Test settings	
Tolerance Out	±7,8125e-03 (±256 LSB)

Test statistics	
Min CPU cycles	48
Max CPU cycles	48
Avg CPU cycles	48

Verification: TypeConv FiP8_16 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for General block TypeConv.

Test results						
Time step	1	2	3	4	...	8
CPU cycles	29	29	29	29	...	29
Inputs						
In (DSP)	0	26	64	127	...	-127
In	0	0.2	0.5	0.992	...	-0.992
Outputs						
Out	0	0.203	0.5	0.992	...	-0.992
Exp. Out	0	0.2	0.5	0.992	...	-0.992
Out (DSP)	0	6656	16384	32512	...	-32512
Exp. Out (DSP)	0	6553	16384	32512	...	-32512

Test settings	
Tolerance Out	±7,8125e-03 (±256 LSB)

Test statistics	
Min CPU cycles	29
Max CPU cycles	29
Avg CPU cycles	29

Verification: TypeConv FiP8_16 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for General block TypeConv.

Test results						
Time step	1	2	3	4	...	8
CPU cycles	42	42	42	42	...	42
Inputs						
In (DSP)	0	26	64	127	...	-127
In	0	0.2	0.5	0.992	...	-0.992
Outputs						
Out	0	0.203	0.5	0.992	...	-0.992
Exp. Out	0	0.2	0.5	0.992	...	-0.992
Out (DSP)	0	6656	16384	32512	...	-32512
Exp. Out (DSP)	0	6553	16384	32512	...	-32512

Test settings	
Tolerance Out	±7,8125e-03 (±256 LSB)

Test statistics	
Min CPU cycles	42
Max CPU cycles	42
Avg CPU cycles	42

Verification: TypeConv FiP8_16 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for General block TypeConv.

Test results						
Time step	1	2	3	4	...	8
CPU cycles	66	56	56	56	...	56
Inputs						
In (DSP)	0	26	64	127	...	-127
In	0	0.2	0.5	0.992	...	-0.992
Outputs						
Out	0	0.203	0.5	0.992	...	-0.992
Exp. Out	0	0.2	0.5	0.992	...	-0.992
Out (DSP)	0	6656	16384	32512	...	-32512
Exp. Out (DSP)	0	6553	16384	32512	...	-32512

Test settings	
Tolerance Out	±7,8125e-03 (±256 LSB)

Test statistics	
Min CPU cycles	56
Max CPU cycles	66
Avg CPU cycles	57

Verification: TypeConv FiP8_16 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for General block TypeConv.

Test results						
Time step	1	2	3	4	...	8
CPU cycles	39	39	39	39	...	39
Inputs						
In (DSP)	0	26	64	127	...	-127
In	0	0.2	0.5	0.992	...	-0.992
Outputs						
Out	0	0.203	0.5	0.992	...	-0.992
Exp. Out	0	0.2	0.5	0.992	...	-0.992
Out (DSP)	0	6656	16384	32512	...	-32512
Exp. Out (DSP)	0	6553	16384	32512	...	-32512

Test settings	
Tolerance Out	±7,8125e-03 (±256 LSB)

Test statistics	
Min CPU cycles	39
Max CPU cycles	39
Avg CPU cycles	39

Verification: TypeConv FiP8_32 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for General block TypeConv.

Test results				
Time step	1	2	...	8
CPU cycles	57	57	...	57
Inputs				
In (DSP)	0	26	...	-127
In	0	0.2	...	-0.992
Outputs				
Out	0	0.203	...	-0.992
Exp. Out	0	0.2	...	-0.992
Out (DSP)	0	436207616	...	-2130706432
Exp. Out (DSP)	0	429496729	...	-2130706432

Test settings	
Tolerance Out	±7,8125e-03 (±16777216 LSB)

Test statistics	
Min CPU cycles	57
Max CPU cycles	57
Avg CPU cycles	57

Verification: TypeConv FiP8_32 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for General block TypeConv.

Test results				
Time step	1	2	...	8
CPU cycles	25	25	...	25
Inputs				
In (DSP)	0	26	...	-127
In	0	0.2	...	-0.992
Outputs				
Out	0	0.203	...	-0.992
Exp. Out	0	0.2	...	-0.992
Out (DSP)	0	436207616	...	-2130706432
Exp. Out (DSP)	0	429496729	...	-2130706432

Test settings	
Tolerance Out	±7,8125e-03 (±16777216 LSB)

Test statistics	
Min CPU cycles	25
Max CPU cycles	25
Avg CPU cycles	25

Verification: TypeConv FiP8_32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for General block TypeConv.

Test results				
Time step	1	2	...	8
CPU cycles	57	57	...	57
Inputs				
In (DSP)	0	26	...	-127
In	0	0.2	...	-0.992
Outputs				
Out	0	0.203	...	-0.992
Exp. Out	0	0.2	...	-0.992
Out (DSP)	0	436207616	...	-2130706432
Exp. Out (DSP)	0	429496729	...	-2130706432

Test settings	
Tolerance Out	±7,8125e-03 (±16777216 LSB)

Test statistics	
Min CPU cycles	57
Max CPU cycles	57
Avg CPU cycles	57

Verification: TypeConv FiP8_32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for General block TypeConv.

Test results				
Time step	1	2	...	8
CPU cycles	48	48	...	48
Inputs				
In (DSP)	0	26	...	-127
In	0	0.2	...	-0.992
Outputs				
Out	0	0.203	...	-0.992
Exp. Out	0	0.2	...	-0.992
Out (DSP)	0	436207616	...	-2130706432
Exp. Out (DSP)	0	429496729	...	-2130706432

Test settings	
Tolerance Out	±7,8125e-03 (±16777216 LSB)

Test statistics	
Min CPU cycles	48
Max CPU cycles	48
Avg CPU cycles	48

Verification: TypeConv FiP8_32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for General block TypeConv.

Test results				
Time step	1	2	...	8
CPU cycles	29	29	...	29
Inputs				
In (DSP)	0	26	...	-127
In	0	0.2	...	-0.992
Outputs				
Out	0	0.203	...	-0.992
Exp. Out	0	0.2	...	-0.992
Out (DSP)	0	436207616	...	-2130706432
Exp. Out (DSP)	0	429496729	...	-2130706432

Test settings	
Tolerance Out	±7,8125e-03 (±16777216 LSB)

Test statistics	
Min CPU cycles	29
Max CPU cycles	29
Avg CPU cycles	29

Verification: TypeConv FiP8_32 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for General block TypeConv.

Test results				
Time step	1	2	...	8
CPU cycles	45	45	...	45
Inputs				
In (DSP)	0	26	...	-127
In	0	0.2	...	-0.992
Outputs				
Out	0	0.203	...	-0.992
Exp. Out	0	0.2	...	-0.992
Out (DSP)	0	436207616	...	-2130706432
Exp. Out (DSP)	0	429496729	...	-2130706432

Test settings	
Tolerance Out	±7,8125e-03 (±16777216 LSB)

Test statistics	
Min CPU cycles	45
Max CPU cycles	45
Avg CPU cycles	45

Verification: TypeConv FiP8_32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for General block TypeConv.

Test results				
Time step	1	2	...	8
CPU cycles	56	56	...	56
Inputs				
In (DSP)	0	26	...	-127
In	0	0.2	...	-0.992
Outputs				
Out	0	0.203	...	-0.992
Exp. Out	0	0.2	...	-0.992
Out (DSP)	0	436207616	...	-2130706432
Exp. Out (DSP)	0	429496729	...	-2130706432

Test settings	
Tolerance Out	±7,8125e-03 (±16777216 LSB)

Test statistics	
Min CPU cycles	56
Max CPU cycles	56
Avg CPU cycles	56

Verification: TypeConv FiP8_32 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for General block TypeConv.

Test results				
Time step	1	2	...	8
CPU cycles	38	38	...	38
Inputs				
In (DSP)	0	26	...	-127
In	0	0.2	...	-0.992
Outputs				
Out	0	0.203	...	-0.992
Exp. Out	0	0.2	...	-0.992
Out (DSP)	0	436207616	...	-2130706432
Exp. Out (DSP)	0	429496729	...	-2130706432

Test settings	
Tolerance Out	±7,8125e-03 (±16777216 LSB)

Test statistics	
Min CPU cycles	38
Max CPU cycles	38
Avg CPU cycles	38

Verification: TypeConv FiP16_8 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for General block TypeConv.

Test results						
Time step	1	2	3	4	...	8
CPU cycles	62	62	62	62	...	65
Inputs						
In (DSP)	0	6554	16384	32767	...	-32768
In	0	0.2	0.5	1	...	-1
Outputs						
Out	0	0.195	0.5	0.992	...	-0.992
Exp. Out	0	0.195	0.5	0.992	...	-0.992
Out (DSP)	0	25	64	127	...	-127
Exp. Out (DSP)	0	25	64	127	...	-127

Test settings	
Tolerance Out	±0,0000e+00 (±0 LSB)

Test statistics	
Min CPU cycles	62
Max CPU cycles	65
Avg CPU cycles	62

Verification: TypeConv FiP16_8 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for General block TypeConv.

Test results						
Time step	1	2	3	4	...	8
CPU cycles	29	29	29	29	...	29
Inputs						
In (DSP)	0	6554	16384	32767	...	-32768
In	0	0.2	0.5	1	...	-1
Outputs						
Out	0	0.195	0.5	0.992	...	-0.992
Exp. Out	0	0.195	0.5	0.992	...	-0.992
Out (DSP)	0	25	64	127	...	-127
Exp. Out (DSP)	0	25	64	127	...	-127

Test settings	
Tolerance Out	±0,0000e+00 (±0 LSB)

Test statistics	
Min CPU cycles	29
Max CPU cycles	29
Avg CPU cycles	29

Verification: TypeConv FiP16_8 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for General block TypeConv.

Test results						
Time step	1	2	3	4	...	8
CPU cycles	62	62	62	62	...	62
Inputs						
In (DSP)	0	6554	16384	32767	...	-32768
In	0	0.2	0.5	1	...	-1
Outputs						
Out	0	0.195	0.5	0.992	...	-0.992
Exp. Out	0	0.195	0.5	0.992	...	-0.992
Out (DSP)	0	25	64	127	...	-127
Exp. Out (DSP)	0	25	64	127	...	-127

Test settings	
Tolerance Out	±0,0000e+00 (±0 LSB)

Test statistics	
Min CPU cycles	62
Max CPU cycles	62
Avg CPU cycles	62

Verification: TypeConv FiP16_8 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for General block TypeConv.

Test results						
Time step	1	2	3	4	...	8
CPU cycles	53	53	53	53	...	60
Inputs						
In (DSP)	0	6554	16384	32767	...	-32768
In	0	0.2	0.5	1	...	-1
Outputs						
Out	0	0.195	0.5	0.992	...	-0.992
Exp. Out	0	0.195	0.5	0.992	...	-0.992
Out (DSP)	0	25	64	127	...	-127
Exp. Out (DSP)	0	25	64	127	...	-127

Test settings	
Tolerance Out	±0,0000e+00 (±0 LSB)

Test statistics	
Min CPU cycles	53
Max CPU cycles	60
Avg CPU cycles	54

Verification: TypeConv FiP16_8 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for General block TypeConv.

Test results						
Time step	1	2	3	4	...	8
CPU cycles	31	31	31	31	...	31
Inputs						
In (DSP)	0	6554	16384	32767	...	-32768
In	0	0.2	0.5	1	...	-1
Outputs						
Out	0	0.195	0.5	0.992	...	-0.992
Exp. Out	0	0.195	0.5	0.992	...	-0.992
Out (DSP)	0	25	64	127	...	-127
Exp. Out (DSP)	0	25	64	127	...	-127

Test settings	
Tolerance Out	±0,0000e+00 (±0 LSB)

Test statistics	
Min CPU cycles	31
Max CPU cycles	31
Avg CPU cycles	31

Verification: TypeConv FiP16_8 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test **OK**

Inport test for General block TypeConv.

Test results						
Time step	1	2	3	4	...	8
CPU cycles	45	45	45	45	...	48
Inputs						
In (DSP)	0	6554	16384	32767	...	-32768
In	0	0.2	0.5	1	...	-1
Outputs						
Out	0	0.195	0.5	0.992	...	-0.992
Exp. Out	0	0.195	0.5	0.992	...	-0.992
Out (DSP)	0	25	64	127	...	-127
Exp. Out (DSP)	0	25	64	127	...	-127

Test settings	
Tolerance Out	±0,0000e+00 (±0 LSB)

Test statistics	
Min CPU cycles	45
Max CPU cycles	48
Avg CPU cycles	45

Verification: TypeConv FiP16_8 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for General block TypeConv.

Test results						
Time step	1	2	3	4	...	8
CPU cycles	69	59	59	59	...	59
Inputs						
In (DSP)	0	6554	16384	32767	...	-32768
In	0	0.2	0.5	1	...	-1
Outputs						
Out	0	0.195	0.5	0.992	...	-0.992
Exp. Out	0	0.195	0.5	0.992	...	-0.992
Out (DSP)	0	25	64	127	...	-127
Exp. Out (DSP)	0	25	64	127	...	-127

Test settings	
Tolerance Out	±0,0000e+00 (±0 LSB)

Test statistics	
Min CPU cycles	59
Max CPU cycles	69
Avg CPU cycles	60

Verification: TypeConv FiP16_8 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for General block TypeConv.

Test results						
Time step	1	2	3	4	...	8
CPU cycles	42	42	42	42	...	52
Inputs						
In (DSP)	0	6554	16384	32767	...	-32768
In	0	0.2	0.5	1	...	-1
Outputs						
Out	0	0.195	0.5	0.992	...	-0.992
Exp. Out	0	0.195	0.5	0.992	...	-0.992
Out (DSP)	0	25	64	127	...	-127
Exp. Out (DSP)	0	25	64	127	...	-127

Test settings	
Tolerance Out	±0,0000e+00 (±0 LSB)

Test statistics	
Min CPU cycles	42
Max CPU cycles	52
Avg CPU cycles	44

Verification: TypeConv FiP16_32 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for General block TypeConv.

Test results				
Time step	1	2	...	8
CPU cycles	56	56	...	56
Inputs				
In (DSP)	0	6554	...	-32768
In	0	0.2	...	-1
Outputs				
Out	0	0.2	...	-1
Exp. Out	0	0.2	...	-1
Out (DSP)	0	429522944	...	-2147483648
Exp. Out (DSP)	0	429496729	...	-2147483648

Test settings	
Tolerance Out	±3,0518e-05 (±65536 LSB)

Test statistics	
Min CPU cycles	56
Max CPU cycles	56
Avg CPU cycles	56

Verification: TypeConv FiP16_32 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for General block TypeConv.

Test results				
Time step	1	2	...	8
CPU cycles	25	25	...	25
Inputs				
In (DSP)	0	6554	...	-32768
In	0	0.2	...	-1
Outputs				
Out	0	0.2	...	-1
Exp. Out	0	0.2	...	-1
Out (DSP)	0	429522944	...	-2147483648
Exp. Out (DSP)	0	429496729	...	-2147483648

Test settings	
Tolerance Out	±3,0518e-05 (±65536 LSB)

Test statistics	
Min CPU cycles	25
Max CPU cycles	25
Avg CPU cycles	25

Verification: TypeConv FiP16_32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for General block TypeConv.

Test results				
Time step	1	2	...	8
CPU cycles	57	57	...	57
Inputs				
In (DSP)	0	6554	...	-32768
In	0	0.2	...	-1
Outputs				
Out	0	0.2	...	-1
Exp. Out	0	0.2	...	-1
Out (DSP)	0	429522944	...	-2147483648
Exp. Out (DSP)	0	429496729	...	-2147483648

Test settings	
Tolerance Out	±3,0518e-05 (±65536 LSB)

Test statistics	
Min CPU cycles	57
Max CPU cycles	57
Avg CPU cycles	57

Verification: TypeConv FiP16_32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for General block TypeConv.

Test results				
Time step	1	2	...	8
CPU cycles	48	48	...	48
Inputs				
In (DSP)	0	6554	...	-32768
In	0	0.2	...	-1
Outputs				
Out	0	0.2	...	-1
Exp. Out	0	0.2	...	-1
Out (DSP)	0	429522944	...	-2147483648
Exp. Out (DSP)	0	429496729	...	-2147483648

Test settings	
Tolerance Out	±3,0518e-05 (±65536 LSB)

Test statistics	
Min CPU cycles	48
Max CPU cycles	48
Avg CPU cycles	48

Verification: TypeConv FiP16_32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for General block TypeConv.

Test results				
Time step	1	2	...	8
CPU cycles	29	29	...	29
Inputs				
In (DSP)	0	6554	...	-32768
In	0	0.2	...	-1
Outputs				
Out	0	0.2	...	-1
Exp. Out	0	0.2	...	-1
Out (DSP)	0	429522944	...	-2147483648
Exp. Out (DSP)	0	429496729	...	-2147483648

Test settings	
Tolerance Out	±3,0518e-05 (±65536 LSB)

Test statistics	
Min CPU cycles	29
Max CPU cycles	29
Avg CPU cycles	29

Verification: TypeConv FiP16_32 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for General block TypeConv.

Test results				
Time step	1	2	...	8
CPU cycles	43	43	...	43
Inputs				
In (DSP)	0	6554	...	-32768
In	0	0.2	...	-1
Outputs				
Out	0	0.2	...	-1
Exp. Out	0	0.2	...	-1
Out (DSP)	0	429522944	...	-2147483648
Exp. Out (DSP)	0	429496729	...	-2147483648

Test settings	
Tolerance Out	±3,0518e-05 (±65536 LSB)

Test statistics	
Min CPU cycles	43
Max CPU cycles	43
Avg CPU cycles	43

Verification: TypeConv FiP16_32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for General block TypeConv.

Test results				
Time step	1	2	...	8
CPU cycles	56	56	...	56
Inputs				
In (DSP)	0	6554	...	-32768
In	0	0.2	...	-1
Outputs				
Out	0	0.2	...	-1
Exp. Out	0	0.2	...	-1
Out (DSP)	0	429522944	...	-2147483648
Exp. Out (DSP)	0	429496729	...	-2147483648

Test settings	
Tolerance Out	±3,0518e-05 (±65536 LSB)

Test statistics	
Min CPU cycles	56
Max CPU cycles	56
Avg CPU cycles	56

Verification: TypeConv FiP16_32 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for General block TypeConv.

Test results				
Time step	1	2	...	8
CPU cycles	36	36	...	36
Inputs				
In (DSP)	0	6554	...	-32768
In	0	0.2	...	-1
Outputs				
Out	0	0.2	...	-1
Exp. Out	0	0.2	...	-1
Out (DSP)	0	429522944	...	-2147483648
Exp. Out (DSP)	0	429496729	...	-2147483648

Test settings	
Tolerance Out	±3,0518e-05 (±65536 LSB)

Test statistics	
Min CPU cycles	36
Max CPU cycles	36
Avg CPU cycles	36

Verification: TypeConv FiP32_8 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for General block TypeConv.

Test results				
Time step	1	2	...	8
CPU cycles	63	63	...	64
Inputs				
In (DSP)	0	429496730	...	-2147483648
In	0	0.2	...	-1
Outputs				
Out	0	0.195	...	-0.992
Exp. Out	0	0.195	...	-0.992
Out (DSP)	0	25	...	-127
Exp. Out (DSP)	0	25	...	-127

Test settings	
Tolerance Out	±0,0000e+00 (±0 LSB)

Test statistics	
Min CPU cycles	63
Max CPU cycles	64
Avg CPU cycles	63

Verification: TypeConv FiP32_8 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for General block TypeConv.

Test results				
Time step	1	2	...	8
CPU cycles	29	29	...	31
Inputs				
In (DSP)	0	429496730	...	-2147483648
In	0	0.2	...	-1
Outputs				
Out	0	0.195	...	-0.992
Exp. Out	0	0.195	...	-0.992
Out (DSP)	0	25	...	-127
Exp. Out (DSP)	0	25	...	-127

Test settings	
Tolerance Out	±0,0000e+00 (±0 LSB)

Test statistics	
Min CPU cycles	29
Max CPU cycles	31
Avg CPU cycles	29

Verification: TypeConv FiP32_8 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for General block TypeConv.

Test results				
Time step	1	2	...	8
CPU cycles	62	62	...	62
Inputs				
In (DSP)	0	429496730	...	-2147483648
In	0	0.2	...	-1
Outputs				
Out	0	0.195	...	-0.992
Exp. Out	0	0.195	...	-0.992
Out (DSP)	0	25	...	-127
Exp. Out (DSP)	0	25	...	-127

Test settings	
Tolerance Out	±0,0000e+00 (±0 LSB)

Test statistics	
Min CPU cycles	62
Max CPU cycles	62
Avg CPU cycles	62

Verification: TypeConv FiP32_8 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for General block TypeConv.

Test results				
Time step	1	2	...	8
CPU cycles	51	51	...	58
Inputs				
In (DSP)	0	429496730	...	-2147483648
In	0	0.2	...	-1
Outputs				
Out	0	0.195	...	-0.992
Exp. Out	0	0.195	...	-0.992
Out (DSP)	0	25	...	-127
Exp. Out (DSP)	0	25	...	-127

Test settings	
Tolerance Out	±0,0000e+00 (±0 LSB)

Test statistics	
Min CPU cycles	51
Max CPU cycles	58
Avg CPU cycles	52

Verification: TypeConv FiP32_8 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for General block TypeConv.

Test results				
Time step	1	2	...	8
CPU cycles	31	31	...	31
Inputs				
In (DSP)	0	429496730	...	-2147483648
In	0	0.2	...	-1
Outputs				
Out	0	0.195	...	-0.992
Exp. Out	0	0.195	...	-0.992
Out (DSP)	0	25	...	-127
Exp. Out (DSP)	0	25	...	-127

Test settings	
Tolerance Out	±0,0000e+00 (±0 LSB)

Test statistics	
Min CPU cycles	31
Max CPU cycles	31
Avg CPU cycles	31

Verification: TypeConv FiP32_8 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for General block TypeConv.

Test results				
Time step	1	2	...	8
CPU cycles	48	48	...	51
Inputs				
In (DSP)	0	429496730	...	-2147483648
In	0	0.2	...	-1
Outputs				
Out	0	0.195	...	-0.992
Exp. Out	0	0.195	...	-0.992
Out (DSP)	0	25	...	-127
Exp. Out (DSP)	0	25	...	-127

Test settings	
Tolerance Out	±0,0000e+00 (±0 LSB)

Test statistics	
Min CPU cycles	48
Max CPU cycles	51
Avg CPU cycles	48

Verification: TypeConv FiP32_8 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for General block TypeConv.

Test results				
Time step	1	2	...	8
CPU cycles	67	59	...	59
Inputs				
In (DSP)	0	429496730	...	-2147483648
In	0	0.2	...	-1
Outputs				
Out	0	0.195	...	-0.992
Exp. Out	0	0.195	...	-0.992
Out (DSP)	0	25	...	-127
Exp. Out (DSP)	0	25	...	-127

Test settings	
Tolerance Out	±0,0000e+00 (±0 LSB)

Test statistics	
Min CPU cycles	59
Max CPU cycles	67
Avg CPU cycles	60

Verification: TypeConv FiP32_8 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for General block TypeConv.

Test results				
Time step	1	2	...	8
CPU cycles	47	47	...	51
Inputs				
In (DSP)	0	429496730	...	-2147483648
In	0	0.2	...	-1
Outputs				
Out	0	0.195	...	-0.992
Exp. Out	0	0.195	...	-0.992
Out (DSP)	0	25	...	-127
Exp. Out (DSP)	0	25	...	-127

Test settings	
Tolerance Out	±0,0000e+00 (±0 LSB)

Test statistics	
Min CPU cycles	47
Max CPU cycles	51
Avg CPU cycles	48

Verification: TypeConv FiP32_16 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for General block TypeConv.

Test results				
Time step	1	2	...	8
CPU cycles	61	61	...	63
Inputs				
In (DSP)	0	429496730	...	-2147483648
In	0	0.2	...	-1
Outputs				
Out	0	0.2	...	-1
Exp. Out	0	0.2	...	-1
Out (DSP)	0	6553	...	-32767
Exp. Out (DSP)	0	6553	...	-32767

Test settings	
Tolerance Out	±0,0000e+00 (±0 LSB)

Test statistics	
Min CPU cycles	61
Max CPU cycles	63
Avg CPU cycles	61

Verification: TypeConv FiP32_16 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for General block TypeConv.

Test results				
Time step	1	2	...	8
CPU cycles	31	31	...	33
Inputs				
In (DSP)	0	429496730	...	-2147483648
In	0	0.2	...	-1
Outputs				
Out	0	0.2	...	-1
Exp. Out	0	0.2	...	-1
Out (DSP)	0	6553	...	-32767
Exp. Out (DSP)	0	6553	...	-32767

Test settings	
Tolerance Out	±0,0000e+00 (±0 LSB)

Test statistics	
Min CPU cycles	31
Max CPU cycles	33
Avg CPU cycles	31

Verification: TypeConv FiP32_16 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for General block TypeConv.

Test results				
Time step	1	2	...	8
CPU cycles	62	62	...	67
Inputs				
In (DSP)	0	429496730	...	-2147483648
In	0	0.2	...	-1
Outputs				
Out	0	0.2	...	-1
Exp. Out	0	0.2	...	-1
Out (DSP)	0	6553	...	-32767
Exp. Out (DSP)	0	6553	...	-32767

Test settings	
Tolerance Out	±0,0000e+00 (±0 LSB)

Test statistics	
Min CPU cycles	62
Max CPU cycles	67
Avg CPU cycles	63

Verification: TypeConv FiP32_16 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for General block TypeConv.

Test results				
Time step	1	2	...	8
CPU cycles	52	52	...	60
Inputs				
In (DSP)	0	429496730	...	-2147483648
In	0	0.2	...	-1
Outputs				
Out	0	0.2	...	-1
Exp. Out	0	0.2	...	-1
Out (DSP)	0	6553	...	-32767
Exp. Out (DSP)	0	6553	...	-32767

Test settings	
Tolerance Out	±0,0000e+00 (±0 LSB)

Test statistics	
Min CPU cycles	52
Max CPU cycles	60
Avg CPU cycles	54

Verification: TypeConv FiP32_16 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for General block TypeConv.

Test results				
Time step	1	2	...	8
CPU cycles	31	31	...	31
Inputs				
In (DSP)	0	429496730	...	-2147483648
In	0	0.2	...	-1
Outputs				
Out	0	0.2	...	-1
Exp. Out	0	0.2	...	-1
Out (DSP)	0	6553	...	-32767
Exp. Out (DSP)	0	6553	...	-32767

Test settings	
Tolerance Out	±0,0000e+00 (±0 LSB)

Test statistics	
Min CPU cycles	31
Max CPU cycles	31
Avg CPU cycles	31

Verification: TypeConv FiP32_16 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for General block TypeConv.

Test results				
Time step	1	2	...	8
CPU cycles	47	47	...	51
Inputs				
In (DSP)	0	429496730	...	-2147483648
In	0	0.2	...	-1
Outputs				
Out	0	0.2	...	-1
Exp. Out	0	0.2	...	-1
Out (DSP)	0	6553	...	-32767
Exp. Out (DSP)	0	6553	...	-32767

Test settings	
Tolerance Out	±0,0000e+00 (±0 LSB)

Test statistics	
Min CPU cycles	47
Max CPU cycles	51
Avg CPU cycles	48

Verification: TypeConv FiP32_16 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for General block TypeConv.

Test results				
Time step	1	2	...	8
CPU cycles	65	65	...	65
Inputs				
In (DSP)	0	429496730	...	-2147483648
In	0	0.2	...	-1
Outputs				
Out	0	0.2	...	-1
Exp. Out	0	0.2	...	-1
Out (DSP)	0	6553	...	-32767
Exp. Out (DSP)	0	6553	...	-32767

Test settings	
Tolerance Out	±0,0000e+00 (±0 LSB)

Test statistics	
Min CPU cycles	65
Max CPU cycles	65
Avg CPU cycles	65

Verification: TypeConv FiP32_16 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for General block TypeConv.

Test results				
Time step	1	2	...	8
CPU cycles	41	41	...	51
Inputs				
In (DSP)	0	429496730	...	-2147483648
In	0	0.2	...	-1
Outputs				
Out	0	0.2	...	-1
Exp. Out	0	0.2	...	-1
Out (DSP)	0	6553	...	-32767
Exp. Out (DSP)	0	6553	...	-32767

Test settings	
Tolerance Out	±0,0000e+00 (±0 LSB)

Test statistics	
Min CPU cycles	41
Max CPU cycles	51
Avg CPU cycles	43

Verification: TypeConv Bool_FiP16 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for General block TypeConv.

Test results		
Time step	1	2
CPU cycles	60	63
Inputs		
In (DSP)	0	1
In	0	1
Outputs		
Out	0	1
Exp. Out	0	1
Out (DSP)	0	32767
Exp. Out (DSP)	0	32767

Test settings	
Tolerance Out	±0,0000e+00 (±0 LSB)

Test statistics	
Min CPU cycles	60
Max CPU cycles	63
Avg CPU cycles	61

Verification: TypeConv Bool_FiP16 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for General block TypeConv.

Test results		
Time step	1	2
CPU cycles	31	31
Inputs		
In (DSP)	0	1
In	0	1
Outputs		
Out	0	1
Exp. Out	0	1
Out (DSP)	0	32767
Exp. Out (DSP)	0	32767

Test settings	
Tolerance Out	±0,0000e+00 (±0 LSB)

Test statistics	
Min CPU cycles	31
Max CPU cycles	31
Avg CPU cycles	31

Verification: TypeConv Bool_FiP16 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for General block TypeConv.

Test results		
Time step	1	2
CPU cycles	62	62
Inputs		
In (DSP)	0	1
In	0	1
Outputs		
Out	0	1
Exp. Out	0	1
Out (DSP)	0	32767
Exp. Out (DSP)	0	32767

Test settings	
Tolerance Out	±0,0000e+00 (±0 LSB)

Test statistics	
Min CPU cycles	62
Max CPU cycles	62
Avg CPU cycles	62

Verification: TypeConv Bool_FiP16 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for General block TypeConv.

Test results		
Time step	1	2
CPU cycles	51	51
Inputs		
In (DSP)	0	1
In	0	1
Outputs		
Out	0	1
Exp. Out	0	1
Out (DSP)	0	32767
Exp. Out (DSP)	0	32767

Test settings	
Tolerance Out	±0,0000e+00 (±0 LSB)

Test statistics	
Min CPU cycles	51
Max CPU cycles	51
Avg CPU cycles	51

Verification: TypeConv Bool_FiP16 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for General block TypeConv.

Test results		
Time step	1	2
CPU cycles	29	29
Inputs		
In (DSP)	0	1
In	0	1
Outputs		
Out	0	1
Exp. Out	0	1
Out (DSP)	0	32767
Exp. Out (DSP)	0	32767

Test settings	
Tolerance Out	±0,0000e+00 (±0 LSB)

Test statistics	
Min CPU cycles	29
Max CPU cycles	29
Avg CPU cycles	29

Verification: TypeConv Bool_FiP16 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for General block TypeConv.

Test results		
Time step	1	2
CPU cycles	43	46
Inputs		
In (DSP)	0	1
In	0	1
Outputs		
Out	0	1
Exp. Out	0	1
Out (DSP)	0	32767
Exp. Out (DSP)	0	32767

Test settings	
Tolerance Out	±0,0000e+00 (±0 LSB)

Test statistics	
Min CPU cycles	43
Max CPU cycles	46
Avg CPU cycles	44

Verification: TypeConv Bool_FiP16 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for General block TypeConv.

Test results		
Time step	1	2
CPU cycles	56	60
Inputs		
In (DSP)	0	1
In	0	1
Outputs		
Out	0	1
Exp. Out	0	1
Out (DSP)	0	32767
Exp. Out (DSP)	0	32767

Test settings	
Tolerance Out	±0,0000e+00 (±0 LSB)

Test statistics	
Min CPU cycles	56
Max CPU cycles	60
Avg CPU cycles	58

Verification: TypeConv Bool_FiP16 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for General block TypeConv.

Test results		
Time step	1	2
CPU cycles	40	46
Inputs		
In (DSP)	0	1
In	0	1
Outputs		
Out	0	1
Exp. Out	0	1
Out (DSP)	0	32767
Exp. Out (DSP)	0	32767

Test settings	
Tolerance Out	±0,0000e+00 (±0 LSB)

Test statistics	
Min CPU cycles	40
Max CPU cycles	46
Avg CPU cycles	43

Verification: TypeConv Bool_FiP32 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for General block TypeConv.

Test results		
Time step	1	2
CPU cycles	65	66
Inputs		
In (DSP)	0	1
In	0	1
Outputs		
Out	0	1
Exp. Out	0	1
Out (DSP)	0	2147483647
Exp. Out (DSP)	0	2147483647

Test settings	
Tolerance Out	±0,0000e+00 (±0 LSB)

Test statistics	
Min CPU cycles	65
Max CPU cycles	66
Avg CPU cycles	65

Verification: TypeConv Bool_FiP32 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for General block TypeConv.

Test results		
Time step	1	2
CPU cycles	31	31
Inputs		
In (DSP)	0	1
In	0	1
Outputs		
Out	0	1
Exp. Out	0	1
Out (DSP)	0	2147483647
Exp. Out (DSP)	0	2147483647

Test settings	
Tolerance Out	±0,0000e+00 (±0 LSB)

Test statistics	
Min CPU cycles	31
Max CPU cycles	31
Avg CPU cycles	31

Verification: TypeConv Bool_FiP32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for General block TypeConv.

Test results		
Time step	1	2
CPU cycles	57	57
Inputs		
In (DSP)	0	1
In	0	1
Outputs		
Out	0	1
Exp. Out	0	1
Out (DSP)	0	2147483647
Exp. Out (DSP)	0	2147483647

Test settings	
Tolerance Out	±0,0000e+00 (±0 LSB)

Test statistics	
Min CPU cycles	57
Max CPU cycles	57
Avg CPU cycles	57

Verification: TypeConv Bool_FiP32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for General block TypeConv.

Test results		
Time step	1	2
CPU cycles	51	51
Inputs		
In (DSP)	0	1
In	0	1
Outputs		
Out	0	1
Exp. Out	0	1
Out (DSP)	0	2147483647
Exp. Out (DSP)	0	2147483647

Test settings	
Tolerance Out	±0,0000e+00 (±0 LSB)

Test statistics	
Min CPU cycles	51
Max CPU cycles	51
Avg CPU cycles	51

Verification: TypeConv Bool_FiP32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for General block TypeConv.

Test results		
Time step	1	2
CPU cycles	30	32
Inputs		
In (DSP)	0	1
In	0	1
Outputs		
Out	0	1
Exp. Out	0	1
Out (DSP)	0	2147483647
Exp. Out (DSP)	0	2147483647

Test settings	
Tolerance Out	±0,0000e+00 (±0 LSB)

Test statistics	
Min CPU cycles	30
Max CPU cycles	32
Avg CPU cycles	31

Verification: TypeConv Bool_FiP32 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for General block TypeConv.

Test results		
Time step	1	2
CPU cycles	44	48
Inputs		
In (DSP)	0	1
In	0	1
Outputs		
Out	0	1
Exp. Out	0	1
Out (DSP)	0	2147483647
Exp. Out (DSP)	0	2147483647

Test settings	
Tolerance Out	±0,0000e+00 (±0 LSB)

Test statistics	
Min CPU cycles	44
Max CPU cycles	48
Avg CPU cycles	46

Verification: TypeConv Bool_FiP32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for General block TypeConv.

Test results		
Time step	1	2
CPU cycles	56	60
Inputs		
In (DSP)	0	1
In	0	1
Outputs		
Out	0	1
Exp. Out	0	1
Out (DSP)	0	2147483647
Exp. Out (DSP)	0	2147483647

Test settings	
Tolerance Out	±0,0000e+00 (±0 LSB)

Test statistics	
Min CPU cycles	56
Max CPU cycles	60
Avg CPU cycles	58

Verification: TypeConv Bool_FiP32 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for General block TypeConv.

Test results		
Time step	1	2
CPU cycles	48	54
Inputs		
In (DSP)	0	1
In	0	1
Outputs		
Out	0	1
Exp. Out	0	1
Out (DSP)	0	2147483647
Exp. Out (DSP)	0	2147483647

Test settings	
Tolerance Out	±0,0000e+00 (±0 LSB)

Test statistics	
Min CPU cycles	48
Max CPU cycles	54
Avg CPU cycles	51

Verification: TypeConv FiP16_Bool CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for General block TypeConv.

Test results						
Time step	1	2	3	4	...	8
CPU cycles	60	63	63	63	...	63
Inputs						
In (DSP)	0	6554	16384	32767	...	-32768
In	0	0.2	0.5	1	...	-1
Outputs						
Out	0	1	1	1	...	1
Exp. Out	0	1	1	1	...	1
Out (DSP)	0	1	1	1	...	1
Exp. Out (DSP)	0	1	1	1	...	1

Test settings	
Tolerance Out	±0,0000e+00 (±0 LSB)

Test statistics	
Min CPU cycles	60
Max CPU cycles	63
Avg CPU cycles	62

Verification: TypeConv FiP16_Bool CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for General block TypeConv.

Test results						
Time step	1	2	3	4	...	8
CPU cycles	29	29	29	29	...	29
Inputs						
In (DSP)	0	6554	16384	32767	...	-32768
In	0	0.2	0.5	1	...	-1
Outputs						
Out	0	1	1	1	...	1
Exp. Out	0	1	1	1	...	1
Out (DSP)	0	1	1	1	...	1
Exp. Out (DSP)	0	1	1	1	...	1

Test settings	
Tolerance Out	±0,0000e+00 (±0 LSB)

Test statistics	
Min CPU cycles	29
Max CPU cycles	29
Avg CPU cycles	29

Verification: TypeConv FiP16_Bool CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for General block TypeConv.

Test results						
Time step	1	2	3	4	...	8
CPU cycles	57	57	57	57	...	57
Inputs						
In (DSP)	0	6554	16384	32767	...	-32768
In	0	0.2	0.5	1	...	-1
Outputs						
Out	0	1	1	1	...	1
Exp. Out	0	1	1	1	...	1
Out (DSP)	0	1	1	1	...	1
Exp. Out (DSP)	0	1	1	1	...	1

Test settings	
Tolerance Out	±0,0000e+00 (±0 LSB)

Test statistics	
Min CPU cycles	57
Max CPU cycles	57
Avg CPU cycles	57

Verification: TypeConv FiP16_Bool CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for General block TypeConv.

Test results						
Time step	1	2	3	4	...	8
CPU cycles	49	49	49	49	...	49
Inputs						
In (DSP)	0	6554	16384	32767	...	-32768
In	0	0.2	0.5	1	...	-1
Outputs						
Out	0	1	1	1	...	1
Exp. Out	0	1	1	1	...	1
Out (DSP)	0	1	1	1	...	1
Exp. Out (DSP)	0	1	1	1	...	1

Test settings	
Tolerance Out	±0,0000e+00 (±0 LSB)

Test statistics	
Min CPU cycles	49
Max CPU cycles	49
Avg CPU cycles	49

Verification: TypeConv FiP16_Bool CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for General block TypeConv.

Test results						
Time step	1	2	3	4	...	8
CPU cycles	29	29	29	29	...	29
Inputs						
In (DSP)	0	6554	16384	32767	...	-32768
In	0	0.2	0.5	1	...	-1
Outputs						
Out	0	1	1	1	...	1
Exp. Out	0	1	1	1	...	1
Out (DSP)	0	1	1	1	...	1
Exp. Out (DSP)	0	1	1	1	...	1

Test settings	
Tolerance Out	±0,0000e+00 (±0 LSB)

Test statistics	
Min CPU cycles	29
Max CPU cycles	29
Avg CPU cycles	29

Verification: TypeConv FiP16_Bool CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for General block TypeConv.

Test results						
Time step	1	2	3	4	...	8
CPU cycles	43	47	47	47	...	47
Inputs						
In (DSP)	0	6554	16384	32767	...	-32768
In	0	0.2	0.5	1	...	-1
Outputs						
Out	0	1	1	1	...	1
Exp. Out	0	1	1	1	...	1
Out (DSP)	0	1	1	1	...	1
Exp. Out (DSP)	0	1	1	1	...	1

Test settings	
Tolerance Out	±0,0000e+00 (±0 LSB)

Test statistics	
Min CPU cycles	43
Max CPU cycles	47
Avg CPU cycles	46

Verification: TypeConv FiP16_Bool CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for General block TypeConv.

Test results						
Time step	1	2	3	4	...	8
CPU cycles	66	59	59	59	...	59
Inputs						
In (DSP)	0	6554	16384	32767	...	-32768
In	0	0.2	0.5	1	...	-1
Outputs						
Out	0	1	1	1	...	1
Exp. Out	0	1	1	1	...	1
Out (DSP)	0	1	1	1	...	1
Exp. Out (DSP)	0	1	1	1	...	1

Test settings	
Tolerance Out	±0,0000e+00 (±0 LSB)

Test statistics	
Min CPU cycles	59
Max CPU cycles	66
Avg CPU cycles	59

Verification: TypeConv FiP16_Bool CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for General block TypeConv.

Test results						
Time step	1	2	3	4	...	8
CPU cycles	40	46	46	46	...	46
Inputs						
In (DSP)	0	6554	16384	32767	...	-32768
In	0	0.2	0.5	1	...	-1
Outputs						
Out	0	1	1	1	...	1
Exp. Out	0	1	1	1	...	1
Out (DSP)	0	1	1	1	...	1
Exp. Out (DSP)	0	1	1	1	...	1

Test settings	
Tolerance Out	±0,0000e+00 (±0 LSB)

Test statistics	
Min CPU cycles	40
Max CPU cycles	46
Avg CPU cycles	45

Verification: TypeConv FiP32_Bool CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for General block TypeConv.

Test results				
Time step	1	2	...	7
CPU cycles	60	63	...	63
Inputs				
In (DSP)	0	429496730	...	-429496730
In	0	0.2	...	-0.2
Outputs				
Out	0	1	...	1
Exp. Out	0	1	...	1
Out (DSP)	0	1	...	1
Exp. Out (DSP)	0	1	...	1

Test settings	
Tolerance Out	±0,0000e+00 (±0 LSB)

Test statistics	
Min CPU cycles	60
Max CPU cycles	63
Avg CPU cycles	62

Verification: TypeConv FiP32_Bool CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for General block TypeConv.

Test results				
Time step	1	2	...	7
CPU cycles	31	29	...	29
Inputs				
In (DSP)	0	429496730	...	-429496730
In	0	0.2	...	-0.2
Outputs				
Out	0	1	...	1
Exp. Out	0	1	...	1
Out (DSP)	0	1	...	1
Exp. Out (DSP)	0	1	...	1

Test settings	
Tolerance Out	±0,0000e+00 (±0 LSB)

Test statistics	
Min CPU cycles	29
Max CPU cycles	31
Avg CPU cycles	29

Verification: TypeConv FiP32_Bool CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for General block TypeConv.

Test results				
Time step	1	2	...	7
CPU cycles	57	57	...	57
Inputs				
In (DSP)	0	429496730	...	-429496730
In	0	0.2	...	-0.2
Outputs				
Out	0	1	...	1
Exp. Out	0	1	...	1
Out (DSP)	0	1	...	1
Exp. Out (DSP)	0	1	...	1

Test settings	
Tolerance Out	±0,0000e+00 (±0 LSB)

Test statistics	
Min CPU cycles	57
Max CPU cycles	57
Avg CPU cycles	57

Verification: TypeConv FiP32_Bool CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for General block TypeConv.

Test results				
Time step	1	2	...	7
CPU cycles	48	48	...	48
Inputs				
In (DSP)	0	429496730	...	-429496730
In	0	0.2	...	-0.2
Outputs				
Out	0	1	...	1
Exp. Out	0	1	...	1
Out (DSP)	0	1	...	1
Exp. Out (DSP)	0	1	...	1

Test settings	
Tolerance Out	±0,0000e+00 (±0 LSB)

Test statistics	
Min CPU cycles	48
Max CPU cycles	48
Avg CPU cycles	48

Verification: TypeConv FiP32_Bool CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for General block TypeConv.

Test results				
Time step	1	2	...	7
CPU cycles	29	29	...	29
Inputs				
In (DSP)	0	429496730	...	-429496730
In	0	0.2	...	-0.2
Outputs				
Out	0	1	...	1
Exp. Out	0	1	...	1
Out (DSP)	0	1	...	1
Exp. Out (DSP)	0	1	...	1

Test settings	
Tolerance Out	±0,0000e+00 (±0 LSB)

Test statistics	
Min CPU cycles	29
Max CPU cycles	29
Avg CPU cycles	29

Verification: TypeConv FiP32_Bool CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for General block TypeConv.

Test results				
Time step	1	2	...	7
CPU cycles	46	49	...	49
Inputs				
In (DSP)	0	429496730	...	-429496730
In	0	0.2	...	-0.2
Outputs				
Out	0	1	...	1
Exp. Out	0	1	...	1
Out (DSP)	0	1	...	1
Exp. Out (DSP)	0	1	...	1

Test settings	
Tolerance Out	±0,0000e+00 (±0 LSB)

Test statistics	
Min CPU cycles	46
Max CPU cycles	49
Avg CPU cycles	48

Verification: TypeConv FiP32_Bool CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for General block TypeConv.

Test results				
Time step	1	2	...	7
CPU cycles	56	59	...	59
Inputs				
In (DSP)	0	429496730	...	-429496730
In	0	0.2	...	-0.2
Outputs				
Out	0	1	...	1
Exp. Out	0	1	...	1
Out (DSP)	0	1	...	1
Exp. Out (DSP)	0	1	...	1

Test settings	
Tolerance Out	±0,0000e+00 (±0 LSB)

Test statistics	
Min CPU cycles	56
Max CPU cycles	59
Avg CPU cycles	58

Verification: TypeConv FiP32_Bool CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for General block TypeConv.

Test results				
Time step	1	2	...	7
CPU cycles	40	46	...	46
Inputs				
In (DSP)	0	429496730	...	-429496730
In	0	0.2	...	-0.2
Outputs				
Out	0	1	...	1
Exp. Out	0	1	...	1
Out (DSP)	0	1	...	1
Exp. Out (DSP)	0	1	...	1

Test settings	
Tolerance Out	±0,0000e+00 (±0 LSB)

Test statistics	
Min CPU cycles	40
Max CPU cycles	46
Avg CPU cycles	45

Block: uConstant



Constant value.

Outports	
Out	Constant output

Mask Parameters		
Name	**ID**	**Description**
Value	1	Constant factor

Implementations:

Bool	Boolean Integration
Int8	8 Bit Integer Implementation
Int16	16 Bit Integer Implementation
Int32	32 Bit Integer Implementation
FiP8	8 Bit Fixed Point Implementation
FiP16	16 Bit Fixed Point Implementation
FiP32	32 Bit Fixed Point Implementation
Float32	32 Bit Floating Point Implementation
Float64	64 Bit Floating Point Implementation

Implementation: Bool

Boolean Integration

Outports Data Type	
Out	bool

Implementation: Int8

8 Bit Integer Implementation

Outports Data Type	
Out	int8

Implementation: Int16

16 Bit Integer Implementation

Outports Data Type	
Out	int16

Implementation: Int32

32 Bit Integer Implementation

Outports Data Type	
Out	int32

Implementation: FiP8

8 Bit Fixed Point Implementation

Outports Data Type	
Out	int8

Implementation: FiP16

16 Bit Fixed Point Implementation

Outports Data Type	
Out	int16

Implementation: FiP32

32 Bit Fixed Point Implementation

Outports Data Type	
Out	int32

Implementation: Float32

32 Bit Floating Point Implementation

Outports Data Type	
Out	float32

Implementation: Float64

64 Bit Floating Point Implementation

Outports Data Type	
Out	float64

Verification: uConstant Bool CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Conversion test — OK

Conversion test for General block uConstant.

Test results						
Time step	1	2	3	4	...	7
Mask parameters						
Value	1	-1	0	0.5	...	-2.3
Controller parameters						
K	1	1	0	1	...	1
Exp. K	1	1	0	1	...	1

Test settings	
Tolerance K	±0,0000e+00

Test case: Conversion-on-Target test — OK

Conversion-on-Target test for General block uConstant.

Test results						
Time step	1	2	3	4	...	7
Mask parameters						
Value	1	-1	0	0.5	...	-2.3
Controller parameters						
K	1	1	0	1	...	1
Exp. K	1	1	0	1	...	1

Test settings	
Tolerance K	±0,0000e+00

Test statistics	
Min CPU cycles	787
Max CPU cycles	817
Avg CPU cycles	812

Verification: uConstant Bool CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Conversion test — OK

Conversion test for General block uConstant.

Test results						
Time step	1	2	3	4	...	7
Mask parameters						
Value	1	-1	0	0.5	...	-2.3
Controller parameters						
K	1	1	0	1	...	1
Exp. K	1	1	0	1	...	1

Test settings	
Tolerance K	±0,0000e+00

Test case: Conversion-on-Target test — OK

Conversion-on-Target test for General block uConstant.

Test results						
Time step	1	2	3	4	...	7
Mask parameters						
Value	1	-1	0	0.5	...	-2.3
Controller parameters						
K	1	1	0	1	...	1
Exp. K	1	1	0	1	...	1

Test settings	
Tolerance K	±0,0000e+00

Test statistics	
Min CPU cycles	373
Max CPU cycles	399
Avg CPU cycles	393

Verification: uConstant Bool CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Conversion test OK

Conversion test for General block uConstant.

Test results						
Time step	1	2	3	4	...	7
Mask parameters						
Value	1	-1	0	0.5	...	-2.3
Controller parameters						
K	1	1	0	1	...	1
Exp. K	1	1	0	1	...	1

Test settings	
Tolerance K	±0,0000e+00

Test case: Conversion-on-Target test OK

Conversion-on-Target test for General block uConstant.

Test results						
Time step	1	2	3	4	...	7
Mask parameters						
Value	1	-1	0	0.5	...	-2.3
Controller parameters						
K	1	1	0	1	...	1
Exp. K	1	1	0	1	...	1

Test settings	
Tolerance K	±0,0000e+00

Test statistics	
Min CPU cycles	514
Max CPU cycles	534
Avg CPU cycles	531

Verification: uConstant Bool CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Conversion test — OK

Conversion test for General block uConstant.

Test results						
Time step	1	2	3	4	...	7
Mask parameters						
Value	1	-1	0	0.5	...	-2.3
Controller parameters						
K	1	1	0	1	...	1
Exp. K	1	1	0	1	...	1

Test settings	
Tolerance K	±0,0000e+00

Test case: Conversion-on-Target test — OK

Conversion-on-Target test for General block uConstant.

Test results						
Time step	1	2	3	4	...	7
Mask parameters						
Value	1	-1	0	0.5	...	-2.3
Controller parameters						
K	1	1	0	1	...	1
Exp. K	1	1	0	1	...	1

Test settings	
Tolerance K	±0,0000e+00

Test statistics	
Min CPU cycles	593
Max CPU cycles	606
Avg CPU cycles	594

Verification: uConstant Bool CPU PIC32MX170F256

Date of Test 2026-06-19

Target controller PIC32MX170F256

Test case: Conversion test OK

Conversion test for General block uConstant.

Test results						
Time step	1	2	3	4	...	7
Mask parameters						
Value	1	-1	0	0.5	...	-2.3
Controller parameters						
K	1	1	0	1	...	1
Exp. K	1	1	0	1	...	1

Test settings	
Tolerance K	±0,0000e+00

Test case: Conversion-on-Target test OK

Conversion-on-Target test for General block uConstant.

Test results						
Time step	1	2	3	4	...	7
Mask parameters						
Value	1	-1	0	0.5	...	-2.3
Controller parameters						
K	1	1	0	1	...	1
Exp. K	1	1	0	1	...	1

Test settings	
Tolerance K	±0,0000e+00

Test statistics	
Min CPU cycles	243
Max CPU cycles	276
Avg CPU cycles	265

Verification: uConstant Bool CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Conversion test — OK

Conversion test for General block uConstant.

Test results						
Time step	1	2	3	4	...	7
Mask parameters						
Value	1	-1	0	0.5	...	-2.3
Controller parameters						
K	1	1	0	1	...	1
Exp. K	1	1	0	1	...	1

Test settings	
Tolerance K	±0,0000e+00

Test case: Conversion-on-Target test — OK

Conversion-on-Target test for General block uConstant.

Test results						
Time step	1	2	3	4	...	7
Mask parameters						
Value	1	-1	0	0.5	...	-2.3
Controller parameters						
K	1	1	0	1	...	1
Exp. K	1	1	0	1	...	1

Test settings	
Tolerance K	±0,0000e+00

Test statistics	
Min CPU cycles	521
Max CPU cycles	552
Avg CPU cycles	528

Verification: uConstant Bool CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Conversion test — OK

Conversion test for General block uConstant.

Test results						
Time step	1	2	3	4	...	7
Mask parameters						
Value	1	-1	0	0.5	...	-2.3
Controller parameters						
K	1	1	0	1	...	1
Exp. K	1	1	0	1	...	1

Test settings	
Tolerance K	±0,0000e+00

Test case: Conversion-on-Target test — OK

Conversion-on-Target test for General block uConstant.

Test results						
Time step	1	2	3	4	...	7
Mask parameters						
Value	1	-1	0	0.5	...	-2.3
Controller parameters						
K	1	1	0	1	...	1
Exp. K	1	1	0	1	...	1

Test settings	
Tolerance K	±0,0000e+00

Test statistics	
Min CPU cycles	417
Max CPU cycles	491
Avg CPU cycles	434

Verification: uConstant Bool CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Conversion test — OK

Conversion test for General block uConstant.

Test results						
Time step	1	2	3	4	...	7
Mask parameters						
Value	1	-1	0	0.5	...	-2.3
Controller parameters						
K	1	1	0	1	...	1
Exp. K	1	1	0	1	...	1

Test settings	
Tolerance K	±0,0000e+00

Test case: Conversion-on-Target test — OK

Conversion-on-Target test for General block uConstant.

Test results						
Time step	1	2	3	4	...	7
Mask parameters						
Value	1	-1	0	0.5	...	-2.3
Controller parameters						
K	1	1	0	1	...	1
Exp. K	1	1	0	1	...	1

Test settings	
Tolerance K	±0,0000e+00

Test statistics	
Min CPU cycles	615
Max CPU cycles	641
Avg CPU cycles	637

Verification: uConstant Int16 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Conversion test — OK

Conversion test for General block uConstant.

Test results						
Time step	1	2	3	4	...	17
Mask parameters						
Value	33000	32768	32767	32766	...	-33000
Controller parameters						
K	32767	32767	32767	32766	...	-32767
Exp. K	32767	32767	32767	32766	...	-32767

Test settings	
Tolerance K	±0,0000e+00

Test case: Conversion-on-Target test — OK

Conversion-on-Target test for General block uConstant.

Test results						
Time step	1	2	3	4	...	17
Mask parameters						
Value	33000	32768	32767	32766	...	-33000
Controller parameters						
K	32767	32767	32767	32766	...	-32767
Exp. K	32767	32767	32767	32766	...	-32767

Test settings	
Tolerance K	±0,0000e+00

Test statistics	
Min CPU cycles	1188
Max CPU cycles	1433
Avg CPU cycles	1399

Verification: uConstant Int16 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Conversion test — OK

Conversion test for General block uConstant.

Test results						
Time step	1	2	3	4	...	17
Mask parameters						
Value	33000	32768	32767	32766	...	-33000
Controller parameters						
K	32767	32767	32767	32766	...	-32767
Exp. K	32767	32767	32767	32766	...	-32767

Test settings	
Tolerance K	±0,0000e+00

Test case: Conversion-on-Target test — OK

Conversion-on-Target test for General block uConstant.

Test results						
Time step	1	2	3	4	...	17
Mask parameters						
Value	33000	32768	32767	32766	...	-33000
Controller parameters						
K	32767	32767	32767	32766	...	-32767
Exp. K	32767	32767	32767	32766	...	-32767

Test settings	
Tolerance K	±0,0000e+00

Test statistics	
Min CPU cycles	653
Max CPU cycles	889
Avg CPU cycles	842

Verification: uConstant Int16 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Conversion test OK

Conversion test for General block uConstant.

Test results						
Time step	1	2	3	4	...	17
Mask parameters						
Value	33000	32768	32767	32766	...	-33000
Controller parameters						
K	32767	32767	32767	32766	...	-32767
Exp. K	32767	32767	32767	32766	...	-32767

Test settings	
Tolerance K	±0,0000e+00

Test case: Conversion-on-Target test OK

Conversion-on-Target test for General block uConstant.

Test results						
Time step	1	2	3	4	...	17
Mask parameters						
Value	33000	32768	32767	32766	...	-33000
Controller parameters						
K	32767	32767	32767	32766	...	-32767
Exp. K	32767	32767	32767	32766	...	-32767

Test settings	
Tolerance K	±0,0000e+00

Test statistics	
Min CPU cycles	860
Max CPU cycles	1089
Avg CPU cycles	1047

Verification: uConstant Int16 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Conversion test — OK

Conversion test for General block uConstant.

Test results						
Time step	1	2	3	4	...	17
Mask parameters						
Value	33000	32768	32767	32766	...	-33000
Controller parameters						
K	32767	32767	32767	32766	...	-32767
Exp. K	32767	32767	32767	32766	...	-32767

Test settings	
Tolerance K	±0,0000e+00

Test case: Conversion-on-Target test — OK

Conversion-on-Target test for General block uConstant.

Test results						
Time step	1	2	3	4	...	17
Mask parameters						
Value	33000	32768	32767	32766	...	-33000
Controller parameters						
K	32767	32767	32767	32766	...	-32767
Exp. K	32767	32767	32767	32766	...	-32767

Test settings	
Tolerance K	±0,0000e+00

Test statistics	
Min CPU cycles	923
Max CPU cycles	1246
Avg CPU cycles	1199

Verification: uConstant Int16 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Conversion test — OK

Conversion test for General block uConstant.

Test results						
Time step	1	2	3	4	...	17
Mask parameters						
Value	33000	32768	32767	32766	...	-33000
Controller parameters						
K	32767	32767	32767	32766	...	-32767
Exp. K	32767	32767	32767	32766	...	-32767

Test settings	
Tolerance K	±0,0000e+00

Test case: Conversion-on-Target test — OK

Conversion-on-Target test for General block uConstant.

Test results						
Time step	1	2	3	4	...	17
Mask parameters						
Value	33000	32768	32767	32766	...	-33000
Controller parameters						
K	32767	32767	32767	32766	...	-32767
Exp. K	32767	32767	32767	32766	...	-32767

Test settings	
Tolerance K	±0,0000e+00

Test statistics	
Min CPU cycles	399
Max CPU cycles	473
Avg CPU cycles	465

Verification: uConstant Int16 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Conversion test — OK

Conversion test for General block uConstant.

Test results						
Time step	1	2	3	4	...	17
Mask parameters						
Value	33000	32768	32767	32766	...	-33000
Controller parameters						
K	32767	32767	32767	32766	...	-32767
Exp. K	32767	32767	32767	32766	...	-32767

Test settings	
Tolerance K	±0,0000e+00

Test case: Conversion-on-Target test — OK

Conversion-on-Target test for General block uConstant.

Test results						
Time step	1	2	3	4	...	17
Mask parameters						
Value	33000	32768	32767	32766	...	-33000
Controller parameters						
K	32767	32767	32767	32766	...	-32767
Exp. K	32767	32767	32767	32766	...	-32767

Test settings	
Tolerance K	±0,0000e+00

Test statistics	
Min CPU cycles	1300
Max CPU cycles	1729
Avg CPU cycles	1607

Verification: uConstant Int16 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Conversion test — OK

Conversion test for General block uConstant.

Test results						
Time step	1	2	3	4	...	17
Mask parameters						
Value	33000	32768	32767	32766	...	-33000
Controller parameters						
K	32767	32767	32767	32766	...	-32767
Exp. K	32767	32767	32767	32766	...	-32767

Test settings	
Tolerance K	±0,0000e+00

Test case: Conversion-on-Target test — OK

Conversion-on-Target test for General block uConstant.

Test results						
Time step	1	2	3	4	...	17
Mask parameters						
Value	33000	32768	32767	32766	...	-33000
Controller parameters						
K	32767	32767	32767	32766	...	-32767
Exp. K	32767	32767	32767	32766	...	-32767

Test settings	
Tolerance K	±0,0000e+00

Test statistics	
Min CPU cycles	723
Max CPU cycles	1023
Avg CPU cycles	895

Verification: uConstant Int16 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Conversion test — OK

Conversion test for General block uConstant.

Test results						
Time step	1	2	3	4	...	17
Mask parameters						
Value	33000	32768	32767	32766	...	-33000
Controller parameters						
K	32767	32767	32767	32766	...	-32767
Exp. K	32767	32767	32767	32766	...	-32767

Test settings	
Tolerance K	±0,0000e+00

Test case: Conversion-on-Target test — OK

Conversion-on-Target test for General block uConstant.

Test results						
Time step	1	2	3	4	...	17
Mask parameters						
Value	33000	32768	32767	32766	...	-33000
Controller parameters						
K	32767	32767	32767	32766	...	-32767
Exp. K	32767	32767	32767	32766	...	-32767

Test settings	
Tolerance K	±0,0000e+00

Test statistics	
Min CPU cycles	1089
Max CPU cycles	1465
Avg CPU cycles	1401

Verification: uConstant Int32 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Conversion test — OK

Conversion test for General block uConstant.

Test results				
Time step	1	2	...	17
Mask parameters				
Value	3300000000	2147483648	...	-3300000000
Controller parameters				
K	2147483647	2147483647	...	-2147483647
Exp. K	2147483647	2147483647	...	-2147483647

Test settings	
Tolerance K	±0,0000e+00

Test case: Conversion-on-Target test — OK

Conversion-on-Target test for General block uConstant.

Test results				
Time step	1	2	...	17
Mask parameters				
Value	3300000000	2147483648	...	-3300000000
Controller parameters				
K	2147483647	2147483647	...	-2147483647
Exp. K	2147483647	2147483647	...	-2147483647

Test settings	
Tolerance K	±3,0000e+00

Test statistics	
Min CPU cycles	1210
Max CPU cycles	1456
Avg CPU cycles	1385

Verification: uConstant Int32 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Conversion test — OK

Conversion test for General block uConstant.

Test results				
Time step	1	2	...	17
Mask parameters				
Value	3300000000	2147483648	...	-3300000000
Controller parameters				
K	2147483647	2147483647	...	-2147483647
Exp. K	2147483647	2147483647	...	-2147483647

Test settings	
Tolerance K	±0,0000e+00

Test case: Conversion-on-Target test — OK

Conversion-on-Target test for General block uConstant.

Test results				
Time step	1	2	...	17
Mask parameters				
Value	3300000000	2147483648	...	-3300000000
Controller parameters				
K	2147483647	2147483647	...	-2147483647
Exp. K	2147483647	2147483647	...	-2147483647

Test settings	
Tolerance K	±3,0000e+00

Test statistics	
Min CPU cycles	677
Max CPU cycles	893
Avg CPU cycles	859

Verification: uConstant Int32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Conversion test — OK

Conversion test for General block uConstant.

Test results				
Time step	1	2	...	17
Mask parameters				
Value	3300000000	2147483648	...	-3300000000
Controller parameters				
K	2147483647	2147483647	...	-2147483647
Exp. K	2147483647	2147483647	...	-2147483647

Test settings	
Tolerance K	±0,0000e+00

Test case: Conversion-on-Target test — OK

Conversion-on-Target test for General block uConstant.

Test results				
Time step	1	2	...	17
Mask parameters				
Value	3300000000	2147483648	...	-3300000000
Controller parameters				
K	2147483647	2147483647	...	-2147483647
Exp. K	2147483647	2147483647	...	-2147483647

Test settings	
Tolerance K	±3,0000e+00

Test statistics	
Min CPU cycles	869
Max CPU cycles	1132
Avg CPU cycles	1068

Verification: uConstant Int32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Conversion test — OK

Conversion test for General block uConstant.

Test results				
Time step	1	2	...	17
Mask parameters				
Value	3300000000	2147483648	...	-3300000000
Controller parameters				
K	2147483647	2147483647	...	-2147483647
Exp. K	2147483647	2147483647	...	-2147483647

Test settings	
Tolerance K	±0,0000e+00

Test case: Conversion-on-Target test — OK

Conversion-on-Target test for General block uConstant.

Test results				
Time step	1	2	...	17
Mask parameters				
Value	3300000000	2147483648	...	-3300000000
Controller parameters				
K	2147483647	2147483647	...	-2147483647
Exp. K	2147483647	2147483647	...	-2147483647

Test settings	
Tolerance K	±3,0000e+00

Test statistics	
Min CPU cycles	953
Max CPU cycles	1269
Avg CPU cycles	1227

Verification: uConstant Int32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Conversion test — OK

Conversion test for General block uConstant.

Test results				
Time step	1	2	...	17
Mask parameters				
Value	3300000000	2147483648	...	-3300000000
Controller parameters				
K	2147483647	2147483647	...	-2147483647
Exp. K	2147483647	2147483647	...	-2147483647

Test settings	
Tolerance K	±0,0000e+00

Test case: Conversion-on-Target test — OK

Conversion-on-Target test for General block uConstant.

Test results				
Time step	1	2	...	17
Mask parameters				
Value	3300000000	2147483648	...	-3300000000
Controller parameters				
K	2147483647	2147483647	...	-2147483647
Exp. K	2147483647	2147483647	...	-2147483647

Test settings	
Tolerance K	±3,0000e+00

Test statistics	
Min CPU cycles	395
Max CPU cycles	475
Avg CPU cycles	461

Verification: uConstant Int32 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Conversion test — OK

Conversion test for General block uConstant.

Test results				
Time step	1	2	...	17
Mask parameters				
Value	3300000000	2147483648	...	-3300000000
Controller parameters				
K	2147483647	2147483647	...	-2147483647
Exp. K	2147483647	2147483647	...	-2147483647

Test settings	
Tolerance K	±0,0000e+00

Test case: Conversion-on-Target test — OK

Conversion-on-Target test for General block uConstant.

Test results				
Time step	1	2	...	17
Mask parameters				
Value	3300000000	2147483648	...	-3300000000
Controller parameters				
K	2147483647	2147483647	...	-2147483647
Exp. K	2147483647	2147483647	...	-2147483647

Test settings	
Tolerance K	±3,0000e+00

Test statistics	
Min CPU cycles	1321
Max CPU cycles	1731
Avg CPU cycles	1611

Verification: uConstant Int32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Conversion test — OK

Conversion test for General block uConstant.

Test results				
Time step	1	2	...	17
Mask parameters				
Value	3300000000	2147483648	...	-3300000000
Controller parameters				
K	2147483647	2147483647	...	-2147483647
Exp. K	2147483647	2147483647	...	-2147483647

Test settings	
Tolerance K	±0,0000e+00

Test case: Conversion-on-Target test — OK

Conversion-on-Target test for General block uConstant.

Test results				
Time step	1	2	...	17
Mask parameters				
Value	3300000000	2147483648	...	-3300000000
Controller parameters				
K	2147483647	2147483647	...	-2147483647
Exp. K	2147483647	2147483647	...	-2147483647

Test settings	
Tolerance K	±3,0000e+00

Test statistics	
Min CPU cycles	698
Max CPU cycles	1019
Avg CPU cycles	874

Verification: uConstant Int32 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Conversion test — OK

Conversion test for General block uConstant.

Test results				
Time step	1	2	...	17
Mask parameters				
Value	3300000000	2147483648	...	-3300000000
Controller parameters				
K	2147483647	2147483647	...	-2147483647
Exp. K	2147483647	2147483647	...	-2147483647

Test settings	
Tolerance K	±0,0000e+00

Test case: Conversion-on-Target test — OK

Conversion-on-Target test for General block uConstant.

Test results				
Time step	1	2	...	17
Mask parameters				
Value	3300000000	2147483648	...	-3300000000
Controller parameters				
K	2147483647	2147483647	...	-2147483647
Exp. K	2147483647	2147483647	...	-2147483647

Test settings	
Tolerance K	±3,0000e+00

Test statistics	
Min CPU cycles	1112
Max CPU cycles	1484
Avg CPU cycles	1440

Verification: uConstant FiP16 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Conversion test — OK

Conversion test for General block uConstant.

Test results						
Time step	1	2	3	4	...	7
Mask parameters						
Value	1	-1	0	0.5	...	-2.3
Controller parameters						
K	32767	-32767	0	16384	...	-32767
Exp. K	32767	-32768	0	16384	...	-32768

Test settings	
Tolerance K	±1,0000e+00

Test case: Conversion-on-Target test — OK

Conversion-on-Target test for General block uConstant.

Test results						
Time step	1	2	3	4	...	7
Mask parameters						
Value	1	-1	0	0.5	...	-2.3
Controller parameters						
K	32767	-32767	0	16384	...	-32767
Exp. K	32767	-32768	0	16384	...	-32768

Test settings	
Tolerance K	±1,0000e+00

Test statistics	
Min CPU cycles	854
Max CPU cycles	871
Avg CPU cycles	856

Verification: uConstant FiP16 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Conversion test — OK

Conversion test for General block uConstant.

Test results						
Time step	1	2	3	4	...	7
Mask parameters						
Value	1	-1	0	0.5	...	-2.3
Controller parameters						
K	32767	-32767	0	16384	...	-32767
Exp. K	32767	-32768	0	16384	...	-32768

Test settings	
Tolerance K	±1,0000e+00

Test case: Conversion-on-Target test — OK

Conversion-on-Target test for General block uConstant.

Test results						
Time step	1	2	3	4	...	7
Mask parameters						
Value	1	-1	0	0.5	...	-2.3
Controller parameters						
K	32767	-32767	0	16384	...	-32767
Exp. K	32767	-32768	0	16384	...	-32768

Test settings	
Tolerance K	±1,0000e+00

Test statistics	
Min CPU cycles	401
Max CPU cycles	407
Avg CPU cycles	404

Verification: uConstant FiP16 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Conversion test — OK

Conversion test for General block uConstant.

Test results						
Time step	1	2	3	4	...	7
Mask parameters						
Value	1	-1	0	0.5	...	-2.3
Controller parameters						
K	32767	-32767	0	16384	...	-32767
Exp. K	32767	-32768	0	16384	...	-32768

Test settings	
Tolerance K	±1,0000e+00

Test case: Conversion-on-Target test — OK

Conversion-on-Target test for General block uConstant.

Test results						
Time step	1	2	3	4	...	7
Mask parameters						
Value	1	-1	0	0.5	...	-2.3
Controller parameters						
K	32767	-32767	0	16384	...	-32767
Exp. K	32767	-32768	0	16384	...	-32768

Test settings	
Tolerance K	±1,0000e+00

Test statistics	
Min CPU cycles	520
Max CPU cycles	520
Avg CPU cycles	520

Verification: uConstant FiP16 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Conversion test — OK

Conversion test for General block uConstant.

Test results						
Time step	1	2	3	4	...	7
Mask parameters						
Value	1	-1	0	0.5	...	-2.3
Controller parameters						
K	32767	-32767	0	16384	...	-32767
Exp. K	32767	-32768	0	16384	...	-32768

Test settings	
Tolerance K	±1,0000e+00

Test case: Conversion-on-Target test — OK

Conversion-on-Target test for General block uConstant.

Test results						
Time step	1	2	3	4	...	7
Mask parameters						
Value	1	-1	0	0.5	...	-2.3
Controller parameters						
K	32767	-32767	0	16384	...	-32767
Exp. K	32767	-32768	0	16384	...	-32768

Test settings	
Tolerance K	±1,0000e+00

Test statistics	
Min CPU cycles	810
Max CPU cycles	912
Avg CPU cycles	890

Verification: uConstant FiP16 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Conversion test OK

Conversion test for General block uConstant.

Test results						
Time step	1	2	3	4	...	7
Mask parameters						
Value	1	-1	0	0.5	...	-2.3
Controller parameters						
K	32767	-32767	0	16384	...	-32767
Exp. K	32767	-32768	0	16384	...	-32768

Test settings	
Tolerance K	±1,0000e+00

Test case: Conversion-on-Target test OK

Conversion-on-Target test for General block uConstant.

Test results						
Time step	1	2	3	4	...	7
Mask parameters						
Value	1	-1	0	0.5	...	-2.3
Controller parameters						
K	32767	-32767	0	16384	...	-32767
Exp. K	32767	-32768	0	16384	...	-32768

Test settings	
Tolerance K	±1,0000e+00

Test statistics	
Min CPU cycles	384
Max CPU cycles	405
Avg CPU cycles	401

Verification: uConstant FiP16 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Conversion test

OK

Conversion test for General block uConstant.

Test results						
Time step	1	2	3	4	...	7
Mask parameters						
Value	1	-1	0	0.5	...	-2.3
Controller parameters						
K	32767	-32767	0	16384	...	-32767
Exp. K	32767	-32768	0	16384	...	-32768

Test settings	
Tolerance K	±1,0000e+00

Test case: Conversion-on-Target test

OK

Conversion-on-Target test for General block uConstant.

Test results						
Time step	1	2	3	4	...	7
Mask parameters						
Value	1	-1	0	0.5	...	-2.3
Controller parameters						
K	32767	-32767	0	16384	...	-32767
Exp. K	32767	-32768	0	16384	...	-32768

Test settings	
Tolerance K	±1,0000e+00

Test statistics	
Min CPU cycles	839
Max CPU cycles	1291
Avg CPU cycles	1219

Verification: uConstant FiP16 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Conversion test — OK

Conversion test for General block uConstant.

Test results						
Time step	1	2	3	4	...	7
Mask parameters						
Value	1	-1	0	0.5	...	-2.3
Controller parameters						
K	32767	-32767	0	16384	...	-32767
Exp. K	32767	-32768	0	16384	...	-32768

Test settings	
Tolerance K	±1,0000e+00

Test case: Conversion-on-Target test — OK

Conversion-on-Target test for General block uConstant.

Test results						
Time step	1	2	3	4	...	7
Mask parameters						
Value	1	-1	0	0.5	...	-2.3
Controller parameters						
K	32767	-32767	0	16384	...	-32767
Exp. K	32767	-32768	0	16384	...	-32768

Test settings	
Tolerance K	±1,0000e+00

Test statistics	
Min CPU cycles	397
Max CPU cycles	473
Avg CPU cycles	409

Verification: uConstant FiP16 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Conversion test

OK

Conversion test for General block uConstant.

Test results						
Time step	1	2	3	4	...	7
Mask parameters						
Value	1	-1	0	0.5	...	-2.3
Controller parameters						
K	32767	-32767	0	16384	...	-32767
Exp. K	32767	-32768	0	16384	...	-32768

Test settings	
Tolerance K	±1,0000e+00

Test case: Conversion-on-Target test

OK

Conversion-on-Target test for General block uConstant.

Test results						
Time step	1	2	3	4	...	7
Mask parameters						
Value	1	-1	0	0.5	...	-2.3
Controller parameters						
K	32767	-32767	0	16384	...	-32767
Exp. K	32767	-32768	0	16384	...	-32768

Test settings	
Tolerance K	±1,0000e+00

Test statistics	
Min CPU cycles	661
Max CPU cycles	665
Avg CPU cycles	662

Verification: uConstant FiP32 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Conversion test — OK

Conversion test for General block uConstant.

Test results				
Time step	1	2	...	7
Mask parameters				
Value	1	-1	...	-2.3
Controller parameters				
K	2147483647	-2147483647	...	-2147483647
Exp. K	2147483647	-2147483648	...	-2147483648

Test settings	
Tolerance K	±1,0000e+00

Test case: Conversion-on-Target test — OK

Conversion-on-Target test for General block uConstant.

Test results				
Time step	1	2	...	7
Mask parameters				
Value	1	-1	...	-2.3
Controller parameters				
K	2147483647	-2147483647	...	-2147483647
Exp. K	2147483647	-2147483648	...	-2147483648

Test settings	
Tolerance K	±1,0000e+00

Test statistics	
Min CPU cycles	1026
Max CPU cycles	1093
Avg CPU cycles	1063

Verification: uConstant FiP32 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Conversion test OK

Conversion test for General block uConstant.

Test results				
Time step	1	2	...	7
Mask parameters				
Value	1	-1	...	-2.3
Controller parameters				
K	2147483647	-2147483647	...	-2147483647
Exp. K	2147483647	-2147483648	...	-2147483648

Test settings	
Tolerance K	±1,0000e+00

Test case: Conversion-on-Target test OK

Conversion-on-Target test for General block uConstant.

Test results				
Time step	1	2	...	7
Mask parameters				
Value	1	-1	...	-2.3
Controller parameters				
K	2147483647	-2147483647	...	-2147483647
Exp. K	2147483647	-2147483648	...	-2147483648

Test settings	
Tolerance K	±1,0000e+00

Test statistics	
Min CPU cycles	457
Max CPU cycles	485
Avg CPU cycles	477

Verification: uConstant FiP32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Conversion test — OK

Conversion test for General block uConstant.

Test results				
Time step	1	2	...	7
Mask parameters				
Value	1	-1	...	-2.3
Controller parameters				
K	2147483647	-2147483647	...	-2147483647
Exp. K	2147483647	-2147483648	...	-2147483648

Test settings	
Tolerance K	±1,0000e+00

Test case: Conversion-on-Target test — OK

Conversion-on-Target test for General block uConstant.

Test results				
Time step	1	2	...	7
Mask parameters				
Value	1	-1	...	-2.3
Controller parameters				
K	2147483647	-2147483647	...	-2147483647
Exp. K	2147483647	-2147483648	...	-2147483648

Test settings	
Tolerance K	±1,0000e+00

Test statistics	
Min CPU cycles	929
Max CPU cycles	1174
Avg CPU cycles	1026

Verification: uConstant FiP32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Conversion test — OK

Conversion test for General block uConstant.

Test results				
Time step	1	2	...	7
Mask parameters				
Value	1	-1	...	-2.3
Controller parameters				
K	2147483647	-2147483647	...	-2147483647
Exp. K	2147483647	-2147483648	...	-2147483648

Test settings	
Tolerance K	±1,0000e+00

Test case: Conversion-on-Target test — OK

Conversion-on-Target test for General block uConstant.

Test results				
Time step	1	2	...	7
Mask parameters				
Value	1	-1	...	-2.3
Controller parameters				
K	2147483647	-2147483647	...	-2147483647
Exp. K	2147483647	-2147483648	...	-2147483648

Test settings	
Tolerance K	±1,0000e+00

Test statistics	
Min CPU cycles	1819
Max CPU cycles	2575
Avg CPU cycles	2263

Verification: uConstant FiP32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Conversion test OK

Conversion test for General block uConstant.

Test results				
Time step	1	2	...	7
Mask parameters				
Value	1	-1	...	-2.3
Controller parameters				
K	2147483647	-2147483647	...	-2147483647
Exp. K	2147483647	-2147483648	...	-2147483648

Test settings	
Tolerance K	±1,0000e+00

Test case: Conversion-on-Target test OK

Conversion-on-Target test for General block uConstant.

Test results				
Time step	1	2	...	7
Mask parameters				
Value	1	-1	...	-2.3
Controller parameters				
K	2147483647	-2147483647	...	-2147483647
Exp. K	2147483647	-2147483648	...	-2147483648

Test settings	
Tolerance K	±1,0000e+00

Test statistics	
Min CPU cycles	729
Max CPU cycles	922
Avg CPU cycles	837

Verification: uConstant FiP32 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Conversion test

OK

Conversion test for General block uConstant.

Test results				
Time step	1	2	...	7
Mask parameters				
Value	1	-1	...	-2.3
Controller parameters				
K	2147483647	-2147483647	...	-2147483647
Exp. K	2147483647	-2147483648	...	-2147483648

Test settings	
Tolerance K	±1,0000e+00

Test case: Conversion-on-Target test

OK

Conversion-on-Target test for General block uConstant.

Test results				
Time step	1	2	...	7
Mask parameters				
Value	1	-1	...	-2.3
Controller parameters				
K	2147483647	-2147483647	...	-2147483647
Exp. K	2147483647	-2147483648	...	-2147483648

Test settings	
Tolerance K	±1,0000e+00

Test statistics	
Min CPU cycles	1155
Max CPU cycles	1629
Avg CPU cycles	1552

Verification: uConstant FiP32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Conversion test — OK

Conversion test for General block uConstant.

Test results				
Time step	1	2	...	7
Mask parameters				
Value	1	-1	...	-2.3
Controller parameters				
K	2147483647	-2147483647	...	-2147483647
Exp. K	2147483647	-2147483648	...	-2147483648

Test settings	
Tolerance K	±1,0000e+00

Test case: Conversion-on-Target test — OK

Conversion-on-Target test for General block uConstant.

Test results				
Time step	1	2	...	7
Mask parameters				
Value	1	-1	...	-2.3
Controller parameters				
K	2147483647	-2147483647	...	-2147483647
Exp. K	2147483647	-2147483648	...	-2147483648

Test settings	
Tolerance K	±1,0000e+00

Test statistics	
Min CPU cycles	667
Max CPU cycles	862
Avg CPU cycles	747

Verification: uConstant FiP32 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Conversion test OK

Conversion test for General block uConstant.

Test results				
Time step	1	2	...	7
Mask parameters				
Value	1	-1	...	-2.3
Controller parameters				
K	2147483647	-2147483647	...	-2147483647
Exp. K	2147483647	-2147483648	...	-2147483648

Test settings	
Tolerance K	±1,0000e+00

Test case: Conversion-on-Target test OK

Conversion-on-Target test for General block uConstant.

Test results				
Time step	1	2	...	7
Mask parameters				
Value	1	-1	...	-2.3
Controller parameters				
K	2147483647	-2147483647	...	-2147483647
Exp. K	2147483647	-2147483648	...	-2147483648

Test settings	
Tolerance K	±1,0000e+00

Test statistics	
Min CPU cycles	801
Max CPU cycles	847
Avg CPU cycles	824

Verification: uConstant Float32 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Conversion test — OK

Conversion test for General block uConstant.

Test results				
Time step	1	2	...	7
Mask parameters				
Value	1	-1	...	-2.3
Controller parameters				
K	1	-1	...	-2.3
Exp. K	1	-1	...	-2.3

Test settings	
Tolerance K	±0,0000e+00

Test case: Conversion-on-Target test — OK

Conversion-on-Target test for General block uConstant.

Test results				
Time step	1	2	...	7
Mask parameters				
Value	1	-1	...	-2.3
Controller parameters				
K	1	-1	...	-2.3
Exp. K	1	-1	...	-2.3

Test settings	
Tolerance K	±5,0000e-08

Test statistics	
Min CPU cycles	1058
Max CPU cycles	1087
Avg CPU cycles	1067

Verification: uConstant Float32 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Conversion test — OK

Conversion test for General block uConstant.

Test results				
Time step	1	2	...	7
Mask parameters				
Value	1	-1	...	-2.3
Controller parameters				
K	1	-1	...	-2.3
Exp. K	1	-1	...	-2.3

Test settings	
Tolerance K	±0,0000e+00

Test case: Conversion-on-Target test — OK

Conversion-on-Target test for General block uConstant.

Test results				
Time step	1	2	...	7
Mask parameters				
Value	1	-1	...	-2.3
Controller parameters				
K	1	-1	...	-2.3
Exp. K	1	-1	...	-2.3

Test settings	
Tolerance K	±5,0000e-08

Test statistics	
Min CPU cycles	519
Max CPU cycles	535
Avg CPU cycles	532

Verification: uConstant Float32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Conversion test OK

Conversion test for General block uConstant.

Test results				
Time step	1	2	...	7
Mask parameters				
Value	1	-1	...	-2.3
Controller parameters				
K	1	-1	...	-2.3
Exp. K	1	-1	...	-2.3

Test settings	
Tolerance K	±0,0000e+00

Test case: Conversion-on-Target test OK

Conversion-on-Target test for General block uConstant.

Test results				
Time step	1	2	...	7
Mask parameters				
Value	1	-1	...	-2.3
Controller parameters				
K	1	-1	...	-2.3
Exp. K	1	-1	...	-2.3

Test settings	
Tolerance K	±5,0000e-08

Test statistics	
Min CPU cycles	741
Max CPU cycles	741
Avg CPU cycles	741

Verification: uConstant Float32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Conversion test — OK

Conversion test for General block uConstant.

Test results				
Time step	1	2	...	7
Mask parameters				
Value	1	-1	...	-2.3
Controller parameters				
K	1	-1	...	-2.3
Exp. K	1	-1	...	-2.3

Test settings	
Tolerance K	±0,0000e+00

Test case: Conversion-on-Target test — OK

Conversion-on-Target test for General block uConstant.

Test results				
Time step	1	2	...	7
Mask parameters				
Value	1	-1	...	-2.3
Controller parameters				
K	1	-1	...	-2.3
Exp. K	1	-1	...	-2.3

Test settings	
Tolerance K	±5,0000e-08

Test statistics	
Min CPU cycles	921
Max CPU cycles	968
Avg CPU cycles	951

Verification: uConstant Float32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Conversion test — OK

Conversion test for General block uConstant.

Test results				
Time step	1	2	...	7
Mask parameters				
Value	1	-1	...	-2.3
Controller parameters				
K	1	-1	...	-2.3
Exp. K	1	-1	...	-2.3

Test settings	
Tolerance K	±0,0000e+00

Test case: Conversion-on-Target test — OK

Conversion-on-Target test for General block uConstant.

Test results				
Time step	1	2	...	7
Mask parameters				
Value	1	-1	...	-2.3
Controller parameters				
K	1	-1	...	-2.3
Exp. K	1	-1	...	-2.3

Test settings	
Tolerance K	±5,0000e-08

Test statistics	
Min CPU cycles	387
Max CPU cycles	390
Avg CPU cycles	388

Verification: uConstant Float32 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Conversion test — OK

Conversion test for General block uConstant.

Test results				
Time step	1	2	...	7
Mask parameters				
Value	1	-1	...	-2.3
Controller parameters				
K	1	-1	...	-2.3
Exp. K	1	-1	...	-2.3

Test settings	
Tolerance K	±0,0000e+00

Test case: Conversion-on-Target test — OK

Conversion-on-Target test for General block uConstant.

Test results				
Time step	1	2	...	7
Mask parameters				
Value	1	-1	...	-2.3
Controller parameters				
K	1	-1	...	-2.3
Exp. K	1	-1	...	-2.3

Test settings	
Tolerance K	±5,0000e-08

Test statistics	
Min CPU cycles	787
Max CPU cycles	1096
Avg CPU cycles	1051

Verification: uConstant Float32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Conversion test — OK

Conversion test for General block uConstant.

Test results				
Time step	1	2	...	7
Mask parameters				
Value	1	-1	...	-2.3
Controller parameters				
K	1	-1	...	-2.3
Exp. K	1	-1	...	-2.3

Test settings	
Tolerance K	±0,0000e+00

Test case: Conversion-on-Target test — OK

Conversion-on-Target test for General block uConstant.

Test results				
Time step	1	2	...	7
Mask parameters				
Value	1	-1	...	-2.3
Controller parameters				
K	1	-1	...	-2.3
Exp. K	1	-1	...	-2.3

Test settings	
Tolerance K	±5,0000e-08

Test statistics	
Min CPU cycles	579
Max CPU cycles	672
Avg CPU cycles	593

Verification: uConstant Float32 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Conversion test — OK

Conversion test for General block uConstant.

Test results				
Time step	1	2	...	7
Mask parameters				
Value	1	-1	...	-2.3
Controller parameters				
K	1	-1	...	-2.3
Exp. K	1	-1	...	-2.3

Test settings	
Tolerance K	±0,0000e+00

Test case: Conversion-on-Target test — OK

Conversion-on-Target test for General block uConstant.

Test results				
Time step	1	2	...	7
Mask parameters				
Value	1	-1	...	-2.3
Controller parameters				
K	1	-1	...	-2.3
Exp. K	1	-1	...	-2.3

Test settings	
Tolerance K	±5,0000e-08

Test statistics	
Min CPU cycles	817
Max CPU cycles	826
Avg CPU cycles	820

Block: uGain



Amplification of input by gain factor with output wrapping.

Inports	
In	Input

Outports	
Out	Amplified input

Mask Parameters		
Name	**ID**	**Description**
Gain	1	Gain factor in floating point format

Implementations:

FiP8 8 Bit Fixed Point Implementation
FiP16 16 Bit Fixed Point Implementation
FiP32 32 Bit Fixed Point Implementation
Float32 32 Bit Floating Point Implementation
Float64 64 Bit Floating Point Implementation

Implementation: FiP8

8 Bit Fixed Point Implementation

Inports Data Type	
In	int8

Outports Data Type	
Out	int8

Implementation: FiP16

16 Bit Fixed Point Implementation

Inports Data Type	
In	int16

Outports Data Type	
Out	int16

Implementation: FiP32

32 Bit Fixed Point Implementation

Inports Data Type	
In	int32

Outports Data Type	
Out	int32

Implementation: Float32

32 Bit Floating Point Implementation

Inports Data Type	
In	float32

Outports Data Type	
Out	float32

Implementation: Float64

64 Bit Floating Point Implementation

Inports Data Type	
In	float64

Outports Data Type	
Out	float64

Verification: uGain FiP16 CPU TMS320F28335

Date of Test 2026-06-19

Target controller TMS320F28335

Test case: Inport test OK

Inport test for General block uGain.

Test results						
Time step	1	2	3	4	...	107
CPU cycles	59	59	59	59	...	59
Inputs						
In (DSP)	-32768	-32150	-31531	-30913	...	32767
In	-1	-0.981	-0.962	-0.943	...	1
Parameters						
Gain	2.1					
Outputs						
Out	-0.1	-0.06	-0.021	0.019	...	0.1
Exp. Out	-0.1	-0.06	-0.021	0.019	...	0.1
Out (DSP)	-3276	-1979	-679	619	...	3273
Exp. Out (DSP)	-3277	-1978	-680	618	...	3277

Test settings	
Tolerance Out	±1,2207e-04 (±4 LSB)

Test statistics	
Min CPU cycles	59
Max CPU cycles	59
Avg CPU cycles	59

Test case: Parameter test OK

Parameter test for General block uGain.

Test results						
Time step	1	2	3	4	...	107
CPU cycles	59	59	59	59	...	59
Inputs						
In (DSP)	13107					
In	0.4					
Parameters						
Gain	-3.7	-3.63	-3.56	-3.491	...	3.7
Outputs						
Out	0.52	0.548	0.576	0.604	...	-0.52
Exp. Out	0.52	0.548	0.576	0.604	...	-0.52
Out (DSP)	17040	17954	18869	19784	...	-17041
Exp. Out (DSP)	17039	17954	18869	19784	...	-17039

Test settings	
Tolerance Out	±9,1553e-05 (±3 LSB)

Test statistics	
Min CPU cycles	59
Max CPU cycles	59
Avg CPU cycles	59

Test case: Conversion test **OK**

Conversion test for General block uGain.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Gain	-10	-9.444	-8.889	-8.333	...	10
Controller parameters						
V	-20480	-19342	-18204	-17067	...	20480
sfr	11	11	11	11	...	11
Exp. V	-20480	-19342	-18204	-17067	...	20480
Exp. sfr	11	11	11	11	...	11

Test settings	
Tolerance V	±0,0000e+00
Tolerance sfr	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block uGain.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Gain	-10	-9.444	-8.889	-8.333	...	10
Controller parameters						
V	-20480	-19342	-18204	-17066	...	20480
sfr	11	11	11	11	...	11
Exp. V	-20480	-19342	-18204	-17067	...	20480
Exp. sfr	11	11	11	11	...	11

Test settings	
Tolerance V	±1,0000e+00
Tolerance sfr	±0,0000e+00

Test statistics	
Min CPU cycles	1502
Max CPU cycles	3610
Avg CPU cycles	2862

Verification: uGain FiP16 CPU TM4C123GH6

Date of Test 2026-06-19

Target controller TM4C123GH6

Test case: Inport test OK

Inport test for General block uGain.

Test results						
Time step	1	2	3	4	...	107
CPU cycles	27	27	27	27	...	27
Inputs						
In (DSP)	-32768	-32150	-31531	-30913	...	32767
In	-1	-0.981	-0.962	-0.943	...	1
Parameters						
Gain	2.1					
Outputs						
Out	-0.1	-0.06	-0.021	0.019	...	0.1
Exp. Out	-0.1	-0.06	-0.021	0.019	...	0.1
Out (DSP)	-3276	-1979	-679	619	...	3273
Exp. Out (DSP)	-3277	-1978	-680	618	...	3277

Test settings	
Tolerance Out	±1,2207e-04 (±4 LSB)

Test statistics	
Min CPU cycles	27
Max CPU cycles	27
Avg CPU cycles	27

Test case: Parameter test OK

Parameter test for General block uGain.

Test results						
Time step	1	2	3	4	...	107
CPU cycles	27	27	27	27	...	27
Inputs						
In (DSP)	13107					
In	0.4					
Parameters						
Gain	-3.7	-3.63	-3.56	-3.491	...	3.7
Outputs						
Out	0.52	0.548	0.576	0.604	...	-0.52
Exp. Out	0.52	0.548	0.576	0.604	...	-0.52
Out (DSP)	17040	17954	18869	19784	...	-17041
Exp. Out (DSP)	17039	17954	18869	19784	...	-17039

Test settings	
Tolerance Out	±9,1553e-05 (±3 LSB)

Test statistics	
Min CPU cycles	27
Max CPU cycles	27
Avg CPU cycles	27

Test case: Conversion test **OK**

Conversion test for General block uGain.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Gain	-10	-9.444	-8.889	-8.333	...	10
Controller parameters						
V	-20480	-19342	-18204	-17067	...	20480
sfr	11	11	11	11	...	11
Exp. V	-20480	-19342	-18204	-17067	...	20480
Exp. sfr	11	11	11	11	...	11

Test settings	
Tolerance V	±0,0000e+00
Tolerance sfr	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block uGain.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Gain	-10	-9.444	-8.889	-8.333	...	10
Controller parameters						
V	-20480	-19342	-18204	-17066	...	20480
sfr	11	11	11	11	...	11
Exp. V	-20480	-19342	-18204	-17067	...	20480
Exp. sfr	11	11	11	11	...	11

Test settings	
Tolerance V	±1,0000e+00
Tolerance sfr	±0,0000e+00

Test statistics	
Min CPU cycles	771
Max CPU cycles	2031
Avg CPU cycles	1585

Verification: uGain FiP16 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for General block uGain.

Test results						
Time step	1	2	3	4	...	107
CPU cycles	57	57	57	57	...	57
Inputs						
In (DSP)	-32768	-32150	-31531	-30913	...	32767
In	-1	-0.981	-0.962	-0.943	...	1
Parameters						
Gain	2.1					
Outputs						
Out	-0.1	-0.06	-0.021	0.019	...	0.1
Exp. Out	-0.1	-0.06	-0.021	0.019	...	0.1
Out (DSP)	-3276	-1979	-679	619	...	3273
Exp. Out (DSP)	-3277	-1978	-680	618	...	3277

Test settings	
Tolerance Out	±1,2207e-04 (±4 LSB)

Test statistics	
Min CPU cycles	57
Max CPU cycles	57
Avg CPU cycles	57

Test case: Parameter test OK

Parameter test for General block uGain.

Test results						
Time step	1	2	3	4	...	107
CPU cycles	57	57	57	57	...	57
Inputs						
In (DSP)	13107					
In	0.4					
Parameters						
Gain	-3.7	-3.63	-3.56	-3.491	...	3.7
Outputs						
Out	0.52	0.548	0.576	0.604	...	-0.52
Exp. Out	0.52	0.548	0.576	0.604	...	-0.52
Out (DSP)	17040	17954	18869	19784	...	-17041
Exp. Out (DSP)	17039	17954	18869	19784	...	-17039

Test settings	
Tolerance Out	±9,1553e-05 (±3 LSB)

Test statistics	
Min CPU cycles	57
Max CPU cycles	57
Avg CPU cycles	57

Test case: Conversion test **OK**

Conversion test for General block uGain.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Gain	-10	-9.444	-8.889	-8.333	...	10
Controller parameters						
V	-20480	-19342	-18204	-17067	...	20480
sfr	11	11	11	11	...	11
Exp. V	-20480	-19342	-18204	-17067	...	20480
Exp. sfr	11	11	11	11	...	11

Test settings	
Tolerance V	±0,0000e+00
Tolerance sfr	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block uGain.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Gain	-10	-9.444	-8.889	-8.333	...	10
Controller parameters						
V	-20480	-19342	-18204	-17066	...	20480
sfr	11	11	11	11	...	11
Exp. V	-20480	-19342	-18204	-17067	...	20480
Exp. sfr	11	11	11	11	...	11

Test settings	
Tolerance V	±1,0000e+00
Tolerance sfr	±0,0000e+00

Test statistics	
Min CPU cycles	963
Max CPU cycles	1486
Avg CPU cycles	1301

Verification: uGain FiP16 CPU STM32F072RB

Date of Test 2026-06-19

Target controller STM32F072RB

Test case: Inport test OK

Inport test for General block uGain.

Test results						
Time step	1	2	3	4	...	107
CPU cycles	54	54	54	54	...	54
Inputs						
In (DSP)	-32768	-32150	-31531	-30913	...	32767
In	-1	-0.981	-0.962	-0.943	...	1
Parameters						
Gain	2.1					
Outputs						
Out	-0.1	-0.06	-0.021	0.019	...	0.1
Exp. Out	-0.1	-0.06	-0.021	0.019	...	0.1
Out (DSP)	-3276	-1979	-679	619	...	3273
Exp. Out (DSP)	-3277	-1978	-680	618	...	3277

Test settings	
Tolerance Out	±1,2207e-04 (±4 LSB)

Test statistics	
Min CPU cycles	54
Max CPU cycles	114
Avg CPU cycles	54

Test case: Parameter test OK

Parameter test for General block uGain.

Test results						
Time step	1	2	3	4	...	107
CPU cycles	54	54	54	54	...	54
Inputs						
In (DSP)	13107					
In	0.4					
Parameters						
Gain	-3.7	-3.63	-3.56	-3.491	...	3.7
Outputs						
Out	0.52	0.548	0.576	0.604	...	-0.52
Exp. Out	0.52	0.548	0.576	0.604	...	-0.52
Out (DSP)	17040	17954	18869	19784	...	-17041
Exp. Out (DSP)	17039	17954	18869	19784	...	-17039

Test settings	
Tolerance Out	±9,1553e-05 (±3 LSB)

Test statistics	
Min CPU cycles	54
Max CPU cycles	54
Avg CPU cycles	54

Test case: Conversion test **OK**

Conversion test for General block uGain.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Gain	-10	-9.444	-8.889	-8.333	...	10
Controller parameters						
V	-20480	-19342	-18204	-17067	...	20480
sfr	11	11	11	11	...	11
Exp. V	-20480	-19342	-18204	-17067	...	20480
Exp. sfr	11	11	11	11	...	11

Test settings	
Tolerance V	±0,0000e+00
Tolerance sfr	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block uGain.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Gain	-10	-9.444	-8.889	-8.333	...	10
Controller parameters						
V	-20480	-19342	-18204	-17066	...	20480
sfr	11	11	11	11	...	11
Exp. V	-20480	-19342	-18204	-17067	...	20480
Exp. sfr	11	11	11	11	...	11

Test settings	
Tolerance V	±1,0000e+00
Tolerance sfr	±0,0000e+00

Test statistics	
Min CPU cycles	1708
Max CPU cycles	4649
Avg CPU cycles	3707

Verification: uGain FiP16 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for General block uGain.

Test results						
Time step	1	2	3	4	...	107
CPU cycles	35	35	35	35	...	35
Inputs						
In (DSP)	-32768	-32150	-31531	-30913	...	32767
In	-1	-0.981	-0.962	-0.943	...	1
Parameters						
Gain	2.1					
Outputs						
Out	-0.1	-0.06	-0.021	0.019	...	0.1
Exp. Out	-0.1	-0.06	-0.021	0.019	...	0.1
Out (DSP)	-3276	-1979	-679	619	...	3273
Exp. Out (DSP)	-3277	-1978	-680	618	...	3277

Test settings	
Tolerance Out	±1,2207e-04 (±4 LSB)

Test statistics	
Min CPU cycles	35
Max CPU cycles	35
Avg CPU cycles	35

Test case: Parameter test OK

Parameter test for General block uGain.

Test results						
Time step	1	2	3	4	...	107
CPU cycles	35	35	35	35	...	35
Inputs						
In (DSP)	13107					
In	0.4					
Parameters						
Gain	-3.7	-3.63	-3.56	-3.491	...	3.7
Outputs						
Out	0.52	0.548	0.576	0.604	...	-0.52
Exp. Out	0.52	0.548	0.576	0.604	...	-0.52
Out (DSP)	17040	17954	18869	19784	...	-17041
Exp. Out (DSP)	17039	17954	18869	19784	...	-17039

Test settings	
Tolerance Out	±9,1553e-05 (±3 LSB)

Test statistics	
Min CPU cycles	35
Max CPU cycles	35
Avg CPU cycles	35

Test case: Conversion test **OK**

Conversion test for General block uGain.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Gain	-10	-9.444	-8.889	-8.333	...	10
Controller parameters						
V	-20480	-19342	-18204	-17067	...	20480
sfr	11	11	11	11	...	11
Exp. V	-20480	-19342	-18204	-17067	...	20480
Exp. sfr	11	11	11	11	...	11

Test settings	
Tolerance V	±0,0000e+00
Tolerance sfr	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block uGain.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Gain	-10	-9.444	-8.889	-8.333	...	10
Controller parameters						
V	-20480	-19342	-18204	-17066	...	20480
sfr	11	11	11	11	...	11
Exp. V	-20480	-19342	-18204	-17067	...	20480
Exp. sfr	11	11	11	11	...	11

Test settings	
Tolerance V	±1,0000e+00
Tolerance sfr	±0,0000e+00

Test statistics	
Min CPU cycles	815
Max CPU cycles	1984
Avg CPU cycles	1588

Verification: uGain FiP16 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for General block uGain.

Test results						
Time step	1	2	3	4	...	107
CPU cycles	54	54	54	54	...	54
Inputs						
In (DSP)	-32768	-32150	-31531	-30913	...	32767
In	-1	-0.981	-0.962	-0.943	...	1
Parameters						
Gain	2.1					
Outputs						
Out	-0.1	-0.06	-0.021	0.019	...	0.1
Exp. Out	-0.1	-0.06	-0.021	0.019	...	0.1
Out (DSP)	-3276	-1979	-679	619	...	3273
Exp. Out (DSP)	-3277	-1978	-680	618	...	3277

Test settings	
Tolerance Out	±1,2207e-04 (±4 LSB)

Test statistics	
Min CPU cycles	54
Max CPU cycles	54
Avg CPU cycles	54

Test case: Parameter test OK

Parameter test for General block uGain.

Test results						
Time step	1	2	3	4	...	107
CPU cycles	54	54	54	54	...	54
Inputs						
In (DSP)	13107					
In	0.4					
Parameters						
Gain	-3.7	-3.63	-3.56	-3.491	...	3.7
Outputs						
Out	0.52	0.548	0.576	0.604	...	-0.52
Exp. Out	0.52	0.548	0.576	0.604	...	-0.52
Out (DSP)	17040	17954	18869	19784	...	-17041
Exp. Out (DSP)	17039	17954	18869	19784	...	-17039

Test settings	
Tolerance Out	±9,1553e-05 (±3 LSB)

Test statistics	
Min CPU cycles	54
Max CPU cycles	54
Avg CPU cycles	54

Test case: Conversion test **OK**

Conversion test for General block uGain.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Gain	-10	-9.444	-8.889	-8.333	...	10
Controller parameters						
V	-20480	-19342	-18204	-17067	...	20480
sfr	11	11	11	11	...	11
Exp. V	-20480	-19342	-18204	-17067	...	20480
Exp. sfr	11	11	11	11	...	11

Test settings	
Tolerance V	±0,0000e+00
Tolerance sfr	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block uGain.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Gain	-10	-9.444	-8.889	-8.333	...	10
Controller parameters						
V	-20480	-19342	-18204	-17066	...	20480
sfr	11	11	11	11	...	11
Exp. V	-20480	-19342	-18204	-17067	...	20480
Exp. sfr	11	11	11	11	...	11

Test settings	
Tolerance V	±1,0000e+00
Tolerance sfr	±0,0000e+00

Test statistics	
Min CPU cycles	2593
Max CPU cycles	10879
Avg CPU cycles	8317

Verification: uGain FiP16 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for General block uGain.

Test results						
Time step	1	2	3	4	...	107
CPU cycles	57	57	57	57	...	57
Inputs						
In (DSP)	-32768	-32150	-31531	-30913	...	32767
In	-1	-0.981	-0.962	-0.943	...	1
Parameters						
Gain	2.1					
Outputs						
Out	-0.1	-0.06	-0.021	0.019	...	0.1
Exp. Out	-0.1	-0.06	-0.021	0.019	...	0.1
Out (DSP)	-3276	-1979	-679	619	...	3273
Exp. Out (DSP)	-3277	-1978	-680	618	...	3277

Test settings	
Tolerance Out	±1,2207e-04 (±4 LSB)

Test statistics	
Min CPU cycles	57
Max CPU cycles	57
Avg CPU cycles	57

Test case: Parameter test OK

Parameter test for General block uGain.

Test results						
Time step	1	2	3	4	...	107
CPU cycles	57	57	57	57	...	57
Inputs						
In (DSP)	13107					
In	0.4					
Parameters						
Gain	-3.7	-3.63	-3.56	-3.491	...	3.7
Outputs						
Out	0.52	0.548	0.576	0.604	...	-0.52
Exp. Out	0.52	0.548	0.576	0.604	...	-0.52
Out (DSP)	17040	17954	18869	19784	...	-17041
Exp. Out (DSP)	17039	17954	18869	19784	...	-17039

Test settings	
Tolerance Out	±9,1553e-05 (±3 LSB)

Test statistics	
Min CPU cycles	57
Max CPU cycles	57
Avg CPU cycles	57

Test case: Conversion test **OK**

Conversion test for General block uGain.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Gain	-10	-9.444	-8.889	-8.333	...	10
Controller parameters						
V	-20480	-19342	-18204	-17067	...	20480
sfr	11	11	11	11	...	11
Exp. V	-20480	-19342	-18204	-17067	...	20480
Exp. sfr	11	11	11	11	...	11

Test settings	
Tolerance V	±0,0000e+00
Tolerance sfr	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block uGain.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Gain	-10	-9.444	-8.889	-8.333	...	10
Controller parameters						
V	-20480	-19342	-18204	-17066	...	20480
sfr	11	11	11	11	...	11
Exp. V	-20480	-19342	-18204	-17067	...	20480
Exp. sfr	11	11	11	11	...	11

Test settings	
Tolerance V	±1,0000e+00
Tolerance sfr	±0,0000e+00

Test statistics	
Min CPU cycles	633
Max CPU cycles	1274
Avg CPU cycles	947

Verification: uGain FiP16 CPU TMS320F28379D

Date of Test 2026-06-22

Target controller TMS320F28379D

Test case: Inport test OK

Inport test for General block uGain.

Test results						
Time step	1	2	3	4	...	107
CPU cycles	39	39	39	39	...	39
Inputs						
In (DSP)	-32768	-32150	-31531	-30913	...	32767
In	-1	-0.981	-0.962	-0.943	...	1
Parameters						
Gain	2.1					
Outputs						
Out	-0.1	-0.06	-0.021	0.019	...	0.1
Exp. Out	-0.1	-0.06	-0.021	0.019	...	0.1
Out (DSP)	-3276	-1979	-679	619	...	3273
Exp. Out (DSP)	-3277	-1978	-680	618	...	3277

Test settings	
Tolerance Out	±1,2207e-04 (±4 LSB)

Test statistics	
Min CPU cycles	39
Max CPU cycles	39
Avg CPU cycles	39

Test case: Parameter test OK

Parameter test for General block uGain.

Test results						
Time step	1	2	3	4	...	107
CPU cycles	39	39	39	39	...	39
Inputs						
In (DSP)	13107					
In	0.4					
Parameters						
Gain	-3.7	-3.63	-3.56	-3.491	...	3.7
Outputs						
Out	0.52	0.548	0.576	0.604	...	-0.52
Exp. Out	0.52	0.548	0.576	0.604	...	-0.52
Out (DSP)	17040	17954	18869	19784	...	-17041
Exp. Out (DSP)	17039	17954	18869	19784	...	-17039

Test settings	
Tolerance Out	±9,1553e-05 (±3 LSB)

Test statistics	
Min CPU cycles	39
Max CPU cycles	39
Avg CPU cycles	39

Test case: Conversion test **OK**

Conversion test for General block uGain.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Gain	-10	-9.444	-8.889	-8.333	...	10
Controller parameters						
V	-20480	-19342	-18204	-17067	...	20480
sfr	11	11	11	11	...	11
Exp. V	-20480	-19342	-18204	-17067	...	20480
Exp. sfr	11	11	11	11	...	11

Test settings	
Tolerance V	±0,0000e+00
Tolerance sfr	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block uGain.

Test results						
Time step	1	2	3	4	...	37
Mask parameters						
Gain	-10	-9.444	-8.889	-8.333	...	10
Controller parameters						
V	-20480	-19342	-18204	-17066	...	20480
sfr	11	11	11	11	...	11
Exp. V	-20480	-19342	-18204	-17067	...	20480
Exp. sfr	11	11	11	11	...	11

Test settings	
Tolerance V	±1,0000e+00
Tolerance sfr	±0,0000e+00

Test statistics	
Min CPU cycles	1117
Max CPU cycles	2821
Avg CPU cycles	2226

Verification: uGain FiP32 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for General block uGain.

Test results				
Time step	1	2	...	107
CPU cycles	62	62	...	62
Inputs				
In (DSP)	-2147483648	-2106965089	...	2147483647
In	-1	-0.981	...	1
Parameters				
Gain	2.1			
Outputs				
Out	-0.1	-0.06	...	0.1
Exp. Out	-0.1	-0.06	...	0.1
Out (DSP)	-214748364	-129659391	...	214748361
Exp. Out (DSP)	-214748365	-129659390	...	214748365

Test settings	
Tolerance Out	±2,3283e-09 (±5 LSB)

Test statistics	
Min CPU cycles	62
Max CPU cycles	62
Avg CPU cycles	62

Test case: Parameter test OK

Parameter test for General block uGain.

Test results				
Time step	1	2	...	107
CPU cycles	62	62	...	62
Inputs				
In (DSP)	858993459			
In	0.4			
Parameters				
Gain	-3.7	-3.63	...	3.7
Outputs				
Out	0.52	0.548	...	-0.52
Exp. Out	0.52	0.548	...	-0.52
Out (DSP)	1116691498	1176658965	...	-1116691499
Exp. Out (DSP)	1116691497	1176658965	...	-1116691497

Test settings	
Tolerance Out	±1,3970e-09 (±3 LSB)

Test statistics	
Min CPU cycles	62
Max CPU cycles	62
Avg CPU cycles	62

Test case: Conversion test **OK**

Conversion test for General block uGain.

Test results				
Time step	1	2	...	37
Mask parameters				
Gain	-10	-9.444	...	10
Controller parameters				
V	-1342177280	-1267611876	...	1342177280
sfr	27	27	...	27
Exp. V	-1342177280	-1267611876	...	1342177280
Exp. sfr	27	27	...	27

Test settings	
Tolerance V	±0,0000e+00
Tolerance sfr	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block uGain.

Test results				
Time step	1	2	...	37
Mask parameters				
Gain	-10	-9.444	...	10
Controller parameters				
V	-1342177280	-1267611904	...	1342177280
sfr	27	27	...	27
Exp. V	-1342177280	-1267611876	...	1342177280
Exp. sfr	27	27	...	27

Test settings	
Tolerance V	±7,0000e+01
Tolerance sfr	±0,0000e+00

Test statistics	
Min CPU cycles	1652
Max CPU cycles	3809
Avg CPU cycles	3056

Verification: uGain FiP32 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for General block uGain.

Test results				
Time step	1	2	...	107
CPU cycles	59	59	...	59
Inputs				
In (DSP)	-2147483648	-2106965089	...	2147483647
In	-1	-0.981	...	1
Parameters				
Gain	2.1			
Outputs				
Out	-0.1	-0.06	...	0.1
Exp. Out	-0.1	-0.06	...	0.1
Out (DSP)	-214748364	-129659391	...	214748361
Exp. Out (DSP)	-214748365	-129659390	...	214748365

Test settings	
Tolerance Out	±2,3283e-09 (±5 LSB)

Test statistics	
Min CPU cycles	59
Max CPU cycles	59
Avg CPU cycles	59

Test case: Parameter test OK

Parameter test for General block uGain.

Test results				
Time step	1	2	...	107
CPU cycles	59	59	...	59
Inputs				
In (DSP)	858993459			
In	0.4			
Parameters				
Gain	-3.7	-3.63	...	3.7
Outputs				
Out	0.52	0.548	...	-0.52
Exp. Out	0.52	0.548	...	-0.52
Out (DSP)	1116691498	1176658965	...	-1116691499
Exp. Out (DSP)	1116691497	1176658965	...	-1116691497

Test settings	
Tolerance Out	±1,3970e-09 (±3 LSB)

Test statistics	
Min CPU cycles	59
Max CPU cycles	59
Avg CPU cycles	59

Test case: Conversion test **OK**

Conversion test for General block uGain.

Test results				
Time step	1	2	...	37
Mask parameters				
Gain	-10	-9.444	...	10
Controller parameters				
V	-1342177280	-1267611876	...	1342177280
sfr	27	27	...	27
Exp. V	-1342177280	-1267611876	...	1342177280
Exp. sfr	27	27	...	27

Test settings	
Tolerance V	±0,0000e+00
Tolerance sfr	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block uGain.

Test results				
Time step	1	2	...	37
Mask parameters				
Gain	-10	-9.444	...	10
Controller parameters				
V	-1342177280	-1267611904	...	1342177280
sfr	27	27	...	27
Exp. V	-1342177280	-1267611876	...	1342177280
Exp. sfr	27	27	...	27

Test settings	
Tolerance V	±7,0000e+01
Tolerance sfr	±0,0000e+00

Test statistics	
Min CPU cycles	725
Max CPU cycles	1629
Avg CPU cycles	1322

Verification: uGain FiP32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for General block uGain.

Test results				
Time step	1	2	...	107
CPU cycles	77	77	...	77
Inputs				
In (DSP)	-2147483648	-2106965089	...	2147483647
In	-1	-0.981	...	1
Parameters				
Gain	2.1			
Outputs				
Out	-0.1	-0.06	...	0.1
Exp. Out	-0.1	-0.06	...	0.1
Out (DSP)	-214748364	-129659391	...	214748361
Exp. Out (DSP)	-214748365	-129659390	...	214748365

Test settings	
Tolerance Out	±2,3283e-09 (±5 LSB)

Test statistics	
Min CPU cycles	77
Max CPU cycles	77
Avg CPU cycles	77

Test case: Parameter test OK

Parameter test for General block uGain.

Test results				
Time step	1	2	...	107
CPU cycles	77	77	...	77
Inputs				
In (DSP)	858993459			
In	0.4			
Parameters				
Gain	-3.7	-3.63	...	3.7
Outputs				
Out	0.52	0.548	...	-0.52
Exp. Out	0.52	0.548	...	-0.52
Out (DSP)	1116691498	1176658965	...	-1116691499
Exp. Out (DSP)	1116691497	1176658965	...	-1116691497

Test settings	
Tolerance Out	±1,3970e-09 (±3 LSB)

Test statistics	
Min CPU cycles	77
Max CPU cycles	77
Avg CPU cycles	77

Test case: Conversion test **OK**

Conversion test for General block uGain.

Test results				
Time step	1	2	...	37
Mask parameters				
Gain	-10	-9.444	...	10
Controller parameters				
V	-1342177280	-1267611876	...	1342177280
sfr	27	27	...	27
Exp. V	-1342177280	-1267611876	...	1342177280
Exp. sfr	27	27	...	27

Test settings	
Tolerance V	±0,0000e+00
Tolerance sfr	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block uGain.

Test results				
Time step	1	2	...	37
Mask parameters				
Gain	-10	-9.444	...	10
Controller parameters				
V	-1342177280	-1267611904	...	1342177280
sfr	27	27	...	27
Exp. V	-1342177280	-1267611876	...	1342177280
Exp. sfr	27	27	...	27

Test settings	
Tolerance V	±7,0000e+01
Tolerance sfr	±0,0000e+00

Test statistics	
Min CPU cycles	1302
Max CPU cycles	1870
Avg CPU cycles	1679

Verification: uGain FiP32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for General block uGain.

Test results				
Time step	1	2	...	107
CPU cycles	142	142	...	142
Inputs				
In (DSP)	-2147483648	-2106965089	...	2147483647
In	-1	-0.981	...	1
Parameters				
Gain	2.1			
Outputs				
Out	-0.1	-0.06	...	0.1
Exp. Out	-0.1	-0.06	...	0.1
Out (DSP)	-214748364	-129659391	...	214748361
Exp. Out (DSP)	-214748365	-129659390	...	214748365

Test settings	
Tolerance Out	±2,3283e-09 (±5 LSB)

Test statistics	
Min CPU cycles	142
Max CPU cycles	142
Avg CPU cycles	142

Test case: Parameter test OK

Parameter test for General block uGain.

Test results				
Time step	1	2	...	107
CPU cycles	142	142	...	142
Inputs				
In (DSP)	858993459			
In	0.4			
Parameters				
Gain	-3.7	-3.63	...	3.7
Outputs				
Out	0.52	0.548	...	-0.52
Exp. Out	0.52	0.548	...	-0.52
Out (DSP)	1116691498	1176658965	...	-1116691499
Exp. Out (DSP)	1116691497	1176658965	...	-1116691497

Test settings	
Tolerance Out	±1,3970e-09 (±3 LSB)

Test statistics	
Min CPU cycles	142
Max CPU cycles	142
Avg CPU cycles	142

Test case: Conversion test **OK**

Conversion test for General block uGain.

Test results				
Time step	1	2	...	37
Mask parameters				
Gain	-10	-9.444	...	10
Controller parameters				
V	-1342177280	-1267611876	...	1342177280
sfr	27	27	...	27
Exp. V	-1342177280	-1267611876	...	1342177280
Exp. sfr	27	27	...	27

Test settings	
Tolerance V	±0,0000e+00
Tolerance sfr	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block uGain.

Test results				
Time step	1	2	...	37
Mask parameters				
Gain	-10	-9.444	...	10
Controller parameters				
V	-1342177280	-1267611904	...	1342177280
sfr	27	27	...	27
Exp. V	-1342177280	-1267611876	...	1342177280
Exp. sfr	27	27	...	27

Test settings	
Tolerance V	±7,0000e+01
Tolerance sfr	±0,0000e+00

Test statistics	
Min CPU cycles	2741
Max CPU cycles	5947
Avg CPU cycles	4977

Verification: uGain FiP32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for General block uGain.

Test results				
Time step	1	2	...	107
CPU cycles	43	43	...	43
Inputs				
In (DSP)	-2147483648	-2106965089	...	2147483647
In	-1	-0.981	...	1
Parameters				
Gain	2.1			
Outputs				
Out	-0.1	-0.06	...	0.1
Exp. Out	-0.1	-0.06	...	0.1
Out (DSP)	-214748364	-129659391	...	214748361
Exp. Out (DSP)	-214748365	-129659390	...	214748365

Test settings	
Tolerance Out	±2,3283e-09 (±5 LSB)

Test statistics	
Min CPU cycles	43
Max CPU cycles	43
Avg CPU cycles	43

Test case: Parameter test OK

Parameter test for General block uGain.

Test results				
Time step	1	2	...	107
CPU cycles	43	43	...	43
Inputs				
In (DSP)	858993459			
In	0.4			
Parameters				
Gain	-3.7	-3.63	...	3.7
Outputs				
Out	0.52	0.548	...	-0.52
Exp. Out	0.52	0.548	...	-0.52
Out (DSP)	1116691498	1176658965	...	-1116691499
Exp. Out (DSP)	1116691497	1176658965	...	-1116691497

Test settings	
Tolerance Out	±1,3970e-09 (±3 LSB)

Test statistics	
Min CPU cycles	43
Max CPU cycles	43
Avg CPU cycles	43

Test case: Conversion test **OK**

Conversion test for General block uGain.

Test results				
Time step	1	2	...	37
Mask parameters				
Gain	-10	-9.444	...	10
Controller parameters				
V	-1342177280	-1267611876	...	1342177280
sfr	27	27	...	27
Exp. V	-1342177280	-1267611876	...	1342177280
Exp. sfr	27	27	...	27

Test settings	
Tolerance V	±0,0000e+00
Tolerance sfr	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block uGain.

Test results				
Time step	1	2	...	37
Mask parameters				
Gain	-10	-9.444	...	10
Controller parameters				
V	-1342177280	-1267611904	...	1342177280
sfr	27	27	...	27
Exp. V	-1342177280	-1267611876	...	1342177280
Exp. sfr	27	27	...	27

Test settings	
Tolerance V	±7,0000e+01
Tolerance sfr	±0,0000e+00

Test statistics	
Min CPU cycles	1271
Max CPU cycles	2454
Avg CPU cycles	2057

Verification: uGain FiP32 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for General block uGain.

Test results				
Time step	1	2	...	107
CPU cycles	450	450	...	443
Inputs				
In (DSP)	-2147483648	-2106965089	...	2147483647
In	-1	-0.981	...	1
Parameters				
Gain	2.1			
Outputs				
Out	-0.1	-0.06	...	0.1
Exp. Out	-0.1	-0.06	...	0.1
Out (DSP)	-214748364	-129659391	...	214748361
Exp. Out (DSP)	-214748365	-129659390	...	214748365

Test settings	
Tolerance Out	±2,3283e-09 (±5 LSB)

Test statistics	
Min CPU cycles	443
Max CPU cycles	450
Avg CPU cycles	446

Test case: Parameter test OK

Parameter test for General block uGain.

Test results				
Time step	1	2	...	107
CPU cycles	450	450	...	443
Inputs				
In (DSP)	858993459			
In	0.4			
Parameters				
Gain	-3.7	-3.63	...	3.7
Outputs				
Out	0.52	0.548	...	-0.52
Exp. Out	0.52	0.548	...	-0.52
Out (DSP)	1116691498	1176658965	...	-1116691499
Exp. Out (DSP)	1116691497	1176658965	...	-1116691497

Test settings	
Tolerance Out	±1,3970e-09 (±3 LSB)

Test statistics	
Min CPU cycles	443
Max CPU cycles	470
Avg CPU cycles	454

Test case: Conversion test **OK**

Conversion test for General block uGain.

Test results				
Time step	1	2	...	37
Mask parameters				
Gain	-10	-9.444	...	10
Controller parameters				
V	-1342177280	-1267611876	...	1342177280
sfr	27	27	...	27
Exp. V	-1342177280	-1267611876	...	1342177280
Exp. sfr	27	27	...	27

Test settings	
Tolerance V	±0,0000e+00
Tolerance sfr	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block uGain.

Test results				
Time step	1	2	...	37
Mask parameters				
Gain	-10	-9.444	...	10
Controller parameters				
V	-1342177280	-1267611904	...	1342177280
sfr	27	27	...	27
Exp. V	-1342177280	-1267611876	...	1342177280
Exp. sfr	27	27	...	27

Test settings	
Tolerance V	±7,0000e+01
Tolerance sfr	±0,0000e+00

Test statistics	
Min CPU cycles	2999
Max CPU cycles	11019
Avg CPU cycles	8556

Verification: uGain FiP32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for General block uGain.

Test results				
Time step	1	2	...	107
CPU cycles	82	74	...	74
Inputs				
In (DSP)	-2147483648	-2106965089	...	2147483647
In	-1	-0.981	...	1
Parameters				
Gain	2.1			
Outputs				
Out	-0.1	-0.06	...	0.1
Exp. Out	-0.1	-0.06	...	0.1
Out (DSP)	-214748364	-129659391	...	214748361
Exp. Out (DSP)	-214748365	-129659390	...	214748365

Test settings	
Tolerance Out	±2,3283e-09 (±5 LSB)

Test statistics	
Min CPU cycles	74
Max CPU cycles	82
Avg CPU cycles	74

Test case: Parameter test OK

Parameter test for General block uGain.

Test results				
Time step	1	2	...	107
CPU cycles	74	74	...	74
Inputs				
In (DSP)	858993459			
In	0.4			
Parameters				
Gain	-3.7	-3.63	...	3.7
Outputs				
Out	0.52	0.548	...	-0.52
Exp. Out	0.52	0.548	...	-0.52
Out (DSP)	1116691498	1176658965	...	-1116691499
Exp. Out (DSP)	1116691497	1176658965	...	-1116691497

Test settings	
Tolerance Out	±1,3970e-09 (±3 LSB)

Test statistics	
Min CPU cycles	74
Max CPU cycles	74
Avg CPU cycles	74

Test case: Conversion test **OK**

Conversion test for General block uGain.

Test results				
Time step	1	2	...	37
Mask parameters				
Gain	-10	-9.444	...	10
Controller parameters				
V	-1342177280	-1267611876	...	1342177280
sfr	27	27	...	27
Exp. V	-1342177280	-1267611876	...	1342177280
Exp. sfr	27	27	...	27

Test settings	
Tolerance V	±0,0000e+00
Tolerance sfr	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block uGain.

Test results				
Time step	1	2	...	37
Mask parameters				
Gain	-10	-9.444	...	10
Controller parameters				
V	-1342177280	-1267611904	...	1342177280
sfr	27	27	...	27
Exp. V	-1342177280	-1267611876	...	1342177280
Exp. sfr	27	27	...	27

Test settings	
Tolerance V	±7,0000e+01
Tolerance sfr	±0,0000e+00

Test statistics	
Min CPU cycles	971
Max CPU cycles	1594
Avg CPU cycles	1293

Verification: uGain FiP32 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for General block uGain.

Test results				
Time step	1	2	...	107
CPU cycles	42	42	...	42
Inputs				
In (DSP)	-2147483648	-2106965089	...	2147483647
In	-1	-0.981	...	1
Parameters				
Gain	2.1			
Outputs				
Out	-0.1	-0.06	...	0.1
Exp. Out	-0.1	-0.06	...	0.1
Out (DSP)	-214748364	-129659391	...	214748361
Exp. Out (DSP)	-214748365	-129659390	...	214748365

Test settings	
Tolerance Out	±2,3283e-09 (±5 LSB)

Test statistics	
Min CPU cycles	42
Max CPU cycles	42
Avg CPU cycles	42

Test case: Parameter test OK

Parameter test for General block uGain.

Test results				
Time step	1	2	...	107
CPU cycles	42	42	...	42
Inputs				
In (DSP)	858993459			
In	0.4			
Parameters				
Gain	-3.7	-3.63	...	3.7
Outputs				
Out	0.52	0.548	...	-0.52
Exp. Out	0.52	0.548	...	-0.52
Out (DSP)	1116691498	1176658965	...	-1116691499
Exp. Out (DSP)	1116691497	1176658965	...	-1116691497

Test settings	
Tolerance Out	±1,3970e-09 (±3 LSB)

Test statistics	
Min CPU cycles	42
Max CPU cycles	42
Avg CPU cycles	42

Test case: Conversion test **OK**

Conversion test for General block uGain.

Test results				
Time step	1	2	...	37
Mask parameters				
Gain	-10	-9.444	...	10
Controller parameters				
V	-1342177280	-1267611876	...	1342177280
sfr	27	27	...	27
Exp. V	-1342177280	-1267611876	...	1342177280
Exp. sfr	27	27	...	27

Test settings	
Tolerance V	±0,0000e+00
Tolerance sfr	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block uGain.

Test results				
Time step	1	2	...	37
Mask parameters				
Gain	-10	-9.444	...	10
Controller parameters				
V	-1342177280	-1267611904	...	1342177280
sfr	27	27	...	27
Exp. V	-1342177280	-1267611876	...	1342177280
Exp. sfr	27	27	...	27

Test settings	
Tolerance V	±7,0000e+01
Tolerance sfr	±0,0000e+00

Test statistics	
Min CPU cycles	1228
Max CPU cycles	2972
Avg CPU cycles	2372

Verification: uGain Float32 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for General block uGain.

Test results				
Time step	1	2	...	107
CPU cycles	441	441	...	435
Inputs				
In (DSP)	-7.13	-6.995	...	7.13
In	-7.13	-6.995	...	7.13
Parameters				
Gain	2.1			
Outputs				
Out	-2.407	-2.124	...	2.407
Exp. Out	-2.407	-2.124	...	2.407
Out (DSP)	-2.407	-2.124	...	2.407
Exp. Out (DSP)	-2.407	-2.124	...	2.407

Test settings	
Tolerance Out	±1,8626e-06 (±4000 LSB)

Test statistics	
Min CPU cycles	85
Max CPU cycles	537
Avg CPU cycles	315

Test case: Parameter test OK

Parameter test for General block uGain.

Test results				
Time step	1	2	...	107
CPU cycles	189	189	...	179
Inputs				
In (DSP)	1.257			
In	1.257			
Parameters				
Gain	-3.7	-3.63	...	3.7
Outputs				
Out	1.634	1.721	...	-1.634
Exp. Out	1.634	1.721	...	-1.634
Out (DSP)	1.634	1.721	...	-1.634
Exp. Out (DSP)	1.634	1.721	...	-1.634

Test settings	
Tolerance Out	±1,8626e-06 (±4000 LSB)

Test statistics	
Min CPU cycles	85
Max CPU cycles	189
Avg CPU cycles	118

Test case: Conversion test **OK**

Conversion test for General block uGain.

Test results				
Time step	1	2	...	37
Mask parameters				
Gain	-10	-9.444	...	10
Controller parameters				
V	-10	-9.444	...	10
Exp. V	-10	-9.444	...	10

Test settings	
Tolerance V	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block uGain.

Test results				
Time step	1	2	...	37
Mask parameters				
Gain	-10	-9.444	...	10
Controller parameters				
V	-10	-9.444	...	10
Exp. V	-10	-9.444	...	10

Test settings	
Tolerance V	±5,0000e-07

Test statistics	
Min CPU cycles	812
Max CPU cycles	829
Avg CPU cycles	812

Verification: uGain Float32 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for General block uGain.

Test results				
Time step	1	2	...	107
CPU cycles	197	197	...	183
Inputs				
In (DSP)	-7.13	-6.995	...	7.13
In	-7.13	-6.995	...	7.13
Parameters				
Gain	2.1			
Outputs				
Out	-2.407	-2.124	...	2.407
Exp. Out	-2.407	-2.124	...	2.407
Out (DSP)	-2.407	-2.124	...	2.407
Exp. Out (DSP)	-2.407	-2.124	...	2.407

Test settings	
Tolerance Out	±1,8626e-06 (±4000 LSB)

Test statistics	
Min CPU cycles	67
Max CPU cycles	221
Avg CPU cycles	148

Test case: Parameter test OK

Parameter test for General block uGain.

Test results				
Time step	1	2	...	107
CPU cycles	125	125	...	107
Inputs				
In (DSP)	1.257			
In	1.257			
Parameters				
Gain	-3.7	-3.63	...	3.7
Outputs				
Out	1.634	1.721	...	-1.634
Exp. Out	1.634	1.721	...	-1.634
Out (DSP)	1.634	1.721	...	-1.634
Exp. Out (DSP)	1.634	1.721	...	-1.634

Test settings	
Tolerance Out	±1,8626e-06 (±4000 LSB)

Test statistics	
Min CPU cycles	67
Max CPU cycles	125
Avg CPU cycles	83

Test case: Conversion test OK

Conversion test for General block uGain.

Test results				
Time step	1	2	...	37
Mask parameters				
Gain	-10	-9.444	...	10
Controller parameters				
V	-10	-9.444	...	10
Exp. V	-10	-9.444	...	10

Test settings	
Tolerance V	±0,0000e+00

Test case: Conversion-on-Target test OK

Conversion-on-Target test for General block uGain.

Test results				
Time step	1	2	...	37
Mask parameters				
Gain	-10	-9.444	...	10
Controller parameters				
V	-10	-9.444	...	10
Exp. V	-10	-9.444	...	10

Test settings	
Tolerance V	±5,0000e-07

Test statistics	
Min CPU cycles	397
Max CPU cycles	397
Avg CPU cycles	397

Verification: uGain Float32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for General block uGain.

Test results				
Time step	1	2	...	107
CPU cycles	382	382	...	383
Inputs				
In (DSP)	-7.13	-6.995	...	7.13
In	-7.13	-6.995	...	7.13
Parameters				
Gain	2.1			
Outputs				
Out	-2.407	-2.124	...	2.407
Exp. Out	-2.407	-2.124	...	2.407
Out (DSP)	-2.407	-2.124	...	2.407
Exp. Out (DSP)	-2.407	-2.124	...	2.407

Test settings	
Tolerance Out	±1,8626e-06 (±4000 LSB)

Test statistics	
Min CPU cycles	100
Max CPU cycles	411
Avg CPU cycles	288

Test case: Parameter test OK

Parameter test for General block uGain.

Test results				
Time step	1	2	...	107
CPU cycles	235	235	...	231
Inputs				
In (DSP)	1.257			
In	1.257			
Parameters				
Gain	-3.7	-3.63	...	3.7
Outputs				
Out	1.634	1.721	...	-1.634
Exp. Out	1.634	1.721	...	-1.634
Out (DSP)	1.634	1.721	...	-1.634
Exp. Out (DSP)	1.634	1.721	...	-1.634

Test settings	
Tolerance Out	±1,8626e-06 (±4000 LSB)

Test statistics	
Min CPU cycles	100
Max CPU cycles	235
Avg CPU cycles	144

Test case: Conversion test OK

Conversion test for General block uGain.

Test results				
Time step	1	2	...	37
Mask parameters				
Gain	-10	-9.444	...	10
Controller parameters				
V	-10	-9.444	...	10
Exp. V	-10	-9.444	...	10

Test settings	
Tolerance V	±0,0000e+00

Test case: Conversion-on-Target test OK

Conversion-on-Target test for General block uGain.

Test results				
Time step	1	2	...	37
Mask parameters				
Gain	-10	-9.444	...	10
Controller parameters				
V	-10	-9.444	...	10
Exp. V	-10	-9.444	...	10

Test settings	
Tolerance V	±5,0000e-07

Test statistics	
Min CPU cycles	466
Max CPU cycles	466
Avg CPU cycles	466

Verification: uGain Float32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for General block uGain.

Test results				
Time step	1	2	...	107
CPU cycles	774	774	...	701
Inputs				
In (DSP)	-7.13	-6.995	...	7.13
In	-7.13	-6.995	...	7.13
Parameters				
Gain	2.1			
Outputs				
Out	-2.407	-2.124	...	2.407
Exp. Out	-2.407	-2.124	...	2.407
Out (DSP)	-2.407	-2.124	...	2.407
Exp. Out (DSP)	-2.407	-2.124	...	2.407

Test settings	
Tolerance Out	±1,8626e-06 (±4000 LSB)

Test statistics	
Min CPU cycles	329
Max CPU cycles	956
Avg CPU cycles	715

Test case: Parameter test OK

Parameter test for General block uGain.

Test results				
Time step	1	2	...	107
CPU cycles	827	827	...	759
Inputs				
In (DSP)	1.257			
In	1.257			
Parameters				
Gain	-3.7	-3.63	...	3.7
Outputs				
Out	1.634	1.721	...	-1.634
Exp. Out	1.634	1.721	...	-1.634
Out (DSP)	1.634	1.721	...	-1.634
Exp. Out (DSP)	1.634	1.721	...	-1.634

Test settings	
Tolerance Out	±1,8626e-06 (±4000 LSB)

Test statistics	
Min CPU cycles	396
Max CPU cycles	855
Avg CPU cycles	539

Test case: Conversion test **OK**

Conversion test for General block uGain.

Test results				
Time step	1	2	...	37
Mask parameters				
Gain	-10	-9.444	...	10
Controller parameters				
V	-10	-9.444	...	10
Exp. V	-10	-9.444	...	10

Test settings	
Tolerance V	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block uGain.

Test results				
Time step	1	2	...	37
Mask parameters				
Gain	-10	-9.444	...	10
Controller parameters				
V	-10	-9.444	...	10
Exp. V	-10	-9.444	...	10

Test settings	
Tolerance V	±5,0000e-07

Test statistics	
Min CPU cycles	667
Max CPU cycles	696
Avg CPU cycles	694

Verification: uGain Float32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for General block uGain.

Test results				
Time step	1	2	...	107
CPU cycles	282	282	...	240
Inputs				
In (DSP)	-7.13	-6.995	...	7.13
In	-7.13	-6.995	...	7.13
Parameters				
Gain	2.1			
Outputs				
Out	-2.407	-2.124	...	2.407
Exp. Out	-2.407	-2.124	...	2.407
Out (DSP)	-2.407	-2.124	...	2.407
Exp. Out (DSP)	-2.407	-2.124	...	2.407

Test settings	
Tolerance Out	±1,8626e-06 (±4000 LSB)

Test statistics	
Min CPU cycles	161
Max CPU cycles	345
Avg CPU cycles	266

Test case: Parameter test OK

Parameter test for General block uGain.

Test results				
Time step	1	2	...	107
CPU cycles	332	332	...	298
Inputs				
In (DSP)	1.257			
In	1.257			
Parameters				
Gain	-3.7	-3.63	...	3.7
Outputs				
Out	1.634	1.721	...	-1.634
Exp. Out	1.634	1.721	...	-1.634
Out (DSP)	1.634	1.721	...	-1.634
Exp. Out (DSP)	1.634	1.721	...	-1.634

Test settings	
Tolerance Out	±1,8626e-06 (±4000 LSB)

Test statistics	
Min CPU cycles	178
Max CPU cycles	332
Avg CPU cycles	222

Test case: Conversion test OK

Conversion test for General block uGain.

Test results				
Time step	1	2	...	37
Mask parameters				
Gain	-10	-9.444	...	10
Controller parameters				
V	-10	-9.444	...	10
Exp. V	-10	-9.444	...	10

Test settings	
Tolerance V	±0,0000e+00

Test case: Conversion-on-Target test OK

Conversion-on-Target test for General block uGain.

Test results				
Time step	1	2	...	37
Mask parameters				
Gain	-10	-9.444	...	10
Controller parameters				
V	-10	-9.444	...	10
Exp. V	-10	-9.444	...	10

Test settings	
Tolerance V	±5,0000e-07

Test statistics	
Min CPU cycles	277
Max CPU cycles	278
Avg CPU cycles	277

Verification: uGain Float32 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for General block uGain.

Test results				
Time step	1	2	...	107
CPU cycles	708	708	...	610
Inputs				
In (DSP)	-7.13	-6.995	...	7.13
In	-7.13	-6.995	...	7.13
Parameters				
Gain	2.1			
Outputs				
Out	-2.407	-2.124	...	2.407
Exp. Out	-2.407	-2.124	...	2.407
Out (DSP)	-2.407	-2.124	...	2.407
Exp. Out (DSP)	-2.407	-2.124	...	2.407

Test settings	
Tolerance Out	±1,8626e-06 (±4000 LSB)

Test statistics	
Min CPU cycles	361
Max CPU cycles	929
Avg CPU cycles	677

Test case: Parameter test OK

Parameter test for General block uGain.

Test results				
Time step	1	2	...	107
CPU cycles	872	872	...	775
Inputs				
In (DSP)	1.257			
In	1.257			
Parameters				
Gain	-3.7	-3.63	...	3.7
Outputs				
Out	1.634	1.721	...	-1.634
Exp. Out	1.634	1.721	...	-1.634
Out (DSP)	1.634	1.721	...	-1.634
Exp. Out (DSP)	1.634	1.721	...	-1.634

Test settings	
Tolerance Out	±1,8626e-06 (±4000 LSB)

Test statistics	
Min CPU cycles	400
Max CPU cycles	876
Avg CPU cycles	531

Test case: Conversion test OK

Conversion test for General block uGain.

Test results				
Time step	1	2	...	37
Mask parameters				
Gain	-10	-9.444	...	10
Controller parameters				
V	-10	-9.444	...	10
Exp. V	-10	-9.444	...	10

Test settings	
Tolerance V	±0,0000e+00

Test case: Conversion-on-Target test OK

Conversion-on-Target test for General block uGain.

Test results				
Time step	1	2	...	37
Mask parameters				
Gain	-10	-9.444	...	10
Controller parameters				
V	-10	-9.444	...	10
Exp. V	-10	-9.444	...	10

Test settings	
Tolerance V	±5,0000e-07

Test statistics	
Min CPU cycles	523
Max CPU cycles	868
Avg CPU cycles	856

Verification: uGain Float32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for General block uGain.

Test results				
Time step	1	2	...	107
CPU cycles	430	343	...	340
Inputs				
In (DSP)	-7.13	-6.995	...	7.13
In	-7.13	-6.995	...	7.13
Parameters				
Gain	2.1			
Outputs				
Out	-2.407	-2.124	...	2.407
Exp. Out	-2.407	-2.124	...	2.407
Out (DSP)	-2.407	-2.124	...	2.407
Exp. Out (DSP)	-2.407	-2.124	...	2.407

Test settings	
Tolerance Out	±1,8626e-06 (±4000 LSB)

Test statistics	
Min CPU cycles	98
Max CPU cycles	430
Avg CPU cycles	274

Test case: Parameter test OK

Parameter test for General block uGain.

Test results				
Time step	1	2	...	107
CPU cycles	278	283	...	269
Inputs				
In (DSP)	1.257			
In	1.257			
Parameters				
Gain	-3.7	-3.63	...	3.7
Outputs				
Out	1.634	1.721	...	-1.634
Exp. Out	1.634	1.721	...	-1.634
Out (DSP)	1.634	1.721	...	-1.634
Exp. Out (DSP)	1.634	1.721	...	-1.634

Test settings	
Tolerance Out	±1,8626e-06 (±4000 LSB)

Test statistics	
Min CPU cycles	98
Max CPU cycles	283
Avg CPU cycles	157

Test case: Conversion test **OK**

Conversion test for General block uGain.

Test results				
Time step	1	2	...	37
Mask parameters				
Gain	-10	-9.444	...	10
Controller parameters				
V	-10	-9.444	...	10
Exp. V	-10	-9.444	...	10

Test settings	
Tolerance V	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block uGain.

Test results				
Time step	1	2	...	37
Mask parameters				
Gain	-10	-9.444	...	10
Controller parameters				
V	-10	-9.444	...	10
Exp. V	-10	-9.444	...	10

Test settings	
Tolerance V	±5,0000e-07

Test statistics	
Min CPU cycles	400
Max CPU cycles	448
Avg CPU cycles	401

Verification: uGain Float32 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for General block uGain.

Test results				
Time step	1	2	...	107
CPU cycles	356	356	...	354
Inputs				
In (DSP)	-7.13	-6.995	...	7.13
In	-7.13	-6.995	...	7.13
Parameters				
Gain	2.1			
Outputs				
Out	-2.407	-2.124	...	2.407
Exp. Out	-2.407	-2.124	...	2.407
Out (DSP)	-2.407	-2.124	...	2.407
Exp. Out (DSP)	-2.407	-2.124	...	2.407

Test settings	
Tolerance Out	±1,8626e-06 (±4000 LSB)

Test statistics	
Min CPU cycles	69
Max CPU cycles	424
Avg CPU cycles	251

Test case: Parameter test OK

Parameter test for General block uGain.

Test results				
Time step	1	2	...	107
CPU cycles	158	158	...	146
Inputs				
In (DSP)	1.257			
In	1.257			
Parameters				
Gain	-3.7	-3.63	...	3.7
Outputs				
Out	1.634	1.721	...	-1.634
Exp. Out	1.634	1.721	...	-1.634
Out (DSP)	1.634	1.721	...	-1.634
Exp. Out (DSP)	1.634	1.721	...	-1.634

Test settings	
Tolerance Out	±1,8626e-06 (±4000 LSB)

Test statistics	
Min CPU cycles	69
Max CPU cycles	158
Avg CPU cycles	96

Test case: Conversion test **OK**

Conversion test for General block uGain.

Test results				
Time step	1	2	...	37
Mask parameters				
Gain	-10	-9.444	...	10
Controller parameters				
V	-10	-9.444	...	10
Exp. V	-10	-9.444	...	10

Test settings	
Tolerance V	±0,0000e+00

Test case: Conversion-on-Target test **OK**

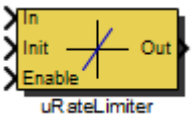
Conversion-on-Target test for General block uGain.

Test results				
Time step	1	2	...	37
Mask parameters				
Gain	-10	-9.444	...	10
Controller parameters				
V	-10	-9.444	...	10
Exp. V	-10	-9.444	...	10

Test settings	
Tolerance V	±5,0000e-07

Test statistics	
Min CPU cycles	644
Max CPU cycles	647
Avg CPU cycles	644

Block: uRateLimiter



Limitation of rising and falling rate.
Function of Enable:
0: rate limiting disabled, signal is passed through
1: rate limiting enabled, signal is rate limited
0->1: preload of output with value from init input

Inports	
In	
Init	Value which is loaded at rising flanke of enable signal
Enable	Enable == 0: Deactivation of block; Out is set to In. Enable != 0: Activation of block; Out is rate limited. Enable 0->1: Preloading of output; Out is set to value of Init input

Outports	
Out	

Mask Parameters		
Name	**ID**	**Description**
Tr	1	Rising time in seconds. Slew rate will be 1/Tr
Tf	2	Falling time in seconds. Slew rate will be 1/Tf
ts_fact	3	Multiplication factor of base sampling time (in integer format)

Description:

Rising and falling time refer to a step from 0 to 1. Entries for *Tr: Rising time* and *Tf: Falling time* smaller than the actual sample time will be limited to the sample time internally.
The 16- and 32-Bit fixed point implementations are based on an internal 32-Bit wide slew-rate variable while the 8-Bit fixed point implementation uses a 16-Bit wide slew-rate variable.

Implementations:

FiP16	16 Bit Fixed Point Implementation
FiP32	32 Bit Fixed Point Implementation
Float32	32 Bit Floating Point Implementation
Float64	64 Bit Floating Point Implementation

Implementation: FiP16

16 Bit Fixed Point Implementation

Inports Data Type	
In	int16
Init	int16
Enable	bool

Outports Data Type	
Out	int16

Implementation: FiP32

32 Bit Fixed Point Implementation

Inports Data Type	
In	int32
Init	int32
Enable	bool

Outports Data Type	
Out	int32

Implementation: Float32

32 Bit Floating Point Implementation

Inports Data Type	
In	float32
Init	float32
Enable	bool

Outports Data Type	
Out	float32

Implementation: Float64

64 Bit Floating Point Implementation

Inports Data Type	
In	float64
Init	float64
Enable	bool

Outports Data Type	
Out	float64

Verification: uRateLimiter FiP16 CPU TMS320F28335

Date of Test 2026-06-19

Target controller TMS320F28335

Test case: Inport test OK

Inport test for General block uRateLimiter.

Test results						
Time step	1	2	3	4	...	266
CPU cycles	83	83	83	83	...	98
Inputs						
In (DSP)	0	-32768	-31508	-30247	...	-6554
Init (DSP)	0	9830	9830	9830	...	9830
Enable (DSP)	0	0	0	0	...	1
In	0	-1	-0.962	-0.923	...	-0.2
Init	0	0.3	0.3	0.3	...	0.3
Enable	0	0	0	0	...	1
Parameters						
Tr	0.001					
Tf	0.003					
ts_fact	1					
Outputs						
Out	0	-1	-0.962	-0.923	...	-0.2
Exp. Out	0	-1	-0.962	-0.923	...	-0.2
Out (DSP)	0	-32768	-31508	-30247	...	-6554
Exp. Out (DSP)	0	-32768	-31508	-30247	...	-6554

Test settings	
Tolerance Out	±6,1035e-05 (±2 LSB)

Test statistics	
Min CPU cycles	83
Max CPU cycles	128
Avg CPU cycles	106

Test case: Conversion test OK

Conversion test for General block uRateLimiter.

Test results				
Time step	1	2	...	37
Mask parameters				
Tr	-10	-9.444	...	10
Tf	-9	-8.5	...	9
ts_fact	3	3	...	3
Controller parameters				
RateUp	2147483647	2147483647	...	64425
RateDown	2147483647	2147483647	...	71583
Exp. RateUp	2147483647	2147483647	...	64425
Exp. RateDown	2147483647	2147483647	...	71583

Test settings	
Tolerance RateUp	±0,0000e+00
Tolerance RateDown	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block uRateLimiter.

Test results				
Time step	1	2	...	37
Mask parameters				
Tr	-10	-9.444	...	10
Tf	-9	-8.5	...	9
ts_fact	3	3	...	3
Controller parameters				
RateUp	2147483647	2147483647	...	64424
RateDown	2147483647	2147483647	...	71582
Exp. RateUp	2147483647	2147483647	...	64425
Exp. RateDown	2147483647	2147483647	...	71583

Test settings	
Tolerance RateUp	±1,0000e+00
Tolerance RateDown	±1,0000e+00

Test statistics	
Min CPU cycles	2856
Max CPU cycles	2966
Avg CPU cycles	2910

Verification: uRateLimiter FiP16 CPU TM4C123GH6

Date of Test 2026-06-19

Target controller TM4C123GH6

Test case: Inport test OK

Inport test for General block uRateLimiter.

Test results						
Time step	1	2	3	4	...	266
CPU cycles	51	51	51	51	...	65
Inputs						
In (DSP)	0	-32768	-31508	-30247	...	-6554
Init (DSP)	0	9830	9830	9830	...	9830
Enable (DSP)	0	0	0	0	...	1
In	0	-1	-0.962	-0.923	...	-0.2
Init	0	0.3	0.3	0.3	...	0.3
Enable	0	0	0	0	...	1
Parameters						
Tr	0.001					
Tf	0.003					
ts_fact	1					
Outputs						
Out	0	-1	-0.962	-0.923	...	-0.2
Exp. Out	0	-1	-0.962	-0.923	...	-0.2
Out (DSP)	0	-32768	-31508	-30247	...	-6554
Exp. Out (DSP)	0	-32768	-31508	-30247	...	-6554

Test settings	
Tolerance Out	±6,1035e-05 (±2 LSB)

Test statistics	
Min CPU cycles	51
Max CPU cycles	81
Avg CPU cycles	68

Test case: Conversion test OK

Conversion test for General block uRateLimiter.

Test results				
Time step	1	2	...	37
Mask parameters				
Tr	-10	-9.444	...	10
Tf	-9	-8.5	...	9
ts_fact	3	3	...	3
Controller parameters				
RateUp	2147483647	2147483647	...	64425
RateDown	2147483647	2147483647	...	71583
Exp. RateUp	2147483647	2147483647	...	64425
Exp. RateDown	2147483647	2147483647	...	71583

Test settings	
Tolerance RateUp	±0,0000e+00
Tolerance RateDown	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block uRateLimiter.

Test results				
Time step	1	2	...	37
Mask parameters				
Tr	-10	-9.444	...	10
Tf	-9	-8.5	...	9
ts_fact	3	3	...	3
Controller parameters				
RateUp	2147483647	2147483647	...	64424
RateDown	2147483647	2147483647	...	71582
Exp. RateUp	2147483647	2147483647	...	64425
Exp. RateDown	2147483647	2147483647	...	71583

Test settings	
Tolerance RateUp	±1,0000e+00
Tolerance RateDown	±1,0000e+00

Test statistics	
Min CPU cycles	1087
Max CPU cycles	1097
Avg CPU cycles	1091

Verification: uRateLimiter FiP16 CPU STM32G474RE

Date of Test 2026-06-19

Target controller STM32G474RE

Test case: Inport test OK

Inport test for General block uRateLimiter.

Test results						
Time step	1	2	3	4	...	266
CPU cycles	67	67	67	67	...	109
Inputs						
In (DSP)	0	-32768	-31508	-30247	...	-6554
Init (DSP)	0	9830	9830	9830	...	9830
Enable (DSP)	0	0	0	0	...	1
In	0	-1	-0.962	-0.923	...	-0.2
Init	0	0.3	0.3	0.3	...	0.3
Enable	0	0	0	0	...	1
Parameters						
Tr	0.001					
Tf	0.003					
ts_fact	1					
Outputs						
Out	0	-1	-0.962	-0.923	...	-0.2
Exp. Out	0	-1	-0.962	-0.923	...	-0.2
Out (DSP)	0	-32768	-31508	-30247	...	-6554
Exp. Out (DSP)	0	-32768	-31508	-30247	...	-6554

Test settings	
Tolerance Out	±6,1035e-05 (±2 LSB)

Test statistics	
Min CPU cycles	67
Max CPU cycles	129
Avg CPU cycles	104

Test case: Conversion test OK

Conversion test for General block uRateLimiter.

Test results				
Time step	1	2	...	37
Mask parameters				
Tr	-10	-9.444	...	10
Tf	-9	-8.5	...	9
ts_fact	3	3	...	3
Controller parameters				
RateUp	2147483647	2147483647	...	64425
RateDown	2147483647	2147483647	...	71583
Exp. RateUp	2147483647	2147483647	...	64425
Exp. RateDown	2147483647	2147483647	...	71583

Test settings	
Tolerance RateUp	±0,0000e+00
Tolerance RateDown	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block uRateLimiter.

Test results				
Time step	1	2	...	37
Mask parameters				
Tr	-10	-9.444	...	10
Tf	-9	-8.5	...	9
ts_fact	3	3	...	3
Controller parameters				
RateUp	2147483647	2147483647	...	64424
RateDown	2147483647	2147483647	...	71582
Exp. RateUp	2147483647	2147483647	...	64425
Exp. RateDown	2147483647	2147483647	...	71583

Test settings	
Tolerance RateUp	±1,0000e+00
Tolerance RateDown	±1,0000e+00

Test statistics	
Min CPU cycles	1654
Max CPU cycles	1711
Avg CPU cycles	1657

Verification: uRateLimiter FiP16 CPU STM32F072RB

Date of Test 2026-06-19

Target controller STM32F072RB

Test case: Inport test OK

Inport test for General block uRateLimiter.

Test results						
Time step	1	2	3	4	...	266
CPU cycles	67	67	67	67	...	90
Inputs						
In (DSP)	0	-32768	-31508	-30247	...	-6554
Init (DSP)	0	9830	9830	9830	...	9830
Enable (DSP)	0	0	0	0	...	1
In	0	-1	-0.962	-0.923	...	-0.2
Init	0	0.3	0.3	0.3	...	0.3
Enable	0	0	0	0	...	1
Parameters						
Tr	0.001					
Tf	0.003					
ts_fact	1					
Outputs						
Out	0	-1	-0.962	-0.923	...	-0.2
Exp. Out	0	-1	-0.962	-0.923	...	-0.2
Out (DSP)	0	-32768	-31508	-30247	...	-6554
Exp. Out (DSP)	0	-32768	-31508	-30247	...	-6554

Test settings	
Tolerance Out	±6,1035e-05 (±2 LSB)

Test statistics	
Min CPU cycles	67
Max CPU cycles	158
Avg CPU cycles	89

Test case: Conversion test OK

Conversion test for General block uRateLimiter.

Test results				
Time step	1	2	...	37
Mask parameters				
Tr	-10	-9.444	...	10
Tf	-9	-8.5	...	9
ts_fact	3	3	...	3
Controller parameters				
RateUp	2147483647	2147483647	...	64425
RateDown	2147483647	2147483647	...	71583
Exp. RateUp	2147483647	2147483647	...	64425
Exp. RateDown	2147483647	2147483647	...	71583

Test settings	
Tolerance RateUp	±0,0000e+00
Tolerance RateDown	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block uRateLimiter.

Test results				
Time step	1	2	...	37
Mask parameters				
Tr	-10	-9.444	...	10
Tf	-9	-8.5	...	9
ts_fact	3	3	...	3
Controller parameters				
RateUp	2147483647	2147483647	...	64424
RateDown	2147483647	2147483647	...	71582
Exp. RateUp	2147483647	2147483647	...	64425
Exp. RateDown	2147483647	2147483647	...	71583

Test settings	
Tolerance RateUp	±1,0000e+00
Tolerance RateDown	±1,0000e+00

Test statistics	
Min CPU cycles	6095
Max CPU cycles	6408
Avg CPU cycles	6235

Verification: uRateLimiter FiP16 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for General block uRateLimiter.

Test results						
Time step	1	2	3	4	...	266
CPU cycles	41	41	41	41	...	46
Inputs						
In (DSP)	0	-32768	-31508	-30247	...	-6554
Init (DSP)	0	9830	9830	9830	...	9830
Enable (DSP)	0	0	0	0	...	1
In	0	-1	-0.962	-0.923	...	-0.2
Init	0	0.3	0.3	0.3	...	0.3
Enable	0	0	0	0	...	1
Parameters						
Tr	0.001					
Tf	0.003					
ts_fact	1					
Outputs						
Out	0	-1	-0.962	-0.923	...	-0.2
Exp. Out	0	-1	-0.962	-0.923	...	-0.2
Out (DSP)	0	-32768	-31508	-30247	...	-6554
Exp. Out (DSP)	0	-32768	-31508	-30247	...	-6554

Test settings	
Tolerance Out	±6,1035e-05 (±2 LSB)

Test statistics	
Min CPU cycles	41
Max CPU cycles	63
Avg CPU cycles	50

Test case: Conversion test OK

Conversion test for General block uRateLimiter.

Test results				
Time step	1	2	...	37
Mask parameters				
Tr	-10	-9.444	...	10
Tf	-9	-8.5	...	9
ts_fact	3	3	...	3
Controller parameters				
RateUp	2147483647	2147483647	...	64425
RateDown	2147483647	2147483647	...	71583
Exp. RateUp	2147483647	2147483647	...	64425
Exp. RateDown	2147483647	2147483647	...	71583

Test settings	
Tolerance RateUp	±0,0000e+00
Tolerance RateDown	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block uRateLimiter.

Test results				
Time step	1	2	...	37
Mask parameters				
Tr	-10	-9.444	...	10
Tf	-9	-8.5	...	9
ts_fact	3	3	...	3
Controller parameters				
RateUp	2147483647	2147483647	...	64424
RateDown	2147483647	2147483647	...	71582
Exp. RateUp	2147483647	2147483647	...	64425
Exp. RateDown	2147483647	2147483647	...	71583

Test settings	
Tolerance RateUp	±1,0000e+00
Tolerance RateDown	±1,0000e+00

Test statistics	
Min CPU cycles	2067
Max CPU cycles	2100
Avg CPU cycles	2082

Verification: uRateLimiter FiP16 CPU dsPIC33EP256MC502

Date of Test 2026-06-19

Target controller dsPIC33EP256MC502

Test case: Inport test OK

Inport test for General block uRateLimiter.

Test results						
Time step	1	2	3	4	...	266
CPU cycles	61	61	61	61	...	65
Inputs						
In (DSP)	0	-32768	-31508	-30247	...	-6554
Init (DSP)	0	9830	9830	9830	...	9830
Enable (DSP)	0	0	0	0	...	1
In	0	-1	-0.962	-0.923	...	-0.2
Init	0	0.3	0.3	0.3	...	0.3
Enable	0	0	0	0	...	1
Parameters						
Tr	0.001					
Tf	0.003					
ts_fact	1					
Outputs						
Out	0	-1	-0.962	-0.923	...	-0.2
Exp. Out	0	-1	-0.962	-0.923	...	-0.2
Out (DSP)	0	-32768	-31508	-30247	...	-6554
Exp. Out (DSP)	0	-32768	-31508	-30247	...	-6554

Test settings	
Tolerance Out	±6,1035e-05 (±2 LSB)

Test statistics	
Min CPU cycles	60
Max CPU cycles	78
Avg CPU cycles	68

Test case: Conversion test OK

Conversion test for General block uRateLimiter.

Test results				
Time step	1	2	...	37
Mask parameters				
Tr	-10	-9.444	...	10
Tf	-9	-8.5	...	9
ts_fact	3	3	...	3
Controller parameters				
RateUp	2147483647	2147483647	...	64425
RateDown	2147483647	2147483647	...	71583
Exp. RateUp	2147483647	2147483647	...	64425
Exp. RateDown	2147483647	2147483647	...	71583

Test settings	
Tolerance RateUp	±0,0000e+00
Tolerance RateDown	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block uRateLimiter.

Test results				
Time step	1	2	...	37
Mask parameters				
Tr	-10	-9.444	...	10
Tf	-9	-8.5	...	9
ts_fact	3	3	...	3
Controller parameters				
RateUp	2147483647	2147483647	...	64424
RateDown	2147483647	2147483647	...	71582
Exp. RateUp	2147483647	2147483647	...	64425
Exp. RateDown	2147483647	2147483647	...	71583

Test settings	
Tolerance RateUp	±1,0000e+00
Tolerance RateDown	±1,0000e+00

Test statistics	
Min CPU cycles	4978
Max CPU cycles	5687
Avg CPU cycles	5633

Verification: uRateLimiter FiP16 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for General block uRateLimiter.

Test results						
Time step	1	2	3	4	...	266
CPU cycles	82	66	66	66	...	81
Inputs						
In (DSP)	0	-32768	-31508	-30247	...	-6554
Init (DSP)	0	9830	9830	9830	...	9830
Enable (DSP)	0	0	0	0	...	1
In	0	-1	-0.962	-0.923	...	-0.2
Init	0	0.3	0.3	0.3	...	0.3
Enable	0	0	0	0	...	1
Parameters						
Tr	0.001					
Tf	0.003					
ts_fact	1					
Outputs						
Out	0	-1	-0.962	-0.923	...	-0.2
Exp. Out	0	-1	-0.962	-0.923	...	-0.2
Out (DSP)	0	-32768	-31508	-30247	...	-6554
Exp. Out (DSP)	0	-32768	-31508	-30247	...	-6554

Test settings	
Tolerance Out	±6,1035e-05 (±2 LSB)

Test statistics	
Min CPU cycles	66
Max CPU cycles	96
Avg CPU cycles	81

Test case: Conversion test OK

Conversion test for General block uRateLimiter.

Test results				
Time step	1	2	...	37
Mask parameters				
Tr	-10	-9.444	...	10
Tf	-9	-8.5	...	9
ts_fact	3	3	...	3
Controller parameters				
RateUp	2147483647	2147483647	...	64425
RateDown	2147483647	2147483647	...	71583
Exp. RateUp	2147483647	2147483647	...	64425
Exp. RateDown	2147483647	2147483647	...	71583

Test settings	
Tolerance RateUp	±0,0000e+00
Tolerance RateDown	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block uRateLimiter.

Test results				
Time step	1	2	...	37
Mask parameters				
Tr	-10	-9.444	...	10
Tf	-9	-8.5	...	9
ts_fact	3	3	...	3
Controller parameters				
RateUp	2147483647	2147483647	...	64424
RateDown	2147483647	2147483647	...	71582
Exp. RateUp	2147483647	2147483647	...	64425
Exp. RateDown	2147483647	2147483647	...	71583

Test settings	
Tolerance RateUp	±1,0000e+00
Tolerance RateDown	±1,0000e+00

Test statistics	
Min CPU cycles	1417
Max CPU cycles	1573
Avg CPU cycles	1421

Verification: uRateLimiter FiP16 CPU TMS320F28379D

Date of Test 2026-06-22

Target controller TMS320F28379D

Test case: Inport test OK

Inport test for General block uRateLimiter.

Test results						
Time step	1	2	3	4	...	266
CPU cycles	70	70	70	70	...	84
Inputs						
In (DSP)	0	-32768	-31508	-30247	...	-6554
Init (DSP)	0	9830	9830	9830	...	9830
Enable (DSP)	0	0	0	0	...	1
In	0	-1	-0.962	-0.923	...	-0.2
Init	0	0.3	0.3	0.3	...	0.3
Enable	0	0	0	0	...	1
Parameters						
Tr	0.001					
Tf	0.003					
ts_fact	1					
Outputs						
Out	0	-1	-0.962	-0.923	...	-0.2
Exp. Out	0	-1	-0.962	-0.923	...	-0.2
Out (DSP)	0	-32768	-31508	-30247	...	-6554
Exp. Out (DSP)	0	-32768	-31508	-30247	...	-6554

Test settings	
Tolerance Out	±6,1035e-05 (±2 LSB)

Test statistics	
Min CPU cycles	70
Max CPU cycles	127
Avg CPU cycles	97

Test case: Conversion test OK

Conversion test for General block uRateLimiter.

Test results				
Time step	1	2	...	37
Mask parameters				
Tr	-10	-9.444	...	10
Tf	-9	-8.5	...	9
ts_fact	3	3	...	3
Controller parameters				
RateUp	2147483647	2147483647	...	64425
RateDown	2147483647	2147483647	...	71583
Exp. RateUp	2147483647	2147483647	...	64425
Exp. RateDown	2147483647	2147483647	...	71583

Test settings	
Tolerance RateUp	±0,0000e+00
Tolerance RateDown	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block uRateLimiter.

Test results				
Time step	1	2	...	37
Mask parameters				
Tr	-10	-9.444	...	10
Tf	-9	-8.5	...	9
ts_fact	3	3	...	3
Controller parameters				
RateUp	2147483647	2147483647	...	64424
RateDown	2147483647	2147483647	...	71582
Exp. RateUp	2147483647	2147483647	...	64425
Exp. RateDown	2147483647	2147483647	...	71583

Test settings	
Tolerance RateUp	±1,0000e+00
Tolerance RateDown	±1,0000e+00

Test statistics	
Min CPU cycles	2163
Max CPU cycles	2241
Avg CPU cycles	2201

Verification: uRateLimiter FiP32 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for General block uRateLimiter.

Test results				
Time step	1	2	...	266
CPU cycles	71	71	...	87
Inputs				
In (DSP)	0	-2147483648	...	-429496730
Init (DSP)	0	644245094	...	644245094
Enable (DSP)	0	0	...	1
In	0	-1	...	-0.2
Init	0	0.3	...	0.3
Enable	0	0	...	1
Parameters				
Tr	0.001			
Tf	0.003			
ts_fact	1			
Outputs				
Out	0	-1	...	-0.2
Exp. Out	0	-1	...	-0.2
Out (DSP)	0	-2147483648	...	-429496730
Exp. Out (DSP)	0	-2147483648	...	-429496730

Test settings	
Tolerance Out	±1,1642e-08 (±25 LSB)

Test statistics	
Min CPU cycles	71
Max CPU cycles	105
Avg CPU cycles	88

Test case: Conversion test OK

Conversion test for General block uRateLimiter.

Test results				
Time step	1	2	...	37
Mask parameters				
Tr	-10	-9.444	...	10
Tf	-9	-8.5	...	9
ts_fact	3	3	...	3
Controller parameters				
RateUp	2147483647	2147483647	...	64425
RateDown	2147483647	2147483647	...	71583
Exp. RateUp	2147483647	2147483647	...	64425
Exp. RateDown	2147483647	2147483647	...	71583

Test settings	
Tolerance RateUp	±0,0000e+00
Tolerance RateDown	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block uRateLimiter.

Test results				
Time step	1	2	...	37
Mask parameters				
Tr	-10	-9.444	...	10
Tf	-9	-8.5	...	9
ts_fact	3	3	...	3
Controller parameters				
RateUp	2147483647	2147483647	...	64424
RateDown	2147483647	2147483647	...	71582
Exp. RateUp	2147483647	2147483647	...	64425
Exp. RateDown	2147483647	2147483647	...	71583

Test settings	
Tolerance RateUp	±3,0000e+00
Tolerance RateDown	±3,0000e+00

Test statistics	
Min CPU cycles	2856
Max CPU cycles	2966
Avg CPU cycles	2910

Verification: uRateLimiter FiP32 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for General block uRateLimiter.

Test results				
Time step	1	2	...	266
CPU cycles	45	45	...	51
Inputs				
In (DSP)	0	-2147483648	...	-429496730
Init (DSP)	0	644245094	...	644245094
Enable (DSP)	0	0	...	1
In	0	-1	...	-0.2
Init	0	0.3	...	0.3
Enable	0	0	...	1
Parameters				
Tr	0.001			
Tf	0.003			
ts_fact	1			
Outputs				
Out	0	-1	...	-0.2
Exp. Out	0	-1	...	-0.2
Out (DSP)	0	-2147483648	...	-429496730
Exp. Out (DSP)	0	-2147483648	...	-429496730

Test settings	
Tolerance Out	±1,1642e-08 (±25 LSB)

Test statistics	
Min CPU cycles	45
Max CPU cycles	61
Avg CPU cycles	53

Test case: Conversion test OK

Conversion test for General block uRateLimiter.

Test results				
Time step	1	2	...	37
Mask parameters				
Tr	-10	-9.444	...	10
Tf	-9	-8.5	...	9
ts_fact	3	3	...	3
Controller parameters				
RateUp	2147483647	2147483647	...	64425
RateDown	2147483647	2147483647	...	71583
Exp. RateUp	2147483647	2147483647	...	64425
Exp. RateDown	2147483647	2147483647	...	71583

Test settings	
Tolerance RateUp	±0,0000e+00
Tolerance RateDown	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block uRateLimiter.

Test results				
Time step	1	2	...	37
Mask parameters				
Tr	-10	-9.444	...	10
Tf	-9	-8.5	...	9
ts_fact	3	3	...	3
Controller parameters				
RateUp	2147483647	2147483647	...	64424
RateDown	2147483647	2147483647	...	71582
Exp. RateUp	2147483647	2147483647	...	64425
Exp. RateDown	2147483647	2147483647	...	71583

Test settings	
Tolerance RateUp	±3,0000e+00
Tolerance RateDown	±3,0000e+00

Test statistics	
Min CPU cycles	1087
Max CPU cycles	1097
Avg CPU cycles	1091

Verification: uRateLimiter FiP32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for General block uRateLimiter.

Test results				
Time step	1	2	...	266
CPU cycles	62	62	...	97
Inputs				
In (DSP)	0	-2147483648	...	-429496730
Init (DSP)	0	644245094	...	644245094
Enable (DSP)	0	0	...	1
In	0	-1	...	-0.2
Init	0	0.3	...	0.3
Enable	0	0	...	1
Parameters				
Tr	0.001			
Tf	0.003			
ts_fact	1			
Outputs				
Out	0	-1	...	-0.2
Exp. Out	0	-1	...	-0.2
Out (DSP)	0	-2147483648	...	-429496730
Exp. Out (DSP)	0	-2147483648	...	-429496730

Test settings	
Tolerance Out	±1,1642e-08 (±25 LSB)

Test statistics	
Min CPU cycles	62
Max CPU cycles	112
Avg CPU cycles	93

Test case: Conversion test OK

Conversion test for General block uRateLimiter.

Test results				
Time step	1	2	...	37
Mask parameters				
Tr	-10	-9.444	...	10
Tf	-9	-8.5	...	9
ts_fact	3	3	...	3
Controller parameters				
RateUp	2147483647	2147483647	...	64425
RateDown	2147483647	2147483647	...	71583
Exp. RateUp	2147483647	2147483647	...	64425
Exp. RateDown	2147483647	2147483647	...	71583

Test settings	
Tolerance RateUp	±0,0000e+00
Tolerance RateDown	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block uRateLimiter.

Test results				
Time step	1	2	...	37
Mask parameters				
Tr	-10	-9.444	...	10
Tf	-9	-8.5	...	9
ts_fact	3	3	...	3
Controller parameters				
RateUp	2147483647	2147483647	...	64424
RateDown	2147483647	2147483647	...	71582
Exp. RateUp	2147483647	2147483647	...	64425
Exp. RateDown	2147483647	2147483647	...	71583

Test settings	
Tolerance RateUp	±3,0000e+00
Tolerance RateDown	±3,0000e+00

Test statistics	
Min CPU cycles	1654
Max CPU cycles	1659
Avg CPU cycles	1654

Verification: uRateLimiter FiP32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for General block uRateLimiter.

Test results				
Time step	1	2	...	266
CPU cycles	62	62	...	84
Inputs				
In (DSP)	0	-2147483648	...	-429496730
Init (DSP)	0	644245094	...	644245094
Enable (DSP)	0	0	...	1
In	0	-1	...	-0.2
Init	0	0.3	...	0.3
Enable	0	0	...	1
Parameters				
Tr	0.001			
Tf	0.003			
ts_fact	1			
Outputs				
Out	0	-1	...	-0.2
Exp. Out	0	-1	...	-0.2
Out (DSP)	0	-2147483648	...	-429496730
Exp. Out (DSP)	0	-2147483648	...	-429496730

Test settings	
Tolerance Out	±1,1642e-08 (±25 LSB)

Test statistics	
Min CPU cycles	62
Max CPU cycles	94
Avg CPU cycles	81

Test case: Conversion test OK

Conversion test for General block uRateLimiter.

Test results				
Time step	1	2	...	37
Mask parameters				
Tr	-10	-9.444	...	10
Tf	-9	-8.5	...	9
ts_fact	3	3	...	3
Controller parameters				
RateUp	2147483647	2147483647	...	64425
RateDown	2147483647	2147483647	...	71583
Exp. RateUp	2147483647	2147483647	...	64425
Exp. RateDown	2147483647	2147483647	...	71583

Test settings	
Tolerance RateUp	±0,0000e+00
Tolerance RateDown	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block uRateLimiter.

Test results				
Time step	1	2	...	37
Mask parameters				
Tr	-10	-9.444	...	10
Tf	-9	-8.5	...	9
ts_fact	3	3	...	3
Controller parameters				
RateUp	2147483647	2147483647	...	64424
RateDown	2147483647	2147483647	...	71582
Exp. RateUp	2147483647	2147483647	...	64425
Exp. RateDown	2147483647	2147483647	...	71583

Test settings	
Tolerance RateUp	±3,0000e+00
Tolerance RateDown	±3,0000e+00

Test statistics	
Min CPU cycles	6095
Max CPU cycles	6409
Avg CPU cycles	6233

Verification: uRateLimiter FiP32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for General block uRateLimiter.

Test results				
Time step	1	2	...	266
CPU cycles	38	38	...	45
Inputs				
In (DSP)	0	-2147483648	...	-429496730
Init (DSP)	0	644245094	...	644245094
Enable (DSP)	0	0	...	1
In	0	-1	...	-0.2
Init	0	0.3	...	0.3
Enable	0	0	...	1
Parameters				
Tr	0.001			
Tf	0.003			
ts_fact	1			
Outputs				
Out	0	-1	...	-0.2
Exp. Out	0	-1	...	-0.2
Out (DSP)	0	-2147483648	...	-429496730
Exp. Out (DSP)	0	-2147483648	...	-429496730

Test settings	
Tolerance Out	±1,1642e-08 (±25 LSB)

Test statistics	
Min CPU cycles	38
Max CPU cycles	54
Avg CPU cycles	46

Test case: Conversion test OK

Conversion test for General block uRateLimiter.

Test results				
Time step	1	2	...	37
Mask parameters				
Tr	-10	-9.444	...	10
Tf	-9	-8.5	...	9
ts_fact	3	3	...	3
Controller parameters				
RateUp	2147483647	2147483647	...	64425
RateDown	2147483647	2147483647	...	71583
Exp. RateUp	2147483647	2147483647	...	64425
Exp. RateDown	2147483647	2147483647	...	71583

Test settings	
Tolerance RateUp	±0,0000e+00
Tolerance RateDown	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block uRateLimiter.

Test results				
Time step	1	2	...	37
Mask parameters				
Tr	-10	-9.444	...	10
Tf	-9	-8.5	...	9
ts_fact	3	3	...	3
Controller parameters				
RateUp	2147483647	2147483647	...	64424
RateDown	2147483647	2147483647	...	71582
Exp. RateUp	2147483647	2147483647	...	64425
Exp. RateDown	2147483647	2147483647	...	71583

Test settings	
Tolerance RateUp	±3,0000e+00
Tolerance RateDown	±3,0000e+00

Test statistics	
Min CPU cycles	2067
Max CPU cycles	2100
Avg CPU cycles	2082

Verification: uRateLimiter FiP32 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for General block uRateLimiter.

Test results				
Time step	1	2	...	266
CPU cycles	56	56	...	69
Inputs				
In (DSP)	0	-2147483648	...	-429496730
Init (DSP)	0	644245094	...	644245094
Enable (DSP)	0	0	...	1
In	0	-1	...	-0.2
Init	0	0.3	...	0.3
Enable	0	0	...	1
Parameters				
Tr	0.001			
Tf	0.003			
ts_fact	1			
Outputs				
Out	0	-1	...	-0.2
Exp. Out	0	-1	...	-0.2
Out (DSP)	0	-2147483648	...	-429496730
Exp. Out (DSP)	0	-2147483648	...	-429496730

Test settings	
Tolerance Out	±1,1642e-08 (±25 LSB)

Test statistics	
Min CPU cycles	56
Max CPU cycles	78
Avg CPU cycles	67

Test case: Conversion test OK

Conversion test for General block uRateLimiter.

Test results				
Time step	1	2	...	37
Mask parameters				
Tr	-10	-9.444	...	10
Tf	-9	-8.5	...	9
ts_fact	3	3	...	3
Controller parameters				
RateUp	2147483647	2147483647	...	64425
RateDown	2147483647	2147483647	...	71583
Exp. RateUp	2147483647	2147483647	...	64425
Exp. RateDown	2147483647	2147483647	...	71583

Test settings	
Tolerance RateUp	±0,0000e+00
Tolerance RateDown	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block uRateLimiter.

Test results				
Time step	1	2	...	37
Mask parameters				
Tr	-10	-9.444	...	10
Tf	-9	-8.5	...	9
ts_fact	3	3	...	3
Controller parameters				
RateUp	2147483647	2147483647	...	64424
RateDown	2147483647	2147483647	...	71582
Exp. RateUp	2147483647	2147483647	...	64425
Exp. RateDown	2147483647	2147483647	...	71583

Test settings	
Tolerance RateUp	±3,0000e+00
Tolerance RateDown	±3,0000e+00

Test statistics	
Min CPU cycles	4978
Max CPU cycles	5687
Avg CPU cycles	5633

Verification: uRateLimiter FiP32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for General block uRateLimiter.

Test results				
Time step	1	2	...	266
CPU cycles	76	64	...	80
Inputs				
In (DSP)	0	-2147483648	...	-429496730
Init (DSP)	0	644245094	...	644245094
Enable (DSP)	0	0	...	1
In	0	-1	...	-0.2
Init	0	0.3	...	0.3
Enable	0	0	...	1
Parameters				
Tr	0.001			
Tf	0.003			
ts_fact	1			
Outputs				
Out	0	-1	...	-0.2
Exp. Out	0	-1	...	-0.2
Out (DSP)	0	-2147483648	...	-429496730
Exp. Out (DSP)	0	-2147483648	...	-429496730

Test settings	
Tolerance Out	±1,1642e-08 (±25 LSB)

Test statistics	
Min CPU cycles	64
Max CPU cycles	89
Avg CPU cycles	78

Test case: Conversion test OK

Conversion test for General block uRateLimiter.

Test results				
Time step	1	2	...	37
Mask parameters				
Tr	-10	-9.444	...	10
Tf	-9	-8.5	...	9
ts_fact	3	3	...	3
Controller parameters				
RateUp	2147483647	2147483647	...	64425
RateDown	2147483647	2147483647	...	71583
Exp. RateUp	2147483647	2147483647	...	64425
Exp. RateDown	2147483647	2147483647	...	71583

Test settings	
Tolerance RateUp	±0,0000e+00
Tolerance RateDown	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block uRateLimiter.

Test results				
Time step	1	2	...	37
Mask parameters				
Tr	-10	-9.444	...	10
Tf	-9	-8.5	...	9
ts_fact	3	3	...	3
Controller parameters				
RateUp	2147483647	2147483647	...	64424
RateDown	2147483647	2147483647	...	71582
Exp. RateUp	2147483647	2147483647	...	64425
Exp. RateDown	2147483647	2147483647	...	71583

Test settings	
Tolerance RateUp	±3,0000e+00
Tolerance RateDown	±3,0000e+00

Test statistics	
Min CPU cycles	1360
Max CPU cycles	1529
Avg CPU cycles	1365

Verification: uRateLimiter FiP32 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for General block uRateLimiter.

Test results				
Time step	1	2	...	266
CPU cycles	58	58	...	72
Inputs				
In (DSP)	0	-2147483648	...	-429496730
Init (DSP)	0	644245094	...	644245094
Enable (DSP)	0	0	...	1
In	0	-1	...	-0.2
Init	0	0.3	...	0.3
Enable	0	0	...	1
Parameters				
Tr	0.001			
Tf	0.003			
ts_fact	1			
Outputs				
Out	0	-1	...	-0.2
Exp. Out	0	-1	...	-0.2
Out (DSP)	0	-2147483648	...	-429496730
Exp. Out (DSP)	0	-2147483648	...	-429496730

Test settings	
Tolerance Out	±1,1642e-08 (±25 LSB)

Test statistics	
Min CPU cycles	58
Max CPU cycles	96
Avg CPU cycles	76

Test case: Conversion test OK

Conversion test for General block uRateLimiter.

Test results				
Time step	1	2	...	37
Mask parameters				
Tr	-10	-9.444	...	10
Tf	-9	-8.5	...	9
ts_fact	3	3	...	3
Controller parameters				
RateUp	2147483647	2147483647	...	64425
RateDown	2147483647	2147483647	...	71583
Exp. RateUp	2147483647	2147483647	...	64425
Exp. RateDown	2147483647	2147483647	...	71583

Test settings	
Tolerance RateUp	±0,0000e+00
Tolerance RateDown	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for General block uRateLimiter.

Test results				
Time step	1	2	...	37
Mask parameters				
Tr	-10	-9.444	...	10
Tf	-9	-8.5	...	9
ts_fact	3	3	...	3
Controller parameters				
RateUp	2147483647	2147483647	...	64424
RateDown	2147483647	2147483647	...	71582
Exp. RateUp	2147483647	2147483647	...	64425
Exp. RateDown	2147483647	2147483647	...	71583

Test settings	
Tolerance RateUp	±3,0000e+00
Tolerance RateDown	±3,0000e+00

Test statistics	
Min CPU cycles	2163
Max CPU cycles	2241
Avg CPU cycles	2201

Block: uSaveSignal



Makes the incoming signal accessible for reading with parameter numbers.

Inports	
In	Input signal to be saved

Implementations:

Bool	Boolean Implementation
FiP8	8 Bit Fixed Point Implementation
FiP16	16 Bit Fixed Point Implementation
FiP32	32 Bit Fixed Point Implementation
Float32	32 Bit Floating Point Implementation
Float64	64 Bit Floating Point Implementation

Implementation: Bool

Boolean Implementation

Inports Data Type	
In	bool

Implementation: FiP8

8 Bit Fixed Point Implementation

Inports Data Type	
In	int8

Implementation: FiP16

16 Bit Fixed Point Implementation

Inports Data Type	
In	int16

Implementation: FiP32

32 Bit Fixed Point Implementation

Inports Data Type	
In	int32

Implementation: Float32

32 Bit Floating Point Implementation

Inports Data Type	
In	float32

Implementation: Float64

64 Bit Floating Point Implementation

Inports Data Type	
In	float64

Block: Xor



Logical XOR block.

Inports	
In1	
In2	

Outports	
Out	

Implementations:

Bool Boolean Implementation

Implementation: Bool

Boolean Implementation

Inports Data Type	
In1	bool
In2	bool

Outports Data Type	
Out	bool

Verification: Xor Bool CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for General block Xor.

Test results						
Time step	1	2	3	4	...	25
CPU cycles	58	58	58	58	...	58
Inputs						
In1 (DSP)	0	0	0	0	...	1
In2 (DSP)	0	0	0	0	...	1
In1	0	-1	-0.5	-0.2	...	1
In2	0	0	0	0	...	1
Outputs						
Out	0	0	0	0	...	0
Exp. Out	0	0	0	0	...	0
Out (DSP)	0	0	0	0	...	0
Exp. Out (DSP)	0	0	0	0	...	0

Test settings	
Tolerance Out	±0,0000e+00 (±0 LSB)

Test statistics	
Min CPU cycles	58
Max CPU cycles	58
Avg CPU cycles	58

Verification: Xor Bool CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test — OK

Inport test for General block Xor.

Test results						
Time step	1	2	3	4	...	25
CPU cycles	27	27	27	27	...	27
Inputs						
In1 (DSP)	0	0	0	0	...	1
In2 (DSP)	0	0	0	0	...	1
In1	0	-1	-0.5	-0.2	...	1
In2	0	0	0	0	...	1
Outputs						
Out	0	0	0	0	...	0
Exp. Out	0	0	0	0	...	0
Out (DSP)	0	0	0	0	...	0
Exp. Out (DSP)	0	0	0	0	...	0

Test settings	
Tolerance Out	±0,0000e+00 (±0 LSB)

Test statistics	
Min CPU cycles	27
Max CPU cycles	27
Avg CPU cycles	27

Verification: Xor Bool CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for General block Xor.

Test results						
Time step	1	2	3	4	...	25
CPU cycles	57	57	57	57	...	57
Inputs						
In1 (DSP)	0	0	0	0	...	1
In2 (DSP)	0	0	0	0	...	1
In1	0	-1	-0.5	-0.2	...	1
In2	0	0	0	0	...	1
Outputs						
Out	0	0	0	0	...	0
Exp. Out	0	0	0	0	...	0
Out (DSP)	0	0	0	0	...	0
Exp. Out (DSP)	0	0	0	0	...	0

Test settings	
Tolerance Out	±0,0000e+00 (±0 LSB)

Test statistics	
Min CPU cycles	57
Max CPU cycles	57
Avg CPU cycles	57

Verification: Xor Bool CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for General block Xor.

Test results						
Time step	1	2	3	4	...	25
CPU cycles	51	51	51	51	...	51
Inputs						
In1 (DSP)	0	0	0	0	...	1
In2 (DSP)	0	0	0	0	...	1
In1	0	-1	-0.5	-0.2	...	1
In2	0	0	0	0	...	1
Outputs						
Out	0	0	0	0	...	0
Exp. Out	0	0	0	0	...	0
Out (DSP)	0	0	0	0	...	0
Exp. Out (DSP)	0	0	0	0	...	0

Test settings	
Tolerance Out	±0,0000e+00 (±0 LSB)

Test statistics	
Min CPU cycles	51
Max CPU cycles	51
Avg CPU cycles	51

Verification: Xor Bool CPU PIC32MX170F256

Date of Test 2026-06-19

Target controller PIC32MX170F256

Test case: Inport test OK

Inport test for General block Xor.

Test results						
Time step	1	2	3	4	...	25
CPU cycles	32	32	32	32	...	32
Inputs						
In1 (DSP)	0	0	0	0	...	1
In2 (DSP)	0	0	0	0	...	1
In1	0	-1	-0.5	-0.2	...	1
In2	0	0	0	0	...	1
Outputs						
Out	0	0	0	0	...	0
Exp. Out	0	0	0	0	...	0
Out (DSP)	0	0	0	0	...	0
Exp. Out (DSP)	0	0	0	0	...	0

Test settings	
Tolerance Out	±0,0000e+00 (±0 LSB)

Test statistics	
Min CPU cycles	32
Max CPU cycles	32
Avg CPU cycles	32

Verification: Xor Bool CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for General block Xor.

Test results						
Time step	1	2	3	4	...	25
CPU cycles	42	42	42	42	...	42
Inputs						
In1 (DSP)	0	0	0	0	...	1
In2 (DSP)	0	0	0	0	...	1
In1	0	-1	-0.5	-0.2	...	1
In2	0	0	0	0	...	1
Outputs						
Out	0	0	0	0	...	0
Exp. Out	0	0	0	0	...	0
Out (DSP)	0	0	0	0	...	0
Exp. Out (DSP)	0	0	0	0	...	0

Test settings	
Tolerance Out	±0,0000e+00 (±0 LSB)

Test statistics	
Min CPU cycles	42
Max CPU cycles	42
Avg CPU cycles	42

Verification: Xor Bool CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for General block Xor.

Test results						
Time step	1	2	3	4	...	25
CPU cycles	67	56	56	56	...	56
Inputs						
In1 (DSP)	0	0	0	0	...	1
In2 (DSP)	0	0	0	0	...	1
In1	0	-1	-0.5	-0.2	...	1
In2	0	0	0	0	...	1
Outputs						
Out	0	0	0	0	...	0
Exp. Out	0	0	0	0	...	0
Out (DSP)	0	0	0	0	...	0
Exp. Out (DSP)	0	0	0	0	...	0

Test settings	
Tolerance Out	±0,0000e+00 (±0 LSB)

Test statistics	
Min CPU cycles	56
Max CPU cycles	67
Avg CPU cycles	56

Verification: Xor Bool CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for General block Xor.

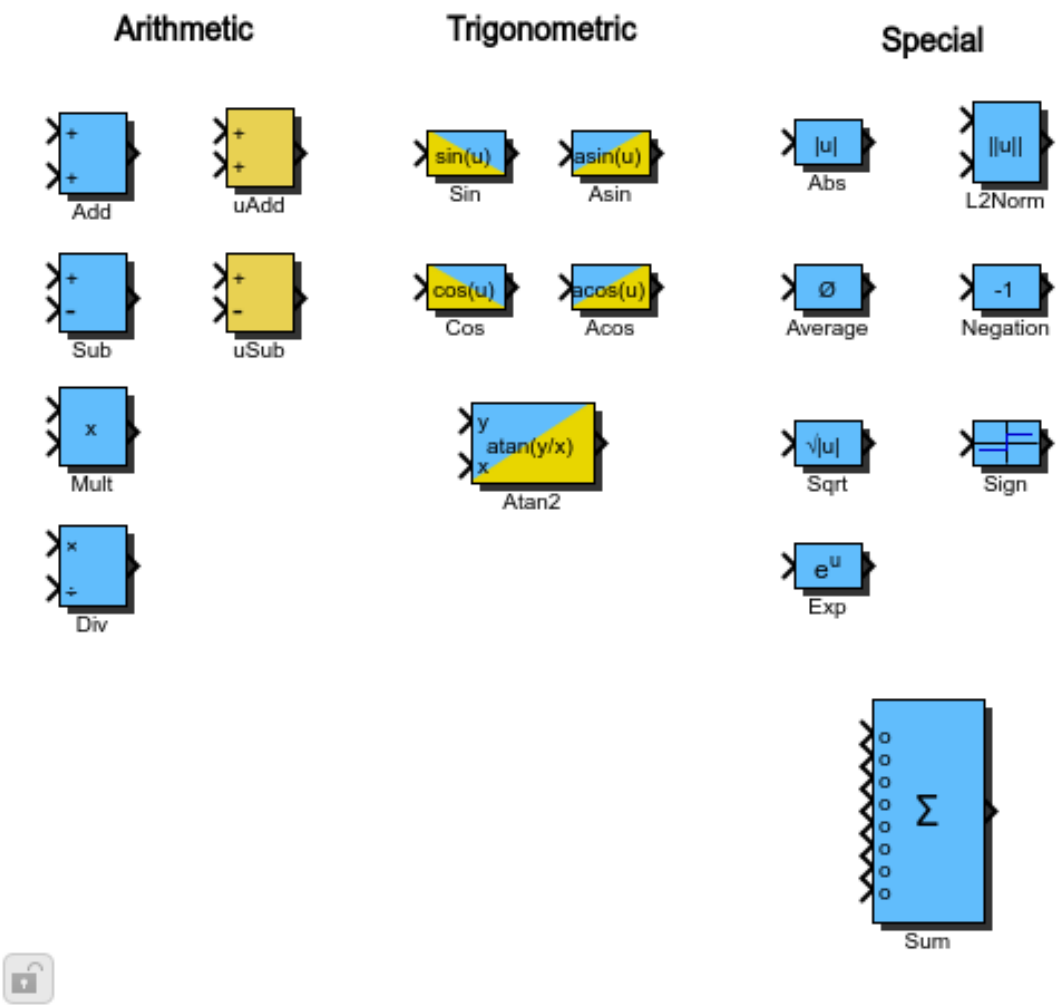
Test results						
Time step	1	2	3	4	...	25
CPU cycles	40	40	40	40	...	40
Inputs						
In1 (DSP)	0	0	0	0	...	1
In2 (DSP)	0	0	0	0	...	1
In1	0	-1	-0.5	-0.2	...	1
In2	0	0	0	0	...	1
Outputs						
Out	0	0	0	0	...	0
Exp. Out	0	0	0	0	...	0
Out (DSP)	0	0	0	0	...	0
Exp. Out (DSP)	0	0	0	0	...	0

Test settings	
Tolerance Out	±0,0000e+00 (±0 LSB)

Test statistics	
Min CPU cycles	40
Max CPU cycles	40
Avg CPU cycles	40

6 Math

This library contains blocks for computation of common mathematical functions.



Block: Abs



Calculation of absolute value of input.

Inports	
In	Input u

Outports	
Out	Absolute value of u

Description:

Calculation:

$$\mathrm{Out} = |\mathrm{In}|$$

Implementations:

FiP8	8 Bit Fixed Point Implementation
FiP16	16 Bit Fixed Point Implementation
FiP32	32 Bit Fixed Point Implementation
Float32	32 Bit Floating Point Implementation
Float64	64 Bit Floating Point Implementation

Implementation: FiP8

8 Bit Fixed Point Implementation

Inports Data Type	
In	int8

Outports Data Type	
Out	int8

Implementation: FiP16

16 Bit Fixed Point Implementation

Inports Data Type	
In	int16

Outports Data Type	
Out	int16

Implementation: FiP32

32 Bit Fixed Point Implementation

Inports Data Type	
In	int32

Outports Data Type	
Out	int32

Implementation: Float32

32 Bit Floating Point Implementation

Inports Data Type	
In	float32

Outports Data Type	
Out	float32

Implementation: Float64

64 Bit Floating Point Implementation

Inports Data Type	
In	float64

Outports Data Type	
Out	float64

Verification: Abs FiP16 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test — OK

Inport test for Math block Abs.

Test results						
Time step	1	2	3	4	...	107
CPU cycles	59	59	59	59	...	62
Inputs						
In (DSP)	-32768	-32768	-32768	-32768	...	32767
In	-1	-1	-1	-1	...	1
Outputs						
Out	1	1	1	1	...	1
Exp. Out	1	1	1	1	...	1
Out (DSP)	32767	32767	32767	32767	...	32767
Exp. Out (DSP)	32767	32767	32767	32767	...	32767

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	59
Max CPU cycles	62
Avg CPU cycles	61

Verification: Abs FiP16 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for Math block Abs.

Test results						
Time step	1	2	3	4	...	107
CPU cycles	31	31	31	31	...	29
Inputs						
In (DSP)	-32768	-32768	-32768	-32768	...	32767
In	-1	-1	-1	-1	...	1
Outputs						
Out	1	1	1	1	...	1
Exp. Out	1	1	1	1	...	1
Out (DSP)	32767	32767	32767	32767	...	32767
Exp. Out (DSP)	32767	32767	32767	32767	...	32767

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	29
Max CPU cycles	35
Avg CPU cycles	30

Verification: Abs FiP16 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for Math block Abs.

Test results						
Time step	1	2	3	4	...	107
CPU cycles	76	76	76	76	...	66
Inputs						
In (DSP)	-32768	-32768	-32768	-32768	...	32767
In	-1	-1	-1	-1	...	1
Outputs						
Out	1	1	1	1	...	1
Exp. Out	1	1	1	1	...	1
Out (DSP)	32767	32767	32767	32767	...	32767
Exp. Out (DSP)	32767	32767	32767	32767	...	32767

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	66
Max CPU cycles	76
Avg CPU cycles	68

Verification: Abs FiP16 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for Math block Abs.

Test results						
Time step	1	2	3	4	...	107
CPU cycles	64	64	64	64	...	54
Inputs						
In (DSP)	-32768	-32768	-32768	-32768	...	32767
In	-1	-1	-1	-1	...	1
Outputs						
Out	1	1	1	1	...	1
Exp. Out	1	1	1	1	...	1
Out (DSP)	32767	32767	32767	32767	...	32767
Exp. Out (DSP)	32767	32767	32767	32767	...	32767

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	54
Max CPU cycles	64
Avg CPU cycles	57

Verification: Abs FiP16 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for Math block Abs.

Test results						
Time step	1	2	3	4	...	107
CPU cycles	30	30	30	30	...	32
Inputs						
In (DSP)	-32768	-32768	-32768	-32768	...	32767
In	-1	-1	-1	-1	...	1
Outputs						
Out	1	1	1	1	...	1
Exp. Out	1	1	1	1	...	1
Out (DSP)	32767	32767	32767	32767	...	32767
Exp. Out (DSP)	32767	32767	32767	32767	...	32767

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	30
Max CPU cycles	33
Avg CPU cycles	32

Verification: Abs FiP16 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test — OK

Inport test for Math block Abs.

Test results						
Time step	1	2	3	4	...	107
CPU cycles	44	44	44	44	...	42
Inputs						
In (DSP)	-32768	-32768	-32768	-32768	...	32767
In	-1	-1	-1	-1	...	1
Outputs						
Out	1	1	1	1	...	1
Exp. Out	1	1	1	1	...	1
Out (DSP)	32767	32767	32767	32767	...	32767
Exp. Out (DSP)	32767	32767	32767	32767	...	32767

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	42
Max CPU cycles	44
Avg CPU cycles	42

Verification: Abs FiP16 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test — OK

Inport test for Math block Abs.

Test results						
Time step	1	2	3	4	...	107
CPU cycles	60	60	60	60	...	61
Inputs						
In (DSP)	-32768	-32768	-32768	-32768	...	32767
In	-1	-1	-1	-1	...	1
Outputs						
Out	1	1	1	1	...	1
Exp. Out	1	1	1	1	...	1
Out (DSP)	32767	32767	32767	32767	...	32767
Exp. Out (DSP)	32767	32767	32767	32767	...	32767

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	60
Max CPU cycles	62
Avg CPU cycles	61

Verification: Abs FiP16 CPU TMS320F28379D

Date of Test 2026-06-22

Target controller TMS320F28379D

Test case: Inport test OK

Inport test for Math block Abs.

Test results						
Time step	1	2	3	4	...	107
CPU cycles	59	59	59	59	...	58
Inputs						
In (DSP)	-32768	-32768	-32768	-32768	...	32767
In	-1	-1	-1	-1	...	1
Outputs						
Out	1	1	1	1	...	1
Exp. Out	1	1	1	1	...	1
Out (DSP)	32767	32767	32767	32767	...	32767
Exp. Out (DSP)	32767	32767	32767	32767	...	32767

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	58
Max CPU cycles	59
Avg CPU cycles	58

Verification: Abs FiP32 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for Math block Abs.

Test results				
Time step	1	2	...	107
CPU cycles	63	63	...	64
Inputs				
In (DSP)	-2147483648	-2147483648	...	2147483647
In	-1	-1	...	1
Outputs				
Out	1	1	...	1
Exp. Out	1	1	...	1
Out (DSP)	2147483647	2147483647	...	2147483647
Exp. Out (DSP)	2147483647	2147483647	...	2147483647

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	63
Max CPU cycles	64
Avg CPU cycles	63

Verification: Abs FiP32 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for Math block Abs.

Test results				
Time step	1	2	...	107
CPU cycles	29	29	...	31
Inputs				
In (DSP)	-2147483648	-2147483648	...	2147483647
In	-1	-1	...	1
Outputs				
Out	1	1	...	1
Exp. Out	1	1	...	1
Out (DSP)	2147483647	2147483647	...	2147483647
Exp. Out (DSP)	2147483647	2147483647	...	2147483647

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	29
Max CPU cycles	33
Avg CPU cycles	31

Verification: Abs FiP32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for Math block Abs.

Test results				
Time step	1	2	...	107
CPU cycles	71	71	...	66
Inputs				
In (DSP)	-2147483648	-2147483648	...	2147483647
In	-1	-1	...	1
Outputs				
Out	1	1	...	1
Exp. Out	1	1	...	1
Out (DSP)	2147483647	2147483647	...	2147483647
Exp. Out (DSP)	2147483647	2147483647	...	2147483647

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	66
Max CPU cycles	71
Avg CPU cycles	66

Verification: Abs FiP32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for Math block Abs.

Test results				
Time step	1	2	...	107
CPU cycles	63	63	...	53
Inputs				
In (DSP)	-2147483648	-2147483648	...	2147483647
In	-1	-1	...	1
Outputs				
Out	1	1	...	1
Exp. Out	1	1	...	1
Out (DSP)	2147483647	2147483647	...	2147483647
Exp. Out (DSP)	2147483647	2147483647	...	2147483647

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	53
Max CPU cycles	63
Avg CPU cycles	53

Verification: Abs FiP32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for Math block Abs.

Test results				
Time step	1	2	...	107
CPU cycles	32	32	...	32
Inputs				
In (DSP)	-2147483648	-2147483648	...	2147483647
In	-1	-1	...	1
Outputs				
Out	1	1	...	1
Exp. Out	1	1	...	1
Out (DSP)	2147483647	2147483647	...	2147483647
Exp. Out (DSP)	2147483647	2147483647	...	2147483647

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	32
Max CPU cycles	32
Avg CPU cycles	32

Verification: Abs FiP32 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for Math block Abs.

Test results				
Time step	1	2	...	107
CPU cycles	49	49	...	47
Inputs				
In (DSP)	-2147483648	-2147483648	...	2147483647
In	-1	-1	...	1
Outputs				
Out	1	1	...	1
Exp. Out	1	1	...	1
Out (DSP)	2147483647	2147483647	...	2147483647
Exp. Out (DSP)	2147483647	2147483647	...	2147483647

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	47
Max CPU cycles	52
Avg CPU cycles	48

Verification: Abs FiP32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for Math block Abs.

Test results				
Time step	1	2	...	107
CPU cycles	67	59	...	59
Inputs				
In (DSP)	-2147483648	-2147483648	...	2147483647
In	-1	-1	...	1
Outputs				
Out	1	1	...	1
Exp. Out	1	1	...	1
Out (DSP)	2147483647	2147483647	...	2147483647
Exp. Out (DSP)	2147483647	2147483647	...	2147483647

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	59
Max CPU cycles	67
Avg CPU cycles	59

Verification: Abs FiP32 CPU TMS320F28379D

Date of Test 2026-06-22

Target controller TMS320F28379D

Test case: Inport test OK

Inport test for Math block Abs.

Test results				
Time step	1	2	...	107
CPU cycles	65	65	...	60
Inputs				
In (DSP)	-2147483648	-2147483648	...	2147483647
In	-1	-1	...	1
Outputs				
Out	1	1	...	1
Exp. Out	1	1	...	1
Out (DSP)	2147483647	2147483647	...	2147483647
Exp. Out (DSP)	2147483647	2147483647	...	2147483647

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	60
Max CPU cycles	65
Avg CPU cycles	60

Verification: Abs Float32 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for Math block Abs.

Test results				
Time step	1	2	...	107
CPU cycles	53	53	...	53
Inputs				
In (DSP)	-1.3	-1.268	...	2.1
In	-1.3	-1.268	...	2.1
Outputs				
Out	1.3	1.268	...	2.1
Exp. Out	1.3	1.268	...	2.1
Out (DSP)	1.3	1.268	...	2.1
Exp. Out (DSP)	1.3	1.268	...	2.1

Test settings	
Tolerance Out	±1,3970e-07 (±300 LSB)

Test statistics	
Min CPU cycles	53
Max CPU cycles	53
Avg CPU cycles	53

Verification: Abs Float32 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for Math block Abs.

Test results				
Time step	1	2	...	107
CPU cycles	29	29	...	29
Inputs				
In (DSP)	-1.3	-1.268	...	2.1
In	-1.3	-1.268	...	2.1
Outputs				
Out	1.3	1.268	...	2.1
Exp. Out	1.3	1.268	...	2.1
Out (DSP)	1.3	1.268	...	2.1
Exp. Out (DSP)	1.3	1.268	...	2.1

Test settings	
Tolerance Out	±1,3970e-07 (±300 LSB)

Test statistics	
Min CPU cycles	29
Max CPU cycles	29
Avg CPU cycles	29

Verification: Abs Float32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for Math block Abs.

Test results				
Time step	1	2	...	107
CPU cycles	71	71	...	71
Inputs				
In (DSP)	-1.3	-1.268	...	2.1
In	-1.3	-1.268	...	2.1
Outputs				
Out	1.3	1.268	...	2.1
Exp. Out	1.3	1.268	...	2.1
Out (DSP)	1.3	1.268	...	2.1
Exp. Out (DSP)	1.3	1.268	...	2.1

Test settings	
Tolerance Out	±1,3970e-07 (±300 LSB)

Test statistics	
Min CPU cycles	71
Max CPU cycles	71
Avg CPU cycles	71

Verification: Abs Float32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for Math block Abs.

Test results				
Time step	1	2	...	107
CPU cycles	141	141	...	138
Inputs				
In (DSP)	-1.3	-1.268	...	2.1
In	-1.3	-1.268	...	2.1
Outputs				
Out	1.3	1.268	...	2.1
Exp. Out	1.3	1.268	...	2.1
Out (DSP)	1.3	1.268	...	2.1
Exp. Out (DSP)	1.3	1.268	...	2.1

Test settings	
Tolerance Out	±1,3970e-07 (±300 LSB)

Test statistics	
Min CPU cycles	138
Max CPU cycles	141
Avg CPU cycles	139

Verification: Abs Float32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for Math block Abs.

Test results				
Time step	1	2	...	107
CPU cycles	78	78	...	78
Inputs				
In (DSP)	-1.3	-1.268	...	2.1
In	-1.3	-1.268	...	2.1
Outputs				
Out	1.3	1.268	...	2.1
Exp. Out	1.3	1.268	...	2.1
Out (DSP)	1.3	1.268	...	2.1
Exp. Out (DSP)	1.3	1.268	...	2.1

Test settings	
Tolerance Out	±1,3970e-07 (±300 LSB)

Test statistics	
Min CPU cycles	78
Max CPU cycles	78
Avg CPU cycles	78

Verification: Abs Float32 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test — OK

Inport test for Math block Abs.

Test results				
Time step	1	2	...	107
CPU cycles	147	147	...	153
Inputs				
In (DSP)	-1.3	-1.268	...	2.1
In	-1.3	-1.268	...	2.1
Outputs				
Out	1.3	1.268	...	2.1
Exp. Out	1.3	1.268	...	2.1
Out (DSP)	1.3	1.268	...	2.1
Exp. Out (DSP)	1.3	1.268	...	2.1

Test settings	
Tolerance Out	±1,3970e-07 (±300 LSB)

Test statistics	
Min CPU cycles	147
Max CPU cycles	153
Avg CPU cycles	150

Verification: Abs Float32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for Math block Abs.

Test results				
Time step	1	2	...	107
CPU cycles	69	59	...	59
Inputs				
In (DSP)	-1.3	-1.268	...	2.1
In	-1.3	-1.268	...	2.1
Outputs				
Out	1.3	1.268	...	2.1
Exp. Out	1.3	1.268	...	2.1
Out (DSP)	1.3	1.268	...	2.1
Exp. Out (DSP)	1.3	1.268	...	2.1

Test settings	
Tolerance Out	±1,3970e-07 (±300 LSB)

Test statistics	
Min CPU cycles	59
Max CPU cycles	69
Avg CPU cycles	59

Verification: Abs Float32 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for Math block Abs.

Test results				
Time step	1	2	...	107
CPU cycles	48	48	...	48
Inputs				
In (DSP)	-1.3	-1.268	...	2.1
In	-1.3	-1.268	...	2.1
Outputs				
Out	1.3	1.268	...	2.1
Exp. Out	1.3	1.268	...	2.1
Out (DSP)	1.3	1.268	...	2.1
Exp. Out (DSP)	1.3	1.268	...	2.1

Test settings	
Tolerance Out	±1,3970e-07 (±300 LSB)

Test statistics	
Min CPU cycles	48
Max CPU cycles	48
Avg CPU cycles	48

Block: Acos



Arccosine computation of input value.

Inports	
In	Input u

Outports	
Out	Result of sin(u)

Description:

Calculation:

$$\mathrm{Out} = \arccos\left(\mathrm{In}\right)$$

Implementations:

FiP8	8 Bit Fixed Point Implementation
FiP16	16 Bit Fixed Point Implementation
FiP32	32 Bit Fixed Point Implementation
Float32	32 Bit Floating Point Implementation
Float64	64 Bit Floating Point Implementation

Implementation: FiP8

8 Bit Fixed Point Implementation

Inports Data Type	
In	int8

Outports Data Type	
Out	int8

Implementation: FiP16

16 Bit Fixed Point Implementation

Inports Data Type	
In	int16

Outports Data Type	
Out	int16

Implementation: FiP32

32 Bit Fixed Point Implementation

Inports Data Type	
In	int32

Outports Data Type	
Out	int32

Implementation: Float32

32 Bit Floating Point Implementation

Inports Data Type	
In	float32

Outports Data Type	
Out	float32

Implementation: Float64

64 Bit Floating Point Implementation

Inports Data Type	
In	float64

Outports Data Type	
Out	float64

Verification: Acos FiP16 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test — OK

Inport test for Math block Acos.

Test results						
Time step	1	2	3	4	...	133
CPU cycles	101	100	100	100	...	86
Inputs						
In (DSP)	-32768	-32272	-31775	-31279	...	32767
In	-1	-0.985	-0.97	-0.955	...	1
Outputs						
Out	1	0.945	0.921	0.904	...	0
Exp. Out	1	0.945	0.921	0.904	...	0
Out (DSP)	32760	30952	30194	29612	...	7
Exp. Out (DSP)	32767	30950	30194	29611	...	0

Test settings	
Tolerance Out	±2,4414e-04 (±8 LSB)

Test statistics	
Min CPU cycles	86
Max CPU cycles	101
Avg CPU cycles	92

Verification: Acos FiP16 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test — OK

Inport test for Math block Acos.

Test results						
Time step	1	2	3	4	...	133
CPU cycles	65	65	65	65	...	65
Inputs						
In (DSP)	-32768	-32272	-31775	-31279	...	32767
In	-1	-0.985	-0.97	-0.955	...	1
Outputs						
Out	1	0.945	0.921	0.904	...	0
Exp. Out	1	0.945	0.921	0.904	...	0
Out (DSP)	32760	30952	30194	29612	...	7
Exp. Out (DSP)	32767	30950	30194	29611	...	0

Test settings	
Tolerance Out	±2,4414e-04 (±8 LSB)

Test statistics	
Min CPU cycles	65
Max CPU cycles	65
Avg CPU cycles	65

Verification: Acos FiP16 CPU STM32G474RE

Date of Test 2026-06-19

Target controller STM32G474RE

Test case: Inport test OK

Inport test for Math block Acos.

Test results						
Time step	1	2	3	4	...	133
CPU cycles	130	116	116	116	...	96
Inputs						
In (DSP)	-32768	-32272	-31775	-31279	...	32767
In	-1	-0.985	-0.97	-0.955	...	1
Outputs						
Out	1	0.945	0.921	0.904	...	0
Exp. Out	1	0.945	0.921	0.904	...	0
Out (DSP)	32760	30952	30194	29612	...	7
Exp. Out (DSP)	32767	30950	30194	29611	...	0

Test settings	
Tolerance Out	±2,4414e-04 (±8 LSB)

Test statistics	
Min CPU cycles	96
Max CPU cycles	130
Avg CPU cycles	107

Verification: Acos FiP16 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for Math block Acos.

Test results						
Time step	1	2	3	4	...	133
CPU cycles	107	103	103	103	...	82
Inputs						
In (DSP)	-32768	-32272	-31775	-31279	...	32767
In	-1	-0.985	-0.97	-0.955	...	1
Outputs						
Out	1	0.945	0.921	0.904	...	0
Exp. Out	1	0.945	0.921	0.904	...	0
Out (DSP)	32760	30952	30194	29612	...	7
Exp. Out (DSP)	32767	30950	30194	29611	...	0

Test settings	
Tolerance Out	±2,4414e-04 (±8 LSB)

Test statistics	
Min CPU cycles	82
Max CPU cycles	107
Avg CPU cycles	92

Verification: Acos FiP16 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for Math block Acos.

Test results						
Time step	1	2	3	4	...	133
CPU cycles	52	55	55	55	...	51
Inputs						
In (DSP)	-32768	-32272	-31775	-31279	...	32767
In	-1	-0.985	-0.97	-0.955	...	1
Outputs						
Out	1	0.945	0.921	0.904	...	0
Exp. Out	1	0.945	0.921	0.904	...	0
Out (DSP)	32760	30952	30194	29612	...	7
Exp. Out (DSP)	32767	30950	30194	29611	...	0

Test settings	
Tolerance Out	±2,4414e-04 (±8 LSB)

Test statistics	
Min CPU cycles	51
Max CPU cycles	55
Avg CPU cycles	52

Verification: Acos FiP16 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test — OK

Inport test for Math block Acos.

Test results						
Time step	1	2	3	4	...	133
CPU cycles	72	71	71	71	...	69
Inputs						
In (DSP)	-32768	-32272	-31775	-31279	...	32767
In	-1	-0.985	-0.97	-0.955	...	1
Outputs						
Out	1	0.945	0.921	0.904	...	0
Exp. Out	1	0.945	0.921	0.904	...	0
Out (DSP)	32760	30952	30194	29612	...	7
Exp. Out (DSP)	32767	30950	30194	29611	...	0

Test settings	
Tolerance Out	±2,4414e-04 (±8 LSB)

Test statistics	
Min CPU cycles	69
Max CPU cycles	72
Avg CPU cycles	70

Verification: Acos FiP16 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for Math block Acos.

Test results						
Time step	1	2	3	4	...	133
CPU cycles	115	102	102	102	...	93
Inputs						
In (DSP)	-32768	-32272	-31775	-31279	...	32767
In	-1	-0.985	-0.97	-0.955	...	1
Outputs						
Out	1	0.945	0.921	0.904	...	0
Exp. Out	1	0.945	0.921	0.904	...	0
Out (DSP)	32760	30952	30194	29612	...	7
Exp. Out (DSP)	32767	30950	30194	29611	...	0

Test settings	
Tolerance Out	±2,4414e-04 (±8 LSB)

Test statistics	
Min CPU cycles	93
Max CPU cycles	115
Avg CPU cycles	97

Verification: Acos FiP16 CPU TMS320F28379D

Date of Test 2026-06-22

Target controller TMS320F28379D

Test case: Inport test OK

Inport test for Math block Acos.

Test results						
Time step	1	2	3	4	...	133
CPU cycles	101	96	96	96	...	78
Inputs						
In (DSP)	-32768	-32272	-31775	-31279	...	32767
In	-1	-0.985	-0.97	-0.955	...	1
Outputs						
Out	1	0.945	0.921	0.904	...	0
Exp. Out	1	0.945	0.921	0.904	...	0
Out (DSP)	32760	30952	30194	29612	...	7
Exp. Out (DSP)	32767	30950	30194	29611	...	0

Test settings	
Tolerance Out	±2,4414e-04 (±8 LSB)

Test statistics	
Min CPU cycles	78
Max CPU cycles	101
Avg CPU cycles	87

Verification: Acos FiP32 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for Math block Acos.

Test results				
Time step	1	2	...	133
CPU cycles	117	118	...	100
Inputs				
In (DSP)	-2147483648	-2114946017	...	2147483647
In	-1	-0.985	...	1
Outputs				
Out	1	0.945	...	0
Exp. Out	1	0.945	...	0
Out (DSP)	2147483640	2028456395	...	7
Exp. Out (DSP)	2147483647	2028339448	...	0

Test settings	
Tolerance Out	±9,3132e-05 (±200000 LSB)

Test statistics	
Min CPU cycles	100
Max CPU cycles	118
Avg CPU cycles	108

Verification: Acos FiP32 CPU TM4C123GH6

Date of Test 2026-06-19

Target controller TM4C123GH6

Test case: Inport test OK

Inport test for Math block Acos.

Test results				
Time step	1	2	...	133
CPU cycles	63	63	...	57
Inputs				
In (DSP)	-2147483648	-2114946017	...	2147483647
In	-1	-0.985	...	1
Outputs				
Out	1	0.945	...	0
Exp. Out	1	0.945	...	0
Out (DSP)	2147483640	2028456395	...	7
Exp. Out (DSP)	2147483647	2028339448	...	0

Test settings	
Tolerance Out	±9,3132e-05 (±200000 LSB)

Test statistics	
Min CPU cycles	57
Max CPU cycles	63
Avg CPU cycles	59

Verification: Acos FiP32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for Math block Acos.

Test results				
Time step	1	2	...	133
CPU cycles	150	127	...	102
Inputs				
In (DSP)	-2147483648	-2114946017	...	2147483647
In	-1	-0.985	...	1
Outputs				
Out	1	0.945	...	0
Exp. Out	1	0.945	...	0
Out (DSP)	2147483640	2028456395	...	7
Exp. Out (DSP)	2147483647	2028339448	...	0

Test settings	
Tolerance Out	±9,3132e-05 (±200000 LSB)

Test statistics	
Min CPU cycles	97
Max CPU cycles	150
Avg CPU cycles	114

Verification: Acos FiP32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for Math block Acos.

Test results				
Time step	1	2	...	133
CPU cycles	175	167	...	148
Inputs				
In (DSP)	-2147483648	-2114946017	...	2147483647
In	-1	-0.985	...	1
Outputs				
Out	1	0.945	...	0
Exp. Out	1	0.945	...	0
Out (DSP)	2147483640	2028456395	...	7
Exp. Out (DSP)	2147483647	2028339448	...	0

Test settings	
Tolerance Out	±9,3132e-05 (±200000 LSB)

Test statistics	
Min CPU cycles	148
Max CPU cycles	227
Avg CPU cycles	158

Verification: Acos FiP32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for Math block Acos.

Test results				
Time step	1	2	...	133
CPU cycles	66	68	...	54
Inputs				
In (DSP)	-2147483648	-2114946017	...	2147483647
In	-1	-0.985	...	1
Outputs				
Out	1	0.945	...	0
Exp. Out	1	0.945	...	0
Out (DSP)	2147483640	2028456395	...	7
Exp. Out (DSP)	2147483647	2028339448	...	0

Test settings	
Tolerance Out	±9,3132e-05 (±200000 LSB)

Test statistics	
Min CPU cycles	53
Max CPU cycles	68
Avg CPU cycles	60

Verification: Acos FiP32 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for Math block Acos.

Test results				
Time step	1	2	...	133
CPU cycles	221	223	...	213
Inputs				
In (DSP)	-2147483648	-2114946017	...	2147483647
In	-1	-0.985	...	1
Outputs				
Out	1	0.945	...	0
Exp. Out	1	0.945	...	0
Out (DSP)	2147483640	2028456395	...	7
Exp. Out (DSP)	2147483647	2028339448	...	0

Test settings	
Tolerance Out	±9,3132e-05 (±200000 LSB)

Test statistics	
Min CPU cycles	213
Max CPU cycles	223
Avg CPU cycles	217

Verification: Acos FiP32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for Math block Acos.

Test results				
Time step	1	2	...	133
CPU cycles	123	109	...	100
Inputs				
In (DSP)	-2147483648	-2114946017	...	2147483647
In	-1	-0.985	...	1
Outputs				
Out	1	0.945	...	0
Exp. Out	1	0.945	...	0
Out (DSP)	2147483640	2028456395	...	7
Exp. Out (DSP)	2147483647	2028339448	...	0

Test settings	
Tolerance Out	±9,3132e-05 (±200000 LSB)

Test statistics	
Min CPU cycles	100
Max CPU cycles	123
Avg CPU cycles	104

Verification: Acos FiP32 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test — OK

Inport test for Math block Acos.

Test results				
Time step	1	2	...	133
CPU cycles	116	118	...	96
Inputs				
In (DSP)	-2147483648	-2114946017	...	2147483647
In	-1	-0.985	...	1
Outputs				
Out	1	0.945	...	0
Exp. Out	1	0.945	...	0
Out (DSP)	2147483640	2028456395	...	7
Exp. Out (DSP)	2147483647	2028339448	...	0

Test settings	
Tolerance Out	±9,3132e-05 (±200000 LSB)

Test statistics	
Min CPU cycles	91
Max CPU cycles	121
Avg CPU cycles	105

Verification: Acos Float32 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for Math block Acos.

Test results				
Time step	1	2	...	133
CPU cycles	167	652	...	151
Inputs				
In (DSP)	-1	-0.985	...	1
In	-1	-0.985	...	1
Outputs				
Out	3.142	2.967	...	0
Exp. Out	3.142	2.967	...	0
Out (DSP)	3.142	2.967	...	0
Exp. Out (DSP)	3.142	2.967	...	0

Test settings	
Tolerance Out	±2,7940e-07 (±600 LSB)

Test statistics	
Min CPU cycles	151
Max CPU cycles	935
Avg CPU cycles	641

Verification: Acos Float32 CPU TM4C123GH6

Date of Test 2026-06-19

Target controller TM4C123GH6

Test case: Inport test OK

Inport test for Math block Acos.

Test results				
Time step	1	2	...	133
CPU cycles	83	169	...	83
Inputs				
In (DSP)	-1	-0.985	...	1
In	-1	-0.985	...	1
Outputs				
Out	3.142	2.967	...	0
Exp. Out	3.142	2.967	...	0
Out (DSP)	3.142	2.967	...	0
Exp. Out (DSP)	3.142	2.967	...	0

Test settings	
Tolerance Out	±2,7940e-07 (±600 LSB)

Test statistics	
Min CPU cycles	83
Max CPU cycles	187
Avg CPU cycles	163

Verification: Acos Float32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for Math block Acos.

Test results				
Time step	1	2	...	133
CPU cycles	218	385	...	218
Inputs				
In (DSP)	-1	-0.985	...	1
In	-1	-0.985	...	1
Outputs				
Out	3.142	2.967	...	0
Exp. Out	3.142	2.967	...	0
Out (DSP)	3.142	2.967	...	0
Exp. Out (DSP)	3.142	2.967	...	0

Test settings	
Tolerance Out	±2,7940e-07 (±600 LSB)

Test statistics	
Min CPU cycles	218
Max CPU cycles	444
Avg CPU cycles	367

Verification: Acos Float32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for Math block Acos.

Test results				
Time step	1	2	...	133
CPU cycles	241	5330	...	240
Inputs				
In (DSP)	-1	-0.985	...	1
In	-1	-0.985	...	1
Outputs				
Out	3.142	2.967	...	0
Exp. Out	3.142	2.967	...	0
Out (DSP)	3.142	2.967	...	0
Exp. Out (DSP)	3.142	2.967	...	0

Test settings	
Tolerance Out	±2,7940e-07 (±600 LSB)

Test statistics	
Min CPU cycles	240
Max CPU cycles	6329
Avg CPU cycles	5152

Verification: Acos Float32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test — OK

Inport test for Math block Acos.

Test results				
Time step	1	2	...	133
CPU cycles	349	649	...	333
Inputs				
In (DSP)	-1	-0.985	...	1
In	-1	-0.985	...	1
Outputs				
Out	3.142	2.967	...	0
Exp. Out	3.142	2.967	...	0
Out (DSP)	3.142	2.967	...	0
Exp. Out (DSP)	3.142	2.967	...	0

Test settings	
Tolerance Out	±2,7940e-07 (±600 LSB)

Test statistics	
Min CPU cycles	333
Max CPU cycles	776
Avg CPU cycles	710

Verification: Acos Float32 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test — OK

Inport test for Math block Acos.

Test results				
Time step	1	2	...	133
CPU cycles	2060	3858	...	1940
Inputs				
In (DSP)	-1	-0.985	...	1
In	-1	-0.985	...	1
Outputs				
Out	3.142	2.967	...	0
Exp. Out	3.142	2.967	...	0
Out (DSP)	3.142	2.967	...	0
Exp. Out (DSP)	3.142	2.967	...	0

Test settings	
Tolerance Out	±2,7940e-07 (±600 LSB)

Test statistics	
Min CPU cycles	443
Max CPU cycles	3858
Avg CPU cycles	3088

Verification: Acos Float32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for Math block Acos.

Test results				
Time step	1	2	...	133
CPU cycles	235	601	...	181
Inputs				
In (DSP)	-1	-0.985	...	1
In	-1	-0.985	...	1
Outputs				
Out	3.142	2.967	...	0
Exp. Out	3.142	2.967	...	0
Out (DSP)	3.142	2.967	...	0
Exp. Out (DSP)	3.142	2.967	...	0

Test settings	
Tolerance Out	±2,7940e-07 (±600 LSB)

Test statistics	
Min CPU cycles	175
Max CPU cycles	601
Avg CPU cycles	412

Verification: Acos Float32 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for Math block Acos.

Test results				
Time step	1	2	...	133
CPU cycles	127	467	...	117
Inputs				
In (DSP)	-1	-0.985	...	1
In	-1	-0.985	...	1
Outputs				
Out	3.142	2.967	...	0
Exp. Out	3.142	2.967	...	0
Out (DSP)	3.142	2.967	...	0
Exp. Out (DSP)	3.142	2.967	...	0

Test settings	
Tolerance Out	±2,7940e-07 (±600 LSB)

Test statistics	
Min CPU cycles	117
Max CPU cycles	719
Avg CPU cycles	480

Block: Add



Addition of input 1 and input 2.

Inports	
In1	Addend 1
In2	Addend 2

Outports	
Out	Sum

Description:

Calculation:

$$\mathrm{Out} = \mathrm{In}_1 + \mathrm{In}_2$$

Implementations:

FiP8	8 Bit Fixed Point Implementation
FiP16	16 Bit Fixed Point Implementation
FiP32	32 Bit Fixed Point Implementation
Float32	32 Bit Floating Point Implementation
Float64	64 Bit Floating Point Implementation

Implementation: FiP8

8 Bit Fixed Point Implementation

Inports Data Type	
In1	int8
In2	int8

Outports Data Type	
Out	int8

Implementation: FiP16

16 Bit Fixed Point Implementation

Inports Data Type	
In1	int16
In2	int16

Outports Data Type	
Out	int16

Implementation: FiP32

32 Bit Fixed Point Implementation

Inports Data Type	
In1	int32
In2	int32

Outports Data Type	
Out	int32

Implementation: Float32

32 Bit Floating Point Implementation

Inports Data Type	
In1	float32
In2	float32

Outports Data Type	
Out	float32

Implementation: Float64

64 Bit Floating Point Implementation

Inports Data Type	
In1	float64
In2	float64

Outports Data Type	
Out	float64

Verification: Add FiP16 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for Math block Add.

Test results						
Time step	1	2	3	4	...	214
CPU cycles	68	68	68	68	...	65
Inputs						
In1 (DSP)	-32768	-32150	-31531	-30913	...	32767
In2 (DSP)	32767	32150	31531	30913	...	32767
In1	-1	-0.981	-0.962	-0.943	...	1
In2	1	0.981	0.962	0.943	...	1
Outputs						
Out	-0	0	0	0	...	1
Exp. Out	0	0	0	0	...	1
Out (DSP)	-1	0	0	0	...	32767
Exp. Out (DSP)	0	0	0	0	...	32767

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	65
Max CPU cycles	68
Avg CPU cycles	67

Verification: Add FiP16 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for Math block Add.

Test results						
Time step	1	2	3	4	...	214
CPU cycles	37	37	37	37	...	31
Inputs						
In1 (DSP)	-32768	-32150	-31531	-30913	...	32767
In2 (DSP)	32767	32150	31531	30913	...	32767
In1	-1	-0.981	-0.962	-0.943	...	1
In2	1	0.981	0.962	0.943	...	1
Outputs						
Out	-0	0	0	0	...	1
Exp. Out	0	0	0	0	...	1
Out (DSP)	-1	0	0	0	...	32767
Exp. Out (DSP)	0	0	0	0	...	32767

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	31
Max CPU cycles	37
Avg CPU cycles	36

Verification: Add FiP16 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for Math block Add.

Test results						
Time step	1	2	3	4	...	214
CPU cycles	81	81	81	81	...	81
Inputs						
In1 (DSP)	-32768	-32150	-31531	-30913	...	32767
In2 (DSP)	32767	32150	31531	30913	...	32767
In1	-1	-0.981	-0.962	-0.943	...	1
In2	1	0.981	0.962	0.943	...	1
Outputs						
Out	-0	0	0	0	...	1
Exp. Out	0	0	0	0	...	1
Out (DSP)	-1	0	0	0	...	32767
Exp. Out (DSP)	0	0	0	0	...	32767

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	81
Max CPU cycles	81
Avg CPU cycles	81

Verification: Add FiP16 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for Math block Add.

Test results						
Time step	1	2	3	4	...	214
CPU cycles	66	66	66	66	...	67
Inputs						
In1 (DSP)	-32768	-32150	-31531	-30913	...	32767
In2 (DSP)	32767	32150	31531	30913	...	32767
In1	-1	-0.981	-0.962	-0.943	...	1
In2	1	0.981	0.962	0.943	...	1
Outputs						
Out	-0	0	0	0	...	1
Exp. Out	0	0	0	0	...	1
Out (DSP)	-1	0	0	0	...	32767
Exp. Out (DSP)	0	0	0	0	...	32767

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	65
Max CPU cycles	126
Avg CPU cycles	66

Verification: Add FiP16 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for Math block Add.

Test results						
Time step	1	2	3	4	...	214
CPU cycles	39	39	39	39	...	39
Inputs						
In1 (DSP)	-32768	-32150	-31531	-30913	...	32767
In2 (DSP)	32767	32150	31531	30913	...	32767
In1	-1	-0.981	-0.962	-0.943	...	1
In2	1	0.981	0.962	0.943	...	1
Outputs						
Out	-0	0	0	0	...	1
Exp. Out	0	0	0	0	...	1
Out (DSP)	-1	0	0	0	...	32767
Exp. Out (DSP)	0	0	0	0	...	32767

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	39
Max CPU cycles	39
Avg CPU cycles	39

Verification: Add FiP16 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for Math block Add.

Test results						
Time step	1	2	3	4	...	214
CPU cycles	59	59	59	59	...	58
Inputs						
In1 (DSP)	-32768	-32150	-31531	-30913	...	32767
In2 (DSP)	32767	32150	31531	30913	...	32767
In1	-1	-0.981	-0.962	-0.943	...	1
In2	1	0.981	0.962	0.943	...	1
Outputs						
Out	-0	0	0	0	...	1
Exp. Out	0	0	0	0	...	1
Out (DSP)	-1	0	0	0	...	32767
Exp. Out (DSP)	0	0	0	0	...	32767

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	58
Max CPU cycles	59
Avg CPU cycles	58

Verification: Add FiP16 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for Math block Add.

Test results						
Time step	1	2	3	4	...	214
CPU cycles	76	69	69	69	...	69
Inputs						
In1 (DSP)	-32768	-32150	-31531	-30913	...	32767
In2 (DSP)	32767	32150	31531	30913	...	32767
In1	-1	-0.981	-0.962	-0.943	...	1
In2	1	0.981	0.962	0.943	...	1
Outputs						
Out	-0	0	0	0	...	1
Exp. Out	0	0	0	0	...	1
Out (DSP)	-1	0	0	0	...	32767
Exp. Out (DSP)	0	0	0	0	...	32767

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	69
Max CPU cycles	76
Avg CPU cycles	69

Verification: Add FiP16 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for Math block Add.

Test results						
Time step	1	2	3	4	...	214
CPU cycles	69	69	69	69	...	63
Inputs						
In1 (DSP)	-32768	-32150	-31531	-30913	...	32767
In2 (DSP)	32767	32150	31531	30913	...	32767
In1	-1	-0.981	-0.962	-0.943	...	1
In2	1	0.981	0.962	0.943	...	1
Outputs						
Out	-0	0	0	0	...	1
Exp. Out	0	0	0	0	...	1
Out (DSP)	-1	0	0	0	...	32767
Exp. Out (DSP)	0	0	0	0	...	32767

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	63
Max CPU cycles	69
Avg CPU cycles	68

Verification: Add FiP32 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for Math block Add.

Test results				
Time step	1	2	...	214
CPU cycles	159	159	...	112
Inputs				
In1 (DSP)	-2147483648	-2106965089	...	2147483647
In2 (DSP)	2147483647	2106965089	...	2147483647
In1	-1	-0.981	...	1
In2	1	0.981	...	1
Outputs				
Out	-0	0	...	1
Exp. Out	0	0	...	1
Out (DSP)	-1	0	...	2147483647
Exp. Out (DSP)	0	0	...	2147483647

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	112
Max CPU cycles	165
Avg CPU cycles	153

Verification: Add FiP32 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for Math block Add.

Test results				
Time step	1	2	...	214
CPU cycles	57	57	...	51
Inputs				
In1 (DSP)	-2147483648	-2106965089	...	2147483647
In2 (DSP)	2147483647	2106965089	...	2147483647
In1	-1	-0.981	...	1
In2	1	0.981	...	1
Outputs				
Out	-0	0	...	1
Exp. Out	0	0	...	1
Out (DSP)	-1	0	...	2147483647
Exp. Out (DSP)	0	0	...	2147483647

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	51
Max CPU cycles	61
Avg CPU cycles	56

Verification: Add FiP32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for Math block Add.

Test results				
Time step	1	2	...	214
CPU cycles	91	91	...	91
Inputs				
In1 (DSP)	-2147483648	-2106965089	...	2147483647
In2 (DSP)	2147483647	2106965089	...	2147483647
In1	-1	-0.981	...	1
In2	1	0.981	...	1
Outputs				
Out	-0	0	...	1
Exp. Out	0	0	...	1
Out (DSP)	-1	0	...	2147483647
Exp. Out (DSP)	0	0	...	2147483647

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	91
Max CPU cycles	153
Avg CPU cycles	91

Verification: Add FiP32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for Math block Add.

Test results				
Time step	1	2	...	214
CPU cycles	87	81	...	86
Inputs				
In1 (DSP)	-2147483648	-2106965089	...	2147483647
In2 (DSP)	2147483647	2106965089	...	2147483647
In1	-1	-0.981	...	1
In2	1	0.981	...	1
Outputs				
Out	-0	0	...	1
Exp. Out	0	0	...	1
Out (DSP)	-1	0	...	2147483647
Exp. Out (DSP)	0	0	...	2147483647

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	81
Max CPU cycles	141
Avg CPU cycles	82

Verification: Add FiP32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for Math block Add.

Test results				
Time step	1	2	...	214
CPU cycles	49	48	...	49
Inputs				
In1 (DSP)	-2147483648	-2106965089	...	2147483647
In2 (DSP)	2147483647	2106965089	...	2147483647
In1	-1	-0.981	...	1
In2	1	0.981	...	1
Outputs				
Out	-0	0	...	1
Exp. Out	0	0	...	1
Out (DSP)	-1	0	...	2147483647
Exp. Out (DSP)	0	0	...	2147483647

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	48
Max CPU cycles	51
Avg CPU cycles	48

Verification: Add FiP32 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for Math block Add.

Test results				
Time step	1	2	...	214
CPU cycles	81	81	...	82
Inputs				
In1 (DSP)	-2147483648	-2106965089	...	2147483647
In2 (DSP)	2147483647	2106965089	...	2147483647
In1	-1	-0.981	...	1
In2	1	0.981	...	1
Outputs				
Out	-0	0	...	1
Exp. Out	0	0	...	1
Out (DSP)	-1	0	...	2147483647
Exp. Out (DSP)	0	0	...	2147483647

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	81
Max CPU cycles	82
Avg CPU cycles	81

Verification: Add FiP32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for Math block Add.

Test results				
Time step	1	2	...	214
CPU cycles	86	87	...	87
Inputs				
In1 (DSP)	-2147483648	-2106965089	...	2147483647
In2 (DSP)	2147483647	2106965089	...	2147483647
In1	-1	-0.981	...	1
In2	1	0.981	...	1
Outputs				
Out	-0	0	...	1
Exp. Out	0	0	...	1
Out (DSP)	-1	0	...	2147483647
Exp. Out (DSP)	0	0	...	2147483647

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	86
Max CPU cycles	87
Avg CPU cycles	86

Verification: Add FiP32 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for Math block Add.

Test results				
Time step	1	2	...	214
CPU cycles	152	152	...	106
Inputs				
In1 (DSP)	-2147483648	-2106965089	...	2147483647
In2 (DSP)	2147483647	2106965089	...	2147483647
In1	-1	-0.981	...	1
In2	1	0.981	...	1
Outputs				
Out	-0	0	...	1
Exp. Out	0	0	...	1
Out (DSP)	-1	0	...	2147483647
Exp. Out (DSP)	0	0	...	2147483647

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	106
Max CPU cycles	154
Avg CPU cycles	146

Verification: Add Float32 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for Math block Add.

Test results				
Time step	1	2	...	214
CPU cycles	53	53	...	53
Inputs				
In1 (DSP)	-2	-1.962	...	2
In2 (DSP)	2	1.962	...	2
In1	-2	-1.962	...	2
In2	2	1.962	...	2
Outputs				
Out	0	0	...	4
Exp. Out	0	0	...	4
Out (DSP)	0	0	...	4
Exp. Out (DSP)	0	0	...	4

Test settings	
Tolerance Out	±5,1223e-07 (±1100 LSB)

Test statistics	
Min CPU cycles	53
Max CPU cycles	53
Avg CPU cycles	53

Verification: Add Float32 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for Math block Add.

Test results				
Time step	1	2	...	214
CPU cycles	29	29	...	29
Inputs				
In1 (DSP)	-2	-1.962	...	2
In2 (DSP)	2	1.962	...	2
In1	-2	-1.962	...	2
In2	2	1.962	...	2
Outputs				
Out	0	0	...	4
Exp. Out	0	0	...	4
Out (DSP)	0	0	...	4
Exp. Out (DSP)	0	0	...	4

Test settings	
Tolerance Out	±5,1223e-07 (±1100 LSB)

Test statistics	
Min CPU cycles	29
Max CPU cycles	29
Avg CPU cycles	29

Verification: Add Float32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for Math block Add.

Test results				
Time step	1	2	...	214
CPU cycles	66	66	...	66
Inputs				
In1 (DSP)	-2	-1.962	...	2
In2 (DSP)	2	1.962	...	2
In1	-2	-1.962	...	2
In2	2	1.962	...	2
Outputs				
Out	0	0	...	4
Exp. Out	0	0	...	4
Out (DSP)	0	0	...	4
Exp. Out (DSP)	0	0	...	4

Test settings	
Tolerance Out	±5,1223e-07 (±1100 LSB)

Test statistics	
Min CPU cycles	66
Max CPU cycles	66
Avg CPU cycles	66

Verification: Add Float32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for Math block Add.

Test results				
Time step	1	2	...	214
CPU cycles	144	144	...	147
Inputs				
In1 (DSP)	-2	-1.962	...	2
In2 (DSP)	2	1.962	...	2
In1	-2	-1.962	...	2
In2	2	1.962	...	2
Outputs				
Out	0	0	...	4
Exp. Out	0	0	...	4
Out (DSP)	0	0	...	4
Exp. Out (DSP)	0	0	...	4

Test settings	
Tolerance Out	±5,1223e-07 (±1100 LSB)

Test statistics	
Min CPU cycles	144
Max CPU cycles	147
Avg CPU cycles	145

Verification: Add Float32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for Math block Add.

Test results				
Time step	1	2	...	214
CPU cycles	86	86	...	102
Inputs				
In1 (DSP)	-2	-1.962	...	2
In2 (DSP)	2	1.962	...	2
In1	-2	-1.962	...	2
In2	2	1.962	...	2
Outputs				
Out	0	0	...	4
Exp. Out	0	0	...	4
Out (DSP)	0	0	...	4
Exp. Out (DSP)	0	0	...	4

Test settings	
Tolerance Out	±5,1223e-07 (±1100 LSB)

Test statistics	
Min CPU cycles	72
Max CPU cycles	102
Avg CPU cycles	93

Verification: Add Float32 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for Math block Add.

Test results				
Time step	1	2	...	214
CPU cycles	240	240	...	203
Inputs				
In1 (DSP)	-2	-1.962	...	2
In2 (DSP)	2	1.962	...	2
In1	-2	-1.962	...	2
In2	2	1.962	...	2
Outputs				
Out	0	0	...	4
Exp. Out	0	0	...	4
Out (DSP)	0	0	...	4
Exp. Out (DSP)	0	0	...	4

Test settings	
Tolerance Out	±5,1223e-07 (±1100 LSB)

Test statistics	
Min CPU cycles	203
Max CPU cycles	240
Avg CPU cycles	221

Verification: Add Float32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for Math block Add.

Test results				
Time step	1	2	...	214
CPU cycles	68	57	...	57
Inputs				
In1 (DSP)	-2	-1.962	...	2
In2 (DSP)	2	1.962	...	2
In1	-2	-1.962	...	2
In2	2	1.962	...	2
Outputs				
Out	0	0	...	4
Exp. Out	0	0	...	4
Out (DSP)	0	0	...	4
Exp. Out (DSP)	0	0	...	4

Test settings	
Tolerance Out	±5,1223e-07 (±1100 LSB)

Test statistics	
Min CPU cycles	57
Max CPU cycles	68
Avg CPU cycles	57

Verification: Add Float32 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for Math block Add.

Test results				
Time step	1	2	...	214
CPU cycles	47	47	...	47
Inputs				
In1 (DSP)	-2	-1.962	...	2
In2 (DSP)	2	1.962	...	2
In1	-2	-1.962	...	2
In2	2	1.962	...	2
Outputs				
Out	0	0	...	4
Exp. Out	0	0	...	4
Out (DSP)	0	0	...	4
Exp. Out (DSP)	0	0	...	4

Test settings	
Tolerance Out	±5,1223e-07 (±1100 LSB)

Test statistics	
Min CPU cycles	47
Max CPU cycles	47
Avg CPU cycles	47

Block: Asin



Arcsine computation of input value.

Inports	
In	Input u

Outports	
Out	Result of sin(u)

Description:

Calculation:

$$\mathrm{Out} = \arcsin\left(\mathrm{In}\right)$$

Implementations:

FiP8	8 Bit Fixed Point Implementation
FiP16	16 Bit Fixed Point Implementation
FiP32	32 Bit Fixed Point Implementation
Float32	32 Bit Floating Point Implementation
Float64	64 Bit Floating Point Implementation

Implementation: FiP8

8 Bit Fixed Point Implementation

Inports Data Type	
In	int8

Outports Data Type	
Out	int8

Implementation: FiP16

16 Bit Fixed Point Implementation

Inports Data Type	
In	int16

Outports Data Type	
Out	int16

Implementation: FiP32

32 Bit Fixed Point Implementation

Inports Data Type	
In	int32

Outports Data Type	
Out	int32

Implementation: Float32

32 Bit Floating Point Implementation

Inports Data Type	
In	float32

Outports Data Type	
Out	float32

Implementation: Float64

64 Bit Floating Point Implementation

Inports Data Type	
In	float64

Outports Data Type	
Out	float64

Verification: Asin FiP16 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for Math block Asin.

Test results						
Time step	1	2	3	4	...	133
CPU cycles	98	97	97	97	...	86
Inputs						
In (DSP)	-32768	-32272	-31775	-31279	...	32767
In	-1	-0.985	-0.97	-0.955	...	1
Outputs						
Out	-0.5	-0.445	-0.421	-0.404	...	0.5
Exp. Out	-0.5	-0.445	-0.421	-0.404	...	0.5
Out (DSP)	-16376	-14569	-13810	-13228	...	16376
Exp. Out (DSP)	-16384	-14566	-13810	-13227	...	16384

Test settings	
Tolerance Out	±2,4414e-04 (±8 LSB)

Test statistics	
Min CPU cycles	86
Max CPU cycles	98
Avg CPU cycles	91

Verification: Asin FiP16 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test — OK

Inport test for Math block Asin.

Test results						
Time step	1	2	3	4	...	133
CPU cycles	65	65	65	65	...	65
Inputs						
In (DSP)	-32768	-32272	-31775	-31279	...	32767
In	-1	-0.985	-0.97	-0.955	...	1
Outputs						
Out	-0.5	-0.445	-0.421	-0.404	...	0.5
Exp. Out	-0.5	-0.445	-0.421	-0.404	...	0.5
Out (DSP)	-16376	-14569	-13810	-13228	...	16376
Exp. Out (DSP)	-16384	-14566	-13810	-13227	...	16384

Test settings	
Tolerance Out	±2,4414e-04 (±8 LSB)

Test statistics	
Min CPU cycles	65
Max CPU cycles	65
Avg CPU cycles	65

Verification: Asin FiP16 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for Math block Asin.

Test results						
Time step	1	2	3	4	...	133
CPU cycles	130	107	107	107	...	101
Inputs						
In (DSP)	-32768	-32272	-31775	-31279	...	32767
In	-1	-0.985	-0.97	-0.955	...	1
Outputs						
Out	-0.5	-0.445	-0.421	-0.404	...	0.5
Exp. Out	-0.5	-0.445	-0.421	-0.404	...	0.5
Out (DSP)	-16376	-14569	-13810	-13228	...	16376
Exp. Out (DSP)	-16384	-14566	-13810	-13227	...	16384

Test settings	
Tolerance Out	±2,4414e-04 (±8 LSB)

Test statistics	
Min CPU cycles	96
Max CPU cycles	130
Avg CPU cycles	102

Verification: Asin FiP16 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for Math block Asin.

Test results						
Time step	1	2	3	4	...	133
CPU cycles	102	97	97	97	...	80
Inputs						
In (DSP)	-32768	-32272	-31775	-31279	...	32767
In	-1	-0.985	-0.97	-0.955	...	1
Outputs						
Out	-0.5	-0.445	-0.421	-0.404	...	0.5
Exp. Out	-0.5	-0.445	-0.421	-0.404	...	0.5
Out (DSP)	-16376	-14569	-13810	-13228	...	16376
Exp. Out (DSP)	-16384	-14566	-13810	-13227	...	16384

Test settings	
Tolerance Out	±2,4414e-04 (±8 LSB)

Test statistics	
Min CPU cycles	80
Max CPU cycles	102
Avg CPU cycles	88

Verification: Asin FiP16 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for Math block Asin.

Test results						
Time step	1	2	3	4	...	133
CPU cycles	52	55	55	55	...	51
Inputs						
In (DSP)	-32768	-32272	-31775	-31279	...	32767
In	-1	-0.985	-0.97	-0.955	...	1
Outputs						
Out	-0.5	-0.445	-0.421	-0.404	...	0.5
Exp. Out	-0.5	-0.445	-0.421	-0.404	...	0.5
Out (DSP)	-16376	-14569	-13810	-13228	...	16376
Exp. Out (DSP)	-16384	-14566	-13810	-13227	...	16384

Test settings	
Tolerance Out	±2,4414e-04 (±8 LSB)

Test statistics	
Min CPU cycles	51
Max CPU cycles	55
Avg CPU cycles	52

Verification: Asin FiP16 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test — OK

Inport test for Math block Asin.

Test results						
Time step	1	2	3	4	...	133
CPU cycles	71	70	70	70	...	69
Inputs						
In (DSP)	-32768	-32272	-31775	-31279	...	32767
In	-1	-0.985	-0.97	-0.955	...	1
Outputs						
Out	-0.5	-0.445	-0.421	-0.404	...	0.5
Exp. Out	-0.5	-0.445	-0.421	-0.404	...	0.5
Out (DSP)	-16376	-14569	-13810	-13228	...	16376
Exp. Out (DSP)	-16384	-14566	-13810	-13227	...	16384

Test settings	
Tolerance Out	±2,4414e-04 (±8 LSB)

Test statistics	
Min CPU cycles	69
Max CPU cycles	71
Avg CPU cycles	69

Verification: Asin FiP16 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test — OK

Inport test for Math block Asin.

Test results						
Time step	1	2	3	4	...	133
CPU cycles	121	101	101	101	...	95
Inputs						
In (DSP)	-32768	-32272	-31775	-31279	...	32767
In	-1	-0.985	-0.97	-0.955	...	1
Outputs						
Out	-0.5	-0.445	-0.421	-0.404	...	0.5
Exp. Out	-0.5	-0.445	-0.421	-0.404	...	0.5
Out (DSP)	-16376	-14569	-13810	-13228	...	16376
Exp. Out (DSP)	-16384	-14566	-13810	-13227	...	16384

Test settings	
Tolerance Out	±2,4414e-04 (±8 LSB)

Test statistics	
Min CPU cycles	93
Max CPU cycles	121
Avg CPU cycles	97

Verification: Asin FiP16 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for Math block Asin.

Test results						
Time step	1	2	3	4	...	133
CPU cycles	97	95	92	95	...	76
Inputs						
In (DSP)	-32768	-32272	-31775	-31279	...	32767
In	-1	-0.985	-0.97	-0.955	...	1
Outputs						
Out	-0.5	-0.445	-0.421	-0.404	...	0.5
Exp. Out	-0.5	-0.445	-0.421	-0.404	...	0.5
Out (DSP)	-16376	-14569	-13810	-13228	...	16376
Exp. Out (DSP)	-16384	-14566	-13810	-13227	...	16384

Test settings	
Tolerance Out	±2,4414e-04 (±8 LSB)

Test statistics	
Min CPU cycles	76
Max CPU cycles	97
Avg CPU cycles	84

Verification: Asin FiP32 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for Math block Asin.

Test results				
Time step	1	2	...	133
CPU cycles	112	112	...	98
Inputs				
In (DSP)	-2147483648	-2114946017	...	2147483647
In	-1	-0.985	...	1
Outputs				
Out	-0.5	-0.445	...	0.5
Exp. Out	-0.5	-0.445	...	0.5
Out (DSP)	-1073741816	-954714571	...	1073741816
Exp. Out (DSP)	-1073741824	-954597624	...	1073741824

Test settings	
Tolerance Out	±9,3132e-05 (±200000 LSB)

Test statistics	
Min CPU cycles	98
Max CPU cycles	112
Avg CPU cycles	104

Verification: Asin FiP32 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for Math block Asin.

Test results				
Time step	1	2	...	133
CPU cycles	61	61	...	57
Inputs				
In (DSP)	-2147483648	-2114946017	...	2147483647
In	-1	-0.985	...	1
Outputs				
Out	-0.5	-0.445	...	0.5
Exp. Out	-0.5	-0.445	...	0.5
Out (DSP)	-1073741816	-954714571	...	1073741816
Exp. Out (DSP)	-1073741824	-954597624	...	1073741824

Test settings	
Tolerance Out	±9,3132e-05 (±200000 LSB)

Test statistics	
Min CPU cycles	57
Max CPU cycles	61
Avg CPU cycles	58

Verification: Asin FiP32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for Math block Asin.

Test results				
Time step	1	2	...	133
CPU cycles	139	130	...	96
Inputs				
In (DSP)	-2147483648	-2114946017	...	2147483647
In	-1	-0.985	...	1
Outputs				
Out	-0.5	-0.445	...	0.5
Exp. Out	-0.5	-0.445	...	0.5
Out (DSP)	-1073741816	-954714571	...	1073741816
Exp. Out (DSP)	-1073741824	-954597624	...	1073741824

Test settings	
Tolerance Out	±9,3132e-05 (±200000 LSB)

Test statistics	
Min CPU cycles	96
Max CPU cycles	139
Avg CPU cycles	113

Verification: Asin FiP32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for Math block Asin.

Test results				
Time step	1	2	...	133
CPU cycles	171	163	...	148
Inputs				
In (DSP)	-2147483648	-2114946017	...	2147483647
In	-1	-0.985	...	1
Outputs				
Out	-0.5	-0.445	...	0.5
Exp. Out	-0.5	-0.445	...	0.5
Out (DSP)	-1073741816	-954714571	...	1073741816
Exp. Out (DSP)	-1073741824	-954597624	...	1073741824

Test settings	
Tolerance Out	±9,3132e-05 (±200000 LSB)

Test statistics	
Min CPU cycles	148
Max CPU cycles	171
Avg CPU cycles	155

Verification: Asin FiP32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for Math block Asin.

Test results				
Time step	1	2	...	133
CPU cycles	64	66	...	54
Inputs				
In (DSP)	-2147483648	-2114946017	...	2147483647
In	-1	-0.985	...	1
Outputs				
Out	-0.5	-0.445	...	0.5
Exp. Out	-0.5	-0.445	...	0.5
Out (DSP)	-1073741816	-954714571	...	1073741816
Exp. Out (DSP)	-1073741824	-954597624	...	1073741824

Test settings	
Tolerance Out	±9,3132e-05 (±200000 LSB)

Test statistics	
Min CPU cycles	53
Max CPU cycles	66
Avg CPU cycles	59

Verification: Asin FiP32 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test — OK

Inport test for Math block Asin.

Test results				
Time step	1	2	...	133
CPU cycles	212	214	...	206
Inputs				
In (DSP)	-2147483648	-2114946017	...	2147483647
In	-1	-0.985	...	1
Outputs				
Out	-0.5	-0.445	...	0.5
Exp. Out	-0.5	-0.445	...	0.5
Out (DSP)	-1073741816	-954714571	...	1073741816
Exp. Out (DSP)	-1073741824	-954597624	...	1073741824

Test settings	
Tolerance Out	±9,3132e-05 (±200000 LSB)

Test statistics	
Min CPU cycles	206
Max CPU cycles	214
Avg CPU cycles	209

Verification: Asin FiP32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test — OK

Inport test for Math block Asin.

Test results				
Time step	1	2	...	133
CPU cycles	110	108	...	100
Inputs				
In (DSP)	-2147483648	-2114946017	...	2147483647
In	-1	-0.985	...	1
Outputs				
Out	-0.5	-0.445	...	0.5
Exp. Out	-0.5	-0.445	...	0.5
Out (DSP)	-1073741816	-954714571	...	1073741816
Exp. Out (DSP)	-1073741824	-954597624	...	1073741824

Test settings	
Tolerance Out	±9,3132e-05 (±200000 LSB)

Test statistics	
Min CPU cycles	100
Max CPU cycles	111
Avg CPU cycles	104

Verification: Asin FiP32 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for Math block Asin.

Test results				
Time step	1	2	...	133
CPU cycles	110	115	...	91
Inputs				
In (DSP)	-2147483648	-2114946017	...	2147483647
In	-1	-0.985	...	1
Outputs				
Out	-0.5	-0.445	...	0.5
Exp. Out	-0.5	-0.445	...	0.5
Out (DSP)	-1073741816	-954714571	...	1073741816
Exp. Out (DSP)	-1073741824	-954597624	...	1073741824

Test settings	
Tolerance Out	±9,3132e-05 (±200000 LSB)

Test statistics	
Min CPU cycles	91
Max CPU cycles	118
Avg CPU cycles	103

Verification: Asin Float32 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for Math block Asin.

Test results				
Time step	1	2	...	133
CPU cycles	549	5130	...	549
Inputs				
In (DSP)	-1	-0.985	...	1
In	-1	-0.985	...	1
Outputs				
Out	-1.571	-1.396	...	1.571
Exp. Out	-1.571	-1.396	...	1.571
Out (DSP)	-1.571	-1.396	...	1.571
Exp. Out (DSP)	-1.571	-1.396	...	1.571

Test settings	
Tolerance Out	±2,7940e-07 (±600 LSB)

Test statistics	
Min CPU cycles	180
Max CPU cycles	5190
Avg CPU cycles	2794

Verification: Asin Float32 CPU TM4C123GH6

Date of Test 2026-06-19

Target controller TM4C123GH6

Test case: Inport test OK

Inport test for Math block Asin.

Test results				
Time step	1	2	...	133
CPU cycles	259	1957	...	259
Inputs				
In (DSP)	-1	-0.985	...	1
In	-1	-0.985	...	1
Outputs				
Out	-1.571	-1.396	...	1.571
Exp. Out	-1.571	-1.396	...	1.571
Out (DSP)	-1.571	-1.396	...	1.571
Exp. Out (DSP)	-1.571	-1.396	...	1.571

Test settings	
Tolerance Out	±2,7940e-07 (±600 LSB)

Test statistics	
Min CPU cycles	109
Max CPU cycles	2057
Avg CPU cycles	1055

Verification: Asin Float32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for Math block Asin.

Test results				
Time step	1	2	...	133
CPU cycles	214	387	...	214
Inputs				
In (DSP)	-1	-0.985	...	1
In	-1	-0.985	...	1
Outputs				
Out	-1.571	-1.396	...	1.571
Exp. Out	-1.571	-1.396	...	1.571
Out (DSP)	-1.571	-1.396	...	1.571
Exp. Out (DSP)	-1.571	-1.396	...	1.571

Test settings	
Tolerance Out	±2,7940e-07 (±600 LSB)

Test statistics	
Min CPU cycles	214
Max CPU cycles	446
Avg CPU cycles	383

Verification: Asin Float32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for Math block Asin.

Test results				
Time step	1	2	...	133
CPU cycles	717	5326	...	717
Inputs				
In (DSP)	-1	-0.985	...	1
In	-1	-0.985	...	1
Outputs				
Out	-1.571	-1.396	...	1.571
Exp. Out	-1.571	-1.396	...	1.571
Out (DSP)	-1.571	-1.396	...	1.571
Exp. Out (DSP)	-1.571	-1.396	...	1.571

Test settings	
Tolerance Out	±2,7940e-07 (±600 LSB)

Test statistics	
Min CPU cycles	430
Max CPU cycles	7053
Avg CPU cycles	5554

Verification: Asin Float32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for Math block Asin.

Test results				
Time step	1	2	...	133
CPU cycles	370	746	...	370
Inputs				
In (DSP)	-1	-0.985	...	1
In	-1	-0.985	...	1
Outputs				
Out	-1.571	-1.396	...	1.571
Exp. Out	-1.571	-1.396	...	1.571
Out (DSP)	-1.571	-1.396	...	1.571
Exp. Out (DSP)	-1.571	-1.396	...	1.571

Test settings	
Tolerance Out	±2,7940e-07 (±600 LSB)

Test statistics	
Min CPU cycles	370
Max CPU cycles	763
Avg CPU cycles	658

Verification: Asin Float32 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for Math block Asin.

Test results				
Time step	1	2	...	133
CPU cycles	2054	3838	...	2054
Inputs				
In (DSP)	-1	-0.985	...	1
In	-1	-0.985	...	1
Outputs				
Out	-1.571	-1.396	...	1.571
Exp. Out	-1.571	-1.396	...	1.571
Out (DSP)	-1.571	-1.396	...	1.571
Exp. Out (DSP)	-1.571	-1.396	...	1.571

Test settings	
Tolerance Out	±2,7940e-07 (±600 LSB)

Test statistics	
Min CPU cycles	321
Max CPU cycles	3838
Avg CPU cycles	3030

Verification: Asin Float32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for Math block Asin.

Test results				
Time step	1	2	...	133
CPU cycles	255	664	...	195
Inputs				
In (DSP)	-1	-0.985	...	1
In	-1	-0.985	...	1
Outputs				
Out	-1.571	-1.396	...	1.571
Exp. Out	-1.571	-1.396	...	1.571
Out (DSP)	-1.571	-1.396	...	1.571
Exp. Out (DSP)	-1.571	-1.396	...	1.571

Test settings	
Tolerance Out	±2,7940e-07 (±600 LSB)

Test statistics	
Min CPU cycles	191
Max CPU cycles	664
Avg CPU cycles	429

Verification: Asin Float32 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for Math block Asin.

Test results				
Time step	1	2	...	133
CPU cycles	402	6717	...	402
Inputs				
In (DSP)	-1	-0.985	...	1
In	-1	-0.985	...	1
Outputs				
Out	-1.571	-1.396	...	1.571
Exp. Out	-1.571	-1.396	...	1.571
Out (DSP)	-1.571	-1.396	...	1.571
Exp. Out (DSP)	-1.571	-1.396	...	1.571

Test settings	
Tolerance Out	±2,7940e-07 (±600 LSB)

Test statistics	
Min CPU cycles	139
Max CPU cycles	6799
Avg CPU cycles	3544

Block: Atan2



Computation of the angle between the inputs x and y.

Inports	
y	
x	

Outports	
Out	Result of atan2(y/x)

Description:

Calculation:

$$\text{Out} = \begin{cases} \arctan\left(\frac{y}{x}\right) & x > 0 \\ \arctan\left(\frac{y}{x}\right) + \pi & x < 0, y \geq 0 \\ \arctan\left(\frac{y}{x}\right) - \pi & x < 0, y < 0 \\ +\frac{\pi}{2} & x = 0, y > 0 \\ -\frac{\pi}{2} & x = 0, y < 0 \\ 0 & x = 0, y = 0 \end{cases}$$

Implementations:

FiP8	8 Bit Fixed Point Implementation
FiP16	16 Bit Fixed Point Implementation
FiP32	32 Bit Fixed Point Implementation
Float32	32 Bit Floating Point Implementation
Float64	64 Bit Floating Point Implementation

Implementation: FiP8

8 Bit Fixed Point Implementation

Inports Data Type	
y	int8
x	int8

Outports Data Type	
Out	int8

Implementation: FiP16

16 Bit Fixed Point Implementation

Inports Data Type	
y	int16
x	int16

Outports Data Type	
Out	int16

Implementation: FiP32

32 Bit Fixed Point Implementation

Inports Data Type	
y	int32
x	int32

Outports Data Type	
Out	int32

Implementation: Float32

32 Bit Floating Point Implementation

Inports Data Type	
y	float32
x	float32

Outports Data Type	
Out	float32

Implementation: Float64

64 Bit Floating Point Implementation

Inports Data Type	
y	float64
x	float64

Outports Data Type	
Out	float64

Verification: Atan2 FiP16 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for Math block Atan2.

Test results						
Time step	1	2	3	4	...	315
CPU cycles	88	223	221	216	...	218
Inputs						
y (DSP)	0	32767	-32768	0	...	2723
x (DSP)	0	0	0	32767	...	-32655
y	0	1	-1	0	...	0.083
x	0	0	0	1	...	-0.997
Outputs						
Out	0	0.5	-0.5	0	...	0.973
Exp. Out	0	0.5	-0.5	0	...	0.974
Out (DSP)	0	16383	-16385	0	...	31898
Exp. Out (DSP)	0	16384	-16384	0	...	31900

Test settings	
Tolerance Out	±7,6294e-04 (±25 LSB)

Test statistics	
Min CPU cycles	88
Max CPU cycles	234
Avg CPU cycles	201

Verification: Atan2 FiP16 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for Math block Atan2.

Test results						
Time step	1	2	3	4	...	315
CPU cycles	57	105	107	103	...	109
Inputs						
y (DSP)	0	32767	-32768	0	...	2723
x (DSP)	0	0	0	32767	...	-32655
y	0	1	-1	0	...	0.083
x	0	0	0	1	...	-0.997
Outputs						
Out	0	0.5	-0.5	0	...	0.973
Exp. Out	0	0.5	-0.5	0	...	0.974
Out (DSP)	0	16383	-16385	0	...	31898
Exp. Out (DSP)	0	16384	-16384	0	...	31900

Test settings	
Tolerance Out	±7,6294e-04 (±25 LSB)

Test statistics	
Min CPU cycles	57
Max CPU cycles	121
Avg CPU cycles	105

Verification: Atan2 FiP16 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for Math block Atan2.

Test results						
Time step	1	2	3	4	...	315
CPU cycles	100	164	179	186	...	211
Inputs						
y (DSP)	0	32767	-32768	0	...	2723
x (DSP)	0	0	0	32767	...	-32655
y	0	1	-1	0	...	0.083
x	0	0	0	1	...	-0.997
Outputs						
Out	0	0.5	-0.5	0	...	0.973
Exp. Out	0	0.5	-0.5	0	...	0.974
Out (DSP)	0	16383	-16385	0	...	31898
Exp. Out (DSP)	0	16384	-16384	0	...	31900

Test settings	
Tolerance Out	±7,6294e-04 (±25 LSB)

Test statistics	
Min CPU cycles	100
Max CPU cycles	213
Avg CPU cycles	181

Verification: Atan2 FiP16 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for Math block Atan2.

Test results						
Time step	1	2	3	4	...	315
CPU cycles	94	161	177	168	...	284
Inputs						
y (DSP)	0	32767	-32768	0	...	2723
x (DSP)	0	0	0	32767	...	-32655
y	0	1	-1	0	...	0.083
x	0	0	0	1	...	-0.997
Outputs						
Out	0	0.5	-0.5	0	...	0.973
Exp. Out	0	0.5	-0.5	0	...	0.974
Out (DSP)	0	16383	-16385	0	...	31898
Exp. Out (DSP)	0	16384	-16384	0	...	31900

Test settings	
Tolerance Out	±7,6294e-04 (±25 LSB)

Test statistics	
Min CPU cycles	94
Max CPU cycles	328
Avg CPU cycles	228

Verification: Atan2 FiP16 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for Math block Atan2.

Test results						
Time step	1	2	3	4	...	315
CPU cycles	39	86	86	90	...	117
Inputs						
y (DSP)	0	32767	-32768	0	...	2723
x (DSP)	0	0	0	32767	...	-32655
y	0	1	-1	0	...	0.083
x	0	0	0	1	...	-0.997
Outputs						
Out	0	0.5	-0.5	0	...	0.973
Exp. Out	0	0.5	-0.5	0	...	0.974
Out (DSP)	0	16383	-16385	0	...	31898
Exp. Out (DSP)	0	16384	-16384	0	...	31900

Test settings	
Tolerance Out	±7,6294e-04 (±25 LSB)

Test statistics	
Min CPU cycles	39
Max CPU cycles	119
Avg CPU cycles	96

Verification: Atan2 FiP16 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for Math block Atan2.

Test results						
Time step	1	2	3	4	...	315
CPU cycles	62	134	132	123	...	143
Inputs						
y (DSP)	0	32767	-32768	0	...	2723
x (DSP)	0	0	0	32767	...	-32655
y	0	1	-1	0	...	0.083
x	0	0	0	1	...	-0.997
Outputs						
Out	0	0.5	-0.5	0	...	0.973
Exp. Out	0	0.5	-0.5	0	...	0.974
Out (DSP)	0	16383	-16385	0	...	31898
Exp. Out (DSP)	0	16384	-16384	0	...	31900

Test settings	
Tolerance Out	±7,6294e-04 (±25 LSB)

Test statistics	
Min CPU cycles	62
Max CPU cycles	150
Avg CPU cycles	124

Verification: Atan2 FiP16 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for Math block Atan2.

Test results						
Time step	1	2	3	4	...	315
CPU cycles	113	151	145	135	...	150
Inputs						
y (DSP)	0	32767	-32768	0	...	2723
x (DSP)	0	0	0	32767	...	-32655
y	0	1	-1	0	...	0.083
x	0	0	0	1	...	-0.997
Outputs						
Out	0	0.5	-0.5	0	...	0.973
Exp. Out	0	0.5	-0.5	0	...	0.974
Out (DSP)	0	16383	-16385	0	...	31898
Exp. Out (DSP)	0	16384	-16384	0	...	31900

Test settings	
Tolerance Out	±7,6294e-04 (±25 LSB)

Test statistics	
Min CPU cycles	83
Max CPU cycles	160
Avg CPU cycles	137

Verification: Atan2 FiP16 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for Math block Atan2.

Test results						
Time step	1	2	3	4	...	315
CPU cycles	86	215	215	214	...	211
Inputs						
y (DSP)	0	32767	-32768	0	...	2723
x (DSP)	0	0	0	32767	...	-32655
y	0	1	-1	0	...	0.083
x	0	0	0	1	...	-0.997
Outputs						
Out	0	0.5	-0.5	0	...	0.973
Exp. Out	0	0.5	-0.5	0	...	0.974
Out (DSP)	0	16383	-16385	0	...	31898
Exp. Out (DSP)	0	16384	-16384	0	...	31900

Test settings	
Tolerance Out	±7,6294e-04 (±25 LSB)

Test statistics	
Min CPU cycles	86
Max CPU cycles	240
Avg CPU cycles	198

Verification: Atan2 FiP32 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for Math block Atan2.

Test results				
Time step	1	2	...	315
CPU cycles	99	303	...	411
Inputs				
y (DSP)	0	2147483647	...	178433134
x (DSP)	0	0	...	-2140057858
y	0	1	...	0.083
x	0	0	...	-0.997
Outputs				
Out	0	0.5	...	0.973
Exp. Out	0	0.5	...	0.974
Out (DSP)	0	1073741823	...	2090479220
Exp. Out (DSP)	0	1073741824	...	2090621061

Test settings	
Tolerance Out	±6,5193e-04 (±1400000 LSB)

Test statistics	
Min CPU cycles	99
Max CPU cycles	420
Avg CPU cycles	336

Verification: Atan2 FiP32 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for Math block Atan2.

Test results				
Time step	1	2	...	315
CPU cycles	59	217	...	577
Inputs				
y (DSP)	0	2147483647	...	178433134
x (DSP)	0	0	...	-2140057858
y	0	1	...	0.083
x	0	0	...	-0.997
Outputs				
Out	0	0.5	...	0.973
Exp. Out	0	0.5	...	0.974
Out (DSP)	0	1073741823	...	2090479220
Exp. Out (DSP)	0	1073741824	...	2090621061

Test settings	
Tolerance Out	±6,5193e-04 (±1400000 LSB)

Test statistics	
Min CPU cycles	59
Max CPU cycles	645
Avg CPU cycles	447

Verification: Atan2 FiP32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for Math block Atan2.

Test results				
Time step	1	2	...	315
CPU cycles	98	335	...	376
Inputs				
y (DSP)	0	2147483647	...	178433134
x (DSP)	0	0	...	-2140057858
y	0	1	...	0.083
x	0	0	...	-0.997
Outputs				
Out	0	0.5	...	0.973
Exp. Out	0	0.5	...	0.974
Out (DSP)	0	1073741823	...	2090479220
Exp. Out (DSP)	0	1073741824	...	2090621061

Test settings	
Tolerance Out	±6,5193e-04 (±1400000 LSB)

Test statistics	
Min CPU cycles	98
Max CPU cycles	431
Avg CPU cycles	322

Verification: Atan2 FiP32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for Math block Atan2.

Test results				
Time step	1	2	...	315
CPU cycles	88	441	...	1101
Inputs				
y (DSP)	0	2147483647	...	178433134
x (DSP)	0	0	...	-2140057858
y	0	1	...	0.083
x	0	0	...	-0.997
Outputs				
Out	0	0.5	...	0.973
Exp. Out	0	0.5	...	0.974
Out (DSP)	0	1073741823	...	2090479220
Exp. Out (DSP)	0	1073741824	...	2090621061

Test settings	
Tolerance Out	±6,5193e-04 (±1400000 LSB)

Test statistics	
Min CPU cycles	88
Max CPU cycles	1229
Avg CPU cycles	797

Verification: Atan2 FiP32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for Math block Atan2.

Test results				
Time step	1	2	...	315
CPU cycles	59	167	...	221
Inputs				
y (DSP)	0	2147483647	...	178433134
x (DSP)	0	0	...	-2140057858
y	0	1	...	0.083
x	0	0	...	-0.997
Outputs				
Out	0	0.5	...	0.973
Exp. Out	0	0.5	...	0.974
Out (DSP)	0	1073741823	...	2090479220
Exp. Out (DSP)	0	1073741824	...	2090621061

Test settings	
Tolerance Out	±6,5193e-04 (±1400000 LSB)

Test statistics	
Min CPU cycles	59
Max CPU cycles	236
Avg CPU cycles	181

Verification: Atan2 FiP32 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test — OK

Inport test for Math block Atan2.

Test results				
Time step	1	2	...	315
CPU cycles	85	9391	...	9931
Inputs				
y (DSP)	0	2147483647	...	178433134
x (DSP)	0	0	...	-2140057858
y	0	1	...	0.083
x	0	0	...	-0.997
Outputs				
Out	0	0.5	...	0.973
Exp. Out	0	0.5	...	0.974
Out (DSP)	0	1073741823	...	2090479220
Exp. Out (DSP)	0	1073741824	...	2090621061

Test settings	
Tolerance Out	±6,5193e-04 (±1400000 LSB)

Test statistics	
Min CPU cycles	85
Max CPU cycles	10093
Avg CPU cycles	7695

Verification: Atan2 FiP32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for Math block Atan2.

Test results				
Time step	1	2	...	315
CPU cycles	128	373	...	355
Inputs				
y (DSP)	0	2147483647	...	178433134
x (DSP)	0	0	...	-2140057858
y	0	1	...	0.083
x	0	0	...	-0.997
Outputs				
Out	0	0.5	...	0.973
Exp. Out	0	0.5	...	0.974
Out (DSP)	0	1073741823	...	2090479220
Exp. Out (DSP)	0	1073741824	...	2090621061

Test settings	
Tolerance Out	±6,5193e-04 (±1400000 LSB)

Test statistics	
Min CPU cycles	92
Max CPU cycles	378
Avg CPU cycles	298

Verification: Atan2 FiP32 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for Math block Atan2.

Test results				
Time step	1	2	...	315
CPU cycles	100	288	...	392
Inputs				
y (DSP)	0	2147483647	...	178433134
x (DSP)	0	0	...	-2140057858
y	0	1	...	0.083
x	0	0	...	-0.997
Outputs				
Out	0	0.5	...	0.973
Exp. Out	0	0.5	...	0.974
Out (DSP)	0	1073741823	...	2090479220
Exp. Out (DSP)	0	1073741824	...	2090621061

Test settings	
Tolerance Out	±6,5193e-04 (±1400000 LSB)

Test statistics	
Min CPU cycles	100
Max CPU cycles	412
Avg CPU cycles	323

Verification: Atan2 Float32 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for Math block Atan2.

Test results				
Time step	1	2	...	315
CPU cycles	187	220	...	818
Inputs				
y (DSP)	0	2	...	0.166
x (DSP)	0	0	...	-1.993
y	0	2	...	0.166
x	0	0	...	-1.993
Outputs				
Out	0	1.571	...	3.058
Exp. Out	0	1.571	...	3.058
Out (DSP)	0	1.571	...	3.058
Exp. Out (DSP)	0	1.571	...	3.058

Test settings	
Tolerance Out	±2,5611e-07 (±550 LSB)

Test statistics	
Min CPU cycles	187
Max CPU cycles	1172
Avg CPU cycles	899

Verification: Atan2 Float32 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for Math block Atan2.

Test results				
Time step	1	2	...	315
CPU cycles	93	101	...	235
Inputs				
y (DSP)	0	2	...	0.166
x (DSP)	0	0	...	-1.993
y	0	2	...	0.166
x	0	0	...	-1.993
Outputs				
Out	0	1.571	...	3.058
Exp. Out	0	1.571	...	3.058
Out (DSP)	0	1.571	...	3.058
Exp. Out (DSP)	0	1.571	...	3.058

Test settings	
Tolerance Out	±2,5611e-07 (±550 LSB)

Test statistics	
Min CPU cycles	93
Max CPU cycles	289
Avg CPU cycles	242

Verification: Atan2 Float32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for Math block Atan2.

Test results				
Time step	1	2	...	315
CPU cycles	157	176	...	433
Inputs				
y (DSP)	0	2	...	0.166
x (DSP)	0	0	...	-1.993
y	0	2	...	0.166
x	0	0	...	-1.993
Outputs				
Out	0	1.571	...	3.058
Exp. Out	0	1.571	...	3.058
Out (DSP)	0	1.571	...	3.058
Exp. Out (DSP)	0	1.571	...	3.058

Test settings	
Tolerance Out	±2,5611e-07 (±550 LSB)

Test statistics	
Min CPU cycles	157
Max CPU cycles	528
Avg CPU cycles	441

Verification: Atan2 Float32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for Math block Atan2.

Test results				
Time step	1	2	...	315
CPU cycles	135	145	...	5077
Inputs				
y (DSP)	0	2	...	0.166
x (DSP)	0	0	...	-1.993
y	0	2	...	0.166
x	0	0	...	-1.993
Outputs				
Out	0	1.571	...	3.058
Exp. Out	0	1.571	...	3.058
Out (DSP)	0	1.571	...	3.058
Exp. Out (DSP)	0	1.571	...	3.058

Test settings	
Tolerance Out	±2,5611e-07 (±550 LSB)

Test statistics	
Min CPU cycles	135
Max CPU cycles	6555
Avg CPU cycles	4608

Verification: Atan2 Float32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for Math block Atan2.

Test results				
Time step	1	2	...	315
CPU cycles	237	272	...	666
Inputs				
y (DSP)	0	2	...	0.166
x (DSP)	0	0	...	-1.993
y	0	2	...	0.166
x	0	0	...	-1.993
Outputs				
Out	0	1.571	...	3.058
Exp. Out	0	1.571	...	3.058
Out (DSP)	0	1.571	...	3.058
Exp. Out (DSP)	0	1.571	...	3.058

Test settings	
Tolerance Out	±2,5611e-07 (±550 LSB)

Test statistics	
Min CPU cycles	237
Max CPU cycles	782
Avg CPU cycles	612

Verification: Atan2 Float32 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for Math block Atan2.

Test results				
Time step	1	2	...	315
CPU cycles	265	438	...	3148
Inputs				
y (DSP)	0	2	...	0.166
x (DSP)	0	0	...	-1.993
y	0	2	...	0.166
x	0	0	...	-1.993
Outputs				
Out	0	1.571	...	3.058
Exp. Out	0	1.571	...	3.058
Out (DSP)	0	1.571	...	3.058
Exp. Out (DSP)	0	1.571	...	3.058

Test settings	
Tolerance Out	±2,5611e-07 (±550 LSB)

Test statistics	
Min CPU cycles	265
Max CPU cycles	5161
Avg CPU cycles	3703

Verification: Atan2 Float32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for Math block Atan2.

Test results				
Time step	1	2	...	315
CPU cycles	166	130	...	292
Inputs				
y (DSP)	0	2	...	0.166
x (DSP)	0	0	...	-1.993
y	0	2	...	0.166
x	0	0	...	-1.993
Outputs				
Out	0	1.571	...	3.058
Exp. Out	0	1.571	...	3.058
Out (DSP)	0	1.571	...	3.058
Exp. Out (DSP)	0	1.571	...	3.058

Test settings	
Tolerance Out	±2,5611e-07 (±550 LSB)

Test statistics	
Min CPU cycles	117
Max CPU cycles	414
Avg CPU cycles	301

Verification: Atan2 Float32 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for Math block Atan2.

Test results				
Time step	1	2	...	315
CPU cycles	147	180	...	622
Inputs				
y (DSP)	0	2	...	0.166
x (DSP)	0	0	...	-1.993
y	0	2	...	0.166
x	0	0	...	-1.993
Outputs				
Out	0	1.571	...	3.058
Exp. Out	0	1.571	...	3.058
Out (DSP)	0	1.571	...	3.058
Exp. Out (DSP)	0	1.571	...	3.058

Test settings	
Tolerance Out	±2,5611e-07 (±550 LSB)

Test statistics	
Min CPU cycles	147
Max CPU cycles	909
Avg CPU cycles	692

Block: Average



Calculation of moving average value over n numbers.

Inports	
In	Input value

Outports	
Out	Averaged value

Mask Parameters		
Name	**ID**	**Description**
n	1	Number of points to be averaged over
ts_fact	2	Multiplication factor of base sampling time (in integer format)

Description:

Calculation:

$$\mathrm{Out}_k = \frac{1}{n} \sum_{i=k-n}^{k} \mathrm{In}_i$$

Implementations:

FiP8 8 Bit Fixed Point Implementation
FiP16 16 Bit Fixed Point Implementation
FiP32 32 Bit Fixed Point Implementation
Float32 32 Bit Floating Point Implementation
Float64 64 Bit Floating Point Implementation

Implementation: FiP8

8 Bit Fixed Point Implementation

Inports Data Type	
In	int8

Outports Data Type	
Out	int8

Implementation: FiP16

16 Bit Fixed Point Implementation

Inports Data Type	
In	int16

Outports Data Type	
Out	int16

Implementation: FiP32

32 Bit Fixed Point Implementation

Inports Data Type	
In	int32

Outports Data Type	
Out	int32

Implementation: Float32

32 Bit Floating Point Implementation

Inports Data Type	
In	float32

Outports Data Type	
Out	float32

Implementation: Float64

64 Bit Floating Point Implementation

Inports Data Type	
In	float64

Outports Data Type	
Out	float64

Verification: Average FiP16 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test

OK

Inport test for Math block Average.

Test results						
Time step	1	2	3	4	...	113
CPU cycles	87	87	87	87	...	87
Inputs						
In (DSP)	-145	2369	4	-2087	...	-1015
In	-0.004	0.072	0	-0.064	...	-0.031
Parameters						
n	1					
ts_fact	1					
Outputs						
Out	-0.004	0.072	0	-0.064	...	-0.031
Exp. Out	-0.004	0.072	0	-0.064	...	-0.031
Out (DSP)	-145	2369	4	-2087	...	-1015
Exp. Out (DSP)	-145	2369	4	-2087	...	-1015

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	87
Max CPU cycles	87
Avg CPU cycles	87

Test case: Inport test

OK

Inport test for Math block Average.

Test results						
Time step	1	2	3	4	...	113
CPU cycles	87	87	87	87	...	87
Inputs						
In (DSP)	-4188	340	-3895	355	...	-3177
In	-0.128	0.01	-0.119	0.011	...	-0.097
Parameters						
n	4					
ts_fact	1					
Outputs						
Out	-0.032	-0.029	-0.059	-0.056	...	0.091
Exp. Out	-0.032	-0.029	-0.059	-0.056	...	0.091
Out (DSP)	-1047	-962	-1936	-1847	...	2994
Exp. Out (DSP)	-1047	-962	-1936	-1847	...	2994

Test settings	
Tolerance Out	±6,1035e-05 (±2 LSB)

Test statistics	
Min CPU cycles	87
Max CPU cycles	87
Avg CPU cycles	87

Test case: Inport test **OK**

Inport test for Math block Average.

Test results						
Time step	1	2	3	4	...	113
CPU cycles	87	87	87	87	...	87
Inputs						
In (DSP)	4496	-3777	1239	-7107	...	2679
In	0.137	-0.115	0.038	-0.217	...	0.082
Parameters						
n	32					
ts_fact	1					
Outputs						
Out	0.004	0.001	0.002	-0.005	...	0.528
Exp. Out	0.004	0.001	0.002	-0.005	...	0.528
Out (DSP)	140	22	61	-161	...	17314
Exp. Out (DSP)	141	22	61	-161	...	17315

Test settings	
Tolerance Out	±6,1035e-05 (±2 LSB)

Test statistics	
Min CPU cycles	87
Max CPU cycles	87
Avg CPU cycles	87

Test case: Conversion test **OK**

Conversion test for Math block Average.

Test results				
Time step	1	2	3	4
Mask parameters				
n	1	2	4	256
ts_fact	1	1	1	1
Controller parameters				
sfrn	0	1	2	8
n	1	2	4	256
Exp. sfrn	0	1	2	8
Exp. n	1	2	4	256

Test settings	
Tolerance sfrn	±0,0000e+00
Tolerance n	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Math block Average.

Test results				
Time step	1	2	3	4
Mask parameters				
n	1	2	4	256
ts_fact	1	1	1	1
Controller parameters				
sfrn	0	1	2	8
n	1	2	4	256
Exp. sfrn	0	1	2	8
Exp. n	1	2	4	256

Test settings	
Tolerance sfrn	±0,0000e+00
Tolerance n	±0,0000e+00

Test statistics	
Min CPU cycles	6543
Max CPU cycles	6578
Avg CPU cycles	6561

Verification: Average FiP16 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for Math block Average.

Test results						
Time step	1	2	3	4	...	113
CPU cycles	61	61	61	61	...	61
Inputs						
In (DSP)	-145	2369	4	-2087	...	-1015
In	-0.004	0.072	0	-0.064	...	-0.031
Parameters						
n	1					
ts_fact	1					
Outputs						
Out	-0.004	0.072	0	-0.064	...	-0.031
Exp. Out	-0.004	0.072	0	-0.064	...	-0.031
Out (DSP)	-145	2369	4	-2087	...	-1015
Exp. Out (DSP)	-145	2369	4	-2087	...	-1015

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	61
Max CPU cycles	61
Avg CPU cycles	61

Test case: Inport test OK

Inport test for Math block Average.

Test results						
Time step	1	2	3	4	...	113
CPU cycles	61	61	61	61	...	61
Inputs						
In (DSP)	-4188	340	-3895	355	...	-3177
In	-0.128	0.01	-0.119	0.011	...	-0.097
Parameters						
n	4					
ts_fact	1					
Outputs						
Out	-0.032	-0.029	-0.059	-0.056	...	0.091
Exp. Out	-0.032	-0.029	-0.059	-0.056	...	0.091
Out (DSP)	-1047	-962	-1936	-1847	...	2994
Exp. Out (DSP)	-1047	-962	-1936	-1847	...	2994

Test settings	
Tolerance Out	±6,1035e-05 (±2 LSB)

Test statistics	
Min CPU cycles	61
Max CPU cycles	61
Avg CPU cycles	61

Test case: Inport test **OK**

Inport test for Math block Average.

Test results						
Time step	1	2	3	4	...	113
CPU cycles	61	61	61	61	...	61
Inputs						
In (DSP)	4496	-3777	1239	-7107	...	2679
In	0.137	-0.115	0.038	-0.217	...	0.082
Parameters						
n	32					
ts_fact	1					
Outputs						
Out	0.004	0.001	0.002	-0.005	...	0.528
Exp. Out	0.004	0.001	0.002	-0.005	...	0.528
Out (DSP)	140	22	61	-161	...	17314
Exp. Out (DSP)	141	22	61	-161	...	17315

Test settings	
Tolerance Out	±6,1035e-05 (±2 LSB)

Test statistics	
Min CPU cycles	61
Max CPU cycles	61
Avg CPU cycles	61

Test case: Conversion test **OK**

Conversion test for Math block Average.

Test results				
Time step	1	2	3	4
Mask parameters				
n	1	2	4	256
ts_fact	1	1	1	1
Controller parameters				
sfrn	0	1	2	8
n	1	2	4	256
Exp. sfrn	0	1	2	8
Exp. n	1	2	4	256

Test settings	
Tolerance sfrn	±0,0000e+00
Tolerance n	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Math block Average.

Test results				
Time step	1	2	3	4
Mask parameters				
n	1	2	4	256
ts_fact	1	1	1	1
Controller parameters				
sfrn	0	1	2	8
n	1	2	4	256
Exp. sfrn	0	1	2	8
Exp. n	1	2	4	256

Test settings	
Tolerance sfrn	±0,0000e+00
Tolerance n	±0,0000e+00

Test statistics	
Min CPU cycles	2613
Max CPU cycles	2619
Avg CPU cycles	2617

Verification: Average FiP16 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for Math block Average.

Test results						
Time step	1	2	3	4	...	113
CPU cycles	92	92	92	92	...	92
Inputs						
In (DSP)	-145	2369	4	-2087	...	-1015
In	-0.004	0.072	0	-0.064	...	-0.031
Parameters						
n	1					
ts_fact	1					
Outputs						
Out	-0.004	0.072	0	-0.064	...	-0.031
Exp. Out	-0.004	0.072	0	-0.064	...	-0.031
Out (DSP)	-145	2369	4	-2087	...	-1015
Exp. Out (DSP)	-145	2369	4	-2087	...	-1015

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	92
Max CPU cycles	92
Avg CPU cycles	92

Test case: Inport test OK

Inport test for Math block Average.

Test results						
Time step	1	2	3	4	...	113
CPU cycles	92	92	92	92	...	92
Inputs						
In (DSP)	-4188	340	-3895	355	...	-3177
In	-0.128	0.01	-0.119	0.011	...	-0.097
Parameters						
n	4					
ts_fact	1					
Outputs						
Out	-0.032	-0.029	-0.059	-0.056	...	0.091
Exp. Out	-0.032	-0.029	-0.059	-0.056	...	0.091
Out (DSP)	-1047	-962	-1936	-1847	...	2994
Exp. Out (DSP)	-1047	-962	-1936	-1847	...	2994

Test settings	
Tolerance Out	±6,1035e-05 (±2 LSB)

Test statistics	
Min CPU cycles	92
Max CPU cycles	92
Avg CPU cycles	92

Test case: Inport test **OK**

Inport test for Math block Average.

Test results						
Time step	1	2	3	4	...	113
CPU cycles	92	92	92	92	...	92
Inputs						
In (DSP)	4496	-3777	1239	-7107	...	2679
In	0.137	-0.115	0.038	-0.217	...	0.082
Parameters						
n	32					
ts_fact	1					
Outputs						
Out	0.004	0.001	0.002	-0.005	...	0.528
Exp. Out	0.004	0.001	0.002	-0.005	...	0.528
Out (DSP)	140	22	61	-161	...	17314
Exp. Out (DSP)	141	22	61	-161	...	17315

Test settings	
Tolerance Out	±6,1035e-05 (±2 LSB)

Test statistics	
Min CPU cycles	92
Max CPU cycles	92
Avg CPU cycles	92

Test case: Conversion test **OK**

Conversion test for Math block Average.

Test results				
Time step	1	2	3	4
Mask parameters				
n	1	2	4	256
ts_fact	1	1	1	1
Controller parameters				
sfrn	0	1	2	8
n	1	2	4	256
Exp. sfrn	0	1	2	8
Exp. n	1	2	4	256

Test settings	
Tolerance sfrn	±0,0000e+00
Tolerance n	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Math block Average.

Test results				
Time step	1	2	3	4
Mask parameters				
n	1	2	4	256
ts_fact	1	1	1	1
Controller parameters				
sfrn	0	1	2	8
n	1	2	4	256
Exp. sfrn	0	1	2	8
Exp. n	1	2	4	256

Test settings	
Tolerance sfrn	±0,0000e+00
Tolerance n	±0,0000e+00

Test statistics	
Min CPU cycles	3379
Max CPU cycles	3391
Avg CPU cycles	3383

Verification: Average FiP16 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for Math block Average.

Test results						
Time step	1	2	3	4	...	113
CPU cycles	84	84	84	84	...	84
Inputs						
In (DSP)	-145	2369	4	-2087	...	-1015
In	-0.004	0.072	0	-0.064	...	-0.031
Parameters						
n	1					
ts_fact	1					
Outputs						
Out	-0.004	0.072	0	-0.064	...	-0.031
Exp. Out	-0.004	0.072	0	-0.064	...	-0.031
Out (DSP)	-145	2369	4	-2087	...	-1015
Exp. Out (DSP)	-145	2369	4	-2087	...	-1015

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	84
Max CPU cycles	84
Avg CPU cycles	84

Test case: Inport test OK

Inport test for Math block Average.

Test results						
Time step	1	2	3	4	...	113
CPU cycles	84	84	84	84	...	84
Inputs						
In (DSP)	-4188	340	-3895	355	...	-3177
In	-0.128	0.01	-0.119	0.011	...	-0.097
Parameters						
n	4					
ts_fact	1					
Outputs						
Out	-0.032	-0.029	-0.059	-0.056	...	0.091
Exp. Out	-0.032	-0.029	-0.059	-0.056	...	0.091
Out (DSP)	-1047	-962	-1936	-1847	...	2994
Exp. Out (DSP)	-1047	-962	-1936	-1847	...	2994

Test settings	
Tolerance Out	±6,1035e-05 (±2 LSB)

Test statistics	
Min CPU cycles	84
Max CPU cycles	84
Avg CPU cycles	84

Test case: Inport test **OK**

Inport test for Math block Average.

Test results						
Time step	1	2	3	4	...	113
CPU cycles	84	84	84	84	...	84
Inputs						
In (DSP)	4496	-3777	1239	-7107	...	2679
In	0.137	-0.115	0.038	-0.217	...	0.082
Parameters						
n	32					
ts_fact	1					
Outputs						
Out	0.004	0.001	0.002	-0.005	...	0.528
Exp. Out	0.004	0.001	0.002	-0.005	...	0.528
Out (DSP)	140	22	61	-161	...	17314
Exp. Out (DSP)	141	22	61	-161	...	17315

Test settings	
Tolerance Out	±6,1035e-05 (±2 LSB)

Test statistics	
Min CPU cycles	84
Max CPU cycles	84
Avg CPU cycles	84

Test case: Conversion test **OK**

Conversion test for Math block Average.

Test results				
Time step	1	2	3	4
Mask parameters				
n	1	2	4	256
ts_fact	1	1	1	1
Controller parameters				
sfrn	0	1	2	8
n	1	2	4	256
Exp. sfrn	0	1	2	8
Exp. n	1	2	4	256

Test settings	
Tolerance sfrn	±0,0000e+00
Tolerance n	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Math block Average.

Test results				
Time step	1	2	3	4
Mask parameters				
n	1	2	4	256
ts_fact	1	1	1	1
Controller parameters				
sfrn	0	1	2	8
n	1	2	4	256
Exp. sfrn	0	1	2	8
Exp. n	1	2	4	256

Test settings	
Tolerance sfrn	±0,0000e+00
Tolerance n	±0,0000e+00

Test statistics	
Min CPU cycles	4342
Max CPU cycles	4351
Avg CPU cycles	4348

Verification: Average FiP16 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for Math block Average.

Test results						
Time step	1	2	3	4	...	113
CPU cycles	58	58	58	58	...	58
Inputs						
In (DSP)	-145	2369	4	-2087	...	-1015
In	-0.004	0.072	0	-0.064	...	-0.031
Parameters						
n	1					
ts_fact	1					
Outputs						
Out	-0.004	0.072	0	-0.064	...	-0.031
Exp. Out	-0.004	0.072	0	-0.064	...	-0.031
Out (DSP)	-145	2369	4	-2087	...	-1015
Exp. Out (DSP)	-145	2369	4	-2087	...	-1015

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	58
Max CPU cycles	58
Avg CPU cycles	58

Test case: Inport test OK

Inport test for Math block Average.

Test results						
Time step	1	2	3	4	...	113
CPU cycles	56	56	56	58	...	56
Inputs						
In (DSP)	-4188	340	-3895	355	...	-3177
In	-0.128	0.01	-0.119	0.011	...	-0.097
Parameters						
n	4					
ts_fact	1					
Outputs						
Out	-0.032	-0.029	-0.059	-0.056	...	0.091
Exp. Out	-0.032	-0.029	-0.059	-0.056	...	0.091
Out (DSP)	-1047	-962	-1936	-1847	...	2994
Exp. Out (DSP)	-1047	-962	-1936	-1847	...	2994

Test settings	
Tolerance Out	±6,1035e-05 (±2 LSB)

Test statistics	
Min CPU cycles	56
Max CPU cycles	58
Avg CPU cycles	56

Test case: Inport test **OK**

Inport test for Math block Average.

Test results						
Time step	1	2	3	4	...	113
CPU cycles	56	56	56	56	...	56
Inputs						
In (DSP)	4496	-3777	1239	-7107	...	2679
In	0.137	-0.115	0.038	-0.217	...	0.082
Parameters						
n	32					
ts_fact	1					
Outputs						
Out	0.004	0.001	0.002	-0.005	...	0.528
Exp. Out	0.004	0.001	0.002	-0.005	...	0.528
Out (DSP)	140	22	61	-161	...	17314
Exp. Out (DSP)	141	22	61	-161	...	17315

Test settings	
Tolerance Out	±6,1035e-05 (±2 LSB)

Test statistics	
Min CPU cycles	56
Max CPU cycles	58
Avg CPU cycles	56

Test case: Conversion test **OK**

Conversion test for Math block Average.

Test results				
Time step	1	2	3	4
Mask parameters				
n	1	2	4	256
ts_fact	1	1	1	1
Controller parameters				
sfrn	0	1	2	8
n	1	2	4	256
Exp. sfrn	0	1	2	8
Exp. n	1	2	4	256

Test settings	
Tolerance sfrn	±0,0000e+00
Tolerance n	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Math block Average.

Test results				
Time step	1	2	3	4
Mask parameters				
n	1	2	4	256
ts_fact	1	1	1	1
Controller parameters				
sfrn	0	1	2	8
n	1	2	4	256
Exp. sfrn	0	1	2	8
Exp. n	1	2	4	256

Test settings	
Tolerance sfrn	±0,0000e+00
Tolerance n	±0,0000e+00

Test statistics	
Min CPU cycles	3676
Max CPU cycles	3678
Avg CPU cycles	3677

Verification: Average FiP16 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test — OK

Inport test for Math block Average.

Test results						
Time step	1	2	3	4	...	113
CPU cycles	72	72	72	72	...	72
Inputs						
In (DSP)	-145	2369	4	-2087	...	-1015
In	-0.004	0.072	0	-0.064	...	-0.031
Parameters						
n	1					
ts_fact	1					
Outputs						
Out	-0.004	0.072	0	-0.064	...	-0.031
Exp. Out	-0.004	0.072	0	-0.064	...	-0.031
Out (DSP)	-145	2369	4	-2087	...	-1015
Exp. Out (DSP)	-145	2369	4	-2087	...	-1015

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	72
Max CPU cycles	72
Avg CPU cycles	72

Test case: Inport test — OK

Inport test for Math block Average.

Test results						
Time step	1	2	3	4	...	113
CPU cycles	73	73	73	72	...	73
Inputs						
In (DSP)	-4188	340	-3895	355	...	-3177
In	-0.128	0.01	-0.119	0.011	...	-0.097
Parameters						
n	4					
ts_fact	1					
Outputs						
Out	-0.032	-0.029	-0.059	-0.056	...	0.091
Exp. Out	-0.032	-0.029	-0.059	-0.056	...	0.091
Out (DSP)	-1047	-962	-1936	-1847	...	2994
Exp. Out (DSP)	-1047	-962	-1936	-1847	...	2994

Test settings	
Tolerance Out	±6,1035e-05 (±2 LSB)

Test statistics	
Min CPU cycles	72
Max CPU cycles	73
Avg CPU cycles	72

Test case: Inport test **OK**

Inport test for Math block Average.

Test results						
Time step	1	2	3	4	...	113
CPU cycles	73	73	73	73	...	73
Inputs						
In (DSP)	4496	-3777	1239	-7107	...	2679
In	0.137	-0.115	0.038	-0.217	...	0.082
Parameters						
n	32					
ts_fact	1					
Outputs						
Out	0.004	0.001	0.002	-0.005	...	0.528
Exp. Out	0.004	0.001	0.002	-0.005	...	0.528
Out (DSP)	140	22	61	-161	...	17314
Exp. Out (DSP)	141	22	61	-161	...	17315

Test settings	
Tolerance Out	±6,1035e-05 (±2 LSB)

Test statistics	
Min CPU cycles	72
Max CPU cycles	73
Avg CPU cycles	72

Test case: Conversion test **OK**

Conversion test for Math block Average.

Test results				
Time step	1	2	3	4
Mask parameters				
n	1	2	4	256
ts_fact	1	1	1	1
Controller parameters				
sfrn	0	1	2	8
n	1	2	4	256
Exp. sfrn	0	1	2	8
Exp. n	1	2	4	256

Test settings	
Tolerance sfrn	±0,0000e+00
Tolerance n	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Math block Average.

Test results				
Time step	1	2	3	4
Mask parameters				
n	1	2	4	256
ts_fact	1	1	1	1
Controller parameters				
sfrn	0	1	2	8
n	1	2	4	256
Exp. sfrn	0	1	2	8
Exp. n	1	2	4	256

Test settings	
Tolerance sfrn	±0,0000e+00
Tolerance n	±0,0000e+00

Test statistics	
Min CPU cycles	3345
Max CPU cycles	3348
Avg CPU cycles	3347

Verification: Average FiP16 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test

OK

Inport test for Math block Average.

Test results						
Time step	1	2	3	4	...	113
CPU cycles	98	87	87	87	...	87
Inputs						
In (DSP)	-145	2369	4	-2087	...	-1015
In	-0.004	0.072	0	-0.064	...	-0.031
Parameters						
n	1					
ts_fact	1					
Outputs						
Out	-0.004	0.072	0	-0.064	...	-0.031
Exp. Out	-0.004	0.072	0	-0.064	...	-0.031
Out (DSP)	-145	2369	4	-2087	...	-1015
Exp. Out (DSP)	-145	2369	4	-2087	...	-1015

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	87
Max CPU cycles	98
Avg CPU cycles	87

Test case: Inport test

OK

Inport test for Math block Average.

Test results						
Time step	1	2	3	4	...	113
CPU cycles	87	87	87	87	...	87
Inputs						
In (DSP)	-4188	340	-3895	355	...	-3177
In	-0.128	0.01	-0.119	0.011	...	-0.097
Parameters						
n	4					
ts_fact	1					
Outputs						
Out	-0.032	-0.029	-0.059	-0.056	...	0.091
Exp. Out	-0.032	-0.029	-0.059	-0.056	...	0.091
Out (DSP)	-1047	-962	-1936	-1847	...	2994
Exp. Out (DSP)	-1047	-962	-1936	-1847	...	2994

Test settings	
Tolerance Out	±6,1035e-05 (±2 LSB)

Test statistics	
Min CPU cycles	87
Max CPU cycles	87
Avg CPU cycles	87

Test case: Inport test **OK**

Inport test for Math block Average.

Test results						
Time step	1	2	3	4	...	113
CPU cycles	87	87	87	87	...	87
Inputs						
In (DSP)	4496	-3777	1239	-7107	...	2679
In	0.137	-0.115	0.038	-0.217	...	0.082
Parameters						
n	32					
ts_fact	1					
Outputs						
Out	0.004	0.001	0.002	-0.005	...	0.528
Exp. Out	0.004	0.001	0.002	-0.005	...	0.528
Out (DSP)	140	22	61	-161	...	17314
Exp. Out (DSP)	141	22	61	-161	...	17315

Test settings	
Tolerance Out	±6,1035e-05 (±2 LSB)

Test statistics	
Min CPU cycles	87
Max CPU cycles	87
Avg CPU cycles	87

Test case: Conversion test **OK**

Conversion test for Math block Average.

Test results				
Time step	1	2	3	4
Mask parameters				
n	1	2	4	256
ts_fact	1	1	1	1
Controller parameters				
sfrn	0	1	2	8
n	1	2	4	256
Exp. sfrn	0	1	2	8
Exp. n	1	2	4	256

Test settings	
Tolerance sfrn	±0,0000e+00
Tolerance n	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Math block Average.

Test results				
Time step	1	2	3	4
Mask parameters				
n	1	2	4	256
ts_fact	1	1	1	1
Controller parameters				
sfrn	0	1	2	8
n	1	2	4	256
Exp. sfrn	0	1	2	8
Exp. n	1	2	4	256

Test settings	
Tolerance sfrn	±0,0000e+00
Tolerance n	±0,0000e+00

Test statistics	
Min CPU cycles	3834
Max CPU cycles	3938
Avg CPU cycles	3862

Verification: Average FiP16 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for Math block Average.

Test results						
Time step	1	2	3	4	...	113
CPU cycles	83	83	83	83	...	83
Inputs						
In (DSP)	-145	2369	4	-2087	...	-1015
In	-0.004	0.072	0	-0.064	...	-0.031
Parameters						
n	1					
ts_fact	1					
Outputs						
Out	-0.004	0.072	0	-0.064	...	-0.031
Exp. Out	-0.004	0.072	0	-0.064	...	-0.031
Out (DSP)	-145	2369	4	-2087	...	-1015
Exp. Out (DSP)	-145	2369	4	-2087	...	-1015

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	83
Max CPU cycles	83
Avg CPU cycles	83

Test case: Inport test OK

Inport test for Math block Average.

Test results						
Time step	1	2	3	4	...	113
CPU cycles	87	87	87	83	...	87
Inputs						
In (DSP)	-4188	340	-3895	355	...	-3177
In	-0.128	0.01	-0.119	0.011	...	-0.097
Parameters						
n	4					
ts_fact	1					
Outputs						
Out	-0.032	-0.029	-0.059	-0.056	...	0.091
Exp. Out	-0.032	-0.029	-0.059	-0.056	...	0.091
Out (DSP)	-1047	-962	-1936	-1847	...	2994
Exp. Out (DSP)	-1047	-962	-1936	-1847	...	2994

Test settings	
Tolerance Out	±6,1035e-05 (±2 LSB)

Test statistics	
Min CPU cycles	83
Max CPU cycles	87
Avg CPU cycles	86

Test case: Inport test **OK**

Inport test for Math block Average.

Test results						
Time step	1	2	3	4	...	113
CPU cycles	87	87	87	87	...	87
Inputs						
In (DSP)	4496	-3777	1239	-7107	...	2679
In	0.137	-0.115	0.038	-0.217	...	0.082
Parameters						
n	32					
ts_fact	1					
Outputs						
Out	0.004	0.001	0.002	-0.005	...	0.528
Exp. Out	0.004	0.001	0.002	-0.005	...	0.528
Out (DSP)	140	22	61	-161	...	17314
Exp. Out (DSP)	141	22	61	-161	...	17315

Test settings	
Tolerance Out	±6,1035e-05 (±2 LSB)

Test statistics	
Min CPU cycles	83
Max CPU cycles	87
Avg CPU cycles	86

Test case: Conversion test **OK**

Conversion test for Math block Average.

Test results				
Time step	1	2	3	4
Mask parameters				
n	1	2	4	256
ts_fact	1	1	1	1
Controller parameters				
sfrn	0	1	2	8
n	1	2	4	256
Exp. sfrn	0	1	2	8
Exp. n	1	2	4	256

Test settings	
Tolerance sfrn	±0,0000e+00
Tolerance n	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Math block Average.

Test results				
Time step	1	2	3	4
Mask parameters				
n	1	2	4	256
ts_fact	1	1	1	1
Controller parameters				
sfrn	0	1	2	8
n	1	2	4	256
Exp. sfrn	0	1	2	8
Exp. n	1	2	4	256

Test settings	
Tolerance sfrn	±0,0000e+00
Tolerance n	±0,0000e+00

Test statistics	
Min CPU cycles	5900
Max CPU cycles	5935
Avg CPU cycles	5918

Verification: Average FiP32 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for Math block Average.

Test results				
Time step	1	2	...	113
CPU cycles	105	105	...	105
Inputs				
In (DSP)	-9515881	155233746	...	-66486533
In	-0.004	0.072	...	-0.031
Parameters				
n	1			
ts_fact	1			
Outputs				
Out	-0.004	0.072	...	-0.031
Exp. Out	-0.004	0.072	...	-0.031
Out (DSP)	-9515881	155233746	...	-66486533
Exp. Out (DSP)	-9515881	155233746	...	-66486533

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	105
Max CPU cycles	105
Avg CPU cycles	105

Test case: Inport test OK

Inport test for Math block Average.

Test results				
Time step	1	2	...	113
CPU cycles	106	106	...	106
Inputs				
In (DSP)	-274451780	22274693	...	-208184544
In	-0.128	0.01	...	-0.097
Parameters				
n	4			
ts_fact	1			
Outputs				
Out	-0.032	-0.029	...	0.091
Exp. Out	-0.032	-0.029	...	0.091
Out (DSP)	-68612945	-63044272	...	196244641
Exp. Out (DSP)	-68612945	-63044272	...	196244642

Test settings	
Tolerance Out	±9,3132e-10 (±2 LSB)

Test statistics	
Min CPU cycles	105
Max CPU cycles	106
Avg CPU cycles	105

Test case: Inport test **OK**

Inport test for Math block Average.

Test results				
Time step	1	2	...	113
CPU cycles	106	106	...	106
Inputs				
In (DSP)	294667413	-247518422	...	175553610
In	0.137	-0.115	...	0.082
Parameters				
n	32			
ts_fact	1			
Outputs				
Out	0.004	0.001	...	0.528
Exp. Out	0.004	0.001	...	0.528
Out (DSP)	9208356	1473405	...	1134727469
Exp. Out (DSP)	9208357	1473406	...	1134727470

Test settings	
Tolerance Out	±9,3132e-10 (±2 LSB)

Test statistics	
Min CPU cycles	105
Max CPU cycles	106
Avg CPU cycles	105

Test case: Conversion test **OK**

Conversion test for Math block Average.

Test results				
Time step	1	2	3	4
Mask parameters				
n	1	2	4	256
ts_fact	1	1	1	1
Controller parameters				
sfrn	0	1	2	8
n	1	2	4	256
Exp. sfrn	0	1	2	8
Exp. n	1	2	4	256

Test settings	
Tolerance sfrn	±0,0000e+00
Tolerance n	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Math block Average.

Test results				
Time step	1	2	3	4
Mask parameters				
n	1	2	4	256
ts_fact	1	1	1	1
Controller parameters				
sfrn	0	1	2	8
n	1	2	4	256
Exp. sfrn	0	1	2	8
Exp. n	1	2	4	256

Test settings	
Tolerance sfrn	±0,0000e+00
Tolerance n	±0,0000e+00

Test statistics	
Min CPU cycles	7336
Max CPU cycles	7370
Avg CPU cycles	7354

Verification: Average FiP32 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for Math block Average.

Test results				
Time step	1	2	...	113
CPU cycles	99	99	...	99
Inputs				
In (DSP)	-9515881	155233746	...	-66486533
In	-0.004	0.072	...	-0.031
Parameters				
n	1			
ts_fact	1			
Outputs				
Out	-0.004	0.072	...	-0.031
Exp. Out	-0.004	0.072	...	-0.031
Out (DSP)	-9515881	155233746	...	-66486533
Exp. Out (DSP)	-9515881	155233746	...	-66486533

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	99
Max CPU cycles	99
Avg CPU cycles	99

Test case: Inport test OK

Inport test for Math block Average.

Test results				
Time step	1	2	...	113
CPU cycles	99	99	...	99
Inputs				
In (DSP)	-274451780	22274693	...	-208184544
In	-0.128	0.01	...	-0.097
Parameters				
n	4			
ts_fact	1			
Outputs				
Out	-0.032	-0.029	...	0.091
Exp. Out	-0.032	-0.029	...	0.091
Out (DSP)	-68612945	-63044272	...	196244641
Exp. Out (DSP)	-68612945	-63044272	...	196244642

Test settings	
Tolerance Out	±9,3132e-10 (±2 LSB)

Test statistics	
Min CPU cycles	99
Max CPU cycles	99
Avg CPU cycles	99

Test case: Inport test **OK**

Inport test for Math block Average.

Test results				
Time step	1	2	...	113
CPU cycles	99	99	...	99
Inputs				
In (DSP)	294667413	-247518422	...	175553610
In	0.137	-0.115	...	0.082
Parameters				
n	32			
ts_fact	1			
Outputs				
Out	0.004	0.001	...	0.528
Exp. Out	0.004	0.001	...	0.528
Out (DSP)	9208356	1473405	...	1134727469
Exp. Out (DSP)	9208357	1473406	...	1134727470

Test settings	
Tolerance Out	±9,3132e-10 (±2 LSB)

Test statistics	
Min CPU cycles	99
Max CPU cycles	99
Avg CPU cycles	99

Test case: Conversion test **OK**

Conversion test for Math block Average.

Test results				
Time step	1	2	3	4
Mask parameters				
n	1	2	4	256
ts_fact	1	1	1	1
Controller parameters				
sfrn	0	1	2	8
n	1	2	4	256
Exp. sfrn	0	1	2	8
Exp. n	1	2	4	256

Test settings	
Tolerance sfrn	±0,0000e+00
Tolerance n	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Math block Average.

Test results				
Time step	1	2	3	4
Mask parameters				
n	1	2	4	256
ts_fact	1	1	1	1
Controller parameters				
sfrn	0	1	2	8
n	1	2	4	256
Exp. sfrn	0	1	2	8
Exp. n	1	2	4	256

Test settings	
Tolerance sfrn	±0,0000e+00
Tolerance n	±0,0000e+00

Test statistics	
Min CPU cycles	2617
Max CPU cycles	2623
Avg CPU cycles	2621

Verification: Average FiP32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for Math block Average.

Test results				
Time step	1	2	...	113
CPU cycles	106	106	...	106
Inputs				
In (DSP)	-9515881	155233746	...	-66486533
In	-0.004	0.072	...	-0.031
Parameters				
n	1			
ts_fact	1			
Outputs				
Out	-0.004	0.072	...	-0.031
Exp. Out	-0.004	0.072	...	-0.031
Out (DSP)	-9515881	155233746	...	-66486533
Exp. Out (DSP)	-9515881	155233746	...	-66486533

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	106
Max CPU cycles	106
Avg CPU cycles	106

Test case: Inport test OK

Inport test for Math block Average.

Test results				
Time step	1	2	...	113
CPU cycles	106	106	...	106
Inputs				
In (DSP)	-274451780	22274693	...	-208184544
In	-0.128	0.01	...	-0.097
Parameters				
n	4			
ts_fact	1			
Outputs				
Out	-0.032	-0.029	...	0.091
Exp. Out	-0.032	-0.029	...	0.091
Out (DSP)	-68612945	-63044272	...	196244641
Exp. Out (DSP)	-68612945	-63044272	...	196244642

Test settings	
Tolerance Out	±9,3132e-10 (±2 LSB)

Test statistics	
Min CPU cycles	106
Max CPU cycles	106
Avg CPU cycles	106

Test case: Inport test **OK**

Inport test for Math block Average.

Test results				
Time step	1	2	...	113
CPU cycles	106	106	...	106
Inputs				
In (DSP)	294667413	-247518422	...	175553610
In	0.137	-0.115	...	0.082
Parameters				
n	32			
ts_fact	1			
Outputs				
Out	0.004	0.001	...	0.528
Exp. Out	0.004	0.001	...	0.528
Out (DSP)	9208356	1473405	...	1134727469
Exp. Out (DSP)	9208357	1473406	...	1134727470

Test settings	
Tolerance Out	±9,3132e-10 (±2 LSB)

Test statistics	
Min CPU cycles	106
Max CPU cycles	106
Avg CPU cycles	106

Test case: Conversion test **OK**

Conversion test for Math block Average.

Test results				
Time step	1	2	3	4
Mask parameters				
n	1	2	4	256
ts_fact	1	1	1	1
Controller parameters				
sfrn	0	1	2	8
n	1	2	4	256
Exp. sfrn	0	1	2	8
Exp. n	1	2	4	256

Test settings	
Tolerance sfrn	±0,0000e+00
Tolerance n	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Math block Average.

Test results				
Time step	1	2	3	4
Mask parameters				
n	1	2	4	256
ts_fact	1	1	1	1
Controller parameters				
sfrn	0	1	2	8
n	1	2	4	256
Exp. sfrn	0	1	2	8
Exp. n	1	2	4	256

Test settings	
Tolerance sfrn	±0,0000e+00
Tolerance n	±0,0000e+00

Test statistics	
Min CPU cycles	7774
Max CPU cycles	7834
Avg CPU cycles	7794

Verification: Average FiP32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for Math block Average.

Test results				
Time step	1	2	...	113
CPU cycles	111	111	...	111
Inputs				
In (DSP)	-9515881	155233746	...	-66486533
In	-0.004	0.072	...	-0.031
Parameters				
n	1			
ts_fact	1			
Outputs				
Out	-0.004	0.072	...	-0.031
Exp. Out	-0.004	0.072	...	-0.031
Out (DSP)	-9515881	155233746	...	-66486533
Exp. Out (DSP)	-9515881	155233746	...	-66486533

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	111
Max CPU cycles	111
Avg CPU cycles	111

Test case: Inport test OK

Inport test for Math block Average.

Test results				
Time step	1	2	...	113
CPU cycles	111	111	...	111
Inputs				
In (DSP)	-274451780	22274693	...	-208184544
In	-0.128	0.01	...	-0.097
Parameters				
n	4			
ts_fact	1			
Outputs				
Out	-0.032	-0.029	...	0.091
Exp. Out	-0.032	-0.029	...	0.091
Out (DSP)	-68612945	-63044272	...	196244641
Exp. Out (DSP)	-68612945	-63044272	...	196244642

Test settings	
Tolerance Out	±9,3132e-10 (±2 LSB)

Test statistics	
Min CPU cycles	111
Max CPU cycles	111
Avg CPU cycles	111

Test case: Inport test **OK**

Inport test for Math block Average.

Test results				
Time step	1	2	...	113
CPU cycles	111	111	...	111
Inputs				
In (DSP)	294667413	-247518422	...	175553610
In	0.137	-0.115	...	0.082
Parameters				
n	32			
ts_fact	1			
Outputs				
Out	0.004	0.001	...	0.528
Exp. Out	0.004	0.001	...	0.528
Out (DSP)	9208356	1473405	...	1134727469
Exp. Out (DSP)	9208357	1473406	...	1134727470

Test settings	
Tolerance Out	±9,3132e-10 (±2 LSB)

Test statistics	
Min CPU cycles	111
Max CPU cycles	111
Avg CPU cycles	111

Test case: Conversion test **OK**

Conversion test for Math block Average.

Test results				
Time step	1	2	3	4
Mask parameters				
n	1	2	4	256
ts_fact	1	1	1	1
Controller parameters				
sfrn	0	1	2	8
n	1	2	4	256
Exp. sfrn	0	1	2	8
Exp. n	1	2	4	256

Test settings	
Tolerance sfrn	±0,0000e+00
Tolerance n	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Math block Average.

Test results				
Time step	1	2	3	4
Mask parameters				
n	1	2	4	256
ts_fact	1	1	1	1
Controller parameters				
sfrn	0	1	2	8
n	1	2	4	256
Exp. sfrn	0	1	2	8
Exp. n	1	2	4	256

Test settings	
Tolerance sfrn	±0,0000e+00
Tolerance n	±0,0000e+00

Test statistics	
Min CPU cycles	13060
Max CPU cycles	13069
Avg CPU cycles	13066

Verification: Average FiP32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test

OK

Inport test for Math block Average.

Test results				
Time step	1	2	...	113
CPU cycles	74	74	...	74
Inputs				
In (DSP)	-9515881	155233746	...	-66486533
In	-0.004	0.072	...	-0.031
Parameters				
n	1			
ts_fact	1			
Outputs				
Out	-0.004	0.072	...	-0.031
Exp. Out	-0.004	0.072	...	-0.031
Out (DSP)	-9515881	155233746	...	-66486533
Exp. Out (DSP)	-9515881	155233746	...	-66486533

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	74
Max CPU cycles	74
Avg CPU cycles	74

Test case: Inport test

OK

Inport test for Math block Average.

Test results				
Time step	1	2	...	113
CPU cycles	72	72	...	72
Inputs				
In (DSP)	-274451780	22274693	...	-208184544
In	-0.128	0.01	...	-0.097
Parameters				
n	4			
ts_fact	1			
Outputs				
Out	-0.032	-0.029	...	0.091
Exp. Out	-0.032	-0.029	...	0.091
Out (DSP)	-68612945	-63044272	...	196244641
Exp. Out (DSP)	-68612945	-63044272	...	196244642

Test settings	
Tolerance Out	±9,3132e-10 (±2 LSB)

Test statistics	
Min CPU cycles	72
Max CPU cycles	74
Avg CPU cycles	72

Test case: Inport test **OK**

Inport test for Math block Average.

Test results				
Time step	1	2	...	113
CPU cycles	72	72	...	72
Inputs				
In (DSP)	294667413	-247518422	...	175553610
In	0.137	-0.115	...	0.082
Parameters				
n	32			
ts_fact	1			
Outputs				
Out	0.004	0.001	...	0.528
Exp. Out	0.004	0.001	...	0.528
Out (DSP)	9208356	1473405	...	1134727469
Exp. Out (DSP)	9208357	1473406	...	1134727470

Test settings	
Tolerance Out	±9,3132e-10 (±2 LSB)

Test statistics	
Min CPU cycles	72
Max CPU cycles	74
Avg CPU cycles	72

Test case: Conversion test **OK**

Conversion test for Math block Average.

Test results				
Time step	1	2	3	4
Mask parameters				
n	1	2	4	256
ts_fact	1	1	1	1
Controller parameters				
sfrn	0	1	2	8
n	1	2	4	256
Exp. sfrn	0	1	2	8
Exp. n	1	2	4	256

Test settings	
Tolerance sfrn	±0,0000e+00
Tolerance n	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Math block Average.

Test results				
Time step	1	2	3	4
Mask parameters				
n	1	2	4	256
ts_fact	1	1	1	1
Controller parameters				
sfrn	0	1	2	8
n	1	2	4	256
Exp. sfrn	0	1	2	8
Exp. n	1	2	4	256

Test settings	
Tolerance sfrn	±0,0000e+00
Tolerance n	±0,0000e+00

Test statistics	
Min CPU cycles	1375
Max CPU cycles	1377
Avg CPU cycles	1376

Verification: Average FiP32 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for Math block Average.

Test results				
Time step	1	2	...	113
CPU cycles	87	87	...	87
Inputs				
In (DSP)	-9515881	155233746	...	-66486533
In	-0.004	0.072	...	-0.031
Parameters				
n	1			
ts_fact	1			
Outputs				
Out	-0.004	0.072	...	-0.031
Exp. Out	-0.004	0.072	...	-0.031
Out (DSP)	-9515881	155233746	...	-66486533
Exp. Out (DSP)	-9515881	155233746	...	-66486533

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	87
Max CPU cycles	87
Avg CPU cycles	87

Test case: Inport test OK

Inport test for Math block Average.

Test results				
Time step	1	2	...	113
CPU cycles	108	108	...	108
Inputs				
In (DSP)	-274451780	22274693	...	-208184544
In	-0.128	0.01	...	-0.097
Parameters				
n	4			
ts_fact	1			
Outputs				
Out	-0.032	-0.029	...	0.091
Exp. Out	-0.032	-0.029	...	0.091
Out (DSP)	-68612945	-63044272	...	196244641
Exp. Out (DSP)	-68612945	-63044272	...	196244642

Test settings	
Tolerance Out	±9,3132e-10 (±2 LSB)

Test statistics	
Min CPU cycles	107
Max CPU cycles	108
Avg CPU cycles	107

Test case: Inport test **OK**

Inport test for Math block Average.

Test results				
Time step	1	2	...	113
CPU cycles	138	138	...	138
Inputs				
In (DSP)	294667413	-247518422	...	175553610
In	0.137	-0.115	...	0.082
Parameters				
n	32			
ts_fact	1			
Outputs				
Out	0.004	0.001	...	0.528
Exp. Out	0.004	0.001	...	0.528
Out (DSP)	9208356	1473405	...	1134727469
Exp. Out (DSP)	9208357	1473406	...	1134727470

Test settings	
Tolerance Out	±9,3132e-10 (±2 LSB)

Test statistics	
Min CPU cycles	137
Max CPU cycles	138
Avg CPU cycles	137

Test case: Conversion test **OK**

Conversion test for Math block Average.

Test results				
Time step	1	2	3	4
Mask parameters				
n	1	2	4	256
ts_fact	1	1	1	1
Controller parameters				
sfrn	0	1	2	8
n	1	2	4	256
Exp. sfrn	0	1	2	8
Exp. n	1	2	4	256

Test settings	
Tolerance sfrn	±0,0000e+00
Tolerance n	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Math block Average.

Test results				
Time step	1	2	3	4
Mask parameters				
n	1	2	4	256
ts_fact	1	1	1	1
Controller parameters				
sfrn	0	1	2	8
n	1	2	4	256
Exp. sfrn	0	1	2	8
Exp. n	1	2	4	256

Test settings	
Tolerance sfrn	±0,0000e+00
Tolerance n	±0,0000e+00

Test statistics	
Min CPU cycles	2321
Max CPU cycles	2324
Avg CPU cycles	2323

Verification: Average FiP32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for Math block Average.

Test results				
Time step	1	2	...	113
CPU cycles	114	102	...	102
Inputs				
In (DSP)	-9515881	155233746	...	-66486533
In	-0.004	0.072	...	-0.031
Parameters				
n	1			
ts_fact	1			
Outputs				
Out	-0.004	0.072	...	-0.031
Exp. Out	-0.004	0.072	...	-0.031
Out (DSP)	-9515881	155233746	...	-66486533
Exp. Out (DSP)	-9515881	155233746	...	-66486533

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	102
Max CPU cycles	114
Avg CPU cycles	102

Test case: Inport test OK

Inport test for Math block Average.

Test results				
Time step	1	2	...	113
CPU cycles	102	102	...	102
Inputs				
In (DSP)	-274451780	22274693	...	-208184544
In	-0.128	0.01	...	-0.097
Parameters				
n	4			
ts_fact	1			
Outputs				
Out	-0.032	-0.029	...	0.091
Exp. Out	-0.032	-0.029	...	0.091
Out (DSP)	-68612945	-63044272	...	196244641
Exp. Out (DSP)	-68612945	-63044272	...	196244642

Test settings	
Tolerance Out	±9,3132e-10 (±2 LSB)

Test statistics	
Min CPU cycles	102
Max CPU cycles	102
Avg CPU cycles	102

Test case: Inport test **OK**

Inport test for Math block Average.

Test results				
Time step	1	2	...	113
CPU cycles	102	102	...	102
Inputs				
In (DSP)	294667413	-247518422	...	175553610
In	0.137	-0.115	...	0.082
Parameters				
n	32			
ts_fact	1			
Outputs				
Out	0.004	0.001	...	0.528
Exp. Out	0.004	0.001	...	0.528
Out (DSP)	9208356	1473405	...	1134727469
Exp. Out (DSP)	9208357	1473406	...	1134727470

Test settings	
Tolerance Out	±9,3132e-10 (±2 LSB)

Test statistics	
Min CPU cycles	102
Max CPU cycles	102
Avg CPU cycles	102

Test case: Conversion test **OK**

Conversion test for Math block Average.

Test results				
Time step	1	2	3	4
Mask parameters				
n	1	2	4	256
ts_fact	1	1	1	1
Controller parameters				
sfrn	0	1	2	8
n	1	2	4	256
Exp. sfrn	0	1	2	8
Exp. n	1	2	4	256

Test settings	
Tolerance sfrn	±0,0000e+00
Tolerance n	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Math block Average.

Test results				
Time step	1	2	3	4
Mask parameters				
n	1	2	4	256
ts_fact	1	1	1	1
Controller parameters				
sfrn	0	1	2	8
n	1	2	4	256
Exp. sfrn	0	1	2	8
Exp. n	1	2	4	256

Test settings	
Tolerance sfrn	±0,0000e+00
Tolerance n	±0,0000e+00

Test statistics	
Min CPU cycles	1769
Max CPU cycles	1846
Avg CPU cycles	1792

Verification: Average FiP32 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for Math block Average.

Test results				
Time step	1	2	...	113
CPU cycles	98	98	...	98
Inputs				
In (DSP)	-9515881	155233746	...	-66486533
In	-0.004	0.072	...	-0.031
Parameters				
n	1			
ts_fact	1			
Outputs				
Out	-0.004	0.072	...	-0.031
Exp. Out	-0.004	0.072	...	-0.031
Out (DSP)	-9515881	155233746	...	-66486533
Exp. Out (DSP)	-9515881	155233746	...	-66486533

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	98
Max CPU cycles	98
Avg CPU cycles	98

Test case: Inport test OK

Inport test for Math block Average.

Test results				
Time step	1	2	...	113
CPU cycles	102	102	...	102
Inputs				
In (DSP)	-274451780	22274693	...	-208184544
In	-0.128	0.01	...	-0.097
Parameters				
n	4			
ts_fact	1			
Outputs				
Out	-0.032	-0.029	...	0.091
Exp. Out	-0.032	-0.029	...	0.091
Out (DSP)	-68612945	-63044272	...	196244641
Exp. Out (DSP)	-68612945	-63044272	...	196244642

Test settings	
Tolerance Out	±9,3132e-10 (±2 LSB)

Test statistics	
Min CPU cycles	98
Max CPU cycles	102
Avg CPU cycles	101

Test case: Inport test **OK**

Inport test for Math block Average.

Test results				
Time step	1	2	...	113
CPU cycles	102	102	...	102
Inputs				
In (DSP)	294667413	-247518422	...	175553610
In	0.137	-0.115	...	0.082
Parameters				
n	32			
ts_fact	1			
Outputs				
Out	0.004	0.001	...	0.528
Exp. Out	0.004	0.001	...	0.528
Out (DSP)	9208356	1473405	...	1134727469
Exp. Out (DSP)	9208357	1473406	...	1134727470

Test settings	
Tolerance Out	±9,3132e-10 (±2 LSB)

Test statistics	
Min CPU cycles	98
Max CPU cycles	102
Avg CPU cycles	101

Test case: Conversion test **OK**

Conversion test for Math block Average.

Test results				
Time step	1	2	3	4
Mask parameters				
n	1	2	4	256
ts_fact	1	1	1	1
Controller parameters				
sfrn	0	1	2	8
n	1	2	4	256
Exp. sfrn	0	1	2	8
Exp. n	1	2	4	256

Test settings	
Tolerance sfrn	±0,0000e+00
Tolerance n	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Math block Average.

Test results				
Time step	1	2	3	4
Mask parameters				
n	1	2	4	256
ts_fact	1	1	1	1
Controller parameters				
sfrn	0	1	2	8
n	1	2	4	256
Exp. sfrn	0	1	2	8
Exp. n	1	2	4	256

Test settings	
Tolerance sfrn	±0,0000e+00
Tolerance n	±0,0000e+00

Test statistics	
Min CPU cycles	6034
Max CPU cycles	6058
Avg CPU cycles	6047

Verification: Average Float32 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test

OK

Inport test for Math block Average.

Test results				
Time step	1	2	...	113
CPU cycles	355	355	...	355
Inputs				
In (DSP)	-0.004	0.072	...	-0.031
In	-0.004	0.072	...	-0.031
Parameters				
n	1			
ts_fact	1			
Outputs				
Out	-0.004	0.072	...	-0.031
Exp. Out	-0.004	0.072	...	-0.031
Out (DSP)	-0.004	0.072	...	-0.031
Exp. Out (DSP)	-0.004	0.072	...	-0.031

Test settings	
Tolerance Out	±4,6566e-08 (±100 LSB)

Test statistics	
Min CPU cycles	355
Max CPU cycles	355
Avg CPU cycles	355

Test case: Inport test

OK

Inport test for Math block Average.

Test results				
Time step	1	2	...	113
CPU cycles	356	356	...	356
Inputs				
In (DSP)	-0.128	0.01	...	-0.097
In	-0.128	0.01	...	-0.097
Parameters				
n	4			
ts_fact	1			
Outputs				
Out	-0.032	-0.029	...	0.091
Exp. Out	-0.032	-0.029	...	0.091
Out (DSP)	-0.032	-0.029	...	0.091
Exp. Out (DSP)	-0.032	-0.029	...	0.091

Test settings	
Tolerance Out	±6,9849e-07 (±1500 LSB)

Test statistics	
Min CPU cycles	355
Max CPU cycles	356
Avg CPU cycles	355

Test case: Inport test **OK**

Inport test for Math block Average.

Test results				
Time step	1	2	...	113
CPU cycles	356	356	...	356
Inputs				
In (DSP)	0.137	-0.115	...	0.082
In	0.137	-0.115	...	0.082
Parameters				
n	32			
ts_fact	1			
Outputs				
Out	0.004	0.001	...	0.528
Exp. Out	0.004	0.001	...	0.528
Out (DSP)	0.004	0.001	...	0.528
Exp. Out (DSP)	0.004	0.001	...	0.528

Test settings	
Tolerance Out	±4,6566e-07 (±1000 LSB)

Test statistics	
Min CPU cycles	355
Max CPU cycles	356
Avg CPU cycles	355

Test case: Conversion test **OK**

Conversion test for Math block Average.

Test results				
Time step	1	2	3	4
Mask parameters				
n	1	2	4	256
ts_fact	1	1	1	1
Controller parameters				
n	1	2	4	256
Exp. n	1	2	4	256

Test settings	
Tolerance n	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Math block Average.

Test results				
Time step	1	2	3	4
Mask parameters				
n	1	2	4	256
ts_fact	1	1	1	1
Controller parameters				
n	1	2	4	256
Exp. n	1	2	4	256

Test settings	
Tolerance n	±0,0000e+00

Test statistics	
Min CPU cycles	8067
Max CPU cycles	8111
Avg CPU cycles	8087

Verification: Average Float32 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test

OK

Inport test for Math block Average.

Test results				
Time step	1	2	...	113
CPU cycles	81	81	...	81
Inputs				
In (DSP)	-0.004	0.072	...	-0.031
In	-0.004	0.072	...	-0.031
Parameters				
n	1			
ts_fact	1			
Outputs				
Out	-0.004	0.072	...	-0.031
Exp. Out	-0.004	0.072	...	-0.031
Out (DSP)	-0.004	0.072	...	-0.031
Exp. Out (DSP)	-0.004	0.072	...	-0.031

Test settings	
Tolerance Out	±4,6566e-08 (±100 LSB)

Test statistics	
Min CPU cycles	81
Max CPU cycles	81
Avg CPU cycles	81

Test case: Inport test

OK

Inport test for Math block Average.

Test results				
Time step	1	2	...	113
CPU cycles	81	81	...	81
Inputs				
In (DSP)	-0.128	0.01	...	-0.097
In	-0.128	0.01	...	-0.097
Parameters				
n	4			
ts_fact	1			
Outputs				
Out	-0.032	-0.029	...	0.091
Exp. Out	-0.032	-0.029	...	0.091
Out (DSP)	-0.032	-0.029	...	0.091
Exp. Out (DSP)	-0.032	-0.029	...	0.091

Test settings	
Tolerance Out	±6,9849e-07 (±1500 LSB)

Test statistics	
Min CPU cycles	81
Max CPU cycles	81
Avg CPU cycles	81

Test case: Inport test **OK**

Inport test for Math block Average.

Test results				
Time step	1	2	...	113
CPU cycles	81	81	...	81
Inputs				
In (DSP)	0.137	-0.115	...	0.082
In	0.137	-0.115	...	0.082
Parameters				
n	32			
ts_fact	1			
Outputs				
Out	0.004	0.001	...	0.528
Exp. Out	0.004	0.001	...	0.528
Out (DSP)	0.004	0.001	...	0.528
Exp. Out (DSP)	0.004	0.001	...	0.528

Test settings	
Tolerance Out	±4,6566e-07 (±1000 LSB)

Test statistics	
Min CPU cycles	81
Max CPU cycles	81
Avg CPU cycles	81

Test case: Conversion test **OK**

Conversion test for Math block Average.

Test results				
Time step	1	2	3	4
Mask parameters				
n	1	2	4	256
ts_fact	1	1	1	1
Controller parameters				
n	1	2	4	256
Exp. n	1	2	4	256

Test settings	
Tolerance n	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Math block Average.

Test results				
Time step	1	2	3	4
Mask parameters				
n	1	2	4	256
ts_fact	1	1	1	1
Controller parameters				
n	1	2	4	256
Exp. n	1	2	4	256

Test settings	
Tolerance n	±0,0000e+00

Test statistics	
Min CPU cycles	2991
Max CPU cycles	2993
Avg CPU cycles	2992

Verification: Average Float32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for Math block Average.

Test results				
Time step	1	2	...	113
CPU cycles	112	112	...	112
Inputs				
In (DSP)	-0.004	0.072	...	-0.031
In	-0.004	0.072	...	-0.031
Parameters				
n	1			
ts_fact	1			
Outputs				
Out	-0.004	0.072	...	-0.031
Exp. Out	-0.004	0.072	...	-0.031
Out (DSP)	-0.004	0.072	...	-0.031
Exp. Out (DSP)	-0.004	0.072	...	-0.031

Test settings	
Tolerance Out	±4,6566e-08 (±100 LSB)

Test statistics	
Min CPU cycles	112
Max CPU cycles	112
Avg CPU cycles	112

Test case: Inport test OK

Inport test for Math block Average.

Test results				
Time step	1	2	...	113
CPU cycles	112	112	...	112
Inputs				
In (DSP)	-0.128	0.01	...	-0.097
In	-0.128	0.01	...	-0.097
Parameters				
n	4			
ts_fact	1			
Outputs				
Out	-0.032	-0.029	...	0.091
Exp. Out	-0.032	-0.029	...	0.091
Out (DSP)	-0.032	-0.029	...	0.091
Exp. Out (DSP)	-0.032	-0.029	...	0.091

Test settings	
Tolerance Out	±6,9849e-07 (±1500 LSB)

Test statistics	
Min CPU cycles	112
Max CPU cycles	112
Avg CPU cycles	112

Test case: Inport test **OK**

Inport test for Math block Average.

Test results				
Time step	1	2	...	113
CPU cycles	112	112	...	112
Inputs				
In (DSP)	0.137	-0.115	...	0.082
In	0.137	-0.115	...	0.082
Parameters				
n	32			
ts_fact	1			
Outputs				
Out	0.004	0.001	...	0.528
Exp. Out	0.004	0.001	...	0.528
Out (DSP)	0.004	0.001	...	0.528
Exp. Out (DSP)	0.004	0.001	...	0.528

Test settings	
Tolerance Out	±4,6566e-07 (±1000 LSB)

Test statistics	
Min CPU cycles	112
Max CPU cycles	112
Avg CPU cycles	112

Test case: Conversion test **OK**

Conversion test for Math block Average.

Test results				
Time step	1	2	3	4
Mask parameters				
n	1	2	4	256
ts_fact	1	1	1	1
Controller parameters				
n	1	2	4	256
Exp. n	1	2	4	256

Test settings	
Tolerance n	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Math block Average.

Test results				
Time step	1	2	3	4
Mask parameters				
n	1	2	4	256
ts_fact	1	1	1	1
Controller parameters				
n	1	2	4	256
Exp. n	1	2	4	256

Test settings	
Tolerance n	±0,0000e+00

Test statistics	
Min CPU cycles	7763
Max CPU cycles	7835
Avg CPU cycles	7783

Verification: Average Float32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for Math block Average.

Test results				
Time step	1	2	...	113
CPU cycles	903	902	...	899
Inputs				
In (DSP)	-0.004	0.072	...	-0.031
In	-0.004	0.072	...	-0.031
Parameters				
n	1			
ts_fact	1			
Outputs				
Out	-0.004	0.072	...	-0.031
Exp. Out	-0.004	0.072	...	-0.031
Out (DSP)	-0.004	0.072	...	-0.031
Exp. Out (DSP)	-0.004	0.072	...	-0.031

Test settings	
Tolerance Out	±4,6566e-08 (±100 LSB)

Test statistics	
Min CPU cycles	899
Max CPU cycles	961
Avg CPU cycles	901

Test case: Inport test OK

Inport test for Math block Average.

Test results				
Time step	1	2	...	113
CPU cycles	903	991	...	1023
Inputs				
In (DSP)	-0.128	0.01	...	-0.097
In	-0.128	0.01	...	-0.097
Parameters				
n	4			
ts_fact	1			
Outputs				
Out	-0.032	-0.029	...	0.091
Exp. Out	-0.032	-0.029	...	0.091
Out (DSP)	-0.032	-0.029	...	0.091
Exp. Out (DSP)	-0.032	-0.029	...	0.091

Test settings	
Tolerance Out	±6,9849e-07 (±1500 LSB)

Test statistics	
Min CPU cycles	903
Max CPU cycles	1061
Avg CPU cycles	1001

Test case: Inport test **OK**

Inport test for Math block Average.

Test results				
Time step	1	2	...	113
CPU cycles	906	984	...	992
Inputs				
In (DSP)	0.137	-0.115	...	0.082
In	0.137	-0.115	...	0.082
Parameters				
n	32			
ts_fact	1			
Outputs				
Out	0.004	0.001	...	0.528
Exp. Out	0.004	0.001	...	0.528
Out (DSP)	0.004	0.001	...	0.528
Exp. Out (DSP)	0.004	0.001	...	0.528

Test settings	
Tolerance Out	±4,6566e-07 (±1000 LSB)

Test statistics	
Min CPU cycles	906
Max CPU cycles	1052
Avg CPU cycles	982

Test case: Conversion test **OK**

Conversion test for Math block Average.

Test results				
Time step	1	2	3	4
Mask parameters				
n	1	2	4	256
ts_fact	1	1	1	1
Controller parameters				
n	1	2	4	256
Exp. n	1	2	4	256

Test settings	
Tolerance n	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Math block Average.

Test results				
Time step	1	2	3	4
Mask parameters				
n	1	2	4	256
ts_fact	1	1	1	1
Controller parameters				
n	1	2	4	256
Exp. n	1	2	4	256

Test settings	
Tolerance n	±0,0000e+00

Test statistics	
Min CPU cycles	13049
Max CPU cycles	13058
Avg CPU cycles	13055

Verification: Average Float32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for Math block Average.

Test results				
Time step	1	2	...	113
CPU cycles	322	330	...	330
Inputs				
In (DSP)	-0.004	0.072	...	-0.031
In	-0.004	0.072	...	-0.031
Parameters				
n	1			
ts_fact	1			
Outputs				
Out	-0.004	0.072	...	-0.031
Exp. Out	-0.004	0.072	...	-0.031
Out (DSP)	-0.004	0.072	...	-0.031
Exp. Out (DSP)	-0.004	0.072	...	-0.031

Test settings	
Tolerance Out	±4,6566e-08 (±100 LSB)

Test statistics	
Min CPU cycles	307
Max CPU cycles	330
Avg CPU cycles	329

Test case: Inport test OK

Inport test for Math block Average.

Test results				
Time step	1	2	...	113
CPU cycles	320	345	...	374
Inputs				
In (DSP)	-0.128	0.01	...	-0.097
In	-0.128	0.01	...	-0.097
Parameters				
n	4			
ts_fact	1			
Outputs				
Out	-0.032	-0.029	...	0.091
Exp. Out	-0.032	-0.029	...	0.091
Out (DSP)	-0.032	-0.029	...	0.091
Exp. Out (DSP)	-0.032	-0.029	...	0.091

Test settings	
Tolerance Out	±6,9849e-07 (±1500 LSB)

Test statistics	
Min CPU cycles	320
Max CPU cycles	377
Avg CPU cycles	369

Test case: Inport test **OK**

Inport test for Math block Average.

Test results				
Time step	1	2	...	113
CPU cycles	320	345	...	367
Inputs				
In (DSP)	0.137	-0.115	...	0.082
In	0.137	-0.115	...	0.082
Parameters				
n	32			
ts_fact	1			
Outputs				
Out	0.004	0.001	...	0.528
Exp. Out	0.004	0.001	...	0.528
Out (DSP)	0.004	0.001	...	0.528
Exp. Out (DSP)	0.004	0.001	...	0.528

Test settings	
Tolerance Out	±4,6566e-07 (±1000 LSB)

Test statistics	
Min CPU cycles	320
Max CPU cycles	377
Avg CPU cycles	359

Test case: Conversion test **OK**

Conversion test for Math block Average.

Test results				
Time step	1	2	3	4
Mask parameters				
n	1	2	4	256
ts_fact	1	1	1	1
Controller parameters				
n	1	2	4	256
Exp. n	1	2	4	256

Test settings	
Tolerance n	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Math block Average.

Test results				
Time step	1	2	3	4
Mask parameters				
n	1	2	4	256
ts_fact	1	1	1	1
Controller parameters				
n	1	2	4	256
Exp. n	1	2	4	256

Test settings	
Tolerance n	±0,0000e+00

Test statistics	
Min CPU cycles	1360
Max CPU cycles	1361
Avg CPU cycles	1360

Verification: Average Float32 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for Math block Average.

Test results				
Time step	1	2	...	113
CPU cycles	1153	1170	...	1174
Inputs				
In (DSP)	-0.004	0.072	...	-0.031
In	-0.004	0.072	...	-0.031
Parameters				
n	1			
ts_fact	1			
Outputs				
Out	-0.004	0.072	...	-0.031
Exp. Out	-0.004	0.072	...	-0.031
Out (DSP)	-0.004	0.072	...	-0.031
Exp. Out (DSP)	-0.004	0.072	...	-0.031

Test settings	
Tolerance Out	±4,6566e-08 (±100 LSB)

Test statistics	
Min CPU cycles	1153
Max CPU cycles	1192
Avg CPU cycles	1174

Test case: Inport test OK

Inport test for Math block Average.

Test results				
Time step	1	2	...	113
CPU cycles	1137	1175	...	1218
Inputs				
In (DSP)	-0.128	0.01	...	-0.097
In	-0.128	0.01	...	-0.097
Parameters				
n	4			
ts_fact	1			
Outputs				
Out	-0.032	-0.029	...	0.091
Exp. Out	-0.032	-0.029	...	0.091
Out (DSP)	-0.032	-0.029	...	0.091
Exp. Out (DSP)	-0.032	-0.029	...	0.091

Test settings	
Tolerance Out	±6,9849e-07 (±1500 LSB)

Test statistics	
Min CPU cycles	1129
Max CPU cycles	1254
Avg CPU cycles	1203

Test case: Inport test **OK**

Inport test for Math block Average.

Test results				
Time step	1	2	...	113
CPU cycles	1091	1147	...	1263
Inputs				
In (DSP)	0.137	-0.115	...	0.082
In	0.137	-0.115	...	0.082
Parameters				
n	32			
ts_fact	1			
Outputs				
Out	0.004	0.001	...	0.528
Exp. Out	0.004	0.001	...	0.528
Out (DSP)	0.004	0.001	...	0.528
Exp. Out (DSP)	0.004	0.001	...	0.528

Test settings	
Tolerance Out	±4,6566e-07 (±1000 LSB)

Test statistics	
Min CPU cycles	1086
Max CPU cycles	1343
Avg CPU cycles	1208

Test case: Conversion test **OK**

Conversion test for Math block Average.

Test results				
Time step	1	2	3	4
Mask parameters				
n	1	2	4	256
ts_fact	1	1	1	1
Controller parameters				
n	1	2	4	256
Exp. n	1	2	4	256

Test settings	
Tolerance n	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Math block Average.

Test results				
Time step	1	2	3	4
Mask parameters				
n	1	2	4	256
ts_fact	1	1	1	1
Controller parameters				
n	1	2	4	256
Exp. n	1	2	4	256

Test settings	
Tolerance n	±0,0000e+00

Test statistics	
Min CPU cycles	2314
Max CPU cycles	2317
Avg CPU cycles	2315

Verification: Average Float32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for Math block Average.

Test results				
Time step	1	2	...	113
CPU cycles	114	99	...	99
Inputs				
In (DSP)	-0.004	0.072	...	-0.031
In	-0.004	0.072	...	-0.031
Parameters				
n	1			
ts_fact	1			
Outputs				
Out	-0.004	0.072	...	-0.031
Exp. Out	-0.004	0.072	...	-0.031
Out (DSP)	-0.004	0.072	...	-0.031
Exp. Out (DSP)	-0.004	0.072	...	-0.031

Test settings	
Tolerance Out	±4,6566e-08 (±100 LSB)

Test statistics	
Min CPU cycles	99
Max CPU cycles	114
Avg CPU cycles	99

Test case: Inport test OK

Inport test for Math block Average.

Test results				
Time step	1	2	...	113
CPU cycles	99	99	...	99
Inputs				
In (DSP)	-0.128	0.01	...	-0.097
In	-0.128	0.01	...	-0.097
Parameters				
n	4			
ts_fact	1			
Outputs				
Out	-0.032	-0.029	...	0.091
Exp. Out	-0.032	-0.029	...	0.091
Out (DSP)	-0.032	-0.029	...	0.091
Exp. Out (DSP)	-0.032	-0.029	...	0.091

Test settings	
Tolerance Out	±6,9849e-07 (±1500 LSB)

Test statistics	
Min CPU cycles	99
Max CPU cycles	99
Avg CPU cycles	99

Test case: Inport test **OK**

Inport test for Math block Average.

Test results				
Time step	1	2	...	113
CPU cycles	99	99	...	99
Inputs				
In (DSP)	0.137	-0.115	...	0.082
In	0.137	-0.115	...	0.082
Parameters				
n	32			
ts_fact	1			
Outputs				
Out	0.004	0.001	...	0.528
Exp. Out	0.004	0.001	...	0.528
Out (DSP)	0.004	0.001	...	0.528
Exp. Out (DSP)	0.004	0.001	...	0.528

Test settings	
Tolerance Out	±4,6566e-07 (±1000 LSB)

Test statistics	
Min CPU cycles	99
Max CPU cycles	99
Avg CPU cycles	99

Test case: Conversion test **OK**

Conversion test for Math block Average.

Test results				
Time step	1	2	3	4
Mask parameters				
n	1	2	4	256
ts_fact	1	1	1	1
Controller parameters				
n	1	2	4	256
Exp. n	1	2	4	256

Test settings	
Tolerance n	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Math block Average.

Test results				
Time step	1	2	3	4
Mask parameters				
n	1	2	4	256
ts_fact	1	1	1	1
Controller parameters				
n	1	2	4	256
Exp. n	1	2	4	256

Test settings	
Tolerance n	±0,0000e+00

Test statistics	
Min CPU cycles	1771
Max CPU cycles	1859
Avg CPU cycles	1797

Verification: Average Float32 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test

OK

Inport test for Math block Average.

Test results				
Time step	1	2	...	113
CPU cycles	335	335	...	335
Inputs				
In (DSP)	-0.004	0.072	...	-0.031
In	-0.004	0.072	...	-0.031
Parameters				
n	1			
ts_fact	1			
Outputs				
Out	-0.004	0.072	...	-0.031
Exp. Out	-0.004	0.072	...	-0.031
Out (DSP)	-0.004	0.072	...	-0.031
Exp. Out (DSP)	-0.004	0.072	...	-0.031

Test settings	
Tolerance Out	±4,6566e-08 (±100 LSB)

Test statistics	
Min CPU cycles	335
Max CPU cycles	335
Avg CPU cycles	335

Test case: Inport test

OK

Inport test for Math block Average.

Test results				
Time step	1	2	...	113
CPU cycles	341	341	...	341
Inputs				
In (DSP)	-0.128	0.01	...	-0.097
In	-0.128	0.01	...	-0.097
Parameters				
n	4			
ts_fact	1			
Outputs				
Out	-0.032	-0.029	...	0.091
Exp. Out	-0.032	-0.029	...	0.091
Out (DSP)	-0.032	-0.029	...	0.091
Exp. Out (DSP)	-0.032	-0.029	...	0.091

Test settings	
Tolerance Out	±6,9849e-07 (±1500 LSB)

Test statistics	
Min CPU cycles	335
Max CPU cycles	341
Avg CPU cycles	339

Test case: Inport test **OK**

Inport test for Math block Average.

Test results				
Time step	1	2	...	113
CPU cycles	341	341	...	341
Inputs				
In (DSP)	0.137	-0.115	...	0.082
In	0.137	-0.115	...	0.082
Parameters				
n	32			
ts_fact	1			
Outputs				
Out	0.004	0.001	...	0.528
Exp. Out	0.004	0.001	...	0.528
Out (DSP)	0.004	0.001	...	0.528
Exp. Out (DSP)	0.004	0.001	...	0.528

Test settings	
Tolerance Out	±4,6566e-07 (±1000 LSB)

Test statistics	
Min CPU cycles	335
Max CPU cycles	341
Avg CPU cycles	340

Test case: Conversion test **OK**

Conversion test for Math block Average.

Test results				
Time step	1	2	3	4
Mask parameters				
n	1	2	4	256
ts_fact	1	1	1	1
Controller parameters				
n	1	2	4	256
Exp. n	1	2	4	256

Test settings	
Tolerance n	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Math block Average.

Test results				
Time step	1	2	3	4
Mask parameters				
n	1	2	4	256
ts_fact	1	1	1	1
Controller parameters				
n	1	2	4	256
Exp. n	1	2	4	256

Test settings	
Tolerance n	±0,0000e+00

Test statistics	
Min CPU cycles	5899
Max CPU cycles	5924
Avg CPU cycles	5913

Block: Cos



Cosine computation of input value.

Inports	
In	Input u

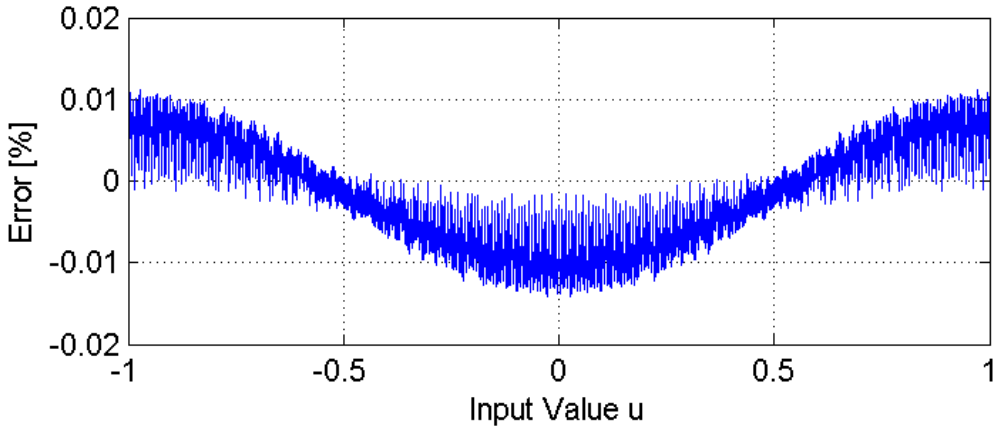
Outports	
Out	Result of cos(u)

Description:

Calculation:

$$\mathrm{Out} = \cos\left(\mathrm{In}\right)$$

Error for 16 Bit Fixed Point Implementation:



Implementations:

FiP8	8 Bit Fixed Point Implementation
FiP16	16 Bit Fixed Point Implementation
FiP32	32 Bit Fixed Point Implementation
Float32	32 Bit Floating Point Implementation
Float64	64 Bit Floating Point Implementation

Implementation: FiP8

8 Bit Fixed Point Implementation

Inports Data Type	
In	int8

Outports Data Type	
Out	int8

Implementation: FiP16

16 Bit Fixed Point Implementation

Inports Data Type	
In	int16

Outports Data Type	
Out	int16

Implementation: FiP32

32 Bit Fixed Point Implementation

Inports Data Type	
In	int32

Outports Data Type	
Out	int32

Implementation: Float32

32 Bit Floating Point Implementation

Inports Data Type	
In	float32

Outports Data Type	
Out	float32

Implementation: Float64

64 Bit Floating Point Implementation

Inports Data Type	
In	float64

Outports Data Type	
Out	float64

Verification: Cos FiP16 CPU TMS320F28335

Date of Test 2026-06-19

Target controller TMS320F28335

Test case: Inport test OK

Inport test for Math block Cos.

Test results						
Time step	1	2	3	4	...	133
CPU cycles	76	76	76	76	...	76
Inputs						
In (DSP)	-32768	-32272	-31775	-31279	...	32767
In	-1	-0.985	-0.97	-0.955	...	1
Outputs						
Out	-1	-0.999	-0.995	-0.99	...	-1
Exp. Out	-1	-0.999	-0.995	-0.99	...	-1
Out (DSP)	-32767	-32730	-32618	-32433	...	-32767
Exp. Out (DSP)	-32768	-32731	-32620	-32434	...	-32768

Test settings	
Tolerance Out	±1,2207e-04 (±4 LSB)

Test statistics	
Min CPU cycles	76
Max CPU cycles	76
Avg CPU cycles	76

Verification: Cos FiP16 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for Math block Cos.

Test results						
Time step	1	2	3	4	...	133
CPU cycles	59	59	59	59	...	59
Inputs						
In (DSP)	-32768	-32272	-31775	-31279	...	32767
In	-1	-0.985	-0.97	-0.955	...	1
Outputs						
Out	-1	-0.999	-0.995	-0.99	...	-1
Exp. Out	-1	-0.999	-0.995	-0.99	...	-1
Out (DSP)	-32767	-32730	-32618	-32433	...	-32767
Exp. Out (DSP)	-32768	-32731	-32620	-32434	...	-32768

Test settings	
Tolerance Out	±1,2207e-04 (±4 LSB)

Test statistics	
Min CPU cycles	59
Max CPU cycles	59
Avg CPU cycles	59

Verification: Cos FiP16 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for Math block Cos.

Test results						
Time step	1	2	3	4	...	133
CPU cycles	96	96	96	96	...	96
Inputs						
In (DSP)	-32768	-32272	-31775	-31279	...	32767
In	-1	-0.985	-0.97	-0.955	...	1
Outputs						
Out	-1	-0.999	-0.995	-0.99	...	-1
Exp. Out	-1	-0.999	-0.995	-0.99	...	-1
Out (DSP)	-32767	-32730	-32618	-32433	...	-32767
Exp. Out (DSP)	-32768	-32731	-32620	-32434	...	-32768

Test settings	
Tolerance Out	±1,2207e-04 (±4 LSB)

Test statistics	
Min CPU cycles	96
Max CPU cycles	101
Avg CPU cycles	97

Verification: Cos FiP16 CPU STM32F072RB

Date of Test 2026-06-19

Target controller STM32F072RB

Test case: Inport test OK

Inport test for Math block Cos.

Test results						
Time step	1	2	3	4	...	133
CPU cycles	75	75	75	75	...	75
Inputs						
In (DSP)	-32768	-32272	-31775	-31279	...	32767
In	-1	-0.985	-0.97	-0.955	...	1
Outputs						
Out	-1	-0.999	-0.995	-0.99	...	-1
Exp. Out	-1	-0.999	-0.995	-0.99	...	-1
Out (DSP)	-32767	-32730	-32618	-32433	...	-32767
Exp. Out (DSP)	-32768	-32731	-32620	-32434	...	-32768

Test settings	
Tolerance Out	±1,2207e-04 (±4 LSB)

Test statistics	
Min CPU cycles	75
Max CPU cycles	75
Avg CPU cycles	75

Verification: Cos FiP16 CPU PIC32MX170F256

Date of Test 2026-06-19

Target controller PIC32MX170F256

Test case: Inport test OK

Inport test for Math block Cos.

Test results						
Time step	1	2	3	4	...	133
CPU cycles	50	50	50	50	...	50
Inputs						
In (DSP)	-32768	-32272	-31775	-31279	...	32767
In	-1	-0.985	-0.97	-0.955	...	1
Outputs						
Out	-1	-0.999	-0.995	-0.99	...	-1
Exp. Out	-1	-0.999	-0.995	-0.99	...	-1
Out (DSP)	-32767	-32730	-32618	-32433	...	-32767
Exp. Out (DSP)	-32768	-32731	-32620	-32434	...	-32768

Test settings	
Tolerance Out	±1,2207e-04 (±4 LSB)

Test statistics	
Min CPU cycles	50
Max CPU cycles	50
Avg CPU cycles	50

Verification: Cos FiP16 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for Math block Cos.

Test results						
Time step	1	2	3	4	...	133
CPU cycles	62	62	62	62	...	62
Inputs						
In (DSP)	-32768	-32272	-31775	-31279	...	32767
In	-1	-0.985	-0.97	-0.955	...	1
Outputs						
Out	-1	-0.999	-0.995	-0.99	...	-1
Exp. Out	-1	-0.999	-0.995	-0.99	...	-1
Out (DSP)	-32767	-32730	-32618	-32433	...	-32767
Exp. Out (DSP)	-32768	-32731	-32620	-32434	...	-32768

Test settings	
Tolerance Out	±1,2207e-04 (±4 LSB)

Test statistics	
Min CPU cycles	62
Max CPU cycles	62
Avg CPU cycles	62

Verification: Cos FiP16 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for Math block Cos.

Test results						
Time step	1	2	3	4	...	133
CPU cycles	94	89	89	89	...	89
Inputs						
In (DSP)	-32768	-32272	-31775	-31279	...	32767
In	-1	-0.985	-0.97	-0.955	...	1
Outputs						
Out	-1	-0.999	-0.995	-0.99	...	-1
Exp. Out	-1	-0.999	-0.995	-0.99	...	-1
Out (DSP)	-32767	-32730	-32618	-32433	...	-32767
Exp. Out (DSP)	-32768	-32731	-32620	-32434	...	-32768

Test settings	
Tolerance Out	±1,2207e-04 (±4 LSB)

Test statistics	
Min CPU cycles	89
Max CPU cycles	94
Avg CPU cycles	89

Verification: Cos FiP16 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for Math block Cos.

Test results						
Time step	1	2	3	4	...	133
CPU cycles	64	64	64	64	...	64
Inputs						
In (DSP)	-32768	-32272	-31775	-31279	...	32767
In	-1	-0.985	-0.97	-0.955	...	1
Outputs						
Out	-1	-0.999	-0.995	-0.99	...	-1
Exp. Out	-1	-0.999	-0.995	-0.99	...	-1
Out (DSP)	-32767	-32730	-32618	-32433	...	-32767
Exp. Out (DSP)	-32768	-32731	-32620	-32434	...	-32768

Test settings	
Tolerance Out	±1,2207e-04 (±4 LSB)

Test statistics	
Min CPU cycles	64
Max CPU cycles	69
Avg CPU cycles	64

Verification: Cos FiP32 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for Math block Cos.

Test results				
Time step	1	2	...	133
CPU cycles	88	88	...	88
Inputs				
In (DSP)	-2147483648	-2114946017	...	2147483647
In	-1	-0.985	...	1
Outputs				
Out	-1	-0.999	...	-1
Exp. Out	-1	-0.999	...	-1
Out (DSP)	-2147483647	-2145014483	...	-2147483647
Exp. Out (DSP)	-2147483648	-2145051277	...	-2147483648

Test settings	
Tolerance Out	±6,9849e-05 (±150000 LSB)

Test statistics	
Min CPU cycles	88
Max CPU cycles	88
Avg CPU cycles	88

Verification: Cos FiP32 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test — OK

Inport test for Math block Cos.

Test results				
Time step	1	2	...	133
CPU cycles	53	53	...	53
Inputs				
In (DSP)	-2147483648	-2114946017	...	2147483647
In	-1	-0.985	...	1
Outputs				
Out	-1	-0.999	...	-1
Exp. Out	-1	-0.999	...	-1
Out (DSP)	-2147483647	-2145014483	...	-2147483647
Exp. Out (DSP)	-2147483648	-2145051277	...	-2147483648

Test settings	
Tolerance Out	±6,9849e-05 (±150000 LSB)

Test statistics	
Min CPU cycles	53
Max CPU cycles	53
Avg CPU cycles	53

Verification: Cos FiP32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for Math block Cos.

Test results				
Time step	1	2	...	133
CPU cycles	91	91	...	91
Inputs				
In (DSP)	-2147483648	-2114946017	...	2147483647
In	-1	-0.985	...	1
Outputs				
Out	-1	-0.999	...	-1
Exp. Out	-1	-0.999	...	-1
Out (DSP)	-2147483647	-2145014483	...	-2147483647
Exp. Out (DSP)	-2147483648	-2145051277	...	-2147483648

Test settings	
Tolerance Out	±6,9849e-05 (±150000 LSB)

Test statistics	
Min CPU cycles	91
Max CPU cycles	96
Avg CPU cycles	93

Verification: Cos FiP32 CPU STM32F072RB

Date of Test 2026-06-19

Target controller STM32F072RB

Test case: Inport test OK

Inport test for Math block Cos.

Test results				
Time step	1	2	...	133
CPU cycles	148	148	...	148
Inputs				
In (DSP)	-2147483648	-2114946017	...	2147483647
In	-1	-0.985	...	1
Outputs				
Out	-1	-0.999	...	-1
Exp. Out	-1	-0.999	...	-1
Out (DSP)	-2147483647	-2145014483	...	-2147483647
Exp. Out (DSP)	-2147483648	-2145051277	...	-2147483648

Test settings	
Tolerance Out	±6,9849e-05 (±150000 LSB)

Test statistics	
Min CPU cycles	148
Max CPU cycles	148
Avg CPU cycles	148

Verification: Cos FiP32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for Math block Cos.

Test results				
Time step	1	2	...	133
CPU cycles	52	53	...	52
Inputs				
In (DSP)	-2147483648	-2114946017	...	2147483647
In	-1	-0.985	...	1
Outputs				
Out	-1	-0.999	...	-1
Exp. Out	-1	-0.999	...	-1
Out (DSP)	-2147483647	-2145014483	...	-2147483647
Exp. Out (DSP)	-2147483648	-2145051277	...	-2147483648

Test settings	
Tolerance Out	±6,9849e-05 (±150000 LSB)

Test statistics	
Min CPU cycles	52
Max CPU cycles	53
Avg CPU cycles	52

Verification: Cos FiP32 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test — OK

Inport test for Math block Cos.

Test results				
Time step	1	2	...	133
CPU cycles	204	211	...	204
Inputs				
In (DSP)	-2147483648	-2114946017	...	2147483647
In	-1	-0.985	...	1
Outputs				
Out	-1	-0.999	...	-1
Exp. Out	-1	-0.999	...	-1
Out (DSP)	-2147483647	-2145014483	...	-2147483647
Exp. Out (DSP)	-2147483648	-2145051277	...	-2147483648

Test settings	
Tolerance Out	±6,9849e-05 (±150000 LSB)

Test statistics	
Min CPU cycles	204
Max CPU cycles	211
Avg CPU cycles	207

Verification: Cos FiP32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for Math block Cos.

Test results				
Time step	1	2	...	133
CPU cycles	106	100	...	100
Inputs				
In (DSP)	-2147483648	-2114946017	...	2147483647
In	-1	-0.985	...	1
Outputs				
Out	-1	-0.999	...	-1
Exp. Out	-1	-0.999	...	-1
Out (DSP)	-2147483647	-2145014483	...	-2147483647
Exp. Out (DSP)	-2147483648	-2145051277	...	-2147483648

Test settings	
Tolerance Out	±6,9849e-05 (±150000 LSB)

Test statistics	
Min CPU cycles	100
Max CPU cycles	106
Avg CPU cycles	100

Verification: Cos FiP32 CPU TMS320F28379D

Date of Test 2026-06-22

Target controller TMS320F28379D

Test case: Inport test OK

Inport test for Math block Cos.

Test results				
Time step	1	2	...	133
CPU cycles	74	74	...	74
Inputs				
In (DSP)	-2147483648	-2114946017	...	2147483647
In	-1	-0.985	...	1
Outputs				
Out	-1	-0.999	...	-1
Exp. Out	-1	-0.999	...	-1
Out (DSP)	-2147483647	-2145014483	...	-2147483647
Exp. Out (DSP)	-2147483648	-2145051277	...	-2147483648

Test settings	
Tolerance Out	±6,9849e-05 (±150000 LSB)

Test statistics	
Min CPU cycles	74
Max CPU cycles	77
Avg CPU cycles	74

Verification: Cos Float32 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for Math block Cos.

Test results				
Time step	1	2	...	133
CPU cycles	234	227	...	234
Inputs				
In (DSP)	-3.142	-3.094	...	3.142
In	-3.142	-3.094	...	3.142
Outputs				
Out	-1	-0.999	...	-1
Exp. Out	-1	-0.999	...	-1
Out (DSP)	-1	-0.999	...	-1
Exp. Out (DSP)	-1	-0.999	...	-1

Test settings	
Tolerance Out	±1,3970e-07 (±300 LSB)

Test statistics	
Min CPU cycles	95
Max CPU cycles	234
Avg CPU cycles	226

Verification: Cos Float32 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for Math block Cos.

Test results				
Time step	1	2	...	133
CPU cycles	119	119	...	119
Inputs				
In (DSP)	-3.142	-3.094	...	3.142
In	-3.142	-3.094	...	3.142
Outputs				
Out	-1	-0.999	...	-1
Exp. Out	-1	-0.999	...	-1
Out (DSP)	-1	-0.999	...	-1
Exp. Out (DSP)	-1	-0.999	...	-1

Test settings	
Tolerance Out	±1,3970e-07 (±300 LSB)

Test statistics	
Min CPU cycles	53
Max CPU cycles	119
Avg CPU cycles	118

Verification: Cos Float32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for Math block Cos.

Test results				
Time step	1	2	...	133
CPU cycles	518	473	...	510
Inputs				
In (DSP)	-3.142	-3.094	...	3.142
In	-3.142	-3.094	...	3.142
Outputs				
Out	-1	-0.999	...	-1
Exp. Out	-1	-0.999	...	-1
Out (DSP)	-1	-0.999	...	-1
Exp. Out (DSP)	-1	-0.999	...	-1

Test settings	
Tolerance Out	±1,3970e-07 (±300 LSB)

Test statistics	
Min CPU cycles	144
Max CPU cycles	518
Avg CPU cycles	362

Verification: Cos Float32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for Math block Cos.

Test results				
Time step	1	2	...	133
CPU cycles	5454	4578	...	5439
Inputs				
In (DSP)	-3.142	-3.094	...	3.142
In	-3.142	-3.094	...	3.142
Outputs				
Out	-1	-0.999	...	-1
Exp. Out	-1	-0.999	...	-1
Out (DSP)	-1	-0.999	...	-1
Exp. Out (DSP)	-1	-0.999	...	-1

Test settings	
Tolerance Out	±1,3970e-07 (±300 LSB)

Test statistics	
Min CPU cycles	154
Max CPU cycles	5454
Avg CPU cycles	3818

Verification: Cos Float32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for Math block Cos.

Test results				
Time step	1	2	...	133
CPU cycles	435	266	...	435
Inputs				
In (DSP)	-3.142	-3.094	...	3.142
In	-3.142	-3.094	...	3.142
Outputs				
Out	-1	-0.999	...	-1
Exp. Out	-1	-0.999	...	-1
Out (DSP)	-1	-0.999	...	-1
Exp. Out (DSP)	-1	-0.999	...	-1

Test settings	
Tolerance Out	±1,3970e-07 (±300 LSB)

Test statistics	
Min CPU cycles	140
Max CPU cycles	435
Avg CPU cycles	214

Verification: Cos Float32 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for Math block Cos.

Test results				
Time step	1	2	...	133
CPU cycles	3796	3833	...	3796
Inputs				
In (DSP)	-3.142	-3.094	...	3.142
In	-3.142	-3.094	...	3.142
Outputs				
Out	-1	-0.999	...	-1
Exp. Out	-1	-0.999	...	-1
Out (DSP)	-1	-0.999	...	-1
Exp. Out (DSP)	-1	-0.999	...	-1

Test settings	
Tolerance Out	±1,3970e-07 (±300 LSB)

Test statistics	
Min CPU cycles	107
Max CPU cycles	4226
Avg CPU cycles	3884

Verification: Cos Float32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for Math block Cos.

Test results				
Time step	1	2	...	133
CPU cycles	435	338	...	381
Inputs				
In (DSP)	-3.142	-3.094	...	3.142
In	-3.142	-3.094	...	3.142
Outputs				
Out	-1	-0.999	...	-1
Exp. Out	-1	-0.999	...	-1
Out (DSP)	-1	-0.999	...	-1
Exp. Out (DSP)	-1	-0.999	...	-1

Test settings	
Tolerance Out	±1,3970e-07 (±300 LSB)

Test statistics	
Min CPU cycles	131
Max CPU cycles	435
Avg CPU cycles	245

Verification: Cos Float32 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for Math block Cos.

Test results				
Time step	1	2	...	133
CPU cycles	143	138	...	143
Inputs				
In (DSP)	-3.142	-3.094	...	3.142
In	-3.142	-3.094	...	3.142
Outputs				
Out	-1	-0.999	...	-1
Exp. Out	-1	-0.999	...	-1
Out (DSP)	-1	-0.999	...	-1
Exp. Out (DSP)	-1	-0.999	...	-1

Test settings	
Tolerance Out	±1,3970e-07 (±300 LSB)

Test statistics	
Min CPU cycles	82
Max CPU cycles	143
Avg CPU cycles	137

Block: Div



Division of input Num by input Den.

Inports	
Num	Dividend (Numerator)
Den	Divisor (Denominator)

Outports	
Out	Quotient

Description:

Calculation:

$$\mathrm{Out} = \begin{cases} 0 & \mathrm{Num} = 0, \mathrm{Den} = 0 \\ \max & \mathrm{Num} > 0, \mathrm{Den} = 0 \\ \min & \mathrm{Num} < 0, \mathrm{Den} = 0 \\ \frac{\mathrm{Num}}{\mathrm{Den}} & \mathrm{otherwise} \end{cases}$$

Note: *maxVal* and *minVal* refer to the maximum/minimum representable value of the implementation.

Implementations:

FiP8	8 Bit Fixed Point Implementation
FiP16	16 Bit Fixed Point Implementation
FiP32	32 Bit Fixed Point Implementation
Float32	32 Bit Floating Point Implementation
Float64	64 Bit Floating Point Implementation

Implementation: FiP8

8 Bit Fixed Point Implementation

Inports Data Type	
Num	int8
Den	int8

Outports Data Type	
Out	int8

Implementation: FiP16

16 Bit Fixed Point Implementation

Inports Data Type	
Num	int16
Den	int16

Outports Data Type	
Out	int16

Implementation: FiP32

32 Bit Fixed Point Implementation

Inports Data Type	
Num	int32
Den	int32

Outports Data Type	
Out	int32

Implementation: Float32

32 Bit Floating Point Implementation

Inports Data Type	
Num	float32
Den	float32

Outports Data Type	
Out	float32

Implementation: Float64

64 Bit Floating Point Implementation

Inports Data Type	
Num	float64
Den	float64

Outports Data Type	
Out	float64

Verification: Div FiP16 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for Math block Div.

Test results						
Time step	1	2	3	4	...	246
CPU cycles	100	111	157	112	...	111
Inputs						
Num (DSP)	0	16384	0	-32768	...	32767
Den (DSP)	0	0	16384	32767	...	32767
Num	0	0.5	0	-1	...	1
Den	0	0	0.5	1	...	1
Outputs						
Out	0	1	0	-1	...	1
Exp. Out	0	1	0	-1	...	1
Out (DSP)	0	32767	0	-32767	...	32767
Exp. Out (DSP)	0	32767	0	-32768	...	32767

Test settings	
Tolerance Out	±1,2207e-04 (±4 LSB)

Test statistics	
Min CPU cycles	100
Max CPU cycles	157
Avg CPU cycles	129

Verification: Div FiP16 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test — OK

Inport test for Math block Div.

Test results						
Time step	1	2	3	4	...	246
CPU cycles	59	65	57	63	...	65
Inputs						
Num (DSP)	0	16384	0	-32768	...	32767
Den (DSP)	0	0	16384	32767	...	32767
Num	0	0.5	0	-1	...	1
Den	0	0	0.5	1	...	1
Outputs						
Out	0	1	0	-1	...	1
Exp. Out	0	1	0	-1	...	1
Out (DSP)	0	32767	0	-32767	...	32767
Exp. Out (DSP)	0	32767	0	-32768	...	32767

Test settings	
Tolerance Out	±1,2207e-04 (±4 LSB)

Test statistics	
Min CPU cycles	57
Max CPU cycles	75
Avg CPU cycles	65

Verification: Div FiP16 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for Math block Div.

Test results						
Time step	1	2	3	4	...	246
CPU cycles	96	97	96	114	...	97
Inputs						
Num (DSP)	0	16384	0	-32768	...	32767
Den (DSP)	0	0	16384	32767	...	32767
Num	0	0.5	0	-1	...	1
Den	0	0	0.5	1	...	1
Outputs						
Out	0	1	0	-1	...	1
Exp. Out	0	1	0	-1	...	1
Out (DSP)	0	32767	0	-32767	...	32767
Exp. Out (DSP)	0	32767	0	-32768	...	32767

Test settings	
Tolerance Out	±1,2207e-04 (±4 LSB)

Test statistics	
Min CPU cycles	87
Max CPU cycles	146
Avg CPU cycles	113

Verification: Div FiP16 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for Math block Div.

Test results						
Time step	1	2	3	4	...	246
CPU cycles	88	106	103	113	...	106
Inputs						
Num (DSP)	0	16384	0	-32768	...	32767
Den (DSP)	0	0	16384	32767	...	32767
Num	0	0.5	0	-1	...	1
Den	0	0	0.5	1	...	1
Outputs						
Out	0	1	0	-1	...	1
Exp. Out	0	1	0	-1	...	1
Out (DSP)	0	32767	0	-32767	...	32767
Exp. Out (DSP)	0	32767	0	-32768	...	32767

Test settings	
Tolerance Out	±1,2207e-04 (±4 LSB)

Test statistics	
Min CPU cycles	88
Max CPU cycles	280
Avg CPU cycles	135

Verification: Div FiP16 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test — OK

Inport test for Math block Div.

Test results						
Time step	1	2	3	4	...	246
CPU cycles	46	50	56	51	...	50
Inputs						
Num (DSP)	0	16384	0	-32768	...	32767
Den (DSP)	0	0	16384	32767	...	32767
Num	0	0.5	0	-1	...	1
Den	0	0	0.5	1	...	1
Outputs						
Out	0	1	0	-1	...	1
Exp. Out	0	1	0	-1	...	1
Out (DSP)	0	32767	0	-32767	...	32767
Exp. Out (DSP)	0	32767	0	-32768	...	32767

Test settings	
Tolerance Out	±1,2207e-04 (±4 LSB)

Test statistics	
Min CPU cycles	36
Max CPU cycles	81
Avg CPU cycles	56

Verification: Div FiP16 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test

OK

Inport test for Math block Div.

Test results						
Time step	1	2	3	4	...	246
CPU cycles	68	64	86	75	...	64
Inputs						
Num (DSP)	0	16384	0	-32768	...	32767
Den (DSP)	0	0	16384	32767	...	32767
Num	0	0.5	0	-1	...	1
Den	0	0	0.5	1	...	1
Outputs						
Out	0	1	0	-1	...	1
Exp. Out	0	1	0	-1	...	1
Out (DSP)	0	32767	0	-32767	...	32767
Exp. Out (DSP)	0	32767	0	-32768	...	32767

Test settings	
Tolerance Out	±1,2207e-04 (±4 LSB)

Test statistics	
Min CPU cycles	64
Max CPU cycles	91
Avg CPU cycles	75

Verification: Div FiP16 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for Math block Div.

Test results						
Time step	1	2	3	4	...	246
CPU cycles	125	89	87	80	...	89
Inputs						
Num (DSP)	0	16384	0	-32768	...	32767
Den (DSP)	0	0	16384	32767	...	32767
Num	0	0.5	0	-1	...	1
Den	0	0	0.5	1	...	1
Outputs						
Out	0	1	0	-1	...	1
Exp. Out	0	1	0	-1	...	1
Out (DSP)	0	32767	0	-32767	...	32767
Exp. Out (DSP)	0	32767	0	-32768	...	32767

Test settings	
Tolerance Out	±1,2207e-04 (±4 LSB)

Test statistics	
Min CPU cycles	76
Max CPU cycles	125
Avg CPU cycles	91

Verification: Div FiP16 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for Math block Div.

Test results						
Time step	1	2	3	4	...	246
CPU cycles	110	120	172	120	...	120
Inputs						
Num (DSP)	0	16384	0	-32768	...	32767
Den (DSP)	0	0	16384	32767	...	32767
Num	0	0.5	0	-1	...	1
Den	0	0	0.5	1	...	1
Outputs						
Out	0	1	0	-1	...	1
Exp. Out	0	1	0	-1	...	1
Out (DSP)	0	32767	0	-32767	...	32767
Exp. Out (DSP)	0	32767	0	-32768	...	32767

Test settings	
Tolerance Out	±1,2207e-04 (±4 LSB)

Test statistics	
Min CPU cycles	110
Max CPU cycles	173
Avg CPU cycles	141

Verification: Div FiP32 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for Math block Div.

Test results				
Time step	1	2	...	246
CPU cycles	112	126	...	126
Inputs				
Num (DSP)	0	1073741824	...	2147483647
Den (DSP)	0	0	...	2147483647
Num	0	0.5	...	1
Den	0	0	...	1
Outputs				
Out	0	1	...	1
Exp. Out	0	1	...	1
Out (DSP)	0	2147483647	...	2147483647
Exp. Out (DSP)	0	2147483647	...	2147483647

Test settings	
Tolerance Out	±1,8626e-09 (±4 LSB)

Test statistics	
Min CPU cycles	112
Max CPU cycles	327
Avg CPU cycles	180

Verification: Div FiP32 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for Math block Div.

Test results				
Time step	1	2	...	246
CPU cycles	61	63	...	63
Inputs				
Num (DSP)	0	1073741824	...	2147483647
Den (DSP)	0	0	...	2147483647
Num	0	0.5	...	1
Den	0	0	...	1
Outputs				
Out	0	1	...	1
Exp. Out	0	1	...	1
Out (DSP)	0	2147483647	...	2147483647
Exp. Out (DSP)	0	2147483647	...	2147483647

Test settings	
Tolerance Out	±1,8626e-09 (±4 LSB)

Test statistics	
Min CPU cycles	61
Max CPU cycles	583
Avg CPU cycles	188

Verification: Div FiP32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for Math block Div.

Test results				
Time step	1	2	...	246
CPU cycles	105	109	...	109
Inputs				
Num (DSP)	0	1073741824	...	2147483647
Den (DSP)	0	0	...	2147483647
Num	0	0.5	...	1
Den	0	0	...	1
Outputs				
Out	0	1	...	1
Exp. Out	0	1	...	1
Out (DSP)	0	2147483647	...	2147483647
Exp. Out (DSP)	0	2147483647	...	2147483647

Test settings	
Tolerance Out	±1,8626e-09 (±4 LSB)

Test statistics	
Min CPU cycles	100
Max CPU cycles	325
Avg CPU cycles	184

Verification: Div FiP32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for Math block Div.

Test results				
Time step	1	2	...	246
CPU cycles	84	95	...	95
Inputs				
Num (DSP)	0	1073741824	...	2147483647
Den (DSP)	0	0	...	2147483647
Num	0	0.5	...	1
Den	0	0	...	1
Outputs				
Out	0	1	...	1
Exp. Out	0	1	...	1
Out (DSP)	0	2147483647	...	2147483647
Exp. Out (DSP)	0	2147483647	...	2147483647

Test settings	
Tolerance Out	±1,8626e-09 (±4 LSB)

Test statistics	
Min CPU cycles	84
Max CPU cycles	989
Avg CPU cycles	316

Verification: Div FiP32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for Math block Div.

Test results				
Time step	1	2	...	246
CPU cycles	46	52	...	52
Inputs				
Num (DSP)	0	1073741824	...	2147483647
Den (DSP)	0	0	...	2147483647
Num	0	0.5	...	1
Den	0	0	...	1
Outputs				
Out	0	1	...	1
Exp. Out	0	1	...	1
Out (DSP)	0	2147483647	...	2147483647
Exp. Out (DSP)	0	2147483647	...	2147483647

Test settings	
Tolerance Out	±1,8626e-09 (±4 LSB)

Test statistics	
Min CPU cycles	37
Max CPU cycles	194
Avg CPU cycles	90

Verification: Div FiP32 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test

OK

Inport test for Math block Div.

Test results				
Time step	1	2	...	246
CPU cycles	82	81	...	81
Inputs				
Num (DSP)	0	1073741824	...	2147483647
Den (DSP)	0	0	...	2147483647
Num	0	0.5	...	1
Den	0	0	...	1
Outputs				
Out	0	1	...	1
Exp. Out	0	1	...	1
Out (DSP)	0	2147483647	...	2147483647
Exp. Out (DSP)	0	2147483647	...	2147483647

Test settings	
Tolerance Out	±1,8626e-09 (±4 LSB)

Test statistics	
Min CPU cycles	81
Max CPU cycles	9822
Avg CPU cycles	3490

Verification: Div FiP32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for Math block Div.

Test results				
Time step	1	2	...	246
CPU cycles	99	81	...	81
Inputs				
Num (DSP)	0	1073741824	...	2147483647
Den (DSP)	0	0	...	2147483647
Num	0	0.5	...	1
Den	0	0	...	1
Outputs				
Out	0	1	...	1
Exp. Out	0	1	...	1
Out (DSP)	0	2147483647	...	2147483647
Exp. Out (DSP)	0	2147483647	...	2147483647

Test settings	
Tolerance Out	±1,8626e-09 (±4 LSB)

Test statistics	
Min CPU cycles	71
Max CPU cycles	264
Avg CPU cycles	141

Verification: Div FiP32 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for Math block Div.

Test results				
Time step	1	2	...	246
CPU cycles	127	147	...	147
Inputs				
Num (DSP)	0	1073741824	...	2147483647
Den (DSP)	0	0	...	2147483647
Num	0	0.5	...	1
Den	0	0	...	1
Outputs				
Out	0	1	...	1
Exp. Out	0	1	...	1
Out (DSP)	0	2147483647	...	2147483647
Exp. Out (DSP)	0	2147483647	...	2147483647

Test settings	
Tolerance Out	±1,8626e-09 (±4 LSB)

Test statistics	
Min CPU cycles	127
Max CPU cycles	307
Avg CPU cycles	190

Verification: Div Float32 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for Math block Div.

Test results				
Time step	1	2	...	246
CPU cycles	85	83	...	328
Inputs				
Num (DSP)	0	0.5	...	1
Den (DSP)	0	0	...	1
Num	0	0.5	...	1
Den	0	0	...	1
Outputs				
Out	0	340282346638528860000000000000000000000	...	1
Exp. Out	0	340282346638528860000000000000000000000	...	1
Out (DSP)	0	340282346638528860000000000000000000000	...	1
Exp. Out (DSP)	0	340282346638528860000000000000000000000	...	1

Test settings	
Tolerance Out	±1,3970e-07 (±300 LSB)

Test statistics	
Min CPU cycles	83
Max CPU cycles	328
Avg CPU cycles	289

Verification: Div Float32 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for Math block Div.

Test results				
Time step	1	2	...	246
CPU cycles	49	43	...	55
Inputs				
Num (DSP)	0	0.5	...	1
Den (DSP)	0	0	...	1
Num	0	0.5	...	1
Den	0	0	...	1
Outputs				
Out	0	340282346638528860000000000000000000000	...	1
Exp. Out	0	340282346638528860000000000000000000000	...	1
Out (DSP)	0	340282346638528860000000000000000000000	...	1
Exp. Out (DSP)	0	340282346638528860000000000000000000000	...	1

Test settings	
Tolerance Out	±1,3970e-07 (±300 LSB)

Test statistics	
Min CPU cycles	43
Max CPU cycles	55
Avg CPU cycles	54

Verification: Div Float32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for Math block Div.

Test results				
Time step	1	2	...	246
CPU cycles	82	77	...	92
Inputs				
Num (DSP)	0	0.5	...	1
Den (DSP)	0	0	...	1
Num	0	0.5	...	1
Den	0	0	...	1
Outputs				
Out	0	340282346638528860000000000000000000000	...	1
Exp. Out	0	340282346638528860000000000000000000000	...	1
Out (DSP)	0	340282346638528860000000000000000000000	...	1
Exp. Out (DSP)	0	340282346638528860000000000000000000000	...	1

Test settings	
Tolerance Out	±1,3970e-07 (±300 LSB)

Test statistics	
Min CPU cycles	77
Max CPU cycles	98
Avg CPU cycles	91

Verification: Div Float32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for Math block Div.

Test results				
Time step	1	2	...	246
CPU cycles	283	218	...	688
Inputs				
Num (DSP)	0	0.5	...	1
Den (DSP)	0	0	...	1
Num	0	0.5	...	1
Den	0	0	...	1
Outputs				
Out	0	340282346638528860000000000000000000000	...	1
Exp. Out	0	340282346638528860000000000000000000000	...	1
Out (DSP)	0	340282346638528860000000000000000000000	...	1
Exp. Out (DSP)	0	340282346638528860000000000000000000000	...	1

Test settings	
Tolerance Out	±1,3970e-07 (±300 LSB)

Test statistics	
Min CPU cycles	218
Max CPU cycles	757
Avg CPU cycles	608

Verification: Div Float32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for Math block Div.

Test results				
Time step	1	2	...	246
CPU cycles	91	103	...	203
Inputs				
Num (DSP)	0	0.5	...	1
Den (DSP)	0	0	...	1
Num	0	0.5	...	1
Den	0	0	...	1
Outputs				
Out	0	340282346638528860000000000000000000000	...	1
Exp. Out	0	340282346638528860000000000000000000000	...	1
Out (DSP)	0	340282346638528860000000000000000000000	...	1
Exp. Out (DSP)	0	340282346638528860000000000000000000000	...	1

Test settings	
Tolerance Out	±1,3970e-07 (±300 LSB)

Test statistics	
Min CPU cycles	91
Max CPU cycles	228
Avg CPU cycles	198

Verification: Div Float32 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for Math block Div.

Test results				
Time step	1	2	...	246
CPU cycles	364	262	...	595
Inputs				
Num (DSP)	0	0.5	...	1
Den (DSP)	0	0	...	1
Num	0	0.5	...	1
Den	0	0	...	1
Outputs				
Out	0	340282346638528860000000000000000000000	...	1
Exp. Out	0	340282346638528860000000000000000000000	...	1
Out (DSP)	0	340282346638528860000000000000000000000	...	1
Exp. Out (DSP)	0	340282346638528860000000000000000000000	...	1

Test settings	
Tolerance Out	±1,3970e-07 (±300 LSB)

Test statistics	
Min CPU cycles	254
Max CPU cycles	658
Avg CPU cycles	553

Verification: Div Float32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for Math block Div.

Test results				
Time step	1	2	...	246
CPU cycles	87	75	...	82
Inputs				
Num (DSP)	0	0.5	...	1
Den (DSP)	0	0	...	1
Num	0	0.5	...	1
Den	0	0	...	1
Outputs				
Out	0	340282346638528860000000000000000000000	...	1
Exp. Out	0	340282346638528860000000000000000000000	...	1
Out (DSP)	0	340282346638528860000000000000000000000	...	1
Exp. Out (DSP)	0	340282346638528860000000000000000000000	...	1

Test settings	
Tolerance Out	±1,3970e-07 (±300 LSB)

Test statistics	
Min CPU cycles	72
Max CPU cycles	87
Avg CPU cycles	81

Verification: Div Float32 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for Math block Div.

Test results				
Time step	1	2	...	246
CPU cycles	87	88	...	306
Inputs				
Num (DSP)	0	0.5	...	1
Den (DSP)	0	0	...	1
Num	0	0.5	...	1
Den	0	0	...	1
Outputs				
Out	0	340282346638528860000000000000000000000	...	1
Exp. Out	0	340282346638528860000000000000000000000	...	1
Out (DSP)	0	340282346638528860000000000000000000000	...	1
Exp. Out (DSP)	0	340282346638528860000000000000000000000	...	1

Test settings	
Tolerance Out	±1,3970e-07 (±300 LSB)

Test statistics	
Min CPU cycles	87
Max CPU cycles	306
Avg CPU cycles	268

Block: Exp



Computation of the exponential of the input.

Inports	
In	Input u

Outports	
Out	Result of exp(u)

Description:

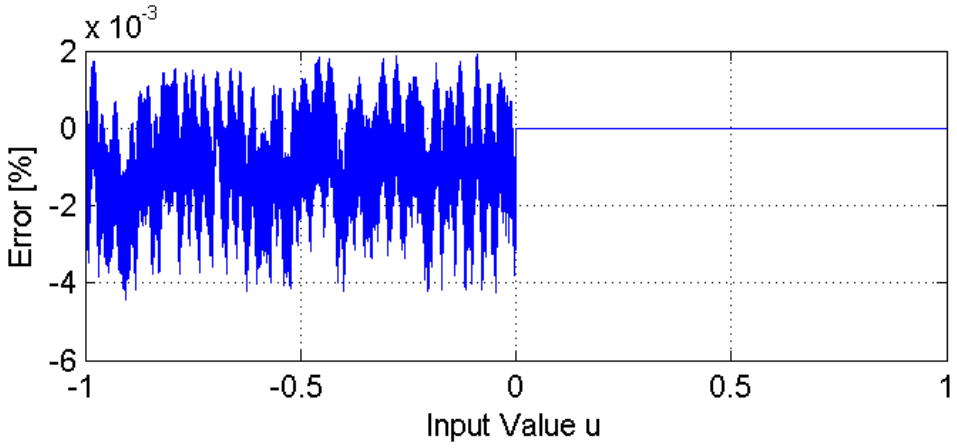
Calculation Floating Point Implementation:

$$\mathrm{Out} = \mathrm{e}^{\mathrm{In}}$$

Calculation Fixed Point Implementation:

$$\mathrm{Out} = \begin{cases} \mathrm{e}^{\mathrm{In}} & \mathrm{In} \leq 0 \\ 1 & \mathrm{In} > 0 \end{cases}$$

Error for 16 Bit Fixed Point Implementation:



Implementations:

FiP8	8 Bit Fixed Point Implementation
FiP16	16 Bit Fixed Point Implementation
FiP32	32 Bit Fixed Point Implementation
Float32	32 Bit Floating Point Implementation
Float64	64 Bit Floating Point Implementation

Implementation: FiP8

8 Bit Fixed Point Implementation

Inports Data Type	
In	int8

Outports Data Type	
Out	int8

Implementation: FiP16

16 Bit Fixed Point Implementation

Inports Data Type	
In	int16

Outports Data Type	
Out	int16

Implementation: FiP32

32 Bit Fixed Point Implementation

Inports Data Type	
In	int32

Outports Data Type	
Out	int32

Implementation: Float32

32 Bit Floating Point Implementation

Inports Data Type	
In	float32

Outports Data Type	
Out	float32

Implementation: Float64

64 Bit Floating Point Implementation

Inports Data Type	
In	float64

Outports Data Type	
Out	float64

Verification: Exp FiP16 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for Math block Exp.

Test results						
Time step	1	2	3	4	...	133
CPU cycles	85	85	85	85	...	59
Inputs						
In (DSP)	-32768	-32272	-31775	-31279	...	32767
In	-1	-0.985	-0.97	-0.955	...	1
Outputs						
Out	0.368	0.374	0.379	0.385	...	1
Exp. Out	0.368	0.373	0.379	0.385	...	1
Out (DSP)	12055	12239	12425	12615	...	32767
Exp. Out (DSP)	12055	12239	12426	12615	...	32767

Test settings	
Tolerance Out	±6,1035e-05 (±2 LSB)

Test statistics	
Min CPU cycles	59
Max CPU cycles	85
Avg CPU cycles	72

Verification: Exp FiP16 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for Math block Exp.

Test results						
Time step	1	2	3	4	...	133
CPU cycles	57	57	57	57	...	41
Inputs						
In (DSP)	-32768	-32272	-31775	-31279	...	32767
In	-1	-0.985	-0.97	-0.955	...	1
Outputs						
Out	0.368	0.374	0.379	0.385	...	1
Exp. Out	0.368	0.373	0.379	0.385	...	1
Out (DSP)	12055	12239	12425	12615	...	32767
Exp. Out (DSP)	12055	12239	12426	12615	...	32767

Test settings	
Tolerance Out	±6,1035e-05 (±2 LSB)

Test statistics	
Min CPU cycles	41
Max CPU cycles	57
Avg CPU cycles	49

Verification: Exp FiP16 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for Math block Exp.

Test results						
Time step	1	2	3	4	...	133
CPU cycles	92	92	97	92	...	66
Inputs						
In (DSP)	-32768	-32272	-31775	-31279	...	32767
In	-1	-0.985	-0.97	-0.955	...	1
Outputs						
Out	0.368	0.374	0.379	0.385	...	1
Exp. Out	0.368	0.373	0.379	0.385	...	1
Out (DSP)	12055	12239	12425	12615	...	32767
Exp. Out (DSP)	12055	12239	12426	12615	...	32767

Test settings	
Tolerance Out	±6,1035e-05 (±2 LSB)

Test statistics	
Min CPU cycles	66
Max CPU cycles	97
Avg CPU cycles	79

Verification: Exp FiP16 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for Math block Exp.

Test results						
Time step	1	2	3	4	...	133
CPU cycles	84	84	84	84	...	58
Inputs						
In (DSP)	-32768	-32272	-31775	-31279	...	32767
In	-1	-0.985	-0.97	-0.955	...	1
Outputs						
Out	0.368	0.374	0.379	0.385	...	1
Exp. Out	0.368	0.373	0.379	0.385	...	1
Out (DSP)	12055	12239	12425	12615	...	32767
Exp. Out (DSP)	12055	12239	12426	12615	...	32767

Test settings	
Tolerance Out	±6,1035e-05 (±2 LSB)

Test statistics	
Min CPU cycles	58
Max CPU cycles	84
Avg CPU cycles	71

Verification: Exp FiP16 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for Math block Exp.

Test results						
Time step	1	2	3	4	...	133
CPU cycles	52	52	52	52	...	30
Inputs						
In (DSP)	-32768	-32272	-31775	-31279	...	32767
In	-1	-0.985	-0.97	-0.955	...	1
Outputs						
Out	0.368	0.374	0.379	0.385	...	1
Exp. Out	0.368	0.373	0.379	0.385	...	1
Out (DSP)	12055	12239	12425	12615	...	32767
Exp. Out (DSP)	12055	12239	12426	12615	...	32767

Test settings	
Tolerance Out	±6,1035e-05 (±2 LSB)

Test statistics	
Min CPU cycles	30
Max CPU cycles	52
Avg CPU cycles	41

Verification: Exp FiP16 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for Math block Exp.

Test results						
Time step	1	2	3	4	...	133
CPU cycles	67	67	67	67	...	40
Inputs						
In (DSP)	-32768	-32272	-31775	-31279	...	32767
In	-1	-0.985	-0.97	-0.955	...	1
Outputs						
Out	0.368	0.374	0.379	0.385	...	1
Exp. Out	0.368	0.373	0.379	0.385	...	1
Out (DSP)	12055	12239	12425	12615	...	32767
Exp. Out (DSP)	12055	12239	12426	12615	...	32767

Test settings	
Tolerance Out	±6,1035e-05 (±2 LSB)

Test statistics	
Min CPU cycles	40
Max CPU cycles	67
Avg CPU cycles	53

Verification: Exp FiP16 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for Math block Exp.

Test results						
Time step	1	2	3	4	...	133
CPU cycles	101	94	94	94	...	59
Inputs						
In (DSP)	-32768	-32272	-31775	-31279	...	32767
In	-1	-0.985	-0.97	-0.955	...	1
Outputs						
Out	0.368	0.374	0.379	0.385	...	1
Exp. Out	0.368	0.373	0.379	0.385	...	1
Out (DSP)	12055	12239	12425	12615	...	32767
Exp. Out (DSP)	12055	12239	12426	12615	...	32767

Test settings	
Tolerance Out	±6,1035e-05 (±2 LSB)

Test statistics	
Min CPU cycles	59
Max CPU cycles	101
Avg CPU cycles	76

Verification: Exp FiP16 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for Math block Exp.

Test results						
Time step	1	2	3	4	...	133
CPU cycles	78	78	78	78	...	58
Inputs						
In (DSP)	-32768	-32272	-31775	-31279	...	32767
In	-1	-0.985	-0.97	-0.955	...	1
Outputs						
Out	0.368	0.374	0.379	0.385	...	1
Exp. Out	0.368	0.373	0.379	0.385	...	1
Out (DSP)	12055	12239	12425	12615	...	32767
Exp. Out (DSP)	12055	12239	12426	12615	...	32767

Test settings	
Tolerance Out	±6,1035e-05 (±2 LSB)

Test statistics	
Min CPU cycles	58
Max CPU cycles	81
Avg CPU cycles	68

Verification: Exp FiP32 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for Math block Exp.

Test results				
Time step	1	2	...	133
CPU cycles	97	97	...	61
Inputs				
In (DSP)	-2147483648	-2114946017	...	2147483647
In	-1	-0.985	...	1
Outputs				
Out	0.368	0.373	...	1
Exp. Out	0.368	0.373	...	1
Out (DSP)	790015084	802077541	...	2147483647
Exp. Out (DSP)	790015084	802076151	...	2147483647

Test settings	
Tolerance Out	±7,4506e-06 (±16000 LSB)

Test statistics	
Min CPU cycles	61
Max CPU cycles	97
Avg CPU cycles	79

Verification: Exp FiP32 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for Math block Exp.

Test results				
Time step	1	2	...	133
CPU cycles	55	55	...	39
Inputs				
In (DSP)	-2147483648	-2114946017	...	2147483647
In	-1	-0.985	...	1
Outputs				
Out	0.368	0.373	...	1
Exp. Out	0.368	0.373	...	1
Out (DSP)	790015084	802077541	...	2147483647
Exp. Out (DSP)	790015084	802076151	...	2147483647

Test settings	
Tolerance Out	±7,4506e-06 (±16000 LSB)

Test statistics	
Min CPU cycles	39
Max CPU cycles	55
Avg CPU cycles	47

Verification: Exp FiP32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for Math block Exp.

Test results				
Time step	1	2	...	133
CPU cycles	101	96	...	61
Inputs				
In (DSP)	-2147483648	-2114946017	...	2147483647
In	-1	-0.985	...	1
Outputs				
Out	0.368	0.373	...	1
Exp. Out	0.368	0.373	...	1
Out (DSP)	790015084	802077541	...	2147483647
Exp. Out (DSP)	790015084	802076151	...	2147483647

Test settings	
Tolerance Out	±7,4506e-06 (±16000 LSB)

Test statistics	
Min CPU cycles	61
Max CPU cycles	101
Avg CPU cycles	79

Verification: Exp FiP32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for Math block Exp.

Test results				
Time step	1	2	...	133
CPU cycles	155	155	...	62
Inputs				
In (DSP)	-2147483648	-2114946017	...	2147483647
In	-1	-0.985	...	1
Outputs				
Out	0.368	0.373	...	1
Exp. Out	0.368	0.373	...	1
Out (DSP)	790015084	802077541	...	2147483647
Exp. Out (DSP)	790015084	802076151	...	2147483647

Test settings	
Tolerance Out	±7,4506e-06 (±16000 LSB)

Test statistics	
Min CPU cycles	62
Max CPU cycles	155
Avg CPU cycles	108

Verification: Exp FiP32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for Math block Exp.

Test results				
Time step	1	2	...	133
CPU cycles	53	54	...	31
Inputs				
In (DSP)	-2147483648	-2114946017	...	2147483647
In	-1	-0.985	...	1
Outputs				
Out	0.368	0.373	...	1
Exp. Out	0.368	0.373	...	1
Out (DSP)	790015084	802077541	...	2147483647
Exp. Out (DSP)	790015084	802076151	...	2147483647

Test settings	
Tolerance Out	±7,4506e-06 (±16000 LSB)

Test statistics	
Min CPU cycles	31
Max CPU cycles	54
Avg CPU cycles	42

Verification: Exp FiP32 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test — OK

Inport test for Math block Exp.

Test results				
Time step	1	2	...	133
CPU cycles	207	207	...	60
Inputs				
In (DSP)	-2147483648	-2114946017	...	2147483647
In	-1	-0.985	...	1
Outputs				
Out	0.368	0.373	...	1
Exp. Out	0.368	0.373	...	1
Out (DSP)	790015084	802077541	...	2147483647
Exp. Out (DSP)	790015084	802076151	...	2147483647

Test settings	
Tolerance Out	±7,4506e-06 (±16000 LSB)

Test statistics	
Min CPU cycles	60
Max CPU cycles	207
Avg CPU cycles	134

Verification: Exp FiP32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for Math block Exp.

Test results				
Time step	1	2	...	133
CPU cycles	111	101	...	58
Inputs				
In (DSP)	-2147483648	-2114946017	...	2147483647
In	-1	-0.985	...	1
Outputs				
Out	0.368	0.373	...	1
Exp. Out	0.368	0.373	...	1
Out (DSP)	790015084	802077541	...	2147483647
Exp. Out (DSP)	790015084	802076151	...	2147483647

Test settings	
Tolerance Out	±7,4506e-06 (±16000 LSB)

Test statistics	
Min CPU cycles	58
Max CPU cycles	111
Avg CPU cycles	79

Verification: Exp FiP32 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for Math block Exp.

Test results				
Time step	1	2	...	133
CPU cycles	94	91	...	57
Inputs				
In (DSP)	-2147483648	-2114946017	...	2147483647
In	-1	-0.985	...	1
Outputs				
Out	0.368	0.373	...	1
Exp. Out	0.368	0.373	...	1
Out (DSP)	790015084	802077541	...	2147483647
Exp. Out (DSP)	790015084	802076151	...	2147483647

Test settings	
Tolerance Out	±7,4506e-06 (±16000 LSB)

Test statistics	
Min CPU cycles	57
Max CPU cycles	94
Avg CPU cycles	74

Verification: Exp Float32 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for Math block Exp.

Test results				
Time step	1	2	...	133
CPU cycles	615	615	...	615
Inputs				
In (DSP)	-1	-0.985	...	1
In	-1	-0.985	...	1
Outputs				
Out	0.368	0.373	...	2.718
Exp. Out	0.368	0.373	...	2.718
Out (DSP)	0.368	0.373	...	2.718
Exp. Out (DSP)	0.368	0.373	...	2.718

Test settings	
Tolerance Out	±2,3283e-07 (±500 LSB)

Test statistics	
Min CPU cycles	193
Max CPU cycles	615
Avg CPU cycles	582

Verification: Exp Float32 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for Math block Exp.

Test results				
Time step	1	2	...	133
CPU cycles	165	165	...	165
Inputs				
In (DSP)	-1	-0.985	...	1
In	-1	-0.985	...	1
Outputs				
Out	0.368	0.373	...	2.718
Exp. Out	0.368	0.373	...	2.718
Out (DSP)	0.368	0.373	...	2.718
Exp. Out (DSP)	0.368	0.373	...	2.718

Test settings	
Tolerance Out	±2,3283e-07 (±500 LSB)

Test statistics	
Min CPU cycles	89
Max CPU cycles	165
Avg CPU cycles	155

Verification: Exp Float32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for Math block Exp.

Test results				
Time step	1	2	...	133
CPU cycles	398	398	...	398
Inputs				
In (DSP)	-1	-0.985	...	1
In	-1	-0.985	...	1
Outputs				
Out	0.368	0.373	...	2.718
Exp. Out	0.368	0.373	...	2.718
Out (DSP)	0.368	0.373	...	2.718
Exp. Out (DSP)	0.368	0.373	...	2.718

Test settings	
Tolerance Out	±2,3283e-07 (±500 LSB)

Test statistics	
Min CPU cycles	288
Max CPU cycles	398
Avg CPU cycles	385

Verification: Exp Float32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for Math block Exp.

Test results				
Time step	1	2	...	133
CPU cycles	3759	3824	...	3762
Inputs				
In (DSP)	-1	-0.985	...	1
In	-1	-0.985	...	1
Outputs				
Out	0.368	0.373	...	2.718
Exp. Out	0.368	0.373	...	2.718
Out (DSP)	0.368	0.373	...	2.718
Exp. Out (DSP)	0.368	0.373	...	2.718

Test settings	
Tolerance Out	±2,3283e-07 (±500 LSB)

Test statistics	
Min CPU cycles	613
Max CPU cycles	3867
Avg CPU cycles	3602

Verification: Exp Float32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for Math block Exp.

Test results				
Time step	1	2	...	133
CPU cycles	254	249	...	252
Inputs				
In (DSP)	-1	-0.985	...	1
In	-1	-0.985	...	1
Outputs				
Out	0.368	0.373	...	2.718
Exp. Out	0.368	0.373	...	2.718
Out (DSP)	0.368	0.373	...	2.718
Exp. Out (DSP)	0.368	0.373	...	2.718

Test settings	
Tolerance Out	±2,3283e-07 (±500 LSB)

Test statistics	
Min CPU cycles	114
Max CPU cycles	257
Avg CPU cycles	249

Verification: Exp Float32 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for Math block Exp.

Test results				
Time step	1	2	...	133
CPU cycles	4035	3980	...	4019
Inputs				
In (DSP)	-1	-0.985	...	1
In	-1	-0.985	...	1
Outputs				
Out	0.368	0.373	...	2.718
Exp. Out	0.368	0.373	...	2.718
Out (DSP)	0.368	0.373	...	2.718
Exp. Out (DSP)	0.368	0.373	...	2.718

Test settings	
Tolerance Out	±2,3283e-07 (±500 LSB)

Test statistics	
Min CPU cycles	400
Max CPU cycles	4430
Avg CPU cycles	3816

Verification: Exp Float32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for Math block Exp.

Test results				
Time step	1	2	...	133
CPU cycles	460	345	...	329
Inputs				
In (DSP)	-1	-0.985	...	1
In	-1	-0.985	...	1
Outputs				
Out	0.368	0.373	...	2.718
Exp. Out	0.368	0.373	...	2.718
Out (DSP)	0.368	0.373	...	2.718
Exp. Out (DSP)	0.368	0.373	...	2.718

Test settings	
Tolerance Out	±2,3283e-07 (±500 LSB)

Test statistics	
Min CPU cycles	220
Max CPU cycles	460
Avg CPU cycles	324

Verification: Exp Float32 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for Math block Exp.

Test results				
Time step	1	2	...	133
CPU cycles	474	474	...	471
Inputs				
In (DSP)	-1	-0.985	...	1
In	-1	-0.985	...	1
Outputs				
Out	0.368	0.373	...	2.718
Exp. Out	0.368	0.373	...	2.718
Out (DSP)	0.368	0.373	...	2.718
Exp. Out (DSP)	0.368	0.373	...	2.718

Test settings	
Tolerance Out	±2,3283e-07 (±500 LSB)

Test statistics	
Min CPU cycles	139
Max CPU cycles	474
Avg CPU cycles	452

Block: L2Norm



Calculation of L2-norm (euclidean norm).

Inports	
u1	Input u1
u2	Input u2

Outports	
Out	Euclidean norm of u1 and u2

Description:

Calculation:

$$\mathrm{Out} = \|u\| = \sqrt{u_1^2 + u_2^2}$$

Implementations:

FiP8	8 Bit Fixed Point Implementation
FiP16	16 Bit Fixed Point Implementation
FiP32	32 Bit Fixed Point Implementation
Float32	32 Bit Floating Point Implementation
Float64	64 Bit Floating Point Implementation

Implementation: FiP8

8 Bit Fixed Point Implementation

Inports Data Type	
u1	int8
u2	int8

Outports Data Type	
Out	int8

Implementation: FiP16

16 Bit Fixed Point Implementation

Inports Data Type	
u1	int16
u2	int16

Outports Data Type	
Out	int16

Implementation: FiP32

32 Bit Fixed Point Implementation

Inports Data Type	
u1	int32
u2	int32

Outports Data Type	
Out	int32

Implementation: Float32

32 Bit Floating Point Implementation

Inports Data Type	
u1	float32
u2	float32

Outports Data Type	
Out	float32

Implementation: Float64

64 Bit Floating Point Implementation

Inports Data Type	
u1	float64
u2	float64

Outports Data Type	
Out	float64

Verification: L2Norm FiP16 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for Math block L2Norm.

Test results						
Time step	1	2	3	4	...	94
CPU cycles	105	105	105	102	...	105
Inputs						
u1 (DSP)	0	32767	0	32767	...	26214
u2 (DSP)	0	0	32767	32767	...	6554
u1	0	1	0	1	...	0.8
u2	0	0	1	1	...	0.2
Outputs						
Out	0	1	1	1	...	0.825
Exp. Out	0	1	1	1	...	0.825
Out (DSP)	0	32766	32766	32766	...	27020
Exp. Out (DSP)	0	32767	32767	32767	...	27021

Test settings	
Tolerance Out	±1,5259e-03 (±50 LSB)

Test statistics	
Min CPU cycles	102
Max CPU cycles	105
Avg CPU cycles	104

Verification: L2Norm FiP16 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for Math block L2Norm.

Test results						
Time step	1	2	3	4	...	94
CPU cycles	69	69	69	65	...	69
Inputs						
u1 (DSP)	0	32767	0	32767	...	26214
u2 (DSP)	0	0	32767	32767	...	6554
u1	0	1	0	1	...	0.8
u2	0	0	1	1	...	0.2
Outputs						
Out	0	1	1	1	...	0.825
Exp. Out	0	1	1	1	...	0.825
Out (DSP)	0	32766	32766	32766	...	27020
Exp. Out (DSP)	0	32767	32767	32767	...	27021

Test settings	
Tolerance Out	±1,5259e-03 (±50 LSB)

Test statistics	
Min CPU cycles	65
Max CPU cycles	69
Avg CPU cycles	68

Verification: L2Norm FiP16 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for Math block L2Norm.

Test results						
Time step	1	2	3	4	...	94
CPU cycles	107	107	107	107	...	107
Inputs						
u1 (DSP)	0	32767	0	32767	...	26214
u2 (DSP)	0	0	32767	32767	...	6554
u1	0	1	0	1	...	0.8
u2	0	0	1	1	...	0.2
Outputs						
Out	0	1	1	1	...	0.825
Exp. Out	0	1	1	1	...	0.825
Out (DSP)	0	32766	32766	32766	...	27020
Exp. Out (DSP)	0	32767	32767	32767	...	27021

Test settings	
Tolerance Out	±1,5259e-03 (±50 LSB)

Test statistics	
Min CPU cycles	107
Max CPU cycles	112
Avg CPU cycles	107

Verification: L2Norm FiP16 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for Math block L2Norm.

Test results						
Time step	1	2	3	4	...	94
CPU cycles	95	95	95	96	...	95
Inputs						
u1 (DSP)	0	32767	0	32767	...	26214
u2 (DSP)	0	0	32767	32767	...	6554
u1	0	1	0	1	...	0.8
u2	0	0	1	1	...	0.2
Outputs						
Out	0	1	1	1	...	0.825
Exp. Out	0	1	1	1	...	0.825
Out (DSP)	0	32766	32766	32766	...	27020
Exp. Out (DSP)	0	32767	32767	32767	...	27021

Test settings	
Tolerance Out	±1,5259e-03 (±50 LSB)

Test statistics	
Min CPU cycles	94
Max CPU cycles	96
Avg CPU cycles	95

Verification: L2Norm FiP16 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for Math block L2Norm.

Test results						
Time step	1	2	3	4	...	94
CPU cycles	63	63	63	63	...	63
Inputs						
u1 (DSP)	0	32767	0	32767	...	26214
u2 (DSP)	0	0	32767	32767	...	6554
u1	0	1	0	1	...	0.8
u2	0	0	1	1	...	0.2
Outputs						
Out	0	1	1	1	...	0.825
Exp. Out	0	1	1	1	...	0.825
Out (DSP)	0	32766	32766	32766	...	27020
Exp. Out (DSP)	0	32767	32767	32767	...	27021

Test settings	
Tolerance Out	±1,5259e-03 (±50 LSB)

Test statistics	
Min CPU cycles	63
Max CPU cycles	63
Avg CPU cycles	63

Verification: L2Norm FiP16 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for Math block L2Norm.

Test results						
Time step	1	2	3	4	...	94
CPU cycles	90	90	90	89	...	90
Inputs						
u1 (DSP)	0	32767	0	32767	...	26214
u2 (DSP)	0	0	32767	32767	...	6554
u1	0	1	0	1	...	0.8
u2	0	0	1	1	...	0.2
Outputs						
Out	0	1	1	1	...	0.825
Exp. Out	0	1	1	1	...	0.825
Out (DSP)	0	32766	32766	32766	...	27020
Exp. Out (DSP)	0	32767	32767	32767	...	27021

Test settings	
Tolerance Out	±1,5259e-03 (±50 LSB)

Test statistics	
Min CPU cycles	89
Max CPU cycles	90
Avg CPU cycles	89

Verification: L2Norm FiP16 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for Math block L2Norm.

Test results						
Time step	1	2	3	4	...	94
CPU cycles	119	102	102	102	...	102
Inputs						
u1 (DSP)	0	32767	0	32767	...	26214
u2 (DSP)	0	0	32767	32767	...	6554
u1	0	1	0	1	...	0.8
u2	0	0	1	1	...	0.2
Outputs						
Out	0	1	1	1	...	0.825
Exp. Out	0	1	1	1	...	0.825
Out (DSP)	0	32766	32766	32766	...	27020
Exp. Out (DSP)	0	32767	32767	32767	...	27021

Test settings	
Tolerance Out	±1,5259e-03 (±50 LSB)

Test statistics	
Min CPU cycles	102
Max CPU cycles	119
Avg CPU cycles	102

Verification: L2Norm FiP16 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for Math block L2Norm.

Test results						
Time step	1	2	3	4	...	94
CPU cycles	103	98	98	92	...	98
Inputs						
u1 (DSP)	0	32767	0	32767	...	26214
u2 (DSP)	0	0	32767	32767	...	6554
u1	0	1	0	1	...	0.8
u2	0	0	1	1	...	0.2
Outputs						
Out	0	1	1	1	...	0.825
Exp. Out	0	1	1	1	...	0.825
Out (DSP)	0	32766	32766	32766	...	27020
Exp. Out (DSP)	0	32767	32767	32767	...	27021

Test settings	
Tolerance Out	±1,5259e-03 (±50 LSB)

Test statistics	
Min CPU cycles	92
Max CPU cycles	103
Avg CPU cycles	97

Verification: L2Norm FiP32 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for Math block L2Norm.

Test results				
Time step	1	2	...	94
CPU cycles	199	199	...	199
Inputs				
u1 (DSP)	0	2147483647	...	1717986918
u2 (DSP)	0	0	...	429496730
u1	0	1	...	0.8
u2	0	0	...	0.2
Outputs				
Out	0	1	...	0.825
Exp. Out	0	1	...	0.825
Out (DSP)	0	2147483645	...	1770859265
Exp. Out (DSP)	0	2147483647	...	1770860382

Test settings	
Tolerance Out	±1,8626e-03 (±4000000 LSB)

Test statistics	
Min CPU cycles	153
Max CPU cycles	206
Avg CPU cycles	188

Verification: L2Norm FiP32 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for Math block L2Norm.

Test results				
Time step	1	2	...	94
CPU cycles	81	81	...	81
Inputs				
u1 (DSP)	0	2147483647	...	1717986918
u2 (DSP)	0	0	...	429496730
u1	0	1	...	0.8
u2	0	0	...	0.2
Outputs				
Out	0	1	...	0.825
Exp. Out	0	1	...	0.825
Out (DSP)	0	2147483645	...	1770859265
Exp. Out (DSP)	0	2147483647	...	1770860382

Test settings	
Tolerance Out	±1,8626e-03 (±4000000 LSB)

Test statistics	
Min CPU cycles	75
Max CPU cycles	85
Avg CPU cycles	79

Verification: L2Norm FiP32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for Math block L2Norm.

Test results				
Time step	1	2	...	94
CPU cycles	126	131	...	131
Inputs				
u1 (DSP)	0	2147483647	...	1717986918
u2 (DSP)	0	0	...	429496730
u1	0	1	...	0.8
u2	0	0	...	0.2
Outputs				
Out	0	1	...	0.825
Exp. Out	0	1	...	0.825
Out (DSP)	0	2147483645	...	1770859265
Exp. Out (DSP)	0	2147483647	...	1770860382

Test settings	
Tolerance Out	±1,8626e-03 (±4000000 LSB)

Test statistics	
Min CPU cycles	126
Max CPU cycles	131
Avg CPU cycles	129

Verification: L2Norm FiP32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for Math block L2Norm.

Test results				
Time step	1	2	...	94
CPU cycles	326	326	...	326
Inputs				
u1 (DSP)	0	2147483647	...	1717986918
u2 (DSP)	0	0	...	429496730
u1	0	1	...	0.8
u2	0	0	...	0.2
Outputs				
Out	0	1	...	0.825
Exp. Out	0	1	...	0.825
Out (DSP)	0	2147483645	...	1770859265
Exp. Out (DSP)	0	2147483647	...	1770860382

Test settings	
Tolerance Out	±1,8626e-03 (±4000000 LSB)

Test statistics	
Min CPU cycles	326
Max CPU cycles	330
Avg CPU cycles	327

Verification: L2Norm FiP32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for Math block L2Norm.

Test results				
Time step	1	2	...	94
CPU cycles	71	73	...	73
Inputs				
u1 (DSP)	0	2147483647	...	1717986918
u2 (DSP)	0	0	...	429496730
u1	0	1	...	0.8
u2	0	0	...	0.2
Outputs				
Out	0	1	...	0.825
Exp. Out	0	1	...	0.825
Out (DSP)	0	2147483645	...	1770859265
Exp. Out (DSP)	0	2147483647	...	1770860382

Test settings	
Tolerance Out	±1,8626e-03 (±4000000 LSB)

Test statistics	
Min CPU cycles	71
Max CPU cycles	77
Avg CPU cycles	73

Verification: L2Norm FiP32 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for Math block L2Norm.

Test results				
Time step	1	2	...	94
CPU cycles	450	450	...	450
Inputs				
u1 (DSP)	0	2147483647	...	1717986918
u2 (DSP)	0	0	...	429496730
u1	0	1	...	0.8
u2	0	0	...	0.2
Outputs				
Out	0	1	...	0.825
Exp. Out	0	1	...	0.825
Out (DSP)	0	2147483645	...	1770859265
Exp. Out (DSP)	0	2147483647	...	1770860382

Test settings	
Tolerance Out	±1,8626e-03 (±4000000 LSB)

Test statistics	
Min CPU cycles	450
Max CPU cycles	474
Avg CPU cycles	458

Verification: L2Norm FiP32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for Math block L2Norm.

Test results				
Time step	1	2	...	94
CPU cycles	129	120	...	120
Inputs				
u1 (DSP)	0	2147483647	...	1717986918
u2 (DSP)	0	0	...	429496730
u1	0	1	...	0.8
u2	0	0	...	0.2
Outputs				
Out	0	1	...	0.825
Exp. Out	0	1	...	0.825
Out (DSP)	0	2147483645	...	1770859265
Exp. Out (DSP)	0	2147483647	...	1770860382

Test settings	
Tolerance Out	±1,8626e-03 (±4000000 LSB)

Test statistics	
Min CPU cycles	118
Max CPU cycles	129
Avg CPU cycles	118

Verification: L2Norm FiP32 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for Math block L2Norm.

Test results				
Time step	1	2	...	94
CPU cycles	182	182	...	182
Inputs				
u1 (DSP)	0	2147483647	...	1717986918
u2 (DSP)	0	0	...	429496730
u1	0	1	...	0.8
u2	0	0	...	0.2
Outputs				
Out	0	1	...	0.825
Exp. Out	0	1	...	0.825
Out (DSP)	0	2147483645	...	1770859265
Exp. Out (DSP)	0	2147483647	...	1770860382

Test settings	
Tolerance Out	±1,8626e-03 (±4000000 LSB)

Test statistics	
Min CPU cycles	146
Max CPU cycles	193
Avg CPU cycles	174

Verification: L2Norm Float32 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for Math block L2Norm.

Test results				
Time step	1	2	...	94
CPU cycles	112	180	...	180
Inputs				
u1 (DSP)	0	13.2	...	10.56
u2 (DSP)	0	0	...	2.64
u1	0	13.2	...	10.56
u2	0	0	...	2.64
Outputs				
Out	0	13.2	...	10.885
Exp. Out	0	13.2	...	10.885
Out (DSP)	0	13.2	...	10.885
Exp. Out (DSP)	0	13.2	...	10.885

Test settings	
Tolerance Out	±2,3283e-06 (±5000 LSB)

Test statistics	
Min CPU cycles	112
Max CPU cycles	180
Avg CPU cycles	177

Verification: L2Norm Float32 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for Math block L2Norm.

Test results				
Time step	1	2	...	94
CPU cycles	63	63	...	63
Inputs				
u1 (DSP)	0	13.2	...	10.56
u2 (DSP)	0	0	...	2.64
u1	0	13.2	...	10.56
u2	0	0	...	2.64
Outputs				
Out	0	13.2	...	10.885
Exp. Out	0	13.2	...	10.885
Out (DSP)	0	13.2	...	10.885
Exp. Out (DSP)	0	13.2	...	10.885

Test settings	
Tolerance Out	±2,3283e-06 (±5000 LSB)

Test statistics	
Min CPU cycles	63
Max CPU cycles	63
Avg CPU cycles	63

Verification: L2Norm Float32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for Math block L2Norm.

Test results				
Time step	1	2	...	94
CPU cycles	88	88	...	88
Inputs				
u1 (DSP)	0	13.2	...	10.56
u2 (DSP)	0	0	...	2.64
u1	0	13.2	...	10.56
u2	0	0	...	2.64
Outputs				
Out	0	13.2	...	10.885
Exp. Out	0	13.2	...	10.885
Out (DSP)	0	13.2	...	10.885
Exp. Out (DSP)	0	13.2	...	10.885

Test settings	
Tolerance Out	±2,3283e-06 (±5000 LSB)

Test statistics	
Min CPU cycles	88
Max CPU cycles	88
Avg CPU cycles	88

Verification: L2Norm Float32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for Math block L2Norm.

Test results				
Time step	1	2	...	94
CPU cycles	556	995	...	1091
Inputs				
u1 (DSP)	0	13.2	...	10.56
u2 (DSP)	0	0	...	2.64
u1	0	13.2	...	10.56
u2	0	0	...	2.64
Outputs				
Out	0	13.2	...	10.885
Exp. Out	0	13.2	...	10.885
Out (DSP)	0	13.2	...	10.885
Exp. Out (DSP)	0	13.2	...	10.885

Test settings	
Tolerance Out	±2,3283e-06 (±5000 LSB)

Test statistics	
Min CPU cycles	556
Max CPU cycles	1120
Avg CPU cycles	1052

Verification: L2Norm Float32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for Math block L2Norm.

Test results				
Time step	1	2	...	94
CPU cycles	207	438	...	481
Inputs				
u1 (DSP)	0	13.2	...	10.56
u2 (DSP)	0	0	...	2.64
u1	0	13.2	...	10.56
u2	0	0	...	2.64
Outputs				
Out	0	13.2	...	10.885
Exp. Out	0	13.2	...	10.885
Out (DSP)	0	13.2	...	10.885
Exp. Out (DSP)	0	13.2	...	10.885

Test settings	
Tolerance Out	±2,3283e-06 (±5000 LSB)

Test statistics	
Min CPU cycles	207
Max CPU cycles	513
Avg CPU cycles	468

Verification: L2Norm Float32 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for Math block L2Norm.

Test results				
Time step	1	2	...	94
CPU cycles	496	1012	...	1147
Inputs				
u1 (DSP)	0	13.2	...	10.56
u2 (DSP)	0	0	...	2.64
u1	0	13.2	...	10.56
u2	0	0	...	2.64
Outputs				
Out	0	13.2	...	10.885
Exp. Out	0	13.2	...	10.885
Out (DSP)	0	13.2	...	10.885
Exp. Out (DSP)	0	13.2	...	10.885

Test settings	
Tolerance Out	±2,3283e-06 (±5000 LSB)

Test statistics	
Min CPU cycles	496
Max CPU cycles	1247
Avg CPU cycles	1089

Verification: L2Norm Float32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for Math block L2Norm.

Test results				
Time step	1	2	...	94
CPU cycles	89	78	...	78
Inputs				
u1 (DSP)	0	13.2	...	10.56
u2 (DSP)	0	0	...	2.64
u1	0	13.2	...	10.56
u2	0	0	...	2.64
Outputs				
Out	0	13.2	...	10.885
Exp. Out	0	13.2	...	10.885
Out (DSP)	0	13.2	...	10.885
Exp. Out (DSP)	0	13.2	...	10.885

Test settings	
Tolerance Out	±2,3283e-06 (±5000 LSB)

Test statistics	
Min CPU cycles	78
Max CPU cycles	89
Avg CPU cycles	78

Verification: L2Norm Float32 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for Math block L2Norm.

Test results				
Time step	1	2	...	94
CPU cycles	102	137	...	137
Inputs				
u1 (DSP)	0	13.2	...	10.56
u2 (DSP)	0	0	...	2.64
u1	0	13.2	...	10.56
u2	0	0	...	2.64
Outputs				
Out	0	13.2	...	10.885
Exp. Out	0	13.2	...	10.885
Out (DSP)	0	13.2	...	10.885
Exp. Out (DSP)	0	13.2	...	10.885

Test settings	
Tolerance Out	±2,3283e-06 (±5000 LSB)

Test statistics	
Min CPU cycles	102
Max CPU cycles	137
Avg CPU cycles	135

Block: Mult



Multiplication of input 1 with input 2.

Inports	
In1	Multiplicand 1
In2	Multiplicand 2

Outports	
Out	Product

Description:

Calculation:

$$\mathrm{Out} = \mathrm{In}_1 \cdot \mathrm{In}_2$$

Implementations:

FiP8	8 Bit Fixed Point Implementation
FiP16	16 Bit Fixed Point Implementation
FiP32	32 Bit Fixed Point Implementation
Float32	32 Bit Floating Point Implementation
Float64	64 Bit Floating Point Implementation

Implementation: FiP8

8 Bit Fixed Point Implementation

Inports Data Type	
In1	int8
In2	int8

Outports Data Type	
Out	int8

Implementation: FiP16

16 Bit Fixed Point Implementation

Inports Data Type	
In1	int16
In2	int16

Outports Data Type	
Out	int16

Implementation: FiP32

32 Bit Fixed Point Implementation

Inports Data Type	
In1	int32
In2	int32

Outports Data Type	
Out	int32

Implementation: Float32

32 Bit Floating Point Implementation

Inports Data Type	
In1	float32
In2	float32

Outports Data Type	
Out	float32

Implementation: Float64

64 Bit Floating Point Implementation

Inports Data Type	
In1	float64
In2	float64

Outports Data Type	
Out	float64

Verification: Mult FiP16 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for Math block Mult.

Test results						
Time step	1	2	3	4	...	217
CPU cycles	75	75	75	73	...	75
Inputs						
In1 (DSP)	0	16384	0	-32768	...	32767
In2 (DSP)	0	0	16384	32767	...	32767
In1	0	0.5	0	-1	...	1
In2	0	0	0.5	1	...	1
Outputs						
Out	0	0	0	-1	...	1
Exp. Out	0	0	0	-1	...	1
Out (DSP)	0	0	0	-32767	...	32766
Exp. Out (DSP)	0	0	0	-32768	...	32767

Test settings	
Tolerance Out	±6,1035e-05 (±2 LSB)

Test statistics	
Min CPU cycles	72
Max CPU cycles	75
Avg CPU cycles	74

Verification: Mult FiP16 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for Math block Mult.

Test results						
Time step	1	2	3	4	...	217
CPU cycles	43	43	43	47	...	43
Inputs						
In1 (DSP)	0	16384	0	-32768	...	32767
In2 (DSP)	0	0	16384	32767	...	32767
In1	0	0.5	0	-1	...	1
In2	0	0	0.5	1	...	1
Outputs						
Out	0	0	0	-1	...	1
Exp. Out	0	0	0	-1	...	1
Out (DSP)	0	0	0	-32767	...	32766
Exp. Out (DSP)	0	0	0	-32768	...	32767

Test settings	
Tolerance Out	±6,1035e-05 (±2 LSB)

Test statistics	
Min CPU cycles	43
Max CPU cycles	53
Avg CPU cycles	46

Verification: Mult FiP16 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for Math block Mult.

Test results						
Time step	1	2	3	4	...	217
CPU cycles	91	91	91	91	...	91
Inputs						
In1 (DSP)	0	16384	0	-32768	...	32767
In2 (DSP)	0	0	16384	32767	...	32767
In1	0	0.5	0	-1	...	1
In2	0	0	0.5	1	...	1
Outputs						
Out	0	0	0	-1	...	1
Exp. Out	0	0	0	-1	...	1
Out (DSP)	0	0	0	-32767	...	32766
Exp. Out (DSP)	0	0	0	-32768	...	32767

Test settings	
Tolerance Out	±6,1035e-05 (±2 LSB)

Test statistics	
Min CPU cycles	91
Max CPU cycles	96
Avg CPU cycles	92

Verification: Mult FiP16 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for Math block Mult.

Test results						
Time step	1	2	3	4	...	217
CPU cycles	77	77	77	80	...	77
Inputs						
In1 (DSP)	0	16384	0	-32768	...	32767
In2 (DSP)	0	0	16384	32767	...	32767
In1	0	0.5	0	-1	...	1
In2	0	0	0.5	1	...	1
Outputs						
Out	0	0	0	-1	...	1
Exp. Out	0	0	0	-1	...	1
Out (DSP)	0	0	0	-32767	...	32766
Exp. Out (DSP)	0	0	0	-32768	...	32767

Test settings	
Tolerance Out	±6,1035e-05 (±2 LSB)

Test statistics	
Min CPU cycles	77
Max CPU cycles	84
Avg CPU cycles	79

Verification: Mult FiP16 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for Math block Mult.

Test results						
Time step	1	2	3	4	...	217
CPU cycles	45	45	45	49	...	45
Inputs						
In1 (DSP)	0	16384	0	-32768	...	32767
In2 (DSP)	0	0	16384	32767	...	32767
In1	0	0.5	0	-1	...	1
In2	0	0	0.5	1	...	1
Outputs						
Out	0	0	0	-1	...	1
Exp. Out	0	0	0	-1	...	1
Out (DSP)	0	0	0	-32767	...	32766
Exp. Out (DSP)	0	0	0	-32768	...	32767

Test settings	
Tolerance Out	±6,1035e-05 (±2 LSB)

Test statistics	
Min CPU cycles	45
Max CPU cycles	50
Avg CPU cycles	46

Verification: Mult FiP16 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for Math block Mult.

Test results						
Time step	1	2	3	4	...	217
CPU cycles	49	49	49	57	...	49
Inputs						
In1 (DSP)	0	16384	0	-32768	...	32767
In2 (DSP)	0	0	16384	32767	...	32767
In1	0	0.5	0	-1	...	1
In2	0	0	0.5	1	...	1
Outputs						
Out	0	0	0	-1	...	1
Exp. Out	0	0	0	-1	...	1
Out (DSP)	0	0	0	-32767	...	32766
Exp. Out (DSP)	0	0	0	-32768	...	32767

Test settings	
Tolerance Out	±6,1035e-05 (±2 LSB)

Test statistics	
Min CPU cycles	49
Max CPU cycles	60
Avg CPU cycles	52

Verification: Mult FiP16 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for Math block Mult.

Test results						
Time step	1	2	3	4	...	217
CPU cycles	87	68	68	68	...	68
Inputs						
In1 (DSP)	0	16384	0	-32768	...	32767
In2 (DSP)	0	0	16384	32767	...	32767
In1	0	0.5	0	-1	...	1
In2	0	0	0.5	1	...	1
Outputs						
Out	0	0	0	-1	...	1
Exp. Out	0	0	0	-1	...	1
Out (DSP)	0	0	0	-32767	...	32766
Exp. Out (DSP)	0	0	0	-32768	...	32767

Test settings	
Tolerance Out	±6,1035e-05 (±2 LSB)

Test statistics	
Min CPU cycles	68
Max CPU cycles	87
Avg CPU cycles	70

Verification: Mult FiP16 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for Math block Mult.

Test results						
Time step	1	2	3	4	...	217
CPU cycles	79	79	79	71	...	79
Inputs						
In1 (DSP)	0	16384	0	-32768	...	32767
In2 (DSP)	0	0	16384	32767	...	32767
In1	0	0.5	0	-1	...	1
In2	0	0	0.5	1	...	1
Outputs						
Out	0	0	0	-1	...	1
Exp. Out	0	0	0	-1	...	1
Out (DSP)	0	0	0	-32767	...	32766
Exp. Out (DSP)	0	0	0	-32768	...	32767

Test settings	
Tolerance Out	±6,1035e-05 (±2 LSB)

Test statistics	
Min CPU cycles	65
Max CPU cycles	79
Avg CPU cycles	74

Verification: Mult FiP32 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for Math block Mult.

Test results				
Time step	1	2	...	217
CPU cycles	80	80	...	80
Inputs				
In1 (DSP)	0	1073741824	...	2147483647
In2 (DSP)	0	0	...	2147483647
In1	0	0.5	...	1
In2	0	0	...	1
Outputs				
Out	0	0	...	1
Exp. Out	0	0	...	1
Out (DSP)	0	0	...	2147483646
Exp. Out (DSP)	0	0	...	2147483647

Test settings	
Tolerance Out	±9,3132e-10 (±2 LSB)

Test statistics	
Min CPU cycles	79
Max CPU cycles	80
Avg CPU cycles	79

Verification: Mult FiP32 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for Math block Mult.

Test results				
Time step	1	2	...	217
CPU cycles	43	43	...	43
Inputs				
In1 (DSP)	0	1073741824	...	2147483647
In2 (DSP)	0	0	...	2147483647
In1	0	0.5	...	1
In2	0	0	...	1
Outputs				
Out	0	0	...	1
Exp. Out	0	0	...	1
Out (DSP)	0	0	...	2147483646
Exp. Out (DSP)	0	0	...	2147483647

Test settings	
Tolerance Out	±9,3132e-10 (±2 LSB)

Test statistics	
Min CPU cycles	43
Max CPU cycles	51
Avg CPU cycles	45

Verification: Mult FiP32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for Math block Mult.

Test results				
Time step	1	2	...	217
CPU cycles	96	96	...	96
Inputs				
In1 (DSP)	0	1073741824	...	2147483647
In2 (DSP)	0	0	...	2147483647
In1	0	0.5	...	1
In2	0	0	...	1
Outputs				
Out	0	0	...	1
Exp. Out	0	0	...	1
Out (DSP)	0	0	...	2147483646
Exp. Out (DSP)	0	0	...	2147483647

Test settings	
Tolerance Out	±9,3132e-10 (±2 LSB)

Test statistics	
Min CPU cycles	96
Max CPU cycles	101
Avg CPU cycles	97

Verification: Mult FiP32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for Math block Mult.

Test results				
Time step	1	2	...	217
CPU cycles	142	142	...	142
Inputs				
In1 (DSP)	0	1073741824	...	2147483647
In2 (DSP)	0	0	...	2147483647
In1	0	0.5	...	1
In2	0	0	...	1
Outputs				
Out	0	0	...	1
Exp. Out	0	0	...	1
Out (DSP)	0	0	...	2147483646
Exp. Out (DSP)	0	0	...	2147483647

Test settings	
Tolerance Out	±9,3132e-10 (±2 LSB)

Test statistics	
Min CPU cycles	142
Max CPU cycles	157
Avg CPU cycles	147

Verification: Mult FiP32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for Math block Mult.

Test results				
Time step	1	2	...	217
CPU cycles	54	54	...	56
Inputs				
In1 (DSP)	0	1073741824	...	2147483647
In2 (DSP)	0	0	...	2147483647
In1	0	0.5	...	1
In2	0	0	...	1
Outputs				
Out	0	0	...	1
Exp. Out	0	0	...	1
Out (DSP)	0	0	...	2147483646
Exp. Out (DSP)	0	0	...	2147483647

Test settings	
Tolerance Out	±9,3132e-10 (±2 LSB)

Test statistics	
Min CPU cycles	54
Max CPU cycles	63
Avg CPU cycles	58

Verification: Mult FiP32 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test — OK

Inport test for Math block Mult.

Test results				
Time step	1	2	...	217
CPU cycles	170	170	...	170
Inputs				
In1 (DSP)	0	1073741824	...	2147483647
In2 (DSP)	0	0	...	2147483647
In1	0	0.5	...	1
In2	0	0	...	1
Outputs				
Out	0	0	...	1
Exp. Out	0	0	...	1
Out (DSP)	0	0	...	2147483646
Exp. Out (DSP)	0	0	...	2147483647

Test settings	
Tolerance Out	±9,3132e-10 (±2 LSB)

Test statistics	
Min CPU cycles	170
Max CPU cycles	191
Avg CPU cycles	180

Verification: Mult FiP32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for Math block Mult.

Test results				
Time step	1	2	...	217
CPU cycles	98	87	...	87
Inputs				
In1 (DSP)	0	1073741824	...	2147483647
In2 (DSP)	0	0	...	2147483647
In1	0	0.5	...	1
In2	0	0	...	1
Outputs				
Out	0	0	...	1
Exp. Out	0	0	...	1
Out (DSP)	0	0	...	2147483646
Exp. Out (DSP)	0	0	...	2147483647

Test settings	
Tolerance Out	±9,3132e-10 (±2 LSB)

Test statistics	
Min CPU cycles	87
Max CPU cycles	102
Avg CPU cycles	92

Verification: Mult FiP32 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for Math block Mult.

Test results				
Time step	1	2	...	217
CPU cycles	86	86	...	86
Inputs				
In1 (DSP)	0	1073741824	...	2147483647
In2 (DSP)	0	0	...	2147483647
In1	0	0.5	...	1
In2	0	0	...	1
Outputs				
Out	0	0	...	1
Exp. Out	0	0	...	1
Out (DSP)	0	0	...	2147483646
Exp. Out (DSP)	0	0	...	2147483647

Test settings	
Tolerance Out	±9,3132e-10 (±2 LSB)

Test statistics	
Min CPU cycles	76
Max CPU cycles	86
Avg CPU cycles	82

Verification: Mult Float32 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for Math block Mult.

Test results				
Time step	1	2	...	217
CPU cycles	53	53	...	53
Inputs				
In1 (DSP)	0	0.5	...	3
In2 (DSP)	0	0	...	3
In1	0	0.5	...	3
In2	0	0	...	3
Outputs				
Out	0	0	...	9
Exp. Out	0	0	...	9
Out (DSP)	0	0	...	9
Exp. Out (DSP)	0	0	...	9

Test settings	
Tolerance Out	±8,3819e-07 (±1800 LSB)

Test statistics	
Min CPU cycles	53
Max CPU cycles	53
Avg CPU cycles	53

Verification: Mult Float32 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for Math block Mult.

Test results				
Time step	1	2	...	217
CPU cycles	29	29	...	29
Inputs				
In1 (DSP)	0	0.5	...	3
In2 (DSP)	0	0	...	3
In1	0	0.5	...	3
In2	0	0	...	3
Outputs				
Out	0	0	...	9
Exp. Out	0	0	...	9
Out (DSP)	0	0	...	9
Exp. Out (DSP)	0	0	...	9

Test settings	
Tolerance Out	±8,3819e-07 (±1800 LSB)

Test statistics	
Min CPU cycles	29
Max CPU cycles	29
Avg CPU cycles	29

Verification: Mult Float32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for Math block Mult.

Test results				
Time step	1	2	...	217
CPU cycles	66	66	...	66
Inputs				
In1 (DSP)	0	0.5	...	3
In2 (DSP)	0	0	...	3
In1	0	0.5	...	3
In2	0	0	...	3
Outputs				
Out	0	0	...	9
Exp. Out	0	0	...	9
Out (DSP)	0	0	...	9
Exp. Out (DSP)	0	0	...	9

Test settings	
Tolerance Out	±8,3819e-07 (±1800 LSB)

Test statistics	
Min CPU cycles	66
Max CPU cycles	66
Avg CPU cycles	66

Verification: Mult Float32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for Math block Mult.

Test results				
Time step	1	2	...	217
CPU cycles	176	175	...	285
Inputs				
In1 (DSP)	0	0.5	...	3
In2 (DSP)	0	0	...	3
In1	0	0.5	...	3
In2	0	0	...	3
Outputs				
Out	0	0	...	9
Exp. Out	0	0	...	9
Out (DSP)	0	0	...	9
Exp. Out (DSP)	0	0	...	9

Test settings	
Tolerance Out	±8,3819e-07 (±1800 LSB)

Test statistics	
Min CPU cycles	171
Max CPU cycles	285
Avg CPU cycles	227

Verification: Mult Float32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for Math block Mult.

Test results				
Time step	1	2	...	217
CPU cycles	73	72	...	89
Inputs				
In1 (DSP)	0	0.5	...	3
In2 (DSP)	0	0	...	3
In1	0	0.5	...	3
In2	0	0	...	3
Outputs				
Out	0	0	...	9
Exp. Out	0	0	...	9
Out (DSP)	0	0	...	9
Exp. Out (DSP)	0	0	...	9

Test settings	
Tolerance Out	±8,3819e-07 (±1800 LSB)

Test statistics	
Min CPU cycles	72
Max CPU cycles	92
Avg CPU cycles	90

Verification: Mult Float32 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test — OK

Inport test for Math block Mult.

Test results				
Time step	1	2	...	217
CPU cycles	149	147	...	192
Inputs				
In1 (DSP)	0	0.5	...	3
In2 (DSP)	0	0	...	3
In1	0	0.5	...	3
In2	0	0	...	3
Outputs				
Out	0	0	...	9
Exp. Out	0	0	...	9
Out (DSP)	0	0	...	9
Exp. Out (DSP)	0	0	...	9

Test settings	
Tolerance Out	±8,3819e-07 (±1800 LSB)

Test statistics	
Min CPU cycles	147
Max CPU cycles	195
Avg CPU cycles	191

Verification: Mult Float32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for Math block Mult.

Test results				
Time step	1	2	...	217
CPU cycles	57	57	...	57
Inputs				
In1 (DSP)	0	0.5	...	3
In2 (DSP)	0	0	...	3
In1	0	0.5	...	3
In2	0	0	...	3
Outputs				
Out	0	0	...	9
Exp. Out	0	0	...	9
Out (DSP)	0	0	...	9
Exp. Out (DSP)	0	0	...	9

Test settings	
Tolerance Out	±8,3819e-07 (±1800 LSB)

Test statistics	
Min CPU cycles	57
Max CPU cycles	57
Avg CPU cycles	57

Verification: Mult Float32 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for Math block Mult.

Test results				
Time step	1	2	...	217
CPU cycles	47	47	...	47
Inputs				
In1 (DSP)	0	0.5	...	3
In2 (DSP)	0	0	...	3
In1	0	0.5	...	3
In2	0	0	...	3
Outputs				
Out	0	0	...	9
Exp. Out	0	0	...	9
Out (DSP)	0	0	...	9
Exp. Out (DSP)	0	0	...	9

Test settings	
Tolerance Out	±8,3819e-07 (±1800 LSB)

Test statistics	
Min CPU cycles	47
Max CPU cycles	47
Avg CPU cycles	47

Block: Negation



Negation of input signal.

Inports	
In	Input

Outports	
Out	Negated input value

Description:

Calculation:

$$\mathrm{Out} = -\mathrm{In}$$

Implementations:

FiP8	8 Bit Fixed Point Implementation
FiP16	16 Bit Fixed Point Implementation
FiP32	32 Bit Fixed Point Implementation
Float32	32 Bit Floating Point Implementation
Float64	64 Bit Floating Point Implementation

Implementation: FiP8

8 Bit Fixed Point Implementation

Inports Data Type	
In	int8

Outports Data Type	
Out	int8

Implementation: FiP16

16 Bit Fixed Point Implementation

Inports Data Type	
In	int16

Outports Data Type	
Out	int16

Implementation: FiP32

32 Bit Fixed Point Implementation

Inports Data Type	
In	int32

Outports Data Type	
Out	int32

Implementation: Float32

32 Bit Floating Point Implementation

Inports Data Type	
In	float32

Outports Data Type	
Out	float32

Implementation: Float64

64 Bit Floating Point Implementation

Inports Data Type	
In	float64

Outports Data Type	
Out	float64

Verification: Negation FiP16 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for Math block Negation.

Test results						
Time step	1	2	3	4	...	37
CPU cycles	59	56	56	56	...	56
Inputs						
In (DSP)	-32768	-30948	-29127	-27307	...	32767
In	-1	-0.944	-0.889	-0.833	...	1
Outputs						
Out	1	0.944	0.889	0.833	...	-1
Exp. Out	1	0.944	0.889	0.833	...	-1
Out (DSP)	32767	30948	29127	27307	...	-32767
Exp. Out (DSP)	32767	30948	29127	27307	...	-32768

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	56
Max CPU cycles	59
Avg CPU cycles	56

Verification: Negation FiP16 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for Math block Negation.

Test results						
Time step	1	2	3	4	...	37
CPU cycles	29	29	29	29	...	29
Inputs						
In (DSP)	-32768	-30948	-29127	-27307	...	32767
In	-1	-0.944	-0.889	-0.833	...	1
Outputs						
Out	1	0.944	0.889	0.833	...	-1
Exp. Out	1	0.944	0.889	0.833	...	-1
Out (DSP)	32767	30948	29127	27307	...	-32767
Exp. Out (DSP)	32767	30948	29127	27307	...	-32768

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	29
Max CPU cycles	29
Avg CPU cycles	29

Verification: Negation FiP16 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for Math block Negation.

Test results						
Time step	1	2	3	4	...	37
CPU cycles	66	66	66	66	...	66
Inputs						
In (DSP)	-32768	-30948	-29127	-27307	...	32767
In	-1	-0.944	-0.889	-0.833	...	1
Outputs						
Out	1	0.944	0.889	0.833	...	-1
Exp. Out	1	0.944	0.889	0.833	...	-1
Out (DSP)	32767	30948	29127	27307	...	-32767
Exp. Out (DSP)	32767	30948	29127	27307	...	-32768

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	66
Max CPU cycles	66
Avg CPU cycles	66

Verification: Negation FiP16 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for Math block Negation.

Test results						
Time step	1	2	3	4	...	37
CPU cycles	62	54	54	54	...	54
Inputs						
In (DSP)	-32768	-30948	-29127	-27307	...	32767
In	-1	-0.944	-0.889	-0.833	...	1
Outputs						
Out	1	0.944	0.889	0.833	...	-1
Exp. Out	1	0.944	0.889	0.833	...	-1
Out (DSP)	32767	30948	29127	27307	...	-32767
Exp. Out (DSP)	32767	30948	29127	27307	...	-32768

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	54
Max CPU cycles	62
Avg CPU cycles	54

Verification: Negation FiP16 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for Math block Negation.

Test results						
Time step	1	2	3	4	...	37
CPU cycles	31	31	31	31	...	31
Inputs						
In (DSP)	-32768	-30948	-29127	-27307	...	32767
In	-1	-0.944	-0.889	-0.833	...	1
Outputs						
Out	1	0.944	0.889	0.833	...	-1
Exp. Out	1	0.944	0.889	0.833	...	-1
Out (DSP)	32767	30948	29127	27307	...	-32767
Exp. Out (DSP)	32767	30948	29127	27307	...	-32768

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	31
Max CPU cycles	31
Avg CPU cycles	31

Verification: Negation FiP16 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for Math block Negation.

Test results						
Time step	1	2	3	4	...	37
CPU cycles	44	41	41	41	...	41
Inputs						
In (DSP)	-32768	-30948	-29127	-27307	...	32767
In	-1	-0.944	-0.889	-0.833	...	1
Outputs						
Out	1	0.944	0.889	0.833	...	-1
Exp. Out	1	0.944	0.889	0.833	...	-1
Out (DSP)	32767	30948	29127	27307	...	-32767
Exp. Out (DSP)	32767	30948	29127	27307	...	-32768

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	41
Max CPU cycles	44
Avg CPU cycles	41

Verification: Negation FiP16 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for Math block Negation.

Test results						
Time step	1	2	3	4	...	37
CPU cycles	59	59	59	59	...	59
Inputs						
In (DSP)	-32768	-30948	-29127	-27307	...	32767
In	-1	-0.944	-0.889	-0.833	...	1
Outputs						
Out	1	0.944	0.889	0.833	...	-1
Exp. Out	1	0.944	0.889	0.833	...	-1
Out (DSP)	32767	30948	29127	27307	...	-32767
Exp. Out (DSP)	32767	30948	29127	27307	...	-32768

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	59
Max CPU cycles	59
Avg CPU cycles	59

Verification: Negation FiP16 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for Math block Negation.

Test results						
Time step	1	2	3	4	...	37
CPU cycles	54	49	49	49	...	49
Inputs						
In (DSP)	-32768	-30948	-29127	-27307	...	32767
In	-1	-0.944	-0.889	-0.833	...	1
Outputs						
Out	1	0.944	0.889	0.833	...	-1
Exp. Out	1	0.944	0.889	0.833	...	-1
Out (DSP)	32767	30948	29127	27307	...	-32767
Exp. Out (DSP)	32767	30948	29127	27307	...	-32768

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	49
Max CPU cycles	54
Avg CPU cycles	49

Verification: Negation FiP32 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for Math block Negation.

Test results				
Time step	1	2	...	37
CPU cycles	59	60	...	60
Inputs				
In (DSP)	-2147483648	-2028179001	...	2147483647
In	-1	-0.944	...	1
Outputs				
Out	1	0.944	...	-1
Exp. Out	1	0.944	...	-1
Out (DSP)	2147483647	2028179001	...	-2147483647
Exp. Out (DSP)	2147483647	2028179001	...	-2147483648

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	59
Max CPU cycles	60
Avg CPU cycles	59

Verification: Negation FiP32 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for Math block Negation.

Test results				
Time step	1	2	...	37
CPU cycles	31	29	...	29
Inputs				
In (DSP)	-2147483648	-2028179001	...	2147483647
In	-1	-0.944	...	1
Outputs				
Out	1	0.944	...	-1
Exp. Out	1	0.944	...	-1
Out (DSP)	2147483647	2028179001	...	-2147483647
Exp. Out (DSP)	2147483647	2028179001	...	-2147483648

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	29
Max CPU cycles	31
Avg CPU cycles	29

Verification: Negation FiP32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for Math block Negation.

Test results				
Time step	1	2	...	37
CPU cycles	66	66	...	66
Inputs				
In (DSP)	-2147483648	-2028179001	...	2147483647
In	-1	-0.944	...	1
Outputs				
Out	1	0.944	...	-1
Exp. Out	1	0.944	...	-1
Out (DSP)	2147483647	2028179001	...	-2147483647
Exp. Out (DSP)	2147483647	2028179001	...	-2147483648

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	66
Max CPU cycles	66
Avg CPU cycles	66

Verification: Negation FiP32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for Math block Negation.

Test results				
Time step	1	2	...	37
CPU cycles	59	51	...	51
Inputs				
In (DSP)	-2147483648	-2028179001	...	2147483647
In	-1	-0.944	...	1
Outputs				
Out	1	0.944	...	-1
Exp. Out	1	0.944	...	-1
Out (DSP)	2147483647	2028179001	...	-2147483647
Exp. Out (DSP)	2147483647	2028179001	...	-2147483648

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	51
Max CPU cycles	59
Avg CPU cycles	51

Verification: Negation FiP32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for Math block Negation.

Test results				
Time step	1	2	...	37
CPU cycles	32	30	...	30
Inputs				
In (DSP)	-2147483648	-2028179001	...	2147483647
In	-1	-0.944	...	1
Outputs				
Out	1	0.944	...	-1
Exp. Out	1	0.944	...	-1
Out (DSP)	2147483647	2028179001	...	-2147483647
Exp. Out (DSP)	2147483647	2028179001	...	-2147483648

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	30
Max CPU cycles	32
Avg CPU cycles	30

Verification: Negation FiP32 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for Math block Negation.

Test results				
Time step	1	2	...	37
CPU cycles	49	46	...	46
Inputs				
In (DSP)	-2147483648	-2028179001	...	2147483647
In	-1	-0.944	...	1
Outputs				
Out	1	0.944	...	-1
Exp. Out	1	0.944	...	-1
Out (DSP)	2147483647	2028179001	...	-2147483647
Exp. Out (DSP)	2147483647	2028179001	...	-2147483648

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	46
Max CPU cycles	49
Avg CPU cycles	46

Verification: Negation FiP32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for Math block Negation.

Test results				
Time step	1	2	...	37
CPU cycles	67	59	...	59
Inputs				
In (DSP)	-2147483648	-2028179001	...	2147483647
In	-1	-0.944	...	1
Outputs				
Out	1	0.944	...	-1
Exp. Out	1	0.944	...	-1
Out (DSP)	2147483647	2028179001	...	-2147483647
Exp. Out (DSP)	2147483647	2028179001	...	-2147483648

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	59
Max CPU cycles	67
Avg CPU cycles	59

Verification: Negation FiP32 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for Math block Negation.

Test results				
Time step	1	2	...	37
CPU cycles	57	58	...	58
Inputs				
In (DSP)	-2147483648	-2028179001	...	2147483647
In	-1	-0.944	...	1
Outputs				
Out	1	0.944	...	-1
Exp. Out	1	0.944	...	-1
Out (DSP)	2147483647	2028179001	...	-2147483647
Exp. Out (DSP)	2147483647	2028179001	...	-2147483648

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	57
Max CPU cycles	58
Avg CPU cycles	57

Verification: Negation Float32 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for Math block Negation.

Test results				
Time step	1	2	...	37
CPU cycles	51	51	...	51
Inputs				
In (DSP)	-1	-0.944	...	1
In	-1	-0.944	...	1
Outputs				
Out	1	0.944	...	-1
Exp. Out	1	0.944	...	-1
Out (DSP)	1	0.944	...	-1
Exp. Out (DSP)	1	0.944	...	-1

Test settings	
Tolerance Out	±3,4925e-08 (±75 LSB)

Test statistics	
Min CPU cycles	51
Max CPU cycles	51
Avg CPU cycles	51

Verification: Negation Float32 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for Math block Negation.

Test results				
Time step	1	2	...	37
CPU cycles	25	25	...	25
Inputs				
In (DSP)	-1	-0.944	...	1
In	-1	-0.944	...	1
Outputs				
Out	1	0.944	...	-1
Exp. Out	1	0.944	...	-1
Out (DSP)	1	0.944	...	-1
Exp. Out (DSP)	1	0.944	...	-1

Test settings	
Tolerance Out	±3,4925e-08 (±75 LSB)

Test statistics	
Min CPU cycles	25
Max CPU cycles	25
Avg CPU cycles	25

Verification: Negation Float32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for Math block Negation.

Test results				
Time step	1	2	...	37
CPU cycles	66	66	...	66
Inputs				
In (DSP)	-1	-0.944	...	1
In	-1	-0.944	...	1
Outputs				
Out	1	0.944	...	-1
Exp. Out	1	0.944	...	-1
Out (DSP)	1	0.944	...	-1
Exp. Out (DSP)	1	0.944	...	-1

Test settings	
Tolerance Out	±3,4925e-08 (±75 LSB)

Test statistics	
Min CPU cycles	66
Max CPU cycles	66
Avg CPU cycles	66

Verification: Negation Float32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for Math block Negation.

Test results				
Time step	1	2	...	37
CPU cycles	50	50	...	50
Inputs				
In (DSP)	-1	-0.944	...	1
In	-1	-0.944	...	1
Outputs				
Out	1	0.944	...	-1
Exp. Out	1	0.944	...	-1
Out (DSP)	1	0.944	...	-1
Exp. Out (DSP)	1	0.944	...	-1

Test settings	
Tolerance Out	±3,4925e-08 (±75 LSB)

Test statistics	
Min CPU cycles	50
Max CPU cycles	50
Avg CPU cycles	50

Verification: Negation Float32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for Math block Negation.

Test results				
Time step	1	2	...	37
CPU cycles	29	29	...	29
Inputs				
In (DSP)	-1	-0.944	...	1
In	-1	-0.944	...	1
Outputs				
Out	1	0.944	...	-1
Exp. Out	1	0.944	...	-1
Out (DSP)	1	0.944	...	-1
Exp. Out (DSP)	1	0.944	...	-1

Test settings	
Tolerance Out	±3,4925e-08 (±75 LSB)

Test statistics	
Min CPU cycles	29
Max CPU cycles	29
Avg CPU cycles	29

Verification: Negation Float32 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for Math block Negation.

Test results				
Time step	1	2	...	37
CPU cycles	40	40	...	40
Inputs				
In (DSP)	-1	-0.944	...	1
In	-1	-0.944	...	1
Outputs				
Out	1	0.944	...	-1
Exp. Out	1	0.944	...	-1
Out (DSP)	1	0.944	...	-1
Exp. Out (DSP)	1	0.944	...	-1

Test settings	
Tolerance Out	±3,4925e-08 (±75 LSB)

Test statistics	
Min CPU cycles	40
Max CPU cycles	40
Avg CPU cycles	40

Verification: Negation Float32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for Math block Negation.

Test results				
Time step	1	2	...	37
CPU cycles	56	56	...	56
Inputs				
In (DSP)	-1	-0.944	...	1
In	-1	-0.944	...	1
Outputs				
Out	1	0.944	...	-1
Exp. Out	1	0.944	...	-1
Out (DSP)	1	0.944	...	-1
Exp. Out (DSP)	1	0.944	...	-1

Test settings	
Tolerance Out	±3,4925e-08 (±75 LSB)

Test statistics	
Min CPU cycles	56
Max CPU cycles	56
Avg CPU cycles	56

Verification: Negation Float32 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for Math block Negation.

Test results				
Time step	1	2	...	37
CPU cycles	47	47	...	47
Inputs				
In (DSP)	-1	-0.944	...	1
In	-1	-0.944	...	1
Outputs				
Out	1	0.944	...	-1
Exp. Out	1	0.944	...	-1
Out (DSP)	1	0.944	...	-1
Exp. Out (DSP)	1	0.944	...	-1

Test settings	
Tolerance Out	±3,4925e-08 (±75 LSB)

Test statistics	
Min CPU cycles	47
Max CPU cycles	47
Avg CPU cycles	47

Block: Sign



Signum function.

Inports	
In	Input u

Outports	
Out	Value corresponding to sign of u

Description:

Calculation:

$$\mathrm{Out} = \mathrm{sgn}\left(\mathrm{In}\right) = \begin{cases} 1 & \mathrm{In} \geq 0 \\ -1 & \mathrm{In} < 0 \end{cases}$$

Implementations:

FiP8	8 Bit Fixed Point Implementation
FiP16	16 Bit Fixed Point Implementation
FiP32	32 Bit Fixed Point Implementation
Float32	32 Bit Floating Point Implementation
Float64	64 Bit Floating Point Implementation

Implementation: FiP8

8 Bit Fixed Point Implementation

Inports Data Type	
In	int8

Outports Data Type	
Out	int8

Implementation: FiP16

16 Bit Fixed Point Implementation

Inports Data Type	
In	int16

Outports Data Type	
Out	int16

Implementation: FiP32

32 Bit Fixed Point Implementation

Inports Data Type	
In	int32

Outports Data Type	
Out	int32

Implementation: Float32

32 Bit Floating Point Implementation

Inports Data Type	
In	float32

Outports Data Type	
Out	float32

Implementation: Float64

64 Bit Floating Point Implementation

Inports Data Type	
In	float64

Outports Data Type	
Out	float64

Verification: Sign FiP16 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for Math block Sign.

Test results						
Time step	1	2	3	4	...	37
CPU cycles	58	58	58	58	...	54
Inputs						
In (DSP)	-32768	-30948	-29127	-27307	...	32767
In	-1	-0.944	-0.889	-0.833	...	1
Outputs						
Out	-1	-1	-1	-1	...	1
Exp. Out	-1	-1	-1	-1	...	1
Out (DSP)	-32767	-32767	-32767	-32767	...	32767
Exp. Out (DSP)	-32768	-32768	-32768	-32768	...	32767

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	54
Max CPU cycles	58
Avg CPU cycles	55

Verification: Sign FiP16 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for Math block Sign.

Test results						
Time step	1	2	3	4	...	37
CPU cycles	33	33	33	33	...	29
Inputs						
In (DSP)	-32768	-30948	-29127	-27307	...	32767
In	-1	-0.944	-0.889	-0.833	...	1
Outputs						
Out	-1	-1	-1	-1	...	1
Exp. Out	-1	-1	-1	-1	...	1
Out (DSP)	-32767	-32767	-32767	-32767	...	32767
Exp. Out (DSP)	-32768	-32768	-32768	-32768	...	32767

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	29
Max CPU cycles	33
Avg CPU cycles	30

Verification: Sign FiP16 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for Math block Sign.

Test results						
Time step	1	2	3	4	...	37
CPU cycles	71	71	71	71	...	71
Inputs						
In (DSP)	-32768	-30948	-29127	-27307	...	32767
In	-1	-0.944	-0.889	-0.833	...	1
Outputs						
Out	-1	-1	-1	-1	...	1
Exp. Out	-1	-1	-1	-1	...	1
Out (DSP)	-32767	-32767	-32767	-32767	...	32767
Exp. Out (DSP)	-32768	-32768	-32768	-32768	...	32767

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	71
Max CPU cycles	71
Avg CPU cycles	71

Verification: Sign FiP16 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for Math block Sign.

Test results						
Time step	1	2	3	4	...	37
CPU cycles	57	57	57	57	...	57
Inputs						
In (DSP)	-32768	-30948	-29127	-27307	...	32767
In	-1	-0.944	-0.889	-0.833	...	1
Outputs						
Out	-1	-1	-1	-1	...	1
Exp. Out	-1	-1	-1	-1	...	1
Out (DSP)	-32767	-32767	-32767	-32767	...	32767
Exp. Out (DSP)	-32768	-32768	-32768	-32768	...	32767

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	57
Max CPU cycles	57
Avg CPU cycles	57

Verification: Sign FiP16 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for Math block Sign.

Test results						
Time step	1	2	3	4	...	37
CPU cycles	31	31	31	31	...	31
Inputs						
In (DSP)	-32768	-30948	-29127	-27307	...	32767
In	-1	-0.944	-0.889	-0.833	...	1
Outputs						
Out	-1	-1	-1	-1	...	1
Exp. Out	-1	-1	-1	-1	...	1
Out (DSP)	-32767	-32767	-32767	-32767	...	32767
Exp. Out (DSP)	-32768	-32768	-32768	-32768	...	32767

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	31
Max CPU cycles	31
Avg CPU cycles	31

Verification: Sign FiP16 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for Math block Sign.

Test results						
Time step	1	2	3	4	...	37
CPU cycles	42	42	42	42	...	39
Inputs						
In (DSP)	-32768	-30948	-29127	-27307	...	32767
In	-1	-0.944	-0.889	-0.833	...	1
Outputs						
Out	-1	-1	-1	-1	...	1
Exp. Out	-1	-1	-1	-1	...	1
Out (DSP)	-32767	-32767	-32767	-32767	...	32767
Exp. Out (DSP)	-32768	-32768	-32768	-32768	...	32767

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	39
Max CPU cycles	42
Avg CPU cycles	40

Verification: Sign FiP16 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for Math block Sign.

Test results						
Time step	1	2	3	4	...	37
CPU cycles	59	59	59	59	...	59
Inputs						
In (DSP)	-32768	-30948	-29127	-27307	...	32767
In	-1	-0.944	-0.889	-0.833	...	1
Outputs						
Out	-1	-1	-1	-1	...	1
Exp. Out	-1	-1	-1	-1	...	1
Out (DSP)	-32767	-32767	-32767	-32767	...	32767
Exp. Out (DSP)	-32768	-32768	-32768	-32768	...	32767

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	59
Max CPU cycles	59
Avg CPU cycles	59

Verification: Sign FiP16 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for Math block Sign.

Test results						
Time step	1	2	3	4	...	37
CPU cycles	53	53	53	53	...	47
Inputs						
In (DSP)	-32768	-30948	-29127	-27307	...	32767
In	-1	-0.944	-0.889	-0.833	...	1
Outputs						
Out	-1	-1	-1	-1	...	1
Exp. Out	-1	-1	-1	-1	...	1
Out (DSP)	-32767	-32767	-32767	-32767	...	32767
Exp. Out (DSP)	-32768	-32768	-32768	-32768	...	32767

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	47
Max CPU cycles	53
Avg CPU cycles	49

Verification: Sign FiP32 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for Math block Sign.

Test results				
Time step	1	2	...	37
CPU cycles	59	59	...	60
Inputs				
In (DSP)	-2147483648	-2028179001	...	2147483647
In	-1	-0.944	...	1
Outputs				
Out	-1	-1	...	1
Exp. Out	-1	-1	...	1
Out (DSP)	-2147483647	-2147483647	...	2147483647
Exp. Out (DSP)	-2147483648	-2147483648	...	2147483647

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	59
Max CPU cycles	60
Avg CPU cycles	59

Verification: Sign FiP32 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for Math block Sign.

Test results				
Time step	1	2	...	37
CPU cycles	29	29	...	29
Inputs				
In (DSP)	-2147483648	-2028179001	...	2147483647
In	-1	-0.944	...	1
Outputs				
Out	-1	-1	...	1
Exp. Out	-1	-1	...	1
Out (DSP)	-2147483647	-2147483647	...	2147483647
Exp. Out (DSP)	-2147483648	-2147483648	...	2147483647

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	29
Max CPU cycles	29
Avg CPU cycles	29

Verification: Sign FiP32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for Math block Sign.

Test results				
Time step	1	2	...	37
CPU cycles	71	71	...	71
Inputs				
In (DSP)	-2147483648	-2028179001	...	2147483647
In	-1	-0.944	...	1
Outputs				
Out	-1	-1	...	1
Exp. Out	-1	-1	...	1
Out (DSP)	-2147483647	-2147483647	...	2147483647
Exp. Out (DSP)	-2147483648	-2147483648	...	2147483647

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	71
Max CPU cycles	71
Avg CPU cycles	71

Verification: Sign FiP32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for Math block Sign.

Test results				
Time step	1	2	...	37
CPU cycles	54	54	...	54
Inputs				
In (DSP)	-2147483648	-2028179001	...	2147483647
In	-1	-0.944	...	1
Outputs				
Out	-1	-1	...	1
Exp. Out	-1	-1	...	1
Out (DSP)	-2147483647	-2147483647	...	2147483647
Exp. Out (DSP)	-2147483648	-2147483648	...	2147483647

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	54
Max CPU cycles	54
Avg CPU cycles	54

Verification: Sign FiP32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for Math block Sign.

Test results				
Time step	1	2	...	37
CPU cycles	32	32	...	31
Inputs				
In (DSP)	-2147483648	-2028179001	...	2147483647
In	-1	-0.944	...	1
Outputs				
Out	-1	-1	...	1
Exp. Out	-1	-1	...	1
Out (DSP)	-2147483647	-2147483647	...	2147483647
Exp. Out (DSP)	-2147483648	-2147483648	...	2147483647

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	31
Max CPU cycles	32
Avg CPU cycles	31

Verification: Sign FiP32 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for Math block Sign.

Test results				
Time step	1	2	...	37
CPU cycles	47	47	...	44
Inputs				
In (DSP)	-2147483648	-2028179001	...	2147483647
In	-1	-0.944	...	1
Outputs				
Out	-1	-1	...	1
Exp. Out	-1	-1	...	1
Out (DSP)	-2147483647	-2147483647	...	2147483647
Exp. Out (DSP)	-2147483648	-2147483648	...	2147483647

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	44
Max CPU cycles	47
Avg CPU cycles	45

Verification: Sign FiP32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for Math block Sign.

Test results				
Time step	1	2	...	37
CPU cycles	65	65	...	58
Inputs				
In (DSP)	-2147483648	-2028179001	...	2147483647
In	-1	-0.944	...	1
Outputs				
Out	-1	-1	...	1
Exp. Out	-1	-1	...	1
Out (DSP)	-2147483647	-2147483647	...	2147483647
Exp. Out (DSP)	-2147483648	-2147483648	...	2147483647

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	58
Max CPU cycles	65
Avg CPU cycles	61

Verification: Sign FiP32 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for Math block Sign.

Test results				
Time step	1	2	...	37
CPU cycles	57	57	...	56
Inputs				
In (DSP)	-2147483648	-2028179001	...	2147483647
In	-1	-0.944	...	1
Outputs				
Out	-1	-1	...	1
Exp. Out	-1	-1	...	1
Out (DSP)	-2147483647	-2147483647	...	2147483647
Exp. Out (DSP)	-2147483648	-2147483648	...	2147483647

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	56
Max CPU cycles	57
Avg CPU cycles	56

Verification: Sign Float32 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for Math block Sign.

Test results				
Time step	1	2	...	37
CPU cycles	61	61	...	62
Inputs				
In (DSP)	-1	-0.944	...	1
In	-1	-0.944	...	1
Outputs				
Out	-1	-1	...	1
Exp. Out	-1	-1	...	1
Out (DSP)	-1	-1	...	1
Exp. Out (DSP)	-1	-1	...	1

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	61
Max CPU cycles	62
Avg CPU cycles	61

Verification: Sign Float32 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for Math block Sign.

Test results				
Time step	1	2	...	37
CPU cycles	31	31	...	31
Inputs				
In (DSP)	-1	-0.944	...	1
In	-1	-0.944	...	1
Outputs				
Out	-1	-1	...	1
Exp. Out	-1	-1	...	1
Out (DSP)	-1	-1	...	1
Exp. Out (DSP)	-1	-1	...	1

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	31
Max CPU cycles	31
Avg CPU cycles	31

Verification: Sign Float32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for Math block Sign.

Test results				
Time step	1	2	...	37
CPU cycles	67	67	...	67
Inputs				
In (DSP)	-1	-0.944	...	1
In	-1	-0.944	...	1
Outputs				
Out	-1	-1	...	1
Exp. Out	-1	-1	...	1
Out (DSP)	-1	-1	...	1
Exp. Out (DSP)	-1	-1	...	1

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	67
Max CPU cycles	67
Avg CPU cycles	67

Verification: Sign Float32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for Math block Sign.

Test results				
Time step	1	2	...	37
CPU cycles	146	146	...	133
Inputs				
In (DSP)	-1	-0.944	...	1
In	-1	-0.944	...	1
Outputs				
Out	-1	-1	...	1
Exp. Out	-1	-1	...	1
Out (DSP)	-1	-1	...	1
Exp. Out (DSP)	-1	-1	...	1

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	124
Max CPU cycles	146
Avg CPU cycles	139

Verification: Sign Float32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for Math block Sign.

Test results				
Time step	1	2	...	37
CPU cycles	75	75	...	76
Inputs				
In (DSP)	-1	-0.944	...	1
In	-1	-0.944	...	1
Outputs				
Out	-1	-1	...	1
Exp. Out	-1	-1	...	1
Out (DSP)	-1	-1	...	1
Exp. Out (DSP)	-1	-1	...	1

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	52
Max CPU cycles	76
Avg CPU cycles	74

Verification: Sign Float32 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for Math block Sign.

Test results				
Time step	1	2	...	37
CPU cycles	144	144	...	145
Inputs				
In (DSP)	-1	-0.944	...	1
In	-1	-0.944	...	1
Outputs				
Out	-1	-1	...	1
Exp. Out	-1	-1	...	1
Out (DSP)	-1	-1	...	1
Exp. Out (DSP)	-1	-1	...	1

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	144
Max CPU cycles	145
Avg CPU cycles	144

Verification: Sign Float32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for Math block Sign.

Test results				
Time step	1	2	...	37
CPU cycles	73	67	...	60
Inputs				
In (DSP)	-1	-0.944	...	1
In	-1	-0.944	...	1
Outputs				
Out	-1	-1	...	1
Exp. Out	-1	-1	...	1
Out (DSP)	-1	-1	...	1
Exp. Out (DSP)	-1	-1	...	1

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	60
Max CPU cycles	73
Avg CPU cycles	63

Verification: Sign Float32 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for Math block Sign.

Test results				
Time step	1	2	...	37
CPU cycles	59	59	...	61
Inputs				
In (DSP)	-1	-0.944	...	1
In	-1	-0.944	...	1
Outputs				
Out	-1	-1	...	1
Exp. Out	-1	-1	...	1
Out (DSP)	-1	-1	...	1
Exp. Out (DSP)	-1	-1	...	1

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	59
Max CPU cycles	61
Avg CPU cycles	60

Block: Sin



Sine computation of input value.

Inports	
In	Input u

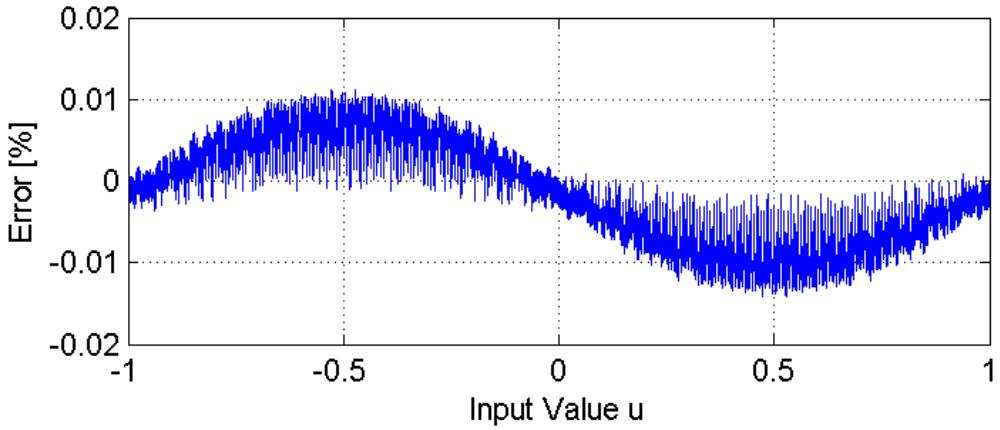
Outports	
Out	Result of sin(u)

Description:

Calculation:

$$\mathrm{Out} = \sin(\mathrm{In})$$

Error for 16 Bit Fixed Point Implementation:



Implementations:

FiP8	8 Bit Fixed Point Implementation
FiP16	16 Bit Fixed Point Implementation
FiP32	32 Bit Fixed Point Implementation
Float32	32 Bit Floating Point Implementation
Float64	64 Bit Floating Point Implementation

Implementation: FiP8

8 Bit Fixed Point Implementation

Inports Data Type	
In	int8

Outports Data Type	
Out	int8

Implementation: FiP16

16 Bit Fixed Point Implementation

Inports Data Type	
In	int16

Outports Data Type	
Out	int16

Implementation: FiP32

32 Bit Fixed Point Implementation

Inports Data Type	
In	int32

Outports Data Type	
Out	int32

Implementation: Float32

32 Bit Floating Point Implementation

Inports Data Type	
In	float32

Outports Data Type	
Out	float32

Implementation: Float64

64 Bit Floating Point Implementation

Inports Data Type	
In	float64

Outports Data Type	
Out	float64

Verification: Sin FiP16 CPU TMS320F28335

Date of Test 2026-06-19

Target controller TMS320F28335

Test case: Inport test OK

Inport test for Math block Sin.

Test results						
Time step	1	2	3	4	...	133
CPU cycles	76	76	76	76	...	76
Inputs						
In (DSP)	-32768	-32272	-31775	-31279	...	32767
In	-1	-0.985	-0.97	-0.955	...	1
Outputs						
Out	0	-0.048	-0.095	-0.142	...	0
Exp. Out	-0	-0.048	-0.095	-0.142	...	0
Out (DSP)	0	-1558	-3115	-4662	...	3
Exp. Out (DSP)	0	-1559	-3115	-4663	...	0

Test settings	
Tolerance Out	±1,2207e-04 (±4 LSB)

Test statistics	
Min CPU cycles	76
Max CPU cycles	76
Avg CPU cycles	76

Verification: Sin FiP16 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for Math block Sin.

Test results						
Time step	1	2	3	4	...	133
CPU cycles	53	53	53	53	...	53
Inputs						
In (DSP)	-32768	-32272	-31775	-31279	...	32767
In	-1	-0.985	-0.97	-0.955	...	1
Outputs						
Out	0	-0.048	-0.095	-0.142	...	0
Exp. Out	-0	-0.048	-0.095	-0.142	...	0
Out (DSP)	0	-1558	-3115	-4662	...	3
Exp. Out (DSP)	0	-1559	-3115	-4663	...	0

Test settings	
Tolerance Out	±1,2207e-04 (±4 LSB)

Test statistics	
Min CPU cycles	53
Max CPU cycles	53
Avg CPU cycles	53

Verification: Sin FiP16 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for Math block Sin.

Test results						
Time step	1	2	3	4	...	133
CPU cycles	91	96	91	96	...	91
Inputs						
In (DSP)	-32768	-32272	-31775	-31279	...	32767
In	-1	-0.985	-0.97	-0.955	...	1
Outputs						
Out	0	-0.048	-0.095	-0.142	...	0
Exp. Out	-0	-0.048	-0.095	-0.142	...	0
Out (DSP)	0	-1558	-3115	-4662	...	3
Exp. Out (DSP)	0	-1559	-3115	-4663	...	0

Test settings	
Tolerance Out	±1,2207e-04 (±4 LSB)

Test statistics	
Min CPU cycles	91
Max CPU cycles	96
Avg CPU cycles	92

Verification: Sin FiP16 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for Math block Sin.

Test results						
Time step	1	2	3	4	...	133
CPU cycles	71	71	71	71	...	71
Inputs						
In (DSP)	-32768	-32272	-31775	-31279	...	32767
In	-1	-0.985	-0.97	-0.955	...	1
Outputs						
Out	0	-0.048	-0.095	-0.142	...	0
Exp. Out	-0	-0.048	-0.095	-0.142	...	0
Out (DSP)	0	-1558	-3115	-4662	...	3
Exp. Out (DSP)	0	-1559	-3115	-4663	...	0

Test settings	
Tolerance Out	±1,2207e-04 (±4 LSB)

Test statistics	
Min CPU cycles	71
Max CPU cycles	71
Avg CPU cycles	71

Verification: Sin FiP16 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for Math block Sin.

Test results						
Time step	1	2	3	4	...	133
CPU cycles	47	47	47	47	...	47
Inputs						
In (DSP)	-32768	-32272	-31775	-31279	...	32767
In	-1	-0.985	-0.97	-0.955	...	1
Outputs						
Out	0	-0.048	-0.095	-0.142	...	0
Exp. Out	-0	-0.048	-0.095	-0.142	...	0
Out (DSP)	0	-1558	-3115	-4662	...	3
Exp. Out (DSP)	0	-1559	-3115	-4663	...	0

Test settings	
Tolerance Out	±1,2207e-04 (±4 LSB)

Test statistics	
Min CPU cycles	47
Max CPU cycles	47
Avg CPU cycles	47

Verification: Sin FiP16 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for Math block Sin.

Test results						
Time step	1	2	3	4	...	133
CPU cycles	62	62	62	62	...	62
Inputs						
In (DSP)	-32768	-32272	-31775	-31279	...	32767
In	-1	-0.985	-0.97	-0.955	...	1
Outputs						
Out	0	-0.048	-0.095	-0.142	...	0
Exp. Out	-0	-0.048	-0.095	-0.142	...	0
Out (DSP)	0	-1558	-3115	-4662	...	3
Exp. Out (DSP)	0	-1559	-3115	-4663	...	0

Test settings	
Tolerance Out	±1,2207e-04 (±4 LSB)

Test statistics	
Min CPU cycles	62
Max CPU cycles	62
Avg CPU cycles	62

Verification: Sin FiP16 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for Math block Sin.

Test results						
Time step	1	2	3	4	...	133
CPU cycles	104	87	87	87	...	87
Inputs						
In (DSP)	-32768	-32272	-31775	-31279	...	32767
In	-1	-0.985	-0.97	-0.955	...	1
Outputs						
Out	0	-0.048	-0.095	-0.142	...	0
Exp. Out	-0	-0.048	-0.095	-0.142	...	0
Out (DSP)	0	-1558	-3115	-4662	...	3
Exp. Out (DSP)	0	-1559	-3115	-4663	...	0

Test settings	
Tolerance Out	±1,2207e-04 (±4 LSB)

Test statistics	
Min CPU cycles	87
Max CPU cycles	104
Avg CPU cycles	87

Verification: Sin FiP16 CPU TMS320F28379D

Date of Test 2026-06-22

Target controller TMS320F28379D

Test case: Inport test OK

Inport test for Math block Sin.

Test results						
Time step	1	2	3	4	...	133
CPU cycles	64	67	64	64	...	64
Inputs						
In (DSP)	-32768	-32272	-31775	-31279	...	32767
In	-1	-0.985	-0.97	-0.955	...	1
Outputs						
Out	0	-0.048	-0.095	-0.142	...	0
Exp. Out	-0	-0.048	-0.095	-0.142	...	0
Out (DSP)	0	-1558	-3115	-4662	...	3
Exp. Out (DSP)	0	-1559	-3115	-4663	...	0

Test settings	
Tolerance Out	±1,2207e-04 (±4 LSB)

Test statistics	
Min CPU cycles	64
Max CPU cycles	67
Avg CPU cycles	64

Verification: Sin FiP32 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for Math block Sin.

Test results				
Time step	1	2	...	133
CPU cycles	85	85	...	85
Inputs				
In (DSP)	-2147483648	-2114946017	...	2147483647
In	-1	-0.985	...	1
Outputs				
Out	0	-0.048	...	0
Exp. Out	-0	-0.048	...	0
Out (DSP)	0	-102179899	...	3
Exp. Out (DSP)	0	-102181386	...	0

Test settings	
Tolerance Out	±6,9849e-05 (±150000 LSB)

Test statistics	
Min CPU cycles	85
Max CPU cycles	85
Avg CPU cycles	85

Verification: Sin FiP32 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for Math block Sin.

Test results				
Time step	1	2	...	133
CPU cycles	53	53	...	53
Inputs				
In (DSP)	-2147483648	-2114946017	...	2147483647
In	-1	-0.985	...	1
Outputs				
Out	0	-0.048	...	0
Exp. Out	-0	-0.048	...	0
Out (DSP)	0	-102179899	...	3
Exp. Out (DSP)	0	-102181386	...	0

Test settings	
Tolerance Out	±6,9849e-05 (±150000 LSB)

Test statistics	
Min CPU cycles	53
Max CPU cycles	53
Avg CPU cycles	53

Verification: Sin FiP32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for Math block Sin.

Test results				
Time step	1	2	...	133
CPU cycles	82	87	...	87
Inputs				
In (DSP)	-2147483648	-2114946017	...	2147483647
In	-1	-0.985	...	1
Outputs				
Out	0	-0.048	...	0
Exp. Out	-0	-0.048	...	0
Out (DSP)	0	-102179899	...	3
Exp. Out (DSP)	0	-102181386	...	0

Test settings	
Tolerance Out	±6,9849e-05 (±150000 LSB)

Test statistics	
Min CPU cycles	82
Max CPU cycles	87
Avg CPU cycles	84

Verification: Sin FiP32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for Math block Sin.

Test results				
Time step	1	2	...	133
CPU cycles	147	147	...	147
Inputs				
In (DSP)	-2147483648	-2114946017	...	2147483647
In	-1	-0.985	...	1
Outputs				
Out	0	-0.048	...	0
Exp. Out	-0	-0.048	...	0
Out (DSP)	0	-102179899	...	3
Exp. Out (DSP)	0	-102181386	...	0

Test settings	
Tolerance Out	±6,9849e-05 (±150000 LSB)

Test statistics	
Min CPU cycles	147
Max CPU cycles	147
Avg CPU cycles	147

Verification: Sin FiP32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for Math block Sin.

Test results				
Time step	1	2	...	133
CPU cycles	50	51	...	51
Inputs				
In (DSP)	-2147483648	-2114946017	...	2147483647
In	-1	-0.985	...	1
Outputs				
Out	0	-0.048	...	0
Exp. Out	-0	-0.048	...	0
Out (DSP)	0	-102179899	...	3
Exp. Out (DSP)	0	-102181386	...	0

Test settings	
Tolerance Out	±6,9849e-05 (±150000 LSB)

Test statistics	
Min CPU cycles	50
Max CPU cycles	51
Avg CPU cycles	50

Verification: Sin FiP32 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for Math block Sin.

Test results				
Time step	1	2	...	133
CPU cycles	208	208	...	208
Inputs				
In (DSP)	-2147483648	-2114946017	...	2147483647
In	-1	-0.985	...	1
Outputs				
Out	0	-0.048	...	0
Exp. Out	-0	-0.048	...	0
Out (DSP)	0	-102179899	...	3
Exp. Out (DSP)	0	-102181386	...	0

Test settings	
Tolerance Out	±6,9849e-05 (±150000 LSB)

Test statistics	
Min CPU cycles	201
Max CPU cycles	208
Avg CPU cycles	204

Verification: Sin FiP32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for Math block Sin.

Test results				
Time step	1	2	...	133
CPU cycles	110	96	...	96
Inputs				
In (DSP)	-2147483648	-2114946017	...	2147483647
In	-1	-0.985	...	1
Outputs				
Out	0	-0.048	...	0
Exp. Out	-0	-0.048	...	0
Out (DSP)	0	-102179899	...	3
Exp. Out (DSP)	0	-102181386	...	0

Test settings	
Tolerance Out	±6,9849e-05 (±150000 LSB)

Test statistics	
Min CPU cycles	96
Max CPU cycles	110
Avg CPU cycles	96

Verification: Sin FiP32 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for Math block Sin.

Test results				
Time step	1	2	...	133
CPU cycles	73	73	...	76
Inputs				
In (DSP)	-2147483648	-2114946017	...	2147483647
In	-1	-0.985	...	1
Outputs				
Out	0	-0.048	...	0
Exp. Out	-0	-0.048	...	0
Out (DSP)	0	-102179899	...	3
Exp. Out (DSP)	0	-102181386	...	0

Test settings	
Tolerance Out	±6,9849e-05 (±150000 LSB)

Test statistics	
Min CPU cycles	73
Max CPU cycles	76
Avg CPU cycles	73

Verification: Sin Float32 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for Math block Sin.

Test results				
Time step	1	2	...	133
CPU cycles	211	211	...	204
Inputs				
In (DSP)	-3.142	-3.094	...	3.142
In	-3.142	-3.094	...	3.142
Outputs				
Out	0	-0.048	...	-0
Exp. Out	-0	-0.048	...	0
Out (DSP)	0	-0.048	...	-0
Exp. Out (DSP)	-0	-0.048	...	0

Test settings	
Tolerance Out	±1,3970e-07 (±300 LSB)

Test statistics	
Min CPU cycles	204
Max CPU cycles	211
Avg CPU cycles	207

Verification: Sin Float32 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for Math block Sin.

Test results				
Time step	1	2	...	133
CPU cycles	109	109	...	109
Inputs				
In (DSP)	-3.142	-3.094	...	3.142
In	-3.142	-3.094	...	3.142
Outputs				
Out	0	-0.048	...	-0
Exp. Out	-0	-0.048	...	0
Out (DSP)	0	-0.048	...	-0
Exp. Out (DSP)	-0	-0.048	...	0

Test settings	
Tolerance Out	±1,3970e-07 (±300 LSB)

Test statistics	
Min CPU cycles	109
Max CPU cycles	109
Avg CPU cycles	109

Verification: Sin Float32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for Math block Sin.

Test results				
Time step	1	2	...	133
CPU cycles	513	468	...	505
Inputs				
In (DSP)	-3.142	-3.094	...	3.142
In	-3.142	-3.094	...	3.142
Outputs				
Out	0	-0.048	...	-0
Exp. Out	-0	-0.048	...	0
Out (DSP)	0	-0.048	...	-0
Exp. Out (DSP)	-0	-0.048	...	0

Test settings	
Tolerance Out	±1,3970e-07 (±300 LSB)

Test statistics	
Min CPU cycles	134
Max CPU cycles	513
Avg CPU cycles	359

Verification: Sin Float32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for Math block Sin.

Test results				
Time step	1	2	...	133
CPU cycles	5410	4645	...	5395
Inputs				
In (DSP)	-3.142	-3.094	...	3.142
In	-3.142	-3.094	...	3.142
Outputs				
Out	0	-0.048	...	-0
Exp. Out	-0	-0.048	...	0
Out (DSP)	0	-0.048	...	-0
Exp. Out (DSP)	-0	-0.048	...	0

Test settings	
Tolerance Out	±1,3970e-07 (±300 LSB)

Test statistics	
Min CPU cycles	148
Max CPU cycles	5410
Avg CPU cycles	3692

Verification: Sin Float32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for Math block Sin.

Test results				
Time step	1	2	...	133
CPU cycles	435	264	...	435
Inputs				
In (DSP)	-3.142	-3.094	...	3.142
In	-3.142	-3.094	...	3.142
Outputs				
Out	0	-0.048	...	-0
Exp. Out	-0	-0.048	...	0
Out (DSP)	0	-0.048	...	-0
Exp. Out (DSP)	-0	-0.048	...	0

Test settings	
Tolerance Out	±1,3970e-07 (±300 LSB)

Test statistics	
Min CPU cycles	139
Max CPU cycles	435
Avg CPU cycles	214

Verification: Sin Float32 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for Math block Sin.

Test results				
Time step	1	2	...	133
CPU cycles	2147	4037	...	2147
Inputs				
In (DSP)	-3.142	-3.094	...	3.142
In	-3.142	-3.094	...	3.142
Outputs				
Out	0	-0.048	...	-0
Exp. Out	-0	-0.048	...	0
Out (DSP)	0	-0.048	...	-0
Exp. Out (DSP)	-0	-0.048	...	0

Test settings	
Tolerance Out	±1,3970e-07 (±300 LSB)

Test statistics	
Min CPU cycles	107
Max CPU cycles	4037
Avg CPU cycles	3330

Verification: Sin Float32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for Math block Sin.

Test results				
Time step	1	2	...	133
CPU cycles	524	332	...	374
Inputs				
In (DSP)	-3.142	-3.094	...	3.142
In	-3.142	-3.094	...	3.142
Outputs				
Out	0	-0.048	...	-0
Exp. Out	-0	-0.048	...	0
Out (DSP)	0	-0.048	...	-0
Exp. Out (DSP)	-0	-0.048	...	0

Test settings	
Tolerance Out	±1,3970e-07 (±300 LSB)

Test statistics	
Min CPU cycles	111
Max CPU cycles	524
Avg CPU cycles	249

Verification: Sin Float32 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for Math block Sin.

Test results				
Time step	1	2	...	133
CPU cycles	137	137	...	133
Inputs				
In (DSP)	-3.142	-3.094	...	3.142
In	-3.142	-3.094	...	3.142
Outputs				
Out	0	-0.048	...	-0
Exp. Out	-0	-0.048	...	0
Out (DSP)	0	-0.048	...	-0
Exp. Out (DSP)	-0	-0.048	...	0

Test settings	
Tolerance Out	±1,3970e-07 (±300 LSB)

Test statistics	
Min CPU cycles	133
Max CPU cycles	137
Avg CPU cycles	135

Block: Sqrt



Square root computation of absolute input value.

Inports	
In	Input u

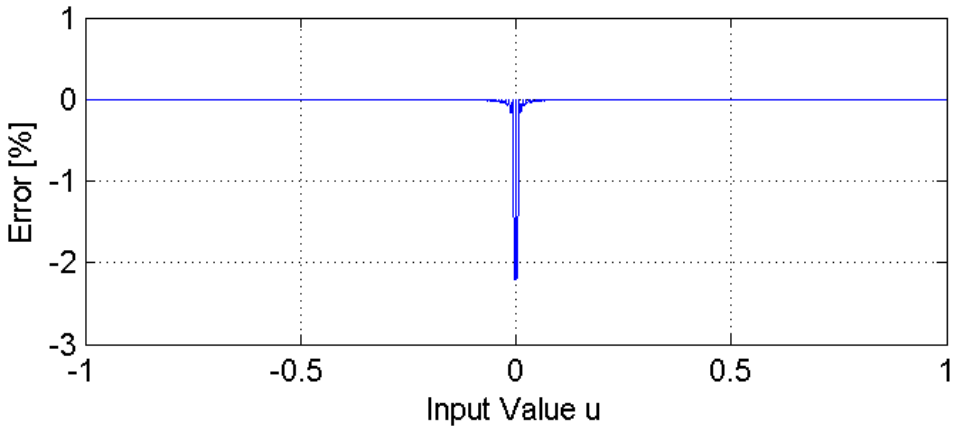
Outports	
Out	Result of sqrt(|u|)

Description:

Calculation:

$$\mathrm{Out} = \sqrt{|\mathrm{In}|}$$

Error for 16 Bit Fixed Point Implementation:



Implementations:

FiP8	8 Bit Fixed Point Implementation
FiP16	16 Bit Fixed Point Implementation
FiP32	32 Bit Fixed Point Implementation
Float32	32 Bit Floating Point Implementation
Float64	64 Bit Floating Point Implementation

Implementation: FiP8

8 Bit Fixed Point Implementation

Inports Data Type	
In	int8

Outports Data Type	
Out	int8

Implementation: FiP16

16 Bit Fixed Point Implementation

Inports Data Type	
In	int16

Outports Data Type	
Out	int16

Implementation: FiP32

32 Bit Fixed Point Implementation

Inports Data Type	
In	int32

Outports Data Type	
Out	int32

Implementation: Float32

32 Bit Floating Point Implementation

Inports Data Type	
In	float32

Outports Data Type	
Out	float32

Implementation: Float64

64 Bit Floating Point Implementation

Inports Data Type	
In	float64

Outports Data Type	
Out	float64

Verification: Sqrt FiP16 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for Math block Sqrt.

Test results						
Time step	1	2	3	4	...	133
CPU cycles	76	76	76	76	...	76
Inputs						
In (DSP)	-32768	-32272	-31775	-31279	...	32767
In	-1	-0.985	-0.97	-0.955	...	1
Outputs						
Out	1	0.992	0.985	0.977	...	1
Exp. Out	1	0.992	0.985	0.977	...	1
Out (DSP)	32767	32519	32267	32015	...	32766
Exp. Out (DSP)	32767	32519	32268	32015	...	32767

Test settings	
Tolerance Out	±3,9673e-04 (±13 LSB)

Test statistics	
Min CPU cycles	76
Max CPU cycles	76
Avg CPU cycles	76

Verification: Sqrt FiP16 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for Math block Sqrt.

Test results						
Time step	1	2	3	4	...	133
CPU cycles	53	53	53	53	...	53
Inputs						
In (DSP)	-32768	-32272	-31775	-31279	...	32767
In	-1	-0.985	-0.97	-0.955	...	1
Outputs						
Out	1	0.992	0.985	0.977	...	1
Exp. Out	1	0.992	0.985	0.977	...	1
Out (DSP)	32767	32519	32267	32015	...	32766
Exp. Out (DSP)	32767	32519	32268	32015	...	32767

Test settings	
Tolerance Out	±3,9673e-04 (±13 LSB)

Test statistics	
Min CPU cycles	53
Max CPU cycles	53
Avg CPU cycles	53

Verification: Sqrt FiP16 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test **OK**

Inport test for Math block Sqrt.

Test results						
Time step	1	2	3	4	...	133
CPU cycles	91	96	91	96	...	91
Inputs						
In (DSP)	-32768	-32272	-31775	-31279	...	32767
In	-1	-0.985	-0.97	-0.955	...	1
Outputs						
Out	1	0.992	0.985	0.977	...	1
Exp. Out	1	0.992	0.985	0.977	...	1
Out (DSP)	32767	32519	32267	32015	...	32766
Exp. Out (DSP)	32767	32519	32268	32015	...	32767

Test settings	
Tolerance Out	±3,9673e-04 (±13 LSB)

Test statistics	
Min CPU cycles	91
Max CPU cycles	96
Avg CPU cycles	92

Verification: Sqrt FiP16 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for Math block Sqrt.

Test results						
Time step	1	2	3	4	...	133
CPU cycles	71	71	71	71	...	71
Inputs						
In (DSP)	-32768	-32272	-31775	-31279	...	32767
In	-1	-0.985	-0.97	-0.955	...	1
Outputs						
Out	1	0.992	0.985	0.977	...	1
Exp. Out	1	0.992	0.985	0.977	...	1
Out (DSP)	32767	32519	32267	32015	...	32766
Exp. Out (DSP)	32767	32519	32268	32015	...	32767

Test settings	
Tolerance Out	±3,9673e-04 (±13 LSB)

Test statistics	
Min CPU cycles	71
Max CPU cycles	71
Avg CPU cycles	71

Verification: Sqrt FiP16 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for Math block Sqrt.

Test results						
Time step	1	2	3	4	...	133
CPU cycles	47	47	47	47	...	47
Inputs						
In (DSP)	-32768	-32272	-31775	-31279	...	32767
In	-1	-0.985	-0.97	-0.955	...	1
Outputs						
Out	1	0.992	0.985	0.977	...	1
Exp. Out	1	0.992	0.985	0.977	...	1
Out (DSP)	32767	32519	32267	32015	...	32766
Exp. Out (DSP)	32767	32519	32268	32015	...	32767

Test settings	
Tolerance Out	±3,9673e-04 (±13 LSB)

Test statistics	
Min CPU cycles	47
Max CPU cycles	47
Avg CPU cycles	47

Verification: Sqrt FiP16 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for Math block Sqrt.

Test results						
Time step	1	2	3	4	...	133
CPU cycles	62	62	62	62	...	62
Inputs						
In (DSP)	-32768	-32272	-31775	-31279	...	32767
In	-1	-0.985	-0.97	-0.955	...	1
Outputs						
Out	1	0.992	0.985	0.977	...	1
Exp. Out	1	0.992	0.985	0.977	...	1
Out (DSP)	32767	32519	32267	32015	...	32766
Exp. Out (DSP)	32767	32519	32268	32015	...	32767

Test settings	
Tolerance Out	±3,9673e-04 (±13 LSB)

Test statistics	
Min CPU cycles	62
Max CPU cycles	62
Avg CPU cycles	62

Verification: Sqrt FiP16 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for Math block Sqrt.

Test results						
Time step	1	2	3	4	...	133
CPU cycles	92	87	87	87	...	87
Inputs						
In (DSP)	-32768	-32272	-31775	-31279	...	32767
In	-1	-0.985	-0.97	-0.955	...	1
Outputs						
Out	1	0.992	0.985	0.977	...	1
Exp. Out	1	0.992	0.985	0.977	...	1
Out (DSP)	32767	32519	32267	32015	...	32766
Exp. Out (DSP)	32767	32519	32268	32015	...	32767

Test settings	
Tolerance Out	±3,9673e-04 (±13 LSB)

Test statistics	
Min CPU cycles	87
Max CPU cycles	92
Avg CPU cycles	87

Verification: Sqrt FiP16 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for Math block Sqrt.

Test results						
Time step	1	2	3	4	...	133
CPU cycles	67	64	64	64	...	64
Inputs						
In (DSP)	-32768	-32272	-31775	-31279	...	32767
In	-1	-0.985	-0.97	-0.955	...	1
Outputs						
Out	1	0.992	0.985	0.977	...	1
Exp. Out	1	0.992	0.985	0.977	...	1
Out (DSP)	32767	32519	32267	32015	...	32766
Exp. Out (DSP)	32767	32519	32268	32015	...	32767

Test settings	
Tolerance Out	±3,9673e-04 (±13 LSB)

Test statistics	
Min CPU cycles	64
Max CPU cycles	67
Avg CPU cycles	64

Verification: Sqrt FiP32 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for Math block Sqrt.

Test results				
Time step	1	2	...	133
CPU cycles	85	85	...	85
Inputs				
In (DSP)	-2147483648	-2114946017	...	2147483647
In	-1	-0.985	...	1
Outputs				
Out	1	0.992	...	1
Exp. Out	1	0.992	...	1
Out (DSP)	2147483647	2131151785	...	2147483646
Exp. Out (DSP)	2147483647	2131152737	...	2147483647

Test settings	
Tolerance Out	±3,1665e-04 (±680000 LSB)

Test statistics	
Min CPU cycles	85
Max CPU cycles	85
Avg CPU cycles	85

Verification: Sqrt FiP32 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for Math block Sqrt.

Test results				
Time step	1	2	...	133
CPU cycles	53	53	...	53
Inputs				
In (DSP)	-2147483648	-2114946017	...	2147483647
In	-1	-0.985	...	1
Outputs				
Out	1	0.992	...	1
Exp. Out	1	0.992	...	1
Out (DSP)	2147483647	2131151785	...	2147483646
Exp. Out (DSP)	2147483647	2131152737	...	2147483647

Test settings	
Tolerance Out	±3,1665e-04 (±680000 LSB)

Test statistics	
Min CPU cycles	53
Max CPU cycles	53
Avg CPU cycles	53

Verification: Sqrt FiP32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for Math block Sqrt.

Test results				
Time step	1	2	...	133
CPU cycles	91	96	...	96
Inputs				
In (DSP)	-2147483648	-2114946017	...	2147483647
In	-1	-0.985	...	1
Outputs				
Out	1	0.992	...	1
Exp. Out	1	0.992	...	1
Out (DSP)	2147483647	2131151785	...	2147483646
Exp. Out (DSP)	2147483647	2131152737	...	2147483647

Test settings	
Tolerance Out	±3,1665e-04 (±680000 LSB)

Test statistics	
Min CPU cycles	91
Max CPU cycles	96
Avg CPU cycles	93

Verification: Sqrt FiP32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for Math block Sqrt.

Test results				
Time step	1	2	...	133
CPU cycles	147	147	...	147
Inputs				
In (DSP)	-2147483648	-2114946017	...	2147483647
In	-1	-0.985	...	1
Outputs				
Out	1	0.992	...	1
Exp. Out	1	0.992	...	1
Out (DSP)	2147483647	2131151785	...	2147483646
Exp. Out (DSP)	2147483647	2131152737	...	2147483647

Test settings	
Tolerance Out	±3,1665e-04 (±680000 LSB)

Test statistics	
Min CPU cycles	147
Max CPU cycles	147
Avg CPU cycles	147

Verification: Sqrt FiP32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for Math block Sqrt.

Test results				
Time step	1	2	...	133
CPU cycles	50	51	...	51
Inputs				
In (DSP)	-2147483648	-2114946017	...	2147483647
In	-1	-0.985	...	1
Outputs				
Out	1	0.992	...	1
Exp. Out	1	0.992	...	1
Out (DSP)	2147483647	2131151785	...	2147483646
Exp. Out (DSP)	2147483647	2131152737	...	2147483647

Test settings	
Tolerance Out	±3,1665e-04 (±680000 LSB)

Test statistics	
Min CPU cycles	50
Max CPU cycles	51
Avg CPU cycles	50

Verification: Sqrt FiP32 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for Math block Sqrt.

Test results				
Time step	1	2	...	133
CPU cycles	208	208	...	201
Inputs				
In (DSP)	-2147483648	-2114946017	...	2147483647
In	-1	-0.985	...	1
Outputs				
Out	1	0.992	...	1
Exp. Out	1	0.992	...	1
Out (DSP)	2147483647	2131151785	...	2147483646
Exp. Out (DSP)	2147483647	2131152737	...	2147483647

Test settings	
Tolerance Out	±3,1665e-04 (±680000 LSB)

Test statistics	
Min CPU cycles	201
Max CPU cycles	208
Avg CPU cycles	204

Verification: Sqrt FiP32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for Math block Sqrt.

Test results				
Time step	1	2	...	133
CPU cycles	98	96	...	98
Inputs				
In (DSP)	-2147483648	-2114946017	...	2147483647
In	-1	-0.985	...	1
Outputs				
Out	1	0.992	...	1
Exp. Out	1	0.992	...	1
Out (DSP)	2147483647	2131151785	...	2147483646
Exp. Out (DSP)	2147483647	2131152737	...	2147483647

Test settings	
Tolerance Out	±3,1665e-04 (±680000 LSB)

Test statistics	
Min CPU cycles	96
Max CPU cycles	98
Avg CPU cycles	96

Verification: Sqrt FiP32 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for Math block Sqrt.

Test results				
Time step	1	2	...	133
CPU cycles	73	73	...	73
Inputs				
In (DSP)	-2147483648	-2114946017	...	2147483647
In	-1	-0.985	...	1
Outputs				
Out	1	0.992	...	1
Exp. Out	1	0.992	...	1
Out (DSP)	2147483647	2131151785	...	2147483646
Exp. Out (DSP)	2147483647	2131152737	...	2147483647

Test settings	
Tolerance Out	±3,1665e-04 (±680000 LSB)

Test statistics	
Min CPU cycles	73
Max CPU cycles	76
Avg CPU cycles	73

Verification: Sqrt Float32 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for Math block Sqrt.

Test results				
Time step	1	2	...	133
CPU cycles	180	180	...	180
Inputs				
In (DSP)	-1	-0.985	...	1
In	-1	-0.985	...	1
Outputs				
Out	1	0.992	...	1
Exp. Out	1	0.992	...	1
Out (DSP)	1	0.992	...	1
Exp. Out (DSP)	1	0.992	...	1

Test settings	
Tolerance Out	±9,3132e-08 (±200 LSB)

Test statistics	
Min CPU cycles	112
Max CPU cycles	180
Avg CPU cycles	179

Verification: Sqrt Float32 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for Math block Sqrt.

Test results				
Time step	1	2	...	133
CPU cycles	63	63	...	63
Inputs				
In (DSP)	-1	-0.985	...	1
In	-1	-0.985	...	1
Outputs				
Out	1	0.992	...	1
Exp. Out	1	0.992	...	1
Out (DSP)	1	0.992	...	1
Exp. Out (DSP)	1	0.992	...	1

Test settings	
Tolerance Out	±9,3132e-08 (±200 LSB)

Test statistics	
Min CPU cycles	63
Max CPU cycles	63
Avg CPU cycles	63

Verification: Sqrt Float32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for Math block Sqrt.

Test results				
Time step	1	2	...	133
CPU cycles	88	88	...	88
Inputs				
In (DSP)	-1	-0.985	...	1
In	-1	-0.985	...	1
Outputs				
Out	1	0.992	...	1
Exp. Out	1	0.992	...	1
Out (DSP)	1	0.992	...	1
Exp. Out (DSP)	1	0.992	...	1

Test settings	
Tolerance Out	±9,3132e-08 (±200 LSB)

Test statistics	
Min CPU cycles	88
Max CPU cycles	88
Avg CPU cycles	88

Verification: Sqrt Float32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for Math block Sqrt.

Test results				
Time step	1	2	...	133
CPU cycles	700	700	...	697
Inputs				
In (DSP)	-1	-0.985	...	1
In	-1	-0.985	...	1
Outputs				
Out	1	0.992	...	1
Exp. Out	1	0.992	...	1
Out (DSP)	1	0.992	...	1
Exp. Out (DSP)	1	0.992	...	1

Test settings	
Tolerance Out	±9,3132e-08 (±200 LSB)

Test statistics	
Min CPU cycles	293
Max CPU cycles	757
Avg CPU cycles	696

Verification: Sqrt Float32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for Math block Sqrt.

Test results				
Time step	1	2	...	133
CPU cycles	316	361	...	317
Inputs				
In (DSP)	-1	-0.985	...	1
In	-1	-0.985	...	1
Outputs				
Out	1	0.992	...	1
Exp. Out	1	0.992	...	1
Out (DSP)	1	0.992	...	1
Exp. Out (DSP)	1	0.992	...	1

Test settings	
Tolerance Out	±9,3132e-08 (±200 LSB)

Test statistics	
Min CPU cycles	115
Max CPU cycles	385
Avg CPU cycles	348

Verification: Sqrt Float32 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for Math block Sqrt.

Test results				
Time step	1	2	...	133
CPU cycles	718	736	...	724
Inputs				
In (DSP)	-1	-0.985	...	1
In	-1	-0.985	...	1
Outputs				
Out	1	0.992	...	1
Exp. Out	1	0.992	...	1
Out (DSP)	1	0.992	...	1
Exp. Out (DSP)	1	0.992	...	1

Test settings	
Tolerance Out	±9,3132e-08 (±200 LSB)

Test statistics	
Min CPU cycles	209
Max CPU cycles	746
Avg CPU cycles	730

Verification: Sqrt Float32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for Math block Sqrt.

Test results				
Time step	1	2	...	133
CPU cycles	87	77	...	77
Inputs				
In (DSP)	-1	-0.985	...	1
In	-1	-0.985	...	1
Outputs				
Out	1	0.992	...	1
Exp. Out	1	0.992	...	1
Out (DSP)	1	0.992	...	1
Exp. Out (DSP)	1	0.992	...	1

Test settings	
Tolerance Out	±9,3132e-08 (±200 LSB)

Test statistics	
Min CPU cycles	77
Max CPU cycles	87
Avg CPU cycles	77

Verification: Sqrt Float32 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for Math block Sqrt.

Test results				
Time step	1	2	...	133
CPU cycles	140	140	...	140
Inputs				
In (DSP)	-1	-0.985	...	1
In	-1	-0.985	...	1
Outputs				
Out	1	0.992	...	1
Exp. Out	1	0.992	...	1
Out (DSP)	1	0.992	...	1
Exp. Out (DSP)	1	0.992	...	1

Test settings	
Tolerance Out	±9,3132e-08 (±200 LSB)

Test statistics	
Min CPU cycles	105
Max CPU cycles	140
Avg CPU cycles	139

Block: Sub



Subtraction of input Minus from input Plus.

Inports	
Plus	Minuend
Minus	Subtrahend

Outports	
Out	Difference

Description:

Calculation:

$$\mathrm{Out} = \mathrm{Plus} - \mathrm{Minus}$$

Implementations:

FiP8	8 Bit Fixed Point Implementation
FiP16	16 Bit Fixed Point Implementation
FiP32	32 Bit Fixed Point Implementation
Float32	32 Bit Floating Point Implementation
Float64	64 Bit Floating Point Implementation

Implementation: FiP8

8 Bit Fixed Point Implementation

Inports Data Type	
Plus	int8
Minus	int8

Outports Data Type	
Out	int8

Implementation: FiP16

16 Bit Fixed Point Implementation

Inports Data Type	
Plus	int16
Minus	int16

Outports Data Type	
Out	int16

Implementation: FiP32

32 Bit Fixed Point Implementation

Inports Data Type	
Plus	int32
Minus	int32

Outports Data Type	
Out	int32

Implementation: Float32

32 Bit Floating Point Implementation

Inports Data Type	
Plus	float32
Minus	float32

Outports Data Type	
Out	float32

Implementation: Float64

64 Bit Floating Point Implementation

Inports Data Type	
Plus	float64
Minus	float64

Outports Data Type	
Out	float64

Verification: Sub FiP16 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for Math block Sub.

Test results						
Time step	1	2	3	4	...	214
CPU cycles	68	68	68	68	...	68
Inputs						
Plus (DSP)	-32768	-32150	-31531	-30913	...	32767
Minus (DSP)	32767	32150	31531	30913	...	32767
Plus	-1	-0.981	-0.962	-0.943	...	1
Minus	1	0.981	0.962	0.943	...	1
Outputs						
Out	-1	-1	-1	-1	...	0
Exp. Out	-1	-1	-1	-1	...	0
Out (DSP)	-32767	-32767	-32767	-32767	...	0
Exp. Out (DSP)	-32768	-32768	-32768	-32768	...	0

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	64
Max CPU cycles	68
Avg CPU cycles	67

Verification: Sub FiP16 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for Math block Sub.

Test results						
Time step	1	2	3	4	...	214
CPU cycles	37	37	37	37	...	37
Inputs						
Plus (DSP)	-32768	-32150	-31531	-30913	...	32767
Minus (DSP)	32767	32150	31531	30913	...	32767
Plus	-1	-0.981	-0.962	-0.943	...	1
Minus	1	0.981	0.962	0.943	...	1
Outputs						
Out	-1	-1	-1	-1	...	0
Exp. Out	-1	-1	-1	-1	...	0
Out (DSP)	-32767	-32767	-32767	-32767	...	0
Exp. Out (DSP)	-32768	-32768	-32768	-32768	...	0

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	31
Max CPU cycles	37
Avg CPU cycles	36

Verification: Sub FiP16 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for Math block Sub.

Test results						
Time step	1	2	3	4	...	214
CPU cycles	77	77	77	77	...	77
Inputs						
Plus (DSP)	-32768	-32150	-31531	-30913	...	32767
Minus (DSP)	32767	32150	31531	30913	...	32767
Plus	-1	-0.981	-0.962	-0.943	...	1
Minus	1	0.981	0.962	0.943	...	1
Outputs						
Out	-1	-1	-1	-1	...	0
Exp. Out	-1	-1	-1	-1	...	0
Out (DSP)	-32767	-32767	-32767	-32767	...	0
Exp. Out (DSP)	-32768	-32768	-32768	-32768	...	0

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	77
Max CPU cycles	77
Avg CPU cycles	77

Verification: Sub FiP16 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for Math block Sub.

Test results						
Time step	1	2	3	4	...	214
CPU cycles	65	65	65	65	...	66
Inputs						
Plus (DSP)	-32768	-32150	-31531	-30913	...	32767
Minus (DSP)	32767	32150	31531	30913	...	32767
Plus	-1	-0.981	-0.962	-0.943	...	1
Minus	1	0.981	0.962	0.943	...	1
Outputs						
Out	-1	-1	-1	-1	...	0
Exp. Out	-1	-1	-1	-1	...	0
Out (DSP)	-32767	-32767	-32767	-32767	...	0
Exp. Out (DSP)	-32768	-32768	-32768	-32768	...	0

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	65
Max CPU cycles	67
Avg CPU cycles	66

Verification: Sub FiP16 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for Math block Sub.

Test results						
Time step	1	2	3	4	...	214
CPU cycles	39	39	39	39	...	39
Inputs						
Plus (DSP)	-32768	-32150	-31531	-30913	...	32767
Minus (DSP)	32767	32150	31531	30913	...	32767
Plus	-1	-0.981	-0.962	-0.943	...	1
Minus	1	0.981	0.962	0.943	...	1
Outputs						
Out	-1	-1	-1	-1	...	0
Exp. Out	-1	-1	-1	-1	...	0
Out (DSP)	-32767	-32767	-32767	-32767	...	0
Exp. Out (DSP)	-32768	-32768	-32768	-32768	...	0

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	39
Max CPU cycles	39
Avg CPU cycles	39

Verification: Sub FiP16 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for Math block Sub.

Test results						
Time step	1	2	3	4	...	214
CPU cycles	58	58	58	58	...	59
Inputs						
Plus (DSP)	-32768	-32150	-31531	-30913	...	32767
Minus (DSP)	32767	32150	31531	30913	...	32767
Plus	-1	-0.981	-0.962	-0.943	...	1
Minus	1	0.981	0.962	0.943	...	1
Outputs						
Out	-1	-1	-1	-1	...	0
Exp. Out	-1	-1	-1	-1	...	0
Out (DSP)	-32767	-32767	-32767	-32767	...	0
Exp. Out (DSP)	-32768	-32768	-32768	-32768	...	0

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	58
Max CPU cycles	59
Avg CPU cycles	58

Verification: Sub FiP16 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for Math block Sub.

Test results						
Time step	1	2	3	4	...	214
CPU cycles	85	69	69	69	...	69
Inputs						
Plus (DSP)	-32768	-32150	-31531	-30913	...	32767
Minus (DSP)	32767	32150	31531	30913	...	32767
Plus	-1	-0.981	-0.962	-0.943	...	1
Minus	1	0.981	0.962	0.943	...	1
Outputs						
Out	-1	-1	-1	-1	...	0
Exp. Out	-1	-1	-1	-1	...	0
Out (DSP)	-32767	-32767	-32767	-32767	...	0
Exp. Out (DSP)	-32768	-32768	-32768	-32768	...	0

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	69
Max CPU cycles	85
Avg CPU cycles	69

Verification: Sub FiP16 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for Math block Sub.

Test results						
Time step	1	2	3	4	...	214
CPU cycles	65	65	65	65	...	65
Inputs						
Plus (DSP)	-32768	-32150	-31531	-30913	...	32767
Minus (DSP)	32767	32150	31531	30913	...	32767
Plus	-1	-0.981	-0.962	-0.943	...	1
Minus	1	0.981	0.962	0.943	...	1
Outputs						
Out	-1	-1	-1	-1	...	0
Exp. Out	-1	-1	-1	-1	...	0
Out (DSP)	-32767	-32767	-32767	-32767	...	0
Exp. Out (DSP)	-32768	-32768	-32768	-32768	...	0

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	63
Max CPU cycles	65
Avg CPU cycles	64

Verification: Sub FiP32 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for Math block Sub.

Test results				
Time step	1	2	...	214
CPU cycles	165	165	...	159
Inputs				
Plus (DSP)	-2147483648	-2106965089	...	2147483647
Minus (DSP)	2147483647	2106965089	...	2147483647
Plus	-1	-0.981	...	1
Minus	1	0.981	...	1
Outputs				
Out	-1	-1	...	0
Exp. Out	-1	-1	...	0
Out (DSP)	-2147483647	-2147483647	...	0
Exp. Out (DSP)	-2147483648	-2147483648	...	0

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	112
Max CPU cycles	165
Avg CPU cycles	153

Verification: Sub FiP32 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for Math block Sub.

Test results				
Time step	1	2	...	214
CPU cycles	59	59	...	55
Inputs				
Plus (DSP)	-2147483648	-2106965089	...	2147483647
Minus (DSP)	2147483647	2106965089	...	2147483647
Plus	-1	-0.981	...	1
Minus	1	0.981	...	1
Outputs				
Out	-1	-1	...	0
Exp. Out	-1	-1	...	0
Out (DSP)	-2147483647	-2147483647	...	0
Exp. Out (DSP)	-2147483648	-2147483648	...	0

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	49
Max CPU cycles	59
Avg CPU cycles	54

Verification: Sub FiP32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for Math block Sub.

Test results				
Time step	1	2	...	214
CPU cycles	82	82	...	82
Inputs				
Plus (DSP)	-2147483648	-2106965089	...	2147483647
Minus (DSP)	2147483647	2106965089	...	2147483647
Plus	-1	-0.981	...	1
Minus	1	0.981	...	1
Outputs				
Out	-1	-1	...	0
Exp. Out	-1	-1	...	0
Out (DSP)	-2147483647	-2147483647	...	0
Exp. Out (DSP)	-2147483648	-2147483648	...	0

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	82
Max CPU cycles	82
Avg CPU cycles	82

Verification: Sub FiP32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for Math block Sub.

Test results				
Time step	1	2	...	214
CPU cycles	82	82	...	81
Inputs				
Plus (DSP)	-2147483648	-2106965089	...	2147483647
Minus (DSP)	2147483647	2106965089	...	2147483647
Plus	-1	-0.981	...	1
Minus	1	0.981	...	1
Outputs				
Out	-1	-1	...	0
Exp. Out	-1	-1	...	0
Out (DSP)	-2147483647	-2147483647	...	0
Exp. Out (DSP)	-2147483648	-2147483648	...	0

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	81
Max CPU cycles	138
Avg CPU cycles	83

Verification: Sub FiP32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for Math block Sub.

Test results				
Time step	1	2	...	214
CPU cycles	51	51	...	48
Inputs				
Plus (DSP)	-2147483648	-2106965089	...	2147483647
Minus (DSP)	2147483647	2106965089	...	2147483647
Plus	-1	-0.981	...	1
Minus	1	0.981	...	1
Outputs				
Out	-1	-1	...	0
Exp. Out	-1	-1	...	0
Out (DSP)	-2147483647	-2147483647	...	0
Exp. Out (DSP)	-2147483648	-2147483648	...	0

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	48
Max CPU cycles	51
Avg CPU cycles	48

Verification: Sub FiP32 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for Math block Sub.

Test results				
Time step	1	2	...	214
CPU cycles	82	82	...	81
Inputs				
Plus (DSP)	-2147483648	-2106965089	...	2147483647
Minus (DSP)	2147483647	2106965089	...	2147483647
Plus	-1	-0.981	...	1
Minus	1	0.981	...	1
Outputs				
Out	-1	-1	...	0
Exp. Out	-1	-1	...	0
Out (DSP)	-2147483647	-2147483647	...	0
Exp. Out (DSP)	-2147483648	-2147483648	...	0

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	81
Max CPU cycles	82
Avg CPU cycles	81

Verification: Sub FiP32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for Math block Sub.

Test results				
Time step	1	2	...	214
CPU cycles	99	92	...	92
Inputs				
Plus (DSP)	-2147483648	-2106965089	...	2147483647
Minus (DSP)	2147483647	2106965089	...	2147483647
Plus	-1	-0.981	...	1
Minus	1	0.981	...	1
Outputs				
Out	-1	-1	...	0
Exp. Out	-1	-1	...	0
Out (DSP)	-2147483647	-2147483647	...	0
Exp. Out (DSP)	-2147483648	-2147483648	...	0

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	92
Max CPU cycles	99
Avg CPU cycles	92

Verification: Sub FiP32 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for Math block Sub.

Test results				
Time step	1	2	...	214
CPU cycles	152	152	...	150
Inputs				
Plus (DSP)	-2147483648	-2106965089	...	2147483647
Minus (DSP)	2147483647	2106965089	...	2147483647
Plus	-1	-0.981	...	1
Minus	1	0.981	...	1
Outputs				
Out	-1	-1	...	0
Exp. Out	-1	-1	...	0
Out (DSP)	-2147483647	-2147483647	...	0
Exp. Out (DSP)	-2147483648	-2147483648	...	0

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	110
Max CPU cycles	152
Avg CPU cycles	145

Verification: Sub Float32 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for Math block Sub.

Test results				
Time step	1	2	...	214
CPU cycles	53	53	...	53
Inputs				
Plus (DSP)	-2	-1.962	...	2
Minus (DSP)	2	1.962	...	2
Plus	-2	-1.962	...	2
Minus	2	1.962	...	2
Outputs				
Out	-4	-3.925	...	0
Exp. Out	-4	-3.925	...	0
Out (DSP)	-4	-3.925	...	0
Exp. Out (DSP)	-4	-3.925	...	0

Test settings	
Tolerance Out	±1,8626e-07 (±400 LSB)

Test statistics	
Min CPU cycles	53
Max CPU cycles	53
Avg CPU cycles	53

Verification: Sub Float32 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for Math block Sub.

Test results				
Time step	1	2	...	214
CPU cycles	29	29	...	29
Inputs				
Plus (DSP)	-2	-1.962	...	2
Minus (DSP)	2	1.962	...	2
Plus	-2	-1.962	...	2
Minus	2	1.962	...	2
Outputs				
Out	-4	-3.925	...	0
Exp. Out	-4	-3.925	...	0
Out (DSP)	-4	-3.925	...	0
Exp. Out (DSP)	-4	-3.925	...	0

Test settings	
Tolerance Out	±1,8626e-07 (±400 LSB)

Test statistics	
Min CPU cycles	29
Max CPU cycles	29
Avg CPU cycles	29

Verification: Sub Float32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for Math block Sub.

Test results				
Time step	1	2	...	214
CPU cycles	62	62	...	62
Inputs				
Plus (DSP)	-2	-1.962	...	2
Minus (DSP)	2	1.962	...	2
Plus	-2	-1.962	...	2
Minus	2	1.962	...	2
Outputs				
Out	-4	-3.925	...	0
Exp. Out	-4	-3.925	...	0
Out (DSP)	-4	-3.925	...	0
Exp. Out (DSP)	-4	-3.925	...	0

Test settings	
Tolerance Out	±1,8626e-07 (±400 LSB)

Test statistics	
Min CPU cycles	62
Max CPU cycles	62
Avg CPU cycles	62

Verification: Sub Float32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for Math block Sub.

Test results				
Time step	1	2	...	214
CPU cycles	158	158	...	152
Inputs				
Plus (DSP)	-2	-1.962	...	2
Minus (DSP)	2	1.962	...	2
Plus	-2	-1.962	...	2
Minus	2	1.962	...	2
Outputs				
Out	-4	-3.925	...	0
Exp. Out	-4	-3.925	...	0
Out (DSP)	-4	-3.925	...	0
Exp. Out (DSP)	-4	-3.925	...	0

Test settings	
Tolerance Out	±1,8626e-07 (±400 LSB)

Test statistics	
Min CPU cycles	152
Max CPU cycles	158
Avg CPU cycles	155

Verification: Sub Float32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for Math block Sub.

Test results				
Time step	1	2	...	214
CPU cycles	104	104	...	88
Inputs				
Plus (DSP)	-2	-1.962	...	2
Minus (DSP)	2	1.962	...	2
Plus	-2	-1.962	...	2
Minus	2	1.962	...	2
Outputs				
Out	-4	-3.925	...	0
Exp. Out	-4	-3.925	...	0
Out (DSP)	-4	-3.925	...	0
Exp. Out (DSP)	-4	-3.925	...	0

Test settings	
Tolerance Out	±1,8626e-07 (±400 LSB)

Test statistics	
Min CPU cycles	80
Max CPU cycles	104
Avg CPU cycles	95

Verification: Sub Float32 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for Math block Sub.

Test results				
Time step	1	2	...	214
CPU cycles	204	204	...	241
Inputs				
Plus (DSP)	-2	-1.962	...	2
Minus (DSP)	2	1.962	...	2
Plus	-2	-1.962	...	2
Minus	2	1.962	...	2
Outputs				
Out	-4	-3.925	...	0
Exp. Out	-4	-3.925	...	0
Out (DSP)	-4	-3.925	...	0
Exp. Out (DSP)	-4	-3.925	...	0

Test settings	
Tolerance Out	±1,8626e-07 (±400 LSB)

Test statistics	
Min CPU cycles	204
Max CPU cycles	241
Avg CPU cycles	222

Verification: Sub Float32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for Math block Sub.

Test results				
Time step	1	2	...	214
CPU cycles	57	57	...	57
Inputs				
Plus (DSP)	-2	-1.962	...	2
Minus (DSP)	2	1.962	...	2
Plus	-2	-1.962	...	2
Minus	2	1.962	...	2
Outputs				
Out	-4	-3.925	...	0
Exp. Out	-4	-3.925	...	0
Out (DSP)	-4	-3.925	...	0
Exp. Out (DSP)	-4	-3.925	...	0

Test settings	
Tolerance Out	±1,8626e-07 (±400 LSB)

Test statistics	
Min CPU cycles	57
Max CPU cycles	57
Avg CPU cycles	57

Verification: Sub Float32 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

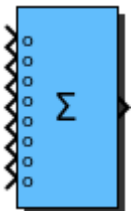
Inport test for Math block Sub.

Test results				
Time step	1	2	...	214
CPU cycles	50	50	...	50
Inputs				
Plus (DSP)	-2	-1.962	...	2
Minus (DSP)	2	1.962	...	2
Plus	-2	-1.962	...	2
Minus	2	1.962	...	2
Outputs				
Out	-4	-3.925	...	0
Exp. Out	-4	-3.925	...	0
Out (DSP)	-4	-3.925	...	0
Exp. Out (DSP)	-4	-3.925	...	0

Test settings	
Tolerance Out	±1,8626e-07 (±400 LSB)

Test statistics	
Min CPU cycles	50
Max CPU cycles	50
Avg CPU cycles	50

Block: Sum



Sum of inputs:
+ ... Input will be added to result.
- ... Input will be subtracted from result.
0 ... Input will be ignored.

Inports	
In1	Input #1
In2	Input #2
In3	Input #3
In4	Input #4
In5	Input #5
In6	Input #6
In7	Input #7
In8	Input #8

Outports	
Out	Result

Mask Parameters		
Name	**ID**	**Description**
In1	1	Input #1
In2	2	Input #2
In3	3	Input #3
In4	4	Input #4
In5	5	Input #5
In6	6	Input #6
In7	7	Input #7
In8	8	Input #8

Implementations:

FiP8	8 Bit Fixed Point Implementation
FiP16	16 Bit Fixed Point Implementation
FiP32	32 Bit Fixed Point Implementation
Float32	32 Bit Floating Point Implementation
Float64	64 Bit Floating Point Implementation

Implementation: FiP8

8 Bit Fixed Point Implementation

Inports Data Type	
In1	int8
In2	int8
In3	int8
In4	int8
In5	int8
In6	int8
In7	int8
In8	int8

Outports Data Type	
Out	int8

Implementation: FiP16

16 Bit Fixed Point Implementation

Inports Data Type	
In1	int16
In2	int16
In3	int16
In4	int16
In5	int16
In6	int16
In7	int16
In8	int16

Outports Data Type	
Out	int16

Implementation: FiP32

32 Bit Fixed Point Implementation

Inports Data Type	
In1	int32
In2	int32
In3	int32
In4	int32
In5	int32
In6	int32
In7	int32
In8	int32

Outports Data Type	
Out	int32

Implementation: Float32

32 Bit Floating Point Implementation

Inports Data Type	
In1	float32
In2	float32
In3	float32
In4	float32
In5	float32
In6	float32
In7	float32
In8	float32

Outports Data Type	
Out	float32

Implementation: Float64

64 Bit Floating Point Implementation

Inports Data Type	
In1	float64
In2	float64
In3	float64
In4	float64
In5	float64
In6	float64
In7	float64
In8	float64

Outports Data Type	
Out	float64

Verification: Sum FiP16 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test — OK

Inport test for Math block Sum.

Test results						
Time step	1	2	3	4	...	74
CPU cycles	222	222	222	222	...	222
Inputs						
In1 (DSP)	-32768	-30948	-29127	-27307	...	32767
In2 (DSP)	-32768	-30948	-29127	-27307	...	32767
In3 (DSP)	-32768	-30948	-29127	-27307	...	32767
In4 (DSP)	-32768	-30948	-29127	-27307	...	32767
In5 (DSP)	-32768	-30948	-29127	-27307	...	32767
In6 (DSP)	-32768	-30948	-29127	-27307	...	32767
In7 (DSP)	-32768	-30948	-29127	-27307	...	32767
In8 (DSP)	-32768	-31870	-30972	-30075	...	32767
In1	-1	-0.944	-0.889	-0.833	...	1
In2	-1	-0.944	-0.889	-0.833	...	1
In3	-1	-0.944	-0.889	-0.833	...	1
In4	-1	-0.944	-0.889	-0.833	...	1
In5	-1	-0.944	-0.889	-0.833	...	1
In6	-1	-0.944	-0.889	-0.833	...	1
In7	-1	-0.944	-0.889	-0.833	...	1
In8	-1	-0.973	-0.945	-0.918	...	1
Parameters						
In1	+					
In2	+					
In3	+					
In4	-					
In5	-					
In6	-					
In7	0					
In8	+					
Outputs						
Out	-1	-0.973	-0.945	-0.918	...	1
Exp. Out	-1	-0.973	-0.945	-0.918	...	1
Out (DSP)	-32767	-31870	-30972	-30075	...	32767
Exp. Out (DSP)	-32768	-31870	-30972	-30075	...	32767

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	222
Max CPU cycles	222
Avg CPU cycles	222

Test case: Conversion test OK

Conversion test for Math block Sum.

Test results			
Time step	1	2	3
Mask parameters			
In1	+	-	0
In2	+	-	0
In3	+	-	0
In4	+	-	0
In5	+	-	0
In6	+	-	0
In7	+	-	0
In8	+	-	0
Controller parameters			
sign	21845	43690	0
Exp. sign	21845	43690	0

Test settings	
Tolerance sign	±0,0000e+00

Test case: Conversion-on-Target test OK

Conversion-on-Target test for Math block Sum.

Test results			
Time step	1	2	3
Mask parameters			
In1	+	-	0
In2	+	-	0
In3	+	-	0
In4	+	-	0
In5	+	-	0
In6	+	-	0
In7	+	-	0
In8	+	-	0
Controller parameters			
sign	21845	43690	0
Exp. sign	21845	43690	0

Test settings	
Tolerance sign	±0,0000e+00

Test statistics	
Min CPU cycles	676
Max CPU cycles	714
Avg CPU cycles	690

Verification: Sum FiP16 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test — OK

Inport test for Math block Sum.

Test results						
Time step	1	2	3	4	...	74
CPU cycles	129	127	127	127	...	127
Inputs						
In1 (DSP)	-32768	-30948	-29127	-27307	...	32767
In2 (DSP)	-32768	-30948	-29127	-27307	...	32767
In3 (DSP)	-32768	-30948	-29127	-27307	...	32767
In4 (DSP)	-32768	-30948	-29127	-27307	...	32767
In5 (DSP)	-32768	-30948	-29127	-27307	...	32767
In6 (DSP)	-32768	-30948	-29127	-27307	...	32767
In7 (DSP)	-32768	-30948	-29127	-27307	...	32767
In8 (DSP)	-32768	-31870	-30972	-30075	...	32767
In1	-1	-0.944	-0.889	-0.833	...	1
In2	-1	-0.944	-0.889	-0.833	...	1
In3	-1	-0.944	-0.889	-0.833	...	1
In4	-1	-0.944	-0.889	-0.833	...	1
In5	-1	-0.944	-0.889	-0.833	...	1
In6	-1	-0.944	-0.889	-0.833	...	1
In7	-1	-0.944	-0.889	-0.833	...	1
In8	-1	-0.973	-0.945	-0.918	...	1
Parameters						
In1	+					
In2	+					
In3	+					
In4	-					
In5	-					
In6	-					
In7	0					
In8	+					
Outputs						
Out	-1	-0.973	-0.945	-0.918	...	1
Exp. Out	-1	-0.973	-0.945	-0.918	...	1
Out (DSP)	-32767	-31870	-30972	-30075	...	32767
Exp. Out (DSP)	-32768	-31870	-30972	-30075	...	32767

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	127
Max CPU cycles	129
Avg CPU cycles	127

Test case: Conversion test OK

Conversion test for Math block Sum.

Test results			
Time step	1	2	3
Mask parameters			
In1	+	-	0
In2	+	-	0
In3	+	-	0
In4	+	-	0
In5	+	-	0
In6	+	-	0
In7	+	-	0
In8	+	-	0
Controller parameters			
sign	21845	43690	0
Exp. sign	21845	43690	0

Test settings	
Tolerance sign	±0,0000e+00

Test case: Conversion-on-Target test OK

Conversion-on-Target test for Math block Sum.

Test results			
Time step	1	2	3
Mask parameters			
In1	+	-	0
In2	+	-	0
In3	+	-	0
In4	+	-	0
In5	+	-	0
In6	+	-	0
In7	+	-	0
In8	+	-	0
Controller parameters			
sign	21845	43690	0
Exp. sign	21845	43690	0

Test settings	
Tolerance sign	±0,0000e+00

Test statistics	
Min CPU cycles	333
Max CPU cycles	357
Avg CPU cycles	341

Verification: Sum FiP16 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for Math block Sum.

Test results						
Time step	1	2	3	4	...	74
CPU cycles	245	245	245	245	...	245
Inputs						
In1 (DSP)	-32768	-30948	-29127	-27307	...	32767
In2 (DSP)	-32768	-30948	-29127	-27307	...	32767
In3 (DSP)	-32768	-30948	-29127	-27307	...	32767
In4 (DSP)	-32768	-30948	-29127	-27307	...	32767
In5 (DSP)	-32768	-30948	-29127	-27307	...	32767
In6 (DSP)	-32768	-30948	-29127	-27307	...	32767
In7 (DSP)	-32768	-30948	-29127	-27307	...	32767
In8 (DSP)	-32768	-31870	-30972	-30075	...	32767
In1	-1	-0.944	-0.889	-0.833	...	1
In2	-1	-0.944	-0.889	-0.833	...	1
In3	-1	-0.944	-0.889	-0.833	...	1
In4	-1	-0.944	-0.889	-0.833	...	1
In5	-1	-0.944	-0.889	-0.833	...	1
In6	-1	-0.944	-0.889	-0.833	...	1
In7	-1	-0.944	-0.889	-0.833	...	1
In8	-1	-0.973	-0.945	-0.918	...	1
Parameters						
In1	+					
In2	+					
In3	+					
In4	-					
In5	-					
In6	-					
In7	0					
In8	+					
Outputs						
Out	-1	-0.973	-0.945	-0.918	...	1
Exp. Out	-1	-0.973	-0.945	-0.918	...	1
Out (DSP)	-32767	-31870	-30972	-30075	...	32767
Exp. Out (DSP)	-32768	-31870	-30972	-30075	...	32767

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	245
Max CPU cycles	245
Avg CPU cycles	245

Test case: Conversion test OK

Conversion test for Math block Sum.

Test results			
Time step	1	2	3
Mask parameters			
In1	+	-	0
In2	+	-	0
In3	+	-	0
In4	+	-	0
In5	+	-	0
In6	+	-	0
In7	+	-	0
In8	+	-	0
Controller parameters			
sign	21845	43690	0
Exp. sign	21845	43690	0

Test settings	
Tolerance sign	±0,0000e+00

Test case: Conversion-on-Target test OK

Conversion-on-Target test for Math block Sum.

Test results			
Time step	1	2	3
Mask parameters			
In1	+	-	0
In2	+	-	0
In3	+	-	0
In4	+	-	0
In5	+	-	0
In6	+	-	0
In7	+	-	0
In8	+	-	0
Controller parameters			
sign	21845	43690	0
Exp. sign	21845	43690	0

Test settings	
Tolerance sign	±0,0000e+00

Test statistics	
Min CPU cycles	507
Max CPU cycles	509
Avg CPU cycles	507

Verification: Sum FiP16 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test — OK

Inport test for Math block Sum.

Test results						
Time step	1	2	3	4	...	74
CPU cycles	198	199	199	199	...	199
Inputs						
In1 (DSP)	-32768	-30948	-29127	-27307	...	32767
In2 (DSP)	-32768	-30948	-29127	-27307	...	32767
In3 (DSP)	-32768	-30948	-29127	-27307	...	32767
In4 (DSP)	-32768	-30948	-29127	-27307	...	32767
In5 (DSP)	-32768	-30948	-29127	-27307	...	32767
In6 (DSP)	-32768	-30948	-29127	-27307	...	32767
In7 (DSP)	-32768	-30948	-29127	-27307	...	32767
In8 (DSP)	-32768	-31870	-30972	-30075	...	32767
In1	-1	-0.944	-0.889	-0.833	...	1
In2	-1	-0.944	-0.889	-0.833	...	1
In3	-1	-0.944	-0.889	-0.833	...	1
In4	-1	-0.944	-0.889	-0.833	...	1
In5	-1	-0.944	-0.889	-0.833	...	1
In6	-1	-0.944	-0.889	-0.833	...	1
In7	-1	-0.944	-0.889	-0.833	...	1
In8	-1	-0.973	-0.945	-0.918	...	1
Parameters						
In1	+					
In2	+					
In3	+					
In4	-					
In5	-					
In6	-					
In7	0					
In8	+					
Outputs						
Out	-1	-0.973	-0.945	-0.918	...	1
Exp. Out	-1	-0.973	-0.945	-0.918	...	1
Out (DSP)	-32767	-31870	-30972	-30075	...	32767
Exp. Out (DSP)	-32768	-31870	-30972	-30075	...	32767

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	198
Max CPU cycles	260
Avg CPU cycles	199

Test case: Conversion test OK

Conversion test for Math block Sum.

Test results			
Time step	1	2	3
Mask parameters			
In1	+	-	0
In2	+	-	0
In3	+	-	0
In4	+	-	0
In5	+	-	0
In6	+	-	0
In7	+	-	0
In8	+	-	0
Controller parameters			
sign	21845	43690	0
Exp. sign	21845	43690	0

Test settings	
Tolerance sign	±0,0000e+00

Test case: Conversion-on-Target test OK

Conversion-on-Target test for Math block Sum.

Test results			
Time step	1	2	3
Mask parameters			
In1	+	-	0
In2	+	-	0
In3	+	-	0
In4	+	-	0
In5	+	-	0
In6	+	-	0
In7	+	-	0
In8	+	-	0
Controller parameters			
sign	21845	43690	0
Exp. sign	21845	43690	0

Test settings	
Tolerance sign	±0,0000e+00

Test statistics	
Min CPU cycles	603
Max CPU cycles	614
Avg CPU cycles	610

Verification: Sum FiP16 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test — OK

Inport test for Math block Sum.

Test results						
Time step	1	2	3	4	...	74
CPU cycles	110	110	110	110	...	110
Inputs						
In1 (DSP)	-32768	-30948	-29127	-27307	...	32767
In2 (DSP)	-32768	-30948	-29127	-27307	...	32767
In3 (DSP)	-32768	-30948	-29127	-27307	...	32767
In4 (DSP)	-32768	-30948	-29127	-27307	...	32767
In5 (DSP)	-32768	-30948	-29127	-27307	...	32767
In6 (DSP)	-32768	-30948	-29127	-27307	...	32767
In7 (DSP)	-32768	-30948	-29127	-27307	...	32767
In8 (DSP)	-32768	-31870	-30972	-30075	...	32767
In1	-1	-0.944	-0.889	-0.833	...	1
In2	-1	-0.944	-0.889	-0.833	...	1
In3	-1	-0.944	-0.889	-0.833	...	1
In4	-1	-0.944	-0.889	-0.833	...	1
In5	-1	-0.944	-0.889	-0.833	...	1
In6	-1	-0.944	-0.889	-0.833	...	1
In7	-1	-0.944	-0.889	-0.833	...	1
In8	-1	-0.973	-0.945	-0.918	...	1
Parameters						
In1	+					
In2	+					
In3	+					
In4	-					
In5	-					
In6	-					
In7	0					
In8	+					
Outputs						
Out	-1	-0.973	-0.945	-0.918	...	1
Exp. Out	-1	-0.973	-0.945	-0.918	...	1
Out (DSP)	-32767	-31870	-30972	-30075	...	32767
Exp. Out (DSP)	-32768	-31870	-30972	-30075	...	32767

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	110
Max CPU cycles	110
Avg CPU cycles	110

Test case: Conversion test OK

Conversion test for Math block Sum.

Test results			
Time step	1	2	3
Mask parameters			
In1	+	-	0
In2	+	-	0
In3	+	-	0
In4	+	-	0
In5	+	-	0
In6	+	-	0
In7	+	-	0
In8	+	-	0
Controller parameters			
sign	21845	43690	0
Exp. sign	21845	43690	0

Test settings	
Tolerance sign	±0,0000e+00

Test case: Conversion-on-Target test OK

Conversion-on-Target test for Math block Sum.

Test results			
Time step	1	2	3
Mask parameters			
In1	+	-	0
In2	+	-	0
In3	+	-	0
In4	+	-	0
In5	+	-	0
In6	+	-	0
In7	+	-	0
In8	+	-	0
Controller parameters			
sign	21845	43690	0
Exp. sign	21845	43690	0

Test settings	
Tolerance sign	±0,0000e+00

Test statistics	
Min CPU cycles	280
Max CPU cycles	301
Avg CPU cycles	293

Verification: Sum FiP16 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test — OK

Inport test for Math block Sum.

Test results						
Time step	1	2	3	4	...	74
CPU cycles	173	174	174	174	...	174
Inputs						
In1 (DSP)	-32768	-30948	-29127	-27307	...	32767
In2 (DSP)	-32768	-30948	-29127	-27307	...	32767
In3 (DSP)	-32768	-30948	-29127	-27307	...	32767
In4 (DSP)	-32768	-30948	-29127	-27307	...	32767
In5 (DSP)	-32768	-30948	-29127	-27307	...	32767
In6 (DSP)	-32768	-30948	-29127	-27307	...	32767
In7 (DSP)	-32768	-30948	-29127	-27307	...	32767
In8 (DSP)	-32768	-31870	-30972	-30075	...	32767
In1	-1	-0.944	-0.889	-0.833	...	1
In2	-1	-0.944	-0.889	-0.833	...	1
In3	-1	-0.944	-0.889	-0.833	...	1
In4	-1	-0.944	-0.889	-0.833	...	1
In5	-1	-0.944	-0.889	-0.833	...	1
In6	-1	-0.944	-0.889	-0.833	...	1
In7	-1	-0.944	-0.889	-0.833	...	1
In8	-1	-0.973	-0.945	-0.918	...	1
Parameters						
In1	+					
In2	+					
In3	+					
In4	-					
In5	-					
In6	-					
In7	0					
In8	+					
Outputs						
Out	-1	-0.973	-0.945	-0.918	...	1
Exp. Out	-1	-0.973	-0.945	-0.918	...	1
Out (DSP)	-32767	-31870	-30972	-30075	...	32767
Exp. Out (DSP)	-32768	-31870	-30972	-30075	...	32767

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	173
Max CPU cycles	174
Avg CPU cycles	173

Test case: Conversion test OK

Conversion test for Math block Sum.

Test results			
Time step	1	2	3
Mask parameters			
In1	+	-	0
In2	+	-	0
In3	+	-	0
In4	+	-	0
In5	+	-	0
In6	+	-	0
In7	+	-	0
In8	+	-	0
Controller parameters			
sign	21845	43690	0
Exp. sign	21845	43690	0

Test settings	
Tolerance sign	±0,0000e+00

Test case: Conversion-on-Target test OK

Conversion-on-Target test for Math block Sum.

Test results			
Time step	1	2	3
Mask parameters			
In1	+	-	0
In2	+	-	0
In3	+	-	0
In4	+	-	0
In5	+	-	0
In6	+	-	0
In7	+	-	0
In8	+	-	0
Controller parameters			
sign	21845	43690	0
Exp. sign	21845	43690	0

Test settings	
Tolerance sign	±0,0000e+00

Test statistics	
Min CPU cycles	303
Max CPU cycles	335
Avg CPU cycles	323

Verification: Sum FiP16 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test — OK

Inport test for Math block Sum.

Test results						
Time step	1	2	3	4	...	74
CPU cycles	246	164	164	164	...	164
Inputs						
In1 (DSP)	-32768	-30948	-29127	-27307	...	32767
In2 (DSP)	-32768	-30948	-29127	-27307	...	32767
In3 (DSP)	-32768	-30948	-29127	-27307	...	32767
In4 (DSP)	-32768	-30948	-29127	-27307	...	32767
In5 (DSP)	-32768	-30948	-29127	-27307	...	32767
In6 (DSP)	-32768	-30948	-29127	-27307	...	32767
In7 (DSP)	-32768	-30948	-29127	-27307	...	32767
In8 (DSP)	-32768	-31870	-30972	-30075	...	32767
In1	-1	-0.944	-0.889	-0.833	...	1
In2	-1	-0.944	-0.889	-0.833	...	1
In3	-1	-0.944	-0.889	-0.833	...	1
In4	-1	-0.944	-0.889	-0.833	...	1
In5	-1	-0.944	-0.889	-0.833	...	1
In6	-1	-0.944	-0.889	-0.833	...	1
In7	-1	-0.944	-0.889	-0.833	...	1
In8	-1	-0.973	-0.945	-0.918	...	1
Parameters						
In1	+					
In2	+					
In3	+					
In4	-					
In5	-					
In6	-					
In7	0					
In8	+					
Outputs						
Out	-1	-0.973	-0.945	-0.918	...	1
Exp. Out	-1	-0.973	-0.945	-0.918	...	1
Out (DSP)	-32767	-31870	-30972	-30075	...	32767
Exp. Out (DSP)	-32768	-31870	-30972	-30075	...	32767

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	164
Max CPU cycles	246
Avg CPU cycles	165

Test case: Conversion test OK

Conversion test for Math block Sum.

Test results			
Time step	1	2	3
Mask parameters			
In1	+	-	0
In2	+	-	0
In3	+	-	0
In4	+	-	0
In5	+	-	0
In6	+	-	0
In7	+	-	0
In8	+	-	0
Controller parameters			
sign	21845	43690	0
Exp. sign	21845	43690	0

Test settings	
Tolerance sign	±0,0000e+00

Test case: Conversion-on-Target test OK

Conversion-on-Target test for Math block Sum.

Test results			
Time step	1	2	3
Mask parameters			
In1	+	-	0
In2	+	-	0
In3	+	-	0
In4	+	-	0
In5	+	-	0
In6	+	-	0
In7	+	-	0
In8	+	-	0
Controller parameters			
sign	21845	43690	0
Exp. sign	21845	43690	0

Test settings	
Tolerance sign	±0,0000e+00

Test statistics	
Min CPU cycles	336
Max CPU cycles	427
Avg CPU cycles	375

Verification: Sum FiP16 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test — OK

Inport test for Math block Sum.

Test results						
Time step	1	2	3	4	...	74
CPU cycles	250	250	250	250	...	250
Inputs						
In1 (DSP)	-32768	-30948	-29127	-27307	...	32767
In2 (DSP)	-32768	-30948	-29127	-27307	...	32767
In3 (DSP)	-32768	-30948	-29127	-27307	...	32767
In4 (DSP)	-32768	-30948	-29127	-27307	...	32767
In5 (DSP)	-32768	-30948	-29127	-27307	...	32767
In6 (DSP)	-32768	-30948	-29127	-27307	...	32767
In7 (DSP)	-32768	-30948	-29127	-27307	...	32767
In8 (DSP)	-32768	-31870	-30972	-30075	...	32767
In1	-1	-0.944	-0.889	-0.833	...	1
In2	-1	-0.944	-0.889	-0.833	...	1
In3	-1	-0.944	-0.889	-0.833	...	1
In4	-1	-0.944	-0.889	-0.833	...	1
In5	-1	-0.944	-0.889	-0.833	...	1
In6	-1	-0.944	-0.889	-0.833	...	1
In7	-1	-0.944	-0.889	-0.833	...	1
In8	-1	-0.973	-0.945	-0.918	...	1
Parameters						
In1	+					
In2	+					
In3	+					
In4	-					
In5	-					
In6	-					
In7	0					
In8	+					
Outputs						
Out	-1	-0.973	-0.945	-0.918	...	1
Exp. Out	-1	-0.973	-0.945	-0.918	...	1
Out (DSP)	-32767	-31870	-30972	-30075	...	32767
Exp. Out (DSP)	-32768	-31870	-30972	-30075	...	32767

Test settings	
Tolerance Out	±3,0518e-05 (±1 LSB)

Test statistics	
Min CPU cycles	250
Max CPU cycles	250
Avg CPU cycles	250

Test case: Conversion test OK

Conversion test for Math block Sum.

Test results			
Time step	1	2	3
Mask parameters			
In1	+	-	0
In2	+	-	0
In3	+	-	0
In4	+	-	0
In5	+	-	0
In6	+	-	0
In7	+	-	0
In8	+	-	0
Controller parameters			
sign	21845	43690	0
Exp. sign	21845	43690	0

Test settings	
Tolerance sign	±0,0000e+00

Test case: Conversion-on-Target test OK

Conversion-on-Target test for Math block Sum.

Test results			
Time step	1	2	3
Mask parameters			
In1	+	-	0
In2	+	-	0
In3	+	-	0
In4	+	-	0
In5	+	-	0
In6	+	-	0
In7	+	-	0
In8	+	-	0
Controller parameters			
sign	21845	43690	0
Exp. sign	21845	43690	0

Test settings	
Tolerance sign	±0,0000e+00

Test statistics	
Min CPU cycles	567
Max CPU cycles	624
Avg CPU cycles	598

Verification: Sum FiP32 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test — OK

Inport test for Math block Sum.

Test results				
Time step	1	2	...	74
CPU cycles	369	364	...	364
Inputs				
In1 (DSP)	-2147483648	-2028179001	...	2147483647
In2 (DSP)	-2147483648	-2028179001	...	2147483647
In3 (DSP)	-2147483648	-2028179001	...	2147483647
In4 (DSP)	-2147483648	-2028179001	...	2147483647
In5 (DSP)	-2147483648	-2028179001	...	2147483647
In6 (DSP)	-2147483648	-2028179001	...	2147483647
In7 (DSP)	-2147483648	-2028179001	...	2147483647
In8 (DSP)	-2147483648	-2088648480	...	2147483647
In1	-1	-0.944	...	1
In2	-1	-0.944	...	1
In3	-1	-0.944	...	1
In4	-1	-0.944	...	1
In5	-1	-0.944	...	1
In6	-1	-0.944	...	1
In7	-1	-0.944	...	1
In8	-1	-0.973	...	1
Parameters				
In1	+			
In2	+			
In3	+			
In4	-			
In5	-			
In6	-			
In7	0			
In8	+			
Outputs				
Out	-1	-0.973	...	1
Exp. Out	-1	-0.973	...	1
Out (DSP)	-2147483647	-2088648480	...	2147483647
Exp. Out (DSP)	-2147483648	-2088648480	...	2147483647

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	364
Max CPU cycles	369
Avg CPU cycles	364

Test case: Conversion test **OK**

Conversion test for Math block Sum.

Test results			
Time step	1	2	3
Mask parameters			
In1	+	-	0
In2	+	-	0
In3	+	-	0
In4	+	-	0
In5	+	-	0
In6	+	-	0
In7	+	-	0
In8	+	-	0
Controller parameters			
sign	21845	43690	0
Exp. sign	21845	43690	0

Test settings	
Tolerance sign	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Math block Sum.

Test results			
Time step	1	2	3
Mask parameters			
In1	+	-	0
In2	+	-	0
In3	+	-	0
In4	+	-	0
In5	+	-	0
In6	+	-	0
In7	+	-	0
In8	+	-	0
Controller parameters			
sign	21845	43690	0
Exp. sign	21845	43690	0

Test settings	
Tolerance sign	±0,0000e+00

Test statistics	
Min CPU cycles	671
Max CPU cycles	704
Avg CPU cycles	684

Verification: Sum FiP32 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test — OK

Inport test for Math block Sum.

Test results				
Time step	1	2	...	74
CPU cycles	159	155	...	155
Inputs				
In1 (DSP)	-2147483648	-2028179001	...	2147483647
In2 (DSP)	-2147483648	-2028179001	...	2147483647
In3 (DSP)	-2147483648	-2028179001	...	2147483647
In4 (DSP)	-2147483648	-2028179001	...	2147483647
In5 (DSP)	-2147483648	-2028179001	...	2147483647
In6 (DSP)	-2147483648	-2028179001	...	2147483647
In7 (DSP)	-2147483648	-2028179001	...	2147483647
In8 (DSP)	-2147483648	-2088648480	...	2147483647
In1	-1	-0.944	...	1
In2	-1	-0.944	...	1
In3	-1	-0.944	...	1
In4	-1	-0.944	...	1
In5	-1	-0.944	...	1
In6	-1	-0.944	...	1
In7	-1	-0.944	...	1
In8	-1	-0.973	...	1
Parameters				
In1	+			
In2	+			
In3	+			
In4	-			
In5	-			
In6	-			
In7	0			
In8	+			
Outputs				
Out	-1	-0.973	...	1
Exp. Out	-1	-0.973	...	1
Out (DSP)	-2147483647	-2088648480	...	2147483647
Exp. Out (DSP)	-2147483648	-2088648480	...	2147483647

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	155
Max CPU cycles	159
Avg CPU cycles	155

Test case: Conversion test OK

Conversion test for Math block Sum.

Test results			
Time step	1	2	3
Mask parameters			
In1	+	-	0
In2	+	-	0
In3	+	-	0
In4	+	-	0
In5	+	-	0
In6	+	-	0
In7	+	-	0
In8	+	-	0
Controller parameters			
sign	21845	43690	0
Exp. sign	21845	43690	0

Test settings	
Tolerance sign	±0,0000e+00

Test case: Conversion-on-Target test OK

Conversion-on-Target test for Math block Sum.

Test results			
Time step	1	2	3
Mask parameters			
In1	+	-	0
In2	+	-	0
In3	+	-	0
In4	+	-	0
In5	+	-	0
In6	+	-	0
In7	+	-	0
In8	+	-	0
Controller parameters			
sign	21845	43690	0
Exp. sign	21845	43690	0

Test settings	
Tolerance sign	±0,0000e+00

Test statistics	
Min CPU cycles	333
Max CPU cycles	357
Avg CPU cycles	341

Verification: Sum FiP32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test — OK

Inport test for Math block Sum.

Test results				
Time step	1	2	...	74
CPU cycles	248	248	...	248
Inputs				
In1 (DSP)	-2147483648	-2028179001	...	2147483647
In2 (DSP)	-2147483648	-2028179001	...	2147483647
In3 (DSP)	-2147483648	-2028179001	...	2147483647
In4 (DSP)	-2147483648	-2028179001	...	2147483647
In5 (DSP)	-2147483648	-2028179001	...	2147483647
In6 (DSP)	-2147483648	-2028179001	...	2147483647
In7 (DSP)	-2147483648	-2028179001	...	2147483647
In8 (DSP)	-2147483648	-2088648480	...	2147483647
In1	-1	-0.944	...	1
In2	-1	-0.944	...	1
In3	-1	-0.944	...	1
In4	-1	-0.944	...	1
In5	-1	-0.944	...	1
In6	-1	-0.944	...	1
In7	-1	-0.944	...	1
In8	-1	-0.973	...	1
Parameters				
In1	+			
In2	+			
In3	+			
In4	-			
In5	-			
In6	-			
In7	0			
In8	+			
Outputs				
Out	-1	-0.973	...	1
Exp. Out	-1	-0.973	...	1
Out (DSP)	-2147483647	-2088648480	...	2147483647
Exp. Out (DSP)	-2147483648	-2088648480	...	2147483647

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	248
Max CPU cycles	248
Avg CPU cycles	248

Test case: Conversion test OK

Conversion test for Math block Sum.

Test results			
Time step	1	2	3
Mask parameters			
In1	+	-	0
In2	+	-	0
In3	+	-	0
In4	+	-	0
In5	+	-	0
In6	+	-	0
In7	+	-	0
In8	+	-	0
Controller parameters			
sign	21845	43690	0
Exp. sign	21845	43690	0

Test settings	
Tolerance sign	±0,0000e+00

Test case: Conversion-on-Target test OK

Conversion-on-Target test for Math block Sum.

Test results			
Time step	1	2	3
Mask parameters			
In1	+	-	0
In2	+	-	0
In3	+	-	0
In4	+	-	0
In5	+	-	0
In6	+	-	0
In7	+	-	0
In8	+	-	0
Controller parameters			
sign	21845	43690	0
Exp. sign	21845	43690	0

Test settings	
Tolerance sign	±0,0000e+00

Test statistics	
Min CPU cycles	507
Max CPU cycles	509
Avg CPU cycles	507

Verification: Sum FiP32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test — OK

Inport test for Math block Sum.

Test results				
Time step	1	2	...	74
CPU cycles	287	283	...	285
Inputs				
In1 (DSP)	-2147483648	-2028179001	...	2147483647
In2 (DSP)	-2147483648	-2028179001	...	2147483647
In3 (DSP)	-2147483648	-2028179001	...	2147483647
In4 (DSP)	-2147483648	-2028179001	...	2147483647
In5 (DSP)	-2147483648	-2028179001	...	2147483647
In6 (DSP)	-2147483648	-2028179001	...	2147483647
In7 (DSP)	-2147483648	-2028179001	...	2147483647
In8 (DSP)	-2147483648	-2088648480	...	2147483647
In1	-1	-0.944	...	1
In2	-1	-0.944	...	1
In3	-1	-0.944	...	1
In4	-1	-0.944	...	1
In5	-1	-0.944	...	1
In6	-1	-0.944	...	1
In7	-1	-0.944	...	1
In8	-1	-0.973	...	1
Parameters				
In1	+			
In2	+			
In3	+			
In4	-			
In5	-			
In6	-			
In7	0			
In8	+			
Outputs				
Out	-1	-0.973	...	1
Exp. Out	-1	-0.973	...	1
Out (DSP)	-2147483647	-2088648480	...	2147483647
Exp. Out (DSP)	-2147483648	-2088648480	...	2147483647

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	283
Max CPU cycles	287
Avg CPU cycles	284

Test case: Conversion test OK

Conversion test for Math block Sum.

Test results			
Time step	1	2	3
Mask parameters			
In1	+	-	0
In2	+	-	0
In3	+	-	0
In4	+	-	0
In5	+	-	0
In6	+	-	0
In7	+	-	0
In8	+	-	0
Controller parameters			
sign	21845	43690	0
Exp. sign	21845	43690	0

Test settings	
Tolerance sign	±0,0000e+00

Test case: Conversion-on-Target test OK

Conversion-on-Target test for Math block Sum.

Test results			
Time step	1	2	3
Mask parameters			
In1	+	-	0
In2	+	-	0
In3	+	-	0
In4	+	-	0
In5	+	-	0
In6	+	-	0
In7	+	-	0
In8	+	-	0
Controller parameters			
sign	21845	43690	0
Exp. sign	21845	43690	0

Test settings	
Tolerance sign	±0,0000e+00

Test statistics	
Min CPU cycles	603
Max CPU cycles	614
Avg CPU cycles	610

Verification: Sum FiP32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test — OK

Inport test for Math block Sum.

Test results				
Time step	1	2	...	74
CPU cycles	158	154	...	153
Inputs				
In1 (DSP)	-2147483648	-2028179001	...	2147483647
In2 (DSP)	-2147483648	-2028179001	...	2147483647
In3 (DSP)	-2147483648	-2028179001	...	2147483647
In4 (DSP)	-2147483648	-2028179001	...	2147483647
In5 (DSP)	-2147483648	-2028179001	...	2147483647
In6 (DSP)	-2147483648	-2028179001	...	2147483647
In7 (DSP)	-2147483648	-2028179001	...	2147483647
In8 (DSP)	-2147483648	-2088648480	...	2147483647
In1	-1	-0.944	...	1
In2	-1	-0.944	...	1
In3	-1	-0.944	...	1
In4	-1	-0.944	...	1
In5	-1	-0.944	...	1
In6	-1	-0.944	...	1
In7	-1	-0.944	...	1
In8	-1	-0.973	...	1
Parameters				
In1	+			
In2	+			
In3	+			
In4	-			
In5	-			
In6	-			
In7	0			
In8	+			
Outputs				
Out	-1	-0.973	...	1
Exp. Out	-1	-0.973	...	1
Out (DSP)	-2147483647	-2088648480	...	2147483647
Exp. Out (DSP)	-2147483648	-2088648480	...	2147483647

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	153
Max CPU cycles	158
Avg CPU cycles	153

Test case: Conversion test OK

Conversion test for Math block Sum.

Test results			
Time step	1	2	3
Mask parameters			
In1	+	-	0
In2	+	-	0
In3	+	-	0
In4	+	-	0
In5	+	-	0
In6	+	-	0
In7	+	-	0
In8	+	-	0
Controller parameters			
sign	21845	43690	0
Exp. sign	21845	43690	0

Test settings	
Tolerance sign	±0,0000e+00

Test case: Conversion-on-Target test OK

Conversion-on-Target test for Math block Sum.

Test results			
Time step	1	2	3
Mask parameters			
In1	+	-	0
In2	+	-	0
In3	+	-	0
In4	+	-	0
In5	+	-	0
In6	+	-	0
In7	+	-	0
In8	+	-	0
Controller parameters			
sign	21845	43690	0
Exp. sign	21845	43690	0

Test settings	
Tolerance sign	±0,0000e+00

Test statistics	
Min CPU cycles	280
Max CPU cycles	301
Avg CPU cycles	293

Verification: Sum FiP32 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test — OK

Inport test for Math block Sum.

Test results				
Time step	1	2	...	74
CPU cycles	212	211	...	211
Inputs				
In1 (DSP)	-2147483648	-2028179001	...	2147483647
In2 (DSP)	-2147483648	-2028179001	...	2147483647
In3 (DSP)	-2147483648	-2028179001	...	2147483647
In4 (DSP)	-2147483648	-2028179001	...	2147483647
In5 (DSP)	-2147483648	-2028179001	...	2147483647
In6 (DSP)	-2147483648	-2028179001	...	2147483647
In7 (DSP)	-2147483648	-2028179001	...	2147483647
In8 (DSP)	-2147483648	-2088648480	...	2147483647
In1	-1	-0.944	...	1
In2	-1	-0.944	...	1
In3	-1	-0.944	...	1
In4	-1	-0.944	...	1
In5	-1	-0.944	...	1
In6	-1	-0.944	...	1
In7	-1	-0.944	...	1
In8	-1	-0.973	...	1
Parameters				
In1	+			
In2	+			
In3	+			
In4	-			
In5	-			
In6	-			
In7	0			
In8	+			
Outputs				
Out	-1	-0.973	...	1
Exp. Out	-1	-0.973	...	1
Out (DSP)	-2147483647	-2088648480	...	2147483647
Exp. Out (DSP)	-2147483648	-2088648480	...	2147483647

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	211
Max CPU cycles	212
Avg CPU cycles	211

Test case: Conversion test OK

Conversion test for Math block Sum.

Test results			
Time step	1	2	3
Mask parameters			
In1	+	-	0
In2	+	-	0
In3	+	-	0
In4	+	-	0
In5	+	-	0
In6	+	-	0
In7	+	-	0
In8	+	-	0
Controller parameters			
sign	21845	43690	0
Exp. sign	21845	43690	0

Test settings	
Tolerance sign	±0,0000e+00

Test case: Conversion-on-Target test OK

Conversion-on-Target test for Math block Sum.

Test results			
Time step	1	2	3
Mask parameters			
In1	+	-	0
In2	+	-	0
In3	+	-	0
In4	+	-	0
In5	+	-	0
In6	+	-	0
In7	+	-	0
In8	+	-	0
Controller parameters			
sign	21845	43690	0
Exp. sign	21845	43690	0

Test settings	
Tolerance sign	±0,0000e+00

Test statistics	
Min CPU cycles	303
Max CPU cycles	335
Avg CPU cycles	323

Verification: Sum FiP32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test — OK

Inport test for Math block Sum.

Test results				
Time step	1	2	...	74
CPU cycles	267	184	...	184
Inputs				
In1 (DSP)	-2147483648	-2028179001	...	2147483647
In2 (DSP)	-2147483648	-2028179001	...	2147483647
In3 (DSP)	-2147483648	-2028179001	...	2147483647
In4 (DSP)	-2147483648	-2028179001	...	2147483647
In5 (DSP)	-2147483648	-2028179001	...	2147483647
In6 (DSP)	-2147483648	-2028179001	...	2147483647
In7 (DSP)	-2147483648	-2028179001	...	2147483647
In8 (DSP)	-2147483648	-2088648480	...	2147483647
In1	-1	-0.944	...	1
In2	-1	-0.944	...	1
In3	-1	-0.944	...	1
In4	-1	-0.944	...	1
In5	-1	-0.944	...	1
In6	-1	-0.944	...	1
In7	-1	-0.944	...	1
In8	-1	-0.973	...	1
Parameters				
In1	+			
In2	+			
In3	+			
In4	-			
In5	-			
In6	-			
In7	0			
In8	+			
Outputs				
Out	-1	-0.973	...	1
Exp. Out	-1	-0.973	...	1
Out (DSP)	-2147483647	-2088648480	...	2147483647
Exp. Out (DSP)	-2147483648	-2088648480	...	2147483647

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	184
Max CPU cycles	267
Avg CPU cycles	185

Test case: Conversion test OK

Conversion test for Math block Sum.

Test results			
Time step	1	2	3
Mask parameters			
In1	+	-	0
In2	+	-	0
In3	+	-	0
In4	+	-	0
In5	+	-	0
In6	+	-	0
In7	+	-	0
In8	+	-	0
Controller parameters			
sign	21845	43690	0
Exp. sign	21845	43690	0

Test settings	
Tolerance sign	±0,0000e+00

Test case: Conversion-on-Target test OK

Conversion-on-Target test for Math block Sum.

Test results			
Time step	1	2	3
Mask parameters			
In1	+	-	0
In2	+	-	0
In3	+	-	0
In4	+	-	0
In5	+	-	0
In6	+	-	0
In7	+	-	0
In8	+	-	0
Controller parameters			
sign	21845	43690	0
Exp. sign	21845	43690	0

Test settings	
Tolerance sign	±0,0000e+00

Test statistics	
Min CPU cycles	336
Max CPU cycles	417
Avg CPU cycles	371

Verification: Sum FiP32 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test — OK

Inport test for Math block Sum.

Test results				
Time step	1	2	...	74
CPU cycles	394	389	...	389
Inputs				
In1 (DSP)	-2147483648	-2028179001	...	2147483647
In2 (DSP)	-2147483648	-2028179001	...	2147483647
In3 (DSP)	-2147483648	-2028179001	...	2147483647
In4 (DSP)	-2147483648	-2028179001	...	2147483647
In5 (DSP)	-2147483648	-2028179001	...	2147483647
In6 (DSP)	-2147483648	-2028179001	...	2147483647
In7 (DSP)	-2147483648	-2028179001	...	2147483647
In8 (DSP)	-2147483648	-2088648480	...	2147483647
In1	-1	-0.944	...	1
In2	-1	-0.944	...	1
In3	-1	-0.944	...	1
In4	-1	-0.944	...	1
In5	-1	-0.944	...	1
In6	-1	-0.944	...	1
In7	-1	-0.944	...	1
In8	-1	-0.973	...	1
Parameters				
In1	+			
In2	+			
In3	+			
In4	-			
In5	-			
In6	-			
In7	0			
In8	+			
Outputs				
Out	-1	-0.973	...	1
Exp. Out	-1	-0.973	...	1
Out (DSP)	-2147483647	-2088648480	...	2147483647
Exp. Out (DSP)	-2147483648	-2088648480	...	2147483647

Test settings	
Tolerance Out	±4,6566e-10 (±1 LSB)

Test statistics	
Min CPU cycles	389
Max CPU cycles	394
Avg CPU cycles	389

Test case: Conversion test **OK**

Conversion test for Math block Sum.

Test results			
Time step	1	2	3
Mask parameters			
In1	+	-	0
In2	+	-	0
In3	+	-	0
In4	+	-	0
In5	+	-	0
In6	+	-	0
In7	+	-	0
In8	+	-	0
Controller parameters			
sign	21845	43690	0
Exp. sign	21845	43690	0

Test settings	
Tolerance sign	±0,0000e+00

Test case: Conversion-on-Target test **OK**

Conversion-on-Target test for Math block Sum.

Test results			
Time step	1	2	3
Mask parameters			
In1	+	-	0
In2	+	-	0
In3	+	-	0
In4	+	-	0
In5	+	-	0
In6	+	-	0
In7	+	-	0
In8	+	-	0
Controller parameters			
sign	21845	43690	0
Exp. sign	21845	43690	0

Test settings	
Tolerance sign	±0,0000e+00

Test statistics	
Min CPU cycles	582
Max CPU cycles	623
Avg CPU cycles	602

Verification: Sum Float32 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test — OK

Inport test for Math block Sum.

Test results				
Time step	1	2	...	74
CPU cycles	203	203	...	203
Inputs				
In1 (DSP)	-1	-0.944	...	1
In2 (DSP)	-1	-0.944	...	1
In3 (DSP)	-1	-0.944	...	1
In4 (DSP)	-1	-0.944	...	1
In5 (DSP)	-1	-0.944	...	1
In6 (DSP)	-1	-0.944	...	1
In7 (DSP)	-1	-0.944	...	1
In8 (DSP)	-1	-0.973	...	1
In1	-1	-0.944	...	1
In2	-1	-0.944	...	1
In3	-1	-0.944	...	1
In4	-1	-0.944	...	1
In5	-1	-0.944	...	1
In6	-1	-0.944	...	1
In7	-1	-0.944	...	1
In8	-1	-0.973	...	1
Parameters				
In1	+			
In2	+			
In3	+			
In4	-			
In5	-			
In6	-			
In7	0			
In8	+			
Outputs				
Out	-1	-0.973	...	1
Exp. Out	-1	-0.973	...	1
Out (DSP)	-1	-0.973	...	1
Exp. Out (DSP)	-1	-0.973	...	1

Test settings	
Tolerance Out	±1,8626e-07 (±400 LSB)

Test statistics	
Min CPU cycles	203
Max CPU cycles	203
Avg CPU cycles	203

Test case: Conversion test OK

Conversion test for Math block Sum.

Test results			
Time step	1	2	3
Mask parameters			
In1	+	-	0
In2	+	-	0
In3	+	-	0
In4	+	-	0
In5	+	-	0
In6	+	-	0
In7	+	-	0
In8	+	-	0
Controller parameters			
sign	21845	43690	0
Exp. sign	21845	43690	0

Test settings	
Tolerance sign	±0,0000e+00

Test case: Conversion-on-Target test OK

Conversion-on-Target test for Math block Sum.

Test results			
Time step	1	2	3
Mask parameters			
In1	+	-	0
In2	+	-	0
In3	+	-	0
In4	+	-	0
In5	+	-	0
In6	+	-	0
In7	+	-	0
In8	+	-	0
Controller parameters			
sign	21845	43690	0
Exp. sign	21845	43690	0

Test settings	
Tolerance sign	±0,0000e+00

Test statistics	
Min CPU cycles	684
Max CPU cycles	716
Avg CPU cycles	697

Verification: Sum Float32 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test — OK

Inport test for Math block Sum.

Test results				
Time step	1	2	...	74
CPU cycles	117	117	...	117
Inputs				
In1 (DSP)	-1	-0.944	...	1
In2 (DSP)	-1	-0.944	...	1
In3 (DSP)	-1	-0.944	...	1
In4 (DSP)	-1	-0.944	...	1
In5 (DSP)	-1	-0.944	...	1
In6 (DSP)	-1	-0.944	...	1
In7 (DSP)	-1	-0.944	...	1
In8 (DSP)	-1	-0.973	...	1
In1	-1	-0.944	...	1
In2	-1	-0.944	...	1
In3	-1	-0.944	...	1
In4	-1	-0.944	...	1
In5	-1	-0.944	...	1
In6	-1	-0.944	...	1
In7	-1	-0.944	...	1
In8	-1	-0.973	...	1
Parameters				
In1	+			
In2	+			
In3	+			
In4	-			
In5	-			
In6	-			
In7	0			
In8	+			
Outputs				
Out	-1	-0.973	...	1
Exp. Out	-1	-0.973	...	1
Out (DSP)	-1	-0.973	...	1
Exp. Out (DSP)	-1	-0.973	...	1

Test settings	
Tolerance Out	±1,8626e-07 (±400 LSB)

Test statistics	
Min CPU cycles	117
Max CPU cycles	117
Avg CPU cycles	117

Test case: Conversion test OK

Conversion test for Math block Sum.

Test results			
Time step	1	2	3
Mask parameters			
In1	+	-	0
In2	+	-	0
In3	+	-	0
In4	+	-	0
In5	+	-	0
In6	+	-	0
In7	+	-	0
In8	+	-	0
Controller parameters			
sign	21845	43690	0
Exp. sign	21845	43690	0

Test settings	
Tolerance sign	±0,0000e+00

Test case: Conversion-on-Target test OK

Conversion-on-Target test for Math block Sum.

Test results			
Time step	1	2	3
Mask parameters			
In1	+	-	0
In2	+	-	0
In3	+	-	0
In4	+	-	0
In5	+	-	0
In6	+	-	0
In7	+	-	0
In8	+	-	0
Controller parameters			
sign	21845	43690	0
Exp. sign	21845	43690	0

Test settings	
Tolerance sign	±0,0000e+00

Test statistics	
Min CPU cycles	333
Max CPU cycles	357
Avg CPU cycles	341

Verification: Sum Float32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for Math block Sum.

Test results				
Time step	1	2	...	74
CPU cycles	235	235	...	235
Inputs				
In1 (DSP)	-1	-0.944	...	1
In2 (DSP)	-1	-0.944	...	1
In3 (DSP)	-1	-0.944	...	1
In4 (DSP)	-1	-0.944	...	1
In5 (DSP)	-1	-0.944	...	1
In6 (DSP)	-1	-0.944	...	1
In7 (DSP)	-1	-0.944	...	1
In8 (DSP)	-1	-0.973	...	1
In1	-1	-0.944	...	1
In2	-1	-0.944	...	1
In3	-1	-0.944	...	1
In4	-1	-0.944	...	1
In5	-1	-0.944	...	1
In6	-1	-0.944	...	1
In7	-1	-0.944	...	1
In8	-1	-0.973	...	1
Parameters				
In1	+			
In2	+			
In3	+			
In4	-			
In5	-			
In6	-			
In7	0			
In8	+			
Outputs				
Out	-1	-0.973	...	1
Exp. Out	-1	-0.973	...	1
Out (DSP)	-1	-0.973	...	1
Exp. Out (DSP)	-1	-0.973	...	1

Test settings	
Tolerance Out	±1,8626e-07 (±400 LSB)

Test statistics	
Min CPU cycles	235
Max CPU cycles	235
Avg CPU cycles	235

Test case: Conversion test OK

Conversion test for Math block Sum.

Test results			
Time step	1	2	3
Mask parameters			
In1	+	-	0
In2	+	-	0
In3	+	-	0
In4	+	-	0
In5	+	-	0
In6	+	-	0
In7	+	-	0
In8	+	-	0
Controller parameters			
sign	21845	43690	0
Exp. sign	21845	43690	0

Test settings	
Tolerance sign	±0,0000e+00

Test case: Conversion-on-Target test OK

Conversion-on-Target test for Math block Sum.

Test results			
Time step	1	2	3
Mask parameters			
In1	+	-	0
In2	+	-	0
In3	+	-	0
In4	+	-	0
In5	+	-	0
In6	+	-	0
In7	+	-	0
In8	+	-	0
Controller parameters			
sign	21845	43690	0
Exp. sign	21845	43690	0

Test settings	
Tolerance sign	±0,0000e+00

Test statistics	
Min CPU cycles	510
Max CPU cycles	512
Avg CPU cycles	510

Verification: Sum Float32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for Math block Sum.

Test results				
Time step	1	2	...	74
CPU cycles	835	908	...	834
Inputs				
In1 (DSP)	-1	-0.944	...	1
In2 (DSP)	-1	-0.944	...	1
In3 (DSP)	-1	-0.944	...	1
In4 (DSP)	-1	-0.944	...	1
In5 (DSP)	-1	-0.944	...	1
In6 (DSP)	-1	-0.944	...	1
In7 (DSP)	-1	-0.944	...	1
In8 (DSP)	-1	-0.973	...	1
In1	-1	-0.944	...	1
In2	-1	-0.944	...	1
In3	-1	-0.944	...	1
In4	-1	-0.944	...	1
In5	-1	-0.944	...	1
In6	-1	-0.944	...	1
In7	-1	-0.944	...	1
In8	-1	-0.973	...	1
Parameters				
In1	+			
In2	+			
In3	+			
In4	-			
In5	-			
In6	-			
In7	0			
In8	+			
Outputs				
Out	-1	-0.973	...	1
Exp. Out	-1	-0.973	...	1
Out (DSP)	-1	-0.973	...	1
Exp. Out (DSP)	-1	-0.973	...	1

Test settings	
Tolerance Out	±1,8626e-07 (±400 LSB)

Test statistics	
Min CPU cycles	741
Max CPU cycles	1025
Avg CPU cycles	958

Test case: Conversion test OK

Conversion test for Math block Sum.

Test results			
Time step	1	2	3
Mask parameters			
In1	+	-	0
In2	+	-	0
In3	+	-	0
In4	+	-	0
In5	+	-	0
In6	+	-	0
In7	+	-	0
In8	+	-	0
Controller parameters			
sign	21845	43690	0
Exp. sign	21845	43690	0

Test settings	
Tolerance sign	±0,0000e+00

Test case: Conversion-on-Target test OK

Conversion-on-Target test for Math block Sum.

Test results			
Time step	1	2	3
Mask parameters			
In1	+	-	0
In2	+	-	0
In3	+	-	0
In4	+	-	0
In5	+	-	0
In6	+	-	0
In7	+	-	0
In8	+	-	0
Controller parameters			
sign	21845	43690	0
Exp. sign	21845	43690	0

Test settings	
Tolerance sign	±0,0000e+00

Test statistics	
Min CPU cycles	603
Max CPU cycles	614
Avg CPU cycles	610

Verification: Sum Float32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test — OK

Inport test for Math block Sum.

Test results				
Time step	1	2	...	74
CPU cycles	419	427	...	419
Inputs				
In1 (DSP)	-1	-0.944	...	1
In2 (DSP)	-1	-0.944	...	1
In3 (DSP)	-1	-0.944	...	1
In4 (DSP)	-1	-0.944	...	1
In5 (DSP)	-1	-0.944	...	1
In6 (DSP)	-1	-0.944	...	1
In7 (DSP)	-1	-0.944	...	1
In8 (DSP)	-1	-0.973	...	1
In1	-1	-0.944	...	1
In2	-1	-0.944	...	1
In3	-1	-0.944	...	1
In4	-1	-0.944	...	1
In5	-1	-0.944	...	1
In6	-1	-0.944	...	1
In7	-1	-0.944	...	1
In8	-1	-0.973	...	1
Parameters				
In1	+			
In2	+			
In3	+			
In4	-			
In5	-			
In6	-			
In7	0			
In8	+			
Outputs				
Out	-1	-0.973	...	1
Exp. Out	-1	-0.973	...	1
Out (DSP)	-1	-0.973	...	1
Exp. Out (DSP)	-1	-0.973	...	1

Test settings	
Tolerance Out	±1,8626e-07 (±400 LSB)

Test statistics	
Min CPU cycles	317
Max CPU cycles	473
Avg CPU cycles	450

Test case: Conversion test OK

Conversion test for Math block Sum.

Test results			
Time step	1	2	3
Mask parameters			
In1	+	-	0
In2	+	-	0
In3	+	-	0
In4	+	-	0
In5	+	-	0
In6	+	-	0
In7	+	-	0
In8	+	-	0
Controller parameters			
sign	21845	43690	0
Exp. sign	21845	43690	0

Test settings	
Tolerance sign	±0,0000e+00

Test case: Conversion-on-Target test OK

Conversion-on-Target test for Math block Sum.

Test results			
Time step	1	2	3
Mask parameters			
In1	+	-	0
In2	+	-	0
In3	+	-	0
In4	+	-	0
In5	+	-	0
In6	+	-	0
In7	+	-	0
In8	+	-	0
Controller parameters			
sign	21845	43690	0
Exp. sign	21845	43690	0

Test settings	
Tolerance sign	±0,0000e+00

Test statistics	
Min CPU cycles	280
Max CPU cycles	301
Avg CPU cycles	293

Verification: Sum Float32 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for Math block Sum.

Test results				
Time step	1	2	...	74
CPU cycles	1160	1176	...	1156
Inputs				
In1 (DSP)	-1	-0.944	...	1
In2 (DSP)	-1	-0.944	...	1
In3 (DSP)	-1	-0.944	...	1
In4 (DSP)	-1	-0.944	...	1
In5 (DSP)	-1	-0.944	...	1
In6 (DSP)	-1	-0.944	...	1
In7 (DSP)	-1	-0.944	...	1
In8 (DSP)	-1	-0.973	...	1
In1	-1	-0.944	...	1
In2	-1	-0.944	...	1
In3	-1	-0.944	...	1
In4	-1	-0.944	...	1
In5	-1	-0.944	...	1
In6	-1	-0.944	...	1
In7	-1	-0.944	...	1
In8	-1	-0.973	...	1
Parameters				
In1	+			
In2	+			
In3	+			
In4	-			
In5	-			
In6	-			
In7	0			
In8	+			
Outputs				
Out	-1	-0.973	...	1
Exp. Out	-1	-0.973	...	1
Out (DSP)	-1	-0.973	...	1
Exp. Out (DSP)	-1	-0.973	...	1

Test settings	
Tolerance Out	±1,8626e-07 (±400 LSB)

Test statistics	
Min CPU cycles	1149
Max CPU cycles	1746
Avg CPU cycles	1536

Test case: Conversion test OK

Conversion test for Math block Sum.

Test results			
Time step	1	2	3
Mask parameters			
In1	+	-	0
In2	+	-	0
In3	+	-	0
In4	+	-	0
In5	+	-	0
In6	+	-	0
In7	+	-	0
In8	+	-	0
Controller parameters			
sign	21845	43690	0
Exp. sign	21845	43690	0

Test settings	
Tolerance sign	±0,0000e+00

Test case: Conversion-on-Target test OK

Conversion-on-Target test for Math block Sum.

Test results			
Time step	1	2	3
Mask parameters			
In1	+	-	0
In2	+	-	0
In3	+	-	0
In4	+	-	0
In5	+	-	0
In6	+	-	0
In7	+	-	0
In8	+	-	0
Controller parameters			
sign	21845	43690	0
Exp. sign	21845	43690	0

Test settings	
Tolerance sign	±0,0000e+00

Test statistics	
Min CPU cycles	303
Max CPU cycles	335
Avg CPU cycles	323

Verification: Sum Float32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test — OK

Inport test for Math block Sum.

Test results				
Time step	1	2	...	74
CPU cycles	234	152	...	152
Inputs				
In1 (DSP)	-1	-0.944	...	1
In2 (DSP)	-1	-0.944	...	1
In3 (DSP)	-1	-0.944	...	1
In4 (DSP)	-1	-0.944	...	1
In5 (DSP)	-1	-0.944	...	1
In6 (DSP)	-1	-0.944	...	1
In7 (DSP)	-1	-0.944	...	1
In8 (DSP)	-1	-0.973	...	1
In1	-1	-0.944	...	1
In2	-1	-0.944	...	1
In3	-1	-0.944	...	1
In4	-1	-0.944	...	1
In5	-1	-0.944	...	1
In6	-1	-0.944	...	1
In7	-1	-0.944	...	1
In8	-1	-0.973	...	1
Parameters				
In1	+			
In2	+			
In3	+			
In4	-			
In5	-			
In6	-			
In7	0			
In8	+			
Outputs				
Out	-1	-0.973	...	1
Exp. Out	-1	-0.973	...	1
Out (DSP)	-1	-0.973	...	1
Exp. Out (DSP)	-1	-0.973	...	1

Test settings	
Tolerance Out	±1,8626e-07 (±400 LSB)

Test statistics	
Min CPU cycles	152
Max CPU cycles	234
Avg CPU cycles	153

Test case: Conversion test OK

Conversion test for Math block Sum.

Test results			
Time step	1	2	3
Mask parameters			
In1	+	-	0
In2	+	-	0
In3	+	-	0
In4	+	-	0
In5	+	-	0
In6	+	-	0
In7	+	-	0
In8	+	-	0
Controller parameters			
sign	21845	43690	0
Exp. sign	21845	43690	0

Test settings	
Tolerance sign	±0,0000e+00

Test case: Conversion-on-Target test OK

Conversion-on-Target test for Math block Sum.

Test results			
Time step	1	2	3
Mask parameters			
In1	+	-	0
In2	+	-	0
In3	+	-	0
In4	+	-	0
In5	+	-	0
In6	+	-	0
In7	+	-	0
In8	+	-	0
Controller parameters			
sign	21845	43690	0
Exp. sign	21845	43690	0

Test settings	
Tolerance sign	±0,0000e+00

Test statistics	
Min CPU cycles	336
Max CPU cycles	424
Avg CPU cycles	374

Verification: Sum Float32 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test — OK

Inport test for Math block Sum.

Test results				
Time step	1	2	...	74
CPU cycles	232	232	...	232
Inputs				
In1 (DSP)	-1	-0.944	...	1
In2 (DSP)	-1	-0.944	...	1
In3 (DSP)	-1	-0.944	...	1
In4 (DSP)	-1	-0.944	...	1
In5 (DSP)	-1	-0.944	...	1
In6 (DSP)	-1	-0.944	...	1
In7 (DSP)	-1	-0.944	...	1
In8 (DSP)	-1	-0.973	...	1
In1	-1	-0.944	...	1
In2	-1	-0.944	...	1
In3	-1	-0.944	...	1
In4	-1	-0.944	...	1
In5	-1	-0.944	...	1
In6	-1	-0.944	...	1
In7	-1	-0.944	...	1
In8	-1	-0.973	...	1
Parameters				
In1	+			
In2	+			
In3	+			
In4	-			
In5	-			
In6	-			
In7	0			
In8	+			
Outputs				
Out	-1	-0.973	...	1
Exp. Out	-1	-0.973	...	1
Out (DSP)	-1	-0.973	...	1
Exp. Out (DSP)	-1	-0.973	...	1

Test settings	
Tolerance Out	±1,8626e-07 (±400 LSB)

Test statistics	
Min CPU cycles	232
Max CPU cycles	232
Avg CPU cycles	232

Test case: Conversion test OK

Conversion test for Math block Sum.

Test results			
Time step	1	2	3
Mask parameters			
In1	+	-	0
In2	+	-	0
In3	+	-	0
In4	+	-	0
In5	+	-	0
In6	+	-	0
In7	+	-	0
In8	+	-	0
Controller parameters			
sign	21845	43690	0
Exp. sign	21845	43690	0

Test settings	
Tolerance sign	±0,0000e+00

Test case: Conversion-on-Target test OK

Conversion-on-Target test for Math block Sum.

Test results			
Time step	1	2	3
Mask parameters			
In1	+	-	0
In2	+	-	0
In3	+	-	0
In4	+	-	0
In5	+	-	0
In6	+	-	0
In7	+	-	0
In8	+	-	0
Controller parameters			
sign	21845	43690	0
Exp. sign	21845	43690	0

Test settings	
Tolerance sign	±0,0000e+00

Test statistics	
Min CPU cycles	574
Max CPU cycles	622
Avg CPU cycles	599

Block: uAdd



Addition of input 1 and input 2 with output wrapping.

Inports	
In1	Addend 1
In2	Addend 2

Outports	
Out	Sum

Description:

Calculation:

$$\mathrm{Out} = \mathrm{In}_1 + \mathrm{In}_2$$

Implementations:

FiP8	8 Bit Fixed Point Implementation
FiP16	16 Bit Fixed Point Implementation
FiP32	32 Bit Fixed Point Implementation
Float32	32 Bit Floating Point Implementation
Float64	64 Bit Floating Point Implementation

Implementation: FiP8

8 Bit Fixed Point Implementation

Inports Data Type	
In1	int8
In2	int8

Outports Data Type	
Out	int8

Implementation: FiP16

16 Bit Fixed Point Implementation

Inports Data Type	
In1	int16
In2	int16

Outports Data Type	
Out	int16

Implementation: FiP32

32 Bit Fixed Point Implementation

Inports Data Type	
In1	int32
In2	int32

Outports Data Type	
Out	int32

Implementation: Float32

32 Bit Floating Point Implementation

Inports Data Type	
In1	float32
In2	float32

Outports Data Type	
Out	float32

Implementation: Float64

64 Bit Floating Point Implementation

Inports Data Type	
In1	float64
In2	float64

Outports Data Type	
Out	float64

Verification: uAdd FiP16 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for Math block uAdd.

Test results						
Time step	1	2	3	4	...	214
CPU cycles	51	51	51	51	...	51
Inputs						
In1 (DSP)	-32768	-32150	-31531	-30913	...	32767
In2 (DSP)	32767	32150	31531	30913	...	32767
In1	-1	-0.981	-0.962	-0.943	...	1
In2	1	0.981	0.962	0.943	...	1
Outputs						
Out	-0	0	0	0	...	-0
Exp. Out	0	0	0	0	...	0
Out (DSP)	-1	0	0	0	...	-2
Exp. Out (DSP)	0	0	0	0	...	0

Test settings	
Tolerance Out	±6,1035e-05 (±2 LSB)

Test statistics	
Min CPU cycles	51
Max CPU cycles	51
Avg CPU cycles	51

Verification: uAdd FiP16 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for Math block uAdd.

Test results						
Time step	1	2	3	4	...	214
CPU cycles	25	25	25	25	...	25
Inputs						
In1 (DSP)	-32768	-32150	-31531	-30913	...	32767
In2 (DSP)	32767	32150	31531	30913	...	32767
In1	-1	-0.981	-0.962	-0.943	...	1
In2	1	0.981	0.962	0.943	...	1
Outputs						
Out	-0	0	0	0	...	-0
Exp. Out	0	0	0	0	...	0
Out (DSP)	-1	0	0	0	...	-2
Exp. Out (DSP)	0	0	0	0	...	0

Test settings	
Tolerance Out	±6,1035e-05 (±2 LSB)

Test statistics	
Min CPU cycles	25
Max CPU cycles	25
Avg CPU cycles	25

Verification: uAdd FiP16 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test **OK**

Inport test for Math block uAdd.

Test results						
Time step	1	2	3	4	...	214
CPU cycles	57	57	57	57	...	57
Inputs						
In1 (DSP)	-32768	-32150	-31531	-30913	...	32767
In2 (DSP)	32767	32150	31531	30913	...	32767
In1	-1	-0.981	-0.962	-0.943	...	1
In2	1	0.981	0.962	0.943	...	1
Outputs						
Out	-0	0	0	0	...	-0
Exp. Out	0	0	0	0	...	0
Out (DSP)	-1	0	0	0	...	-2
Exp. Out (DSP)	0	0	0	0	...	0

Test settings	
Tolerance Out	±6,1035e-05 (±2 LSB)

Test statistics	
Min CPU cycles	57
Max CPU cycles	57
Avg CPU cycles	57

Verification: uAdd FiP16 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test **OK**

Inport test for Math block uAdd.

Test results						
Time step	1	2	3	4	...	214
CPU cycles	51	51	51	51	...	51
Inputs						
In1 (DSP)	-32768	-32150	-31531	-30913	...	32767
In2 (DSP)	32767	32150	31531	30913	...	32767
In1	-1	-0.981	-0.962	-0.943	...	1
In2	1	0.981	0.962	0.943	...	1
Outputs						
Out	-0	0	0	0	...	-0
Exp. Out	0	0	0	0	...	0
Out (DSP)	-1	0	0	0	...	-2
Exp. Out (DSP)	0	0	0	0	...	0

Test settings	
Tolerance Out	±6,1035e-05 (±2 LSB)

Test statistics	
Min CPU cycles	51
Max CPU cycles	112
Avg CPU cycles	51

Verification: uAdd FiP16 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for Math block uAdd.

Test results						
Time step	1	2	3	4	...	214
CPU cycles	32	32	32	32	...	32
Inputs						
In1 (DSP)	-32768	-32150	-31531	-30913	...	32767
In2 (DSP)	32767	32150	31531	30913	...	32767
In1	-1	-0.981	-0.962	-0.943	...	1
In2	1	0.981	0.962	0.943	...	1
Outputs						
Out	-0	0	0	0	...	-0
Exp. Out	0	0	0	0	...	0
Out (DSP)	-1	0	0	0	...	-2
Exp. Out (DSP)	0	0	0	0	...	0

Test settings	
Tolerance Out	±6,1035e-05 (±2 LSB)

Test statistics	
Min CPU cycles	32
Max CPU cycles	32
Avg CPU cycles	32

Verification: uAdd FiP16 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for Math block uAdd.

Test results						
Time step	1	2	3	4	...	214
CPU cycles	38	38	38	38	...	38
Inputs						
In1 (DSP)	-32768	-32150	-31531	-30913	...	32767
In2 (DSP)	32767	32150	31531	30913	...	32767
In1	-1	-0.981	-0.962	-0.943	...	1
In2	1	0.981	0.962	0.943	...	1
Outputs						
Out	-0	0	0	0	...	-0
Exp. Out	0	0	0	0	...	0
Out (DSP)	-1	0	0	0	...	-2
Exp. Out (DSP)	0	0	0	0	...	0

Test settings	
Tolerance Out	±6,1035e-05 (±2 LSB)

Test statistics	
Min CPU cycles	38
Max CPU cycles	38
Avg CPU cycles	38

Verification: uAdd FiP16 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for Math block uAdd.

Test results						
Time step	1	2	3	4	...	214
CPU cycles	56	56	56	56	...	56
Inputs						
In1 (DSP)	-32768	-32150	-31531	-30913	...	32767
In2 (DSP)	32767	32150	31531	30913	...	32767
In1	-1	-0.981	-0.962	-0.943	...	1
In2	1	0.981	0.962	0.943	...	1
Outputs						
Out	-0	0	0	0	...	-0
Exp. Out	0	0	0	0	...	0
Out (DSP)	-1	0	0	0	...	-2
Exp. Out (DSP)	0	0	0	0	...	0

Test settings	
Tolerance Out	±6,1035e-05 (±2 LSB)

Test statistics	
Min CPU cycles	56
Max CPU cycles	56
Avg CPU cycles	56

Verification: uAdd FiP16 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for Math block uAdd.

Test results						
Time step	1	2	3	4	...	214
CPU cycles	46	46	46	46	...	46
Inputs						
In1 (DSP)	-32768	-32150	-31531	-30913	...	32767
In2 (DSP)	32767	32150	31531	30913	...	32767
In1	-1	-0.981	-0.962	-0.943	...	1
In2	1	0.981	0.962	0.943	...	1
Outputs						
Out	-0	0	0	0	...	-0
Exp. Out	0	0	0	0	...	0
Out (DSP)	-1	0	0	0	...	-2
Exp. Out (DSP)	0	0	0	0	...	0

Test settings	
Tolerance Out	±6,1035e-05 (±2 LSB)

Test statistics	
Min CPU cycles	46
Max CPU cycles	46
Avg CPU cycles	46

Verification: uAdd FiP32 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for Math block uAdd.

Test results				
Time step	1	2	...	214
CPU cycles	51	51	...	51
Inputs				
In1 (DSP)	-2147483648	-2106965089	...	2147483647
In2 (DSP)	2147483647	2106965089	...	2147483647
In1	-1	-0.981	...	1
In2	1	0.981	...	1
Outputs				
Out	-0	0	...	-0
Exp. Out	0	0	...	0
Out (DSP)	-1	0	...	-2
Exp. Out (DSP)	0	0	...	0

Test settings	
Tolerance Out	±9,3132e-10 (±2 LSB)

Test statistics	
Min CPU cycles	51
Max CPU cycles	51
Avg CPU cycles	51

Verification: uAdd FiP32 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for Math block uAdd.

Test results				
Time step	1	2	...	214
CPU cycles	27	27	...	27
Inputs				
In1 (DSP)	-2147483648	-2106965089	...	2147483647
In2 (DSP)	2147483647	2106965089	...	2147483647
In1	-1	-0.981	...	1
In2	1	0.981	...	1
Outputs				
Out	-0	0	...	-0
Exp. Out	0	0	...	0
Out (DSP)	-1	0	...	-2
Exp. Out (DSP)	0	0	...	0

Test settings	
Tolerance Out	±9,3132e-10 (±2 LSB)

Test statistics	
Min CPU cycles	27
Max CPU cycles	27
Avg CPU cycles	27

Verification: uAdd FiP32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for Math block uAdd.

Test results				
Time step	1	2	...	214
CPU cycles	57	57	...	57
Inputs				
In1 (DSP)	-2147483648	-2106965089	...	2147483647
In2 (DSP)	2147483647	2106965089	...	2147483647
In1	-1	-0.981	...	1
In2	1	0.981	...	1
Outputs				
Out	-0	0	...	-0
Exp. Out	0	0	...	0
Out (DSP)	-1	0	...	-2
Exp. Out (DSP)	0	0	...	0

Test settings	
Tolerance Out	±9,3132e-10 (±2 LSB)

Test statistics	
Min CPU cycles	57
Max CPU cycles	57
Avg CPU cycles	57

Verification: uAdd FiP32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for Math block uAdd.

Test results				
Time step	1	2	...	214
CPU cycles	51	51	...	51
Inputs				
In1 (DSP)	-2147483648	-2106965089	...	2147483647
In2 (DSP)	2147483647	2106965089	...	2147483647
In1	-1	-0.981	...	1
In2	1	0.981	...	1
Outputs				
Out	-0	0	...	-0
Exp. Out	0	0	...	0
Out (DSP)	-1	0	...	-2
Exp. Out (DSP)	0	0	...	0

Test settings	
Tolerance Out	±9,3132e-10 (±2 LSB)

Test statistics	
Min CPU cycles	51
Max CPU cycles	110
Avg CPU cycles	51

Verification: uAdd FiP32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for Math block uAdd.

Test results				
Time step	1	2	...	214
CPU cycles	32	32	...	32
Inputs				
In1 (DSP)	-2147483648	-2106965089	...	2147483647
In2 (DSP)	2147483647	2106965089	...	2147483647
In1	-1	-0.981	...	1
In2	1	0.981	...	1
Outputs				
Out	-0	0	...	-0
Exp. Out	0	0	...	0
Out (DSP)	-1	0	...	-2
Exp. Out (DSP)	0	0	...	0

Test settings	
Tolerance Out	±9,3132e-10 (±2 LSB)

Test statistics	
Min CPU cycles	32
Max CPU cycles	32
Avg CPU cycles	32

Verification: uAdd FiP32 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for Math block uAdd.

Test results				
Time step	1	2	...	214
CPU cycles	42	42	...	42
Inputs				
In1 (DSP)	-2147483648	-2106965089	...	2147483647
In2 (DSP)	2147483647	2106965089	...	2147483647
In1	-1	-0.981	...	1
In2	1	0.981	...	1
Outputs				
Out	-0	0	...	-0
Exp. Out	0	0	...	0
Out (DSP)	-1	0	...	-2
Exp. Out (DSP)	0	0	...	0

Test settings	
Tolerance Out	±9,3132e-10 (±2 LSB)

Test statistics	
Min CPU cycles	42
Max CPU cycles	42
Avg CPU cycles	42

Verification: uAdd FiP32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for Math block uAdd.

Test results				
Time step	1	2	...	214
CPU cycles	56	56	...	56
Inputs				
In1 (DSP)	-2147483648	-2106965089	...	2147483647
In2 (DSP)	2147483647	2106965089	...	2147483647
In1	-1	-0.981	...	1
In2	1	0.981	...	1
Outputs				
Out	-0	0	...	-0
Exp. Out	0	0	...	0
Out (DSP)	-1	0	...	-2
Exp. Out (DSP)	0	0	...	0

Test settings	
Tolerance Out	±9,3132e-10 (±2 LSB)

Test statistics	
Min CPU cycles	56
Max CPU cycles	56
Avg CPU cycles	56

Verification: uAdd FiP32 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for Math block uAdd.

Test results				
Time step	1	2	...	214
CPU cycles	44	44	...	44
Inputs				
In1 (DSP)	-2147483648	-2106965089	...	2147483647
In2 (DSP)	2147483647	2106965089	...	2147483647
In1	-1	-0.981	...	1
In2	1	0.981	...	1
Outputs				
Out	-0	0	...	-0
Exp. Out	0	0	...	0
Out (DSP)	-1	0	...	-2
Exp. Out (DSP)	0	0	...	0

Test settings	
Tolerance Out	±9,3132e-10 (±2 LSB)

Test statistics	
Min CPU cycles	44
Max CPU cycles	44
Avg CPU cycles	44

Verification: uAdd Float32 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for Math block uAdd.

Test results				
Time step	1	2	...	214
CPU cycles	79	79	...	176
Inputs				
In1 (DSP)	-2	-1.962	...	2
In2 (DSP)	2	1.962	...	2
In1	-2	-1.962	...	2
In2	2	1.962	...	2
Outputs				
Out	0	0	...	-2.283
Exp. Out	0	0	...	-2.283
Out (DSP)	0	0	...	-2.283
Exp. Out (DSP)	0	0	...	-2.283

Test settings	
Tolerance Out	±5,5879e-07 (±1200 LSB)

Test statistics	
Min CPU cycles	79
Max CPU cycles	182
Avg CPU cycles	90

Verification: uAdd Float32 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for Math block uAdd.

Test results				
Time step	1	2	...	214
CPU cycles	67	67	...	107
Inputs				
In1 (DSP)	-2	-1.962	...	2
In2 (DSP)	2	1.962	...	2
In1	-2	-1.962	...	2
In2	2	1.962	...	2
Outputs				
Out	0	0	...	-2.283
Exp. Out	0	0	...	-2.283
Out (DSP)	0	0	...	-2.283
Exp. Out (DSP)	0	0	...	-2.283

Test settings	
Tolerance Out	±5,5879e-07 (±1200 LSB)

Test statistics	
Min CPU cycles	67
Max CPU cycles	123
Avg CPU cycles	72

Verification: uAdd Float32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for Math block uAdd.

Test results				
Time step	1	2	...	214
CPU cycles	104	104	...	240
Inputs				
In1 (DSP)	-2	-1.962	...	2
In2 (DSP)	2	1.962	...	2
In1	-2	-1.962	...	2
In2	2	1.962	...	2
Outputs				
Out	0	0	...	-2.283
Exp. Out	0	0	...	-2.283
Out (DSP)	0	0	...	-2.283
Exp. Out (DSP)	0	0	...	-2.283

Test settings	
Tolerance Out	±5,5879e-07 (±1200 LSB)

Test statistics	
Min CPU cycles	104
Max CPU cycles	240
Avg CPU cycles	119

Verification: uAdd Float32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for Math block uAdd.

Test results				
Time step	1	2	...	214
CPU cycles	299	299	...	673
Inputs				
In1 (DSP)	-2	-1.962	...	2
In2 (DSP)	2	1.962	...	2
In1	-2	-1.962	...	2
In2	2	1.962	...	2
Outputs				
Out	0	0	...	-2.283
Exp. Out	0	0	...	-2.283
Out (DSP)	0	0	...	-2.283
Exp. Out (DSP)	0	0	...	-2.283

Test settings	
Tolerance Out	±5,5879e-07 (±1200 LSB)

Test statistics	
Min CPU cycles	299
Max CPU cycles	764
Avg CPU cycles	355

Verification: uAdd Float32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for Math block uAdd.

Test results				
Time step	1	2	...	214
CPU cycles	176	176	...	312
Inputs				
In1 (DSP)	-2	-1.962	...	2
In2 (DSP)	2	1.962	...	2
In1	-2	-1.962	...	2
In2	2	1.962	...	2
Outputs				
Out	0	0	...	-2.283
Exp. Out	0	0	...	-2.283
Out (DSP)	0	0	...	-2.283
Exp. Out (DSP)	0	0	...	-2.283

Test settings	
Tolerance Out	±5,5879e-07 (±1200 LSB)

Test statistics	
Min CPU cycles	162
Max CPU cycles	346
Avg CPU cycles	197

Verification: uAdd Float32 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for Math block uAdd.

Test results				
Time step	1	2	...	214
CPU cycles	452	452	...	773
Inputs				
In1 (DSP)	-2	-1.962	...	2
In2 (DSP)	2	1.962	...	2
In1	-2	-1.962	...	2
In2	2	1.962	...	2
Outputs				
Out	0	0	...	-2.283
Exp. Out	0	0	...	-2.283
Out (DSP)	0	0	...	-2.283
Exp. Out (DSP)	0	0	...	-2.283

Test settings	
Tolerance Out	±5,5879e-07 (±1200 LSB)

Test statistics	
Min CPU cycles	411
Max CPU cycles	870
Avg CPU cycles	472

Verification: uAdd Float32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for Math block uAdd.

Test results				
Time step	1	2	...	214
CPU cycles	121	91	...	266
Inputs				
In1 (DSP)	-2	-1.962	...	2
In2 (DSP)	2	1.962	...	2
In1	-2	-1.962	...	2
In2	2	1.962	...	2
Outputs				
Out	0	0	...	-2.283
Exp. Out	0	0	...	-2.283
Out (DSP)	0	0	...	-2.283
Exp. Out (DSP)	0	0	...	-2.283

Test settings	
Tolerance Out	±5,5879e-07 (±1200 LSB)

Test statistics	
Min CPU cycles	91
Max CPU cycles	298
Avg CPU cycles	111

Verification: uAdd Float32 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for Math block uAdd.

Test results				
Time step	1	2	...	214
CPU cycles	81	81	...	153
Inputs				
In1 (DSP)	-2	-1.962	...	2
In2 (DSP)	2	1.962	...	2
In1	-2	-1.962	...	2
In2	2	1.962	...	2
Outputs				
Out	0	0	...	-2.283
Exp. Out	0	0	...	-2.283
Out (DSP)	0	0	...	-2.283
Exp. Out (DSP)	0	0	...	-2.283

Test settings	
Tolerance Out	±5,5879e-07 (±1200 LSB)

Test statistics	
Min CPU cycles	81
Max CPU cycles	164
Avg CPU cycles	89

Block: uSub



Subtraction of input Minus from input Plus with output wrapping.

Inports	
Plus	Minuend
Minus	Subtrahend

Outports	
Out	Difference

Description:

Calculation:

$$\mathrm{Out} = \mathrm{Plus} - \mathrm{Minus}$$

Implementations:

FiP8	8 Bit Fixed Point Implementation
FiP16	16 Bit Fixed Point Implementation
FiP32	32 Bit Fixed Point Implementation
Float32	32 Bit Floating Point Implementation
Float64	64 Bit Floating Point Implementation

Implementation: FiP8

8 Bit Fixed Point Implementation

Inports Data Type	
Plus	int8
Minus	int8

Outports Data Type	
Out	int8

Implementation: FiP16

16 Bit Fixed Point Implementation

Inports Data Type	
Plus	int16
Minus	int16

Outports Data Type	
Out	int16

Implementation: FiP32

32 Bit Fixed Point Implementation

Inports Data Type	
Plus	int32
Minus	int32

Outports Data Type	
Out	int32

Implementation: Float32

32 Bit Floating Point Implementation

Inports Data Type	
Plus	float32
Minus	float32

Outports Data Type	
Out	float32

Implementation: Float64

64 Bit Floating Point Implementation

Inports Data Type	
Plus	float64
Minus	float64

Outports Data Type	
Out	float64

Verification: uSub FiP16 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for Math block uSub.

Test results						
Time step	1	2	3	4	...	214
CPU cycles	51	51	51	51	...	51
Inputs						
Plus (DSP)	-32768	-32150	-31531	-30913	...	32767
Minus (DSP)	32767	32150	31531	30913	...	32767
Plus	-1	-0.981	-0.962	-0.943	...	1
Minus	1	0.981	0.962	0.943	...	1
Outputs						
Out	0	0.038	0.076	0.113	...	0
Exp. Out	0	0.038	0.075	0.113	...	0
Out (DSP)	1	1236	2474	3710	...	0
Exp. Out (DSP)	0	1237	2473	3710	...	0

Test settings	
Tolerance Out	±6,1035e-05 (±2 LSB)

Test statistics	
Min CPU cycles	51
Max CPU cycles	51
Avg CPU cycles	51

Verification: uSub FiP16 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for Math block uSub.

Test results						
Time step	1	2	3	4	...	214
CPU cycles	25	25	25	25	...	25
Inputs						
Plus (DSP)	-32768	-32150	-31531	-30913	...	32767
Minus (DSP)	32767	32150	31531	30913	...	32767
Plus	-1	-0.981	-0.962	-0.943	...	1
Minus	1	0.981	0.962	0.943	...	1
Outputs						
Out	0	0.038	0.076	0.113	...	0
Exp. Out	0	0.038	0.075	0.113	...	0
Out (DSP)	1	1236	2474	3710	...	0
Exp. Out (DSP)	0	1237	2473	3710	...	0

Test settings	
Tolerance Out	±6,1035e-05 (±2 LSB)

Test statistics	
Min CPU cycles	25
Max CPU cycles	25
Avg CPU cycles	25

Verification: uSub FiP16 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for Math block uSub.

Test results						
Time step	1	2	3	4	...	214
CPU cycles	57	57	57	57	...	57
Inputs						
Plus (DSP)	-32768	-32150	-31531	-30913	...	32767
Minus (DSP)	32767	32150	31531	30913	...	32767
Plus	-1	-0.981	-0.962	-0.943	...	1
Minus	1	0.981	0.962	0.943	...	1
Outputs						
Out	0	0.038	0.076	0.113	...	0
Exp. Out	0	0.038	0.075	0.113	...	0
Out (DSP)	1	1236	2474	3710	...	0
Exp. Out (DSP)	0	1237	2473	3710	...	0

Test settings	
Tolerance Out	±6,1035e-05 (±2 LSB)

Test statistics	
Min CPU cycles	57
Max CPU cycles	57
Avg CPU cycles	57

Verification: uSub FiP16 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for Math block uSub.

Test results						
Time step	1	2	3	4	...	214
CPU cycles	51	51	51	51	...	51
Inputs						
Plus (DSP)	-32768	-32150	-31531	-30913	...	32767
Minus (DSP)	32767	32150	31531	30913	...	32767
Plus	-1	-0.981	-0.962	-0.943	...	1
Minus	1	0.981	0.962	0.943	...	1
Outputs						
Out	0	0.038	0.076	0.113	...	0
Exp. Out	0	0.038	0.075	0.113	...	0
Out (DSP)	1	1236	2474	3710	...	0
Exp. Out (DSP)	0	1237	2473	3710	...	0

Test settings	
Tolerance Out	±6,1035e-05 (±2 LSB)

Test statistics	
Min CPU cycles	51
Max CPU cycles	51
Avg CPU cycles	51

Verification: uSub FiP16 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for Math block uSub.

Test results						
Time step	1	2	3	4	...	214
CPU cycles	32	32	32	32	...	32
Inputs						
Plus (DSP)	-32768	-32150	-31531	-30913	...	32767
Minus (DSP)	32767	32150	31531	30913	...	32767
Plus	-1	-0.981	-0.962	-0.943	...	1
Minus	1	0.981	0.962	0.943	...	1
Outputs						
Out	0	0.038	0.076	0.113	...	0
Exp. Out	0	0.038	0.075	0.113	...	0
Out (DSP)	1	1236	2474	3710	...	0
Exp. Out (DSP)	0	1237	2473	3710	...	0

Test settings	
Tolerance Out	±6,1035e-05 (±2 LSB)

Test statistics	
Min CPU cycles	32
Max CPU cycles	32
Avg CPU cycles	32

Verification: uSub FiP16 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test OK

Inport test for Math block uSub.

Test results						
Time step	1	2	3	4	...	214
CPU cycles	38	38	38	38	...	38
Inputs						
Plus (DSP)	-32768	-32150	-31531	-30913	...	32767
Minus (DSP)	32767	32150	31531	30913	...	32767
Plus	-1	-0.981	-0.962	-0.943	...	1
Minus	1	0.981	0.962	0.943	...	1
Outputs						
Out	0	0.038	0.076	0.113	...	0
Exp. Out	0	0.038	0.075	0.113	...	0
Out (DSP)	1	1236	2474	3710	...	0
Exp. Out (DSP)	0	1237	2473	3710	...	0

Test settings	
Tolerance Out	±6,1035e-05 (±2 LSB)

Test statistics	
Min CPU cycles	38
Max CPU cycles	38
Avg CPU cycles	38

Verification: uSub FiP16 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for Math block uSub.

Test results						
Time step	1	2	3	4	...	214
CPU cycles	67	56	56	56	...	56
Inputs						
Plus (DSP)	-32768	-32150	-31531	-30913	...	32767
Minus (DSP)	32767	32150	31531	30913	...	32767
Plus	-1	-0.981	-0.962	-0.943	...	1
Minus	1	0.981	0.962	0.943	...	1
Outputs						
Out	0	0.038	0.076	0.113	...	0
Exp. Out	0	0.038	0.075	0.113	...	0
Out (DSP)	1	1236	2474	3710	...	0
Exp. Out (DSP)	0	1237	2473	3710	...	0

Test settings	
Tolerance Out	±6,1035e-05 (±2 LSB)

Test statistics	
Min CPU cycles	56
Max CPU cycles	67
Avg CPU cycles	56

Verification: uSub FiP16 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for Math block uSub.

Test results						
Time step	1	2	3	4	...	214
CPU cycles	46	46	46	46	...	46
Inputs						
Plus (DSP)	-32768	-32150	-31531	-30913	...	32767
Minus (DSP)	32767	32150	31531	30913	...	32767
Plus	-1	-0.981	-0.962	-0.943	...	1
Minus	1	0.981	0.962	0.943	...	1
Outputs						
Out	0	0.038	0.076	0.113	...	0
Exp. Out	0	0.038	0.075	0.113	...	0
Out (DSP)	1	1236	2474	3710	...	0
Exp. Out (DSP)	0	1237	2473	3710	...	0

Test settings	
Tolerance Out	±6,1035e-05 (±2 LSB)

Test statistics	
Min CPU cycles	46
Max CPU cycles	46
Avg CPU cycles	46

Verification: uSub FiP32 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for Math block uSub.

Test results				
Time step	1	2	...	214
CPU cycles	51	51	...	51
Inputs				
Plus (DSP)	-2147483648	-2106965089	...	2147483647
Minus (DSP)	2147483647	2106965089	...	2147483647
Plus	-1	-0.981	...	1
Minus	1	0.981	...	1
Outputs				
Out	0	0.038	...	0
Exp. Out	0	0.038	...	0
Out (DSP)	1	81037118	...	0
Exp. Out (DSP)	0	81037119	...	0

Test settings	
Tolerance Out	±9,3132e-10 (±2 LSB)

Test statistics	
Min CPU cycles	51
Max CPU cycles	51
Avg CPU cycles	51

Verification: uSub FiP32 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for Math block uSub.

Test results				
Time step	1	2	...	214
CPU cycles	27	27	...	27
Inputs				
Plus (DSP)	-2147483648	-2106965089	...	2147483647
Minus (DSP)	2147483647	2106965089	...	2147483647
Plus	-1	-0.981	...	1
Minus	1	0.981	...	1
Outputs				
Out	0	0.038	...	0
Exp. Out	0	0.038	...	0
Out (DSP)	1	81037118	...	0
Exp. Out (DSP)	0	81037119	...	0

Test settings	
Tolerance Out	±9,3132e-10 (±2 LSB)

Test statistics	
Min CPU cycles	27
Max CPU cycles	27
Avg CPU cycles	27

Verification: uSub FiP32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for Math block uSub.

Test results				
Time step	1	2	...	214
CPU cycles	57	57	...	57
Inputs				
Plus (DSP)	-2147483648	-2106965089	...	2147483647
Minus (DSP)	2147483647	2106965089	...	2147483647
Plus	-1	-0.981	...	1
Minus	1	0.981	...	1
Outputs				
Out	0	0.038	...	0
Exp. Out	0	0.038	...	0
Out (DSP)	1	81037118	...	0
Exp. Out (DSP)	0	81037119	...	0

Test settings	
Tolerance Out	±9,3132e-10 (±2 LSB)

Test statistics	
Min CPU cycles	57
Max CPU cycles	57
Avg CPU cycles	57

Verification: uSub FiP32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for Math block uSub.

Test results				
Time step	1	2	...	214
CPU cycles	51	51	...	51
Inputs				
Plus (DSP)	-2147483648	-2106965089	...	2147483647
Minus (DSP)	2147483647	2106965089	...	2147483647
Plus	-1	-0.981	...	1
Minus	1	0.981	...	1
Outputs				
Out	0	0.038	...	0
Exp. Out	0	0.038	...	0
Out (DSP)	1	81037118	...	0
Exp. Out (DSP)	0	81037119	...	0

Test settings	
Tolerance Out	±9,3132e-10 (±2 LSB)

Test statistics	
Min CPU cycles	51
Max CPU cycles	51
Avg CPU cycles	51

Verification: uSub FiP32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for Math block uSub.

Test results				
Time step	1	2	...	214
CPU cycles	32	32	...	32
Inputs				
Plus (DSP)	-2147483648	-2106965089	...	2147483647
Minus (DSP)	2147483647	2106965089	...	2147483647
Plus	-1	-0.981	...	1
Minus	1	0.981	...	1
Outputs				
Out	0	0.038	...	0
Exp. Out	0	0.038	...	0
Out (DSP)	1	81037118	...	0
Exp. Out (DSP)	0	81037119	...	0

Test settings	
Tolerance Out	±9,3132e-10 (±2 LSB)

Test statistics	
Min CPU cycles	32
Max CPU cycles	32
Avg CPU cycles	32

Verification: uSub FiP32 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test — OK

Inport test for Math block uSub.

Test results				
Time step	1	2	...	214
CPU cycles	41	41	...	41
Inputs				
Plus (DSP)	-2147483648	-2106965089	...	2147483647
Minus (DSP)	2147483647	2106965089	...	2147483647
Plus	-1	-0.981	...	1
Minus	1	0.981	...	1
Outputs				
Out	0	0.038	...	0
Exp. Out	0	0.038	...	0
Out (DSP)	1	81037118	...	0
Exp. Out (DSP)	0	81037119	...	0

Test settings	
Tolerance Out	±9,3132e-10 (±2 LSB)

Test statistics	
Min CPU cycles	41
Max CPU cycles	41
Avg CPU cycles	41

Verification: uSub FiP32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for Math block uSub.

Test results				
Time step	1	2	...	214
CPU cycles	56	56	...	56
Inputs				
Plus (DSP)	-2147483648	-2106965089	...	2147483647
Minus (DSP)	2147483647	2106965089	...	2147483647
Plus	-1	-0.981	...	1
Minus	1	0.981	...	1
Outputs				
Out	0	0.038	...	0
Exp. Out	0	0.038	...	0
Out (DSP)	1	81037118	...	0
Exp. Out (DSP)	0	81037119	...	0

Test settings	
Tolerance Out	±9,3132e-10 (±2 LSB)

Test statistics	
Min CPU cycles	56
Max CPU cycles	56
Avg CPU cycles	56

Verification: uSub FiP32 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for Math block uSub.

Test results				
Time step	1	2	...	214
CPU cycles	44	44	...	44
Inputs				
Plus (DSP)	-2147483648	-2106965089	...	2147483647
Minus (DSP)	2147483647	2106965089	...	2147483647
Plus	-1	-0.981	...	1
Minus	1	0.981	...	1
Outputs				
Out	0	0.038	...	0
Exp. Out	0	0.038	...	0
Out (DSP)	1	81037118	...	0
Exp. Out (DSP)	0	81037119	...	0

Test settings	
Tolerance Out	±9,3132e-10 (±2 LSB)

Test statistics	
Min CPU cycles	44
Max CPU cycles	44
Avg CPU cycles	44

Verification: uSub Float32 CPU TMS320F28335

Date of Test	2026-06-19
Target controller	TMS320F28335

Test case: Inport test OK

Inport test for Math block uSub.

Test results				
Time step	1	2	...	214
CPU cycles	182	182	...	79
Inputs				
Plus (DSP)	-2	-1.962	...	2
Minus (DSP)	2	1.962	...	2
Plus	-2	-1.962	...	2
Minus	2	1.962	...	2
Outputs				
Out	2.283	2.359	...	0
Exp. Out	2.283	2.359	...	0
Out (DSP)	2.283	2.359	...	0
Exp. Out (DSP)	2.283	2.359	...	0

Test settings	
Tolerance Out	±2,7940e-07 (±600 LSB)

Test statistics	
Min CPU cycles	79
Max CPU cycles	182
Avg CPU cycles	90

Verification: uSub Float32 CPU TM4C123GH6

Date of Test	2026-06-19
Target controller	TM4C123GH6

Test case: Inport test OK

Inport test for Math block uSub.

Test results				
Time step	1	2	...	214
CPU cycles	123	123	...	67
Inputs				
Plus (DSP)	-2	-1.962	...	2
Minus (DSP)	2	1.962	...	2
Plus	-2	-1.962	...	2
Minus	2	1.962	...	2
Outputs				
Out	2.283	2.359	...	0
Exp. Out	2.283	2.359	...	0
Out (DSP)	2.283	2.359	...	0
Exp. Out (DSP)	2.283	2.359	...	0

Test settings	
Tolerance Out	±2,7940e-07 (±600 LSB)

Test statistics	
Min CPU cycles	67
Max CPU cycles	123
Avg CPU cycles	72

Verification: uSub Float32 CPU STM32G474RE

Date of Test	2026-06-19
Target controller	STM32G474RE

Test case: Inport test OK

Inport test for Math block uSub.

Test results				
Time step	1	2	...	214
CPU cycles	237	237	...	104
Inputs				
Plus (DSP)	-2	-1.962	...	2
Minus (DSP)	2	1.962	...	2
Plus	-2	-1.962	...	2
Minus	2	1.962	...	2
Outputs				
Out	2.283	2.359	...	0
Exp. Out	2.283	2.359	...	0
Out (DSP)	2.283	2.359	...	0
Exp. Out (DSP)	2.283	2.359	...	0

Test settings	
Tolerance Out	±2,7940e-07 (±600 LSB)

Test statistics	
Min CPU cycles	104
Max CPU cycles	240
Avg CPU cycles	119

Verification: uSub Float32 CPU STM32F072RB

Date of Test	2026-06-19
Target controller	STM32F072RB

Test case: Inport test OK

Inport test for Math block uSub.

Test results				
Time step	1	2	...	214
CPU cycles	751	775	...	307
Inputs				
Plus (DSP)	-2	-1.962	...	2
Minus (DSP)	2	1.962	...	2
Plus	-2	-1.962	...	2
Minus	2	1.962	...	2
Outputs				
Out	2.283	2.359	...	0
Exp. Out	2.283	2.359	...	0
Out (DSP)	2.283	2.359	...	0
Exp. Out (DSP)	2.283	2.359	...	0

Test settings	
Tolerance Out	±2,7940e-07 (±600 LSB)

Test statistics	
Min CPU cycles	307
Max CPU cycles	775
Avg CPU cycles	365

Verification: uSub Float32 CPU PIC32MX170F256

Date of Test	2026-06-19
Target controller	PIC32MX170F256

Test case: Inport test OK

Inport test for Math block uSub.

Test results				
Time step	1	2	...	214
CPU cycles	348	328	...	178
Inputs				
Plus (DSP)	-2	-1.962	...	2
Minus (DSP)	2	1.962	...	2
Plus	-2	-1.962	...	2
Minus	2	1.962	...	2
Outputs				
Out	2.283	2.359	...	0
Exp. Out	2.283	2.359	...	0
Out (DSP)	2.283	2.359	...	0
Exp. Out (DSP)	2.283	2.359	...	0

Test settings	
Tolerance Out	±2,7940e-07 (±600 LSB)

Test statistics	
Min CPU cycles	170
Max CPU cycles	348
Avg CPU cycles	199

Verification: uSub Float32 CPU dsPIC33EP256MC502

Date of Test	2026-06-19
Target controller	dsPIC33EP256MC502

Test case: Inport test — OK

Inport test for Math block uSub.

Test results				
Time step	1	2	...	214
CPU cycles	871	818	...	453
Inputs				
Plus (DSP)	-2	-1.962	...	2
Minus (DSP)	2	1.962	...	2
Plus	-2	-1.962	...	2
Minus	2	1.962	...	2
Outputs				
Out	2.283	2.359	...	0
Exp. Out	2.283	2.359	...	0
Out (DSP)	2.283	2.359	...	0
Exp. Out (DSP)	2.283	2.359	...	0

Test settings	
Tolerance Out	±2,7940e-07 (±600 LSB)

Test statistics	
Min CPU cycles	412
Max CPU cycles	871
Avg CPU cycles	473

Verification: uSub Float32 CPU XMC4800-F144K2048

Date of Test	2026-06-19
Target controller	XMC4800-F144K2048

Test case: Inport test OK

Inport test for Math block uSub.

Test results				
Time step	1	2	...	214
CPU cycles	315	268	...	91
Inputs				
Plus (DSP)	-2	-1.962	...	2
Minus (DSP)	2	1.962	...	2
Plus	-2	-1.962	...	2
Minus	2	1.962	...	2
Outputs				
Out	2.283	2.359	...	0
Exp. Out	2.283	2.359	...	0
Out (DSP)	2.283	2.359	...	0
Exp. Out (DSP)	2.283	2.359	...	0

Test settings	
Tolerance Out	±2,7940e-07 (±600 LSB)

Test statistics	
Min CPU cycles	91
Max CPU cycles	315
Avg CPU cycles	111

Verification: uSub Float32 CPU TMS320F28379D

Date of Test	2026-06-22
Target controller	TMS320F28379D

Test case: Inport test OK

Inport test for Math block uSub.

Test results				
Time step	1	2	...	214
CPU cycles	164	164	...	81
Inputs				
Plus (DSP)	-2	-1.962	...	2
Minus (DSP)	2	1.962	...	2
Plus	-2	-1.962	...	2
Minus	2	1.962	...	2
Outputs				
Out	2.283	2.359	...	0
Exp. Out	2.283	2.359	...	0
Out (DSP)	2.283	2.359	...	0
Exp. Out (DSP)	2.283	2.359	...	0

Test settings	
Tolerance Out	±2,7940e-07 (±600 LSB)

Test statistics	
Min CPU cycles	81
Max CPU cycles	164
Avg CPU cycles	89